IP4770/71/72CZ16

VGA/video interface with integrated buffers, ESD protection and integrated termination resistors

Rev. 01 — 25 October 2006

Product data sheet

1. General description

The IP4770CZ16, IP4771CZ16, IP4772CZ16 is connected between the VGA/DVI interface and the video graphics controller and includes level shifting for the DDC signals, buffering for the SYNC lines as well as high-level ESD protection diodes for the RGB signal lines.

The level shifting functions are required when the DDC controller operates at a lower supply voltage than the monitor. To use this level shifting function the gates of the two N-channel MOSFETs have to be connected to the supply rail of the DDC transceivers.

Buffering for the SYNC signals is provided by two non-inverting buffers, which accept TTL input levels and convert these to CMOS compliant output levels between pins $V_{\text{CC(SYNC)}}$ and GND.

The IP4770CZ16 and IP4771CZ16 contain the formerly external termination resistors, which are typically required for the HSYNC and VSYNC lines of the video interface:

- IP4770CZ16: $R_{sync} = 55 \Omega$
- IP4771CZ16: $R_{sync} = 65 \Omega$
- IP4772CZ16: R_{sync} =10 Ω to allow termination of the SYNC lines

All RGB I/Os are protected by a special diode configuration offering a low line capacitance of 4 pF (maximum) only to provide protection to downstream components for ESD voltages as high as ± 8 kV contact discharge according to IEC 61000-4-2, level 4 standard.

2. Features

- Integrated high-level ESD protection, buffering, SYNC signal impedance matching and level shifting
- Terminal connections with integrated rail-to-rail clamping diodes with downstream ESD protection of ±8 kV according to IEC 61000-4-2, level 4 standard
- Backflow protection on DDC lines
- Drivers for HSYNC and VSYNC lines
- Bidirectional level shifting N-channel FETs available for DDC clock and DDC data channels
- Integrated impedance matching resistors on SYNC lines
- Line capacitance < 4 pF per channel
- Lead-free package and RoHS compliant



3. Applications

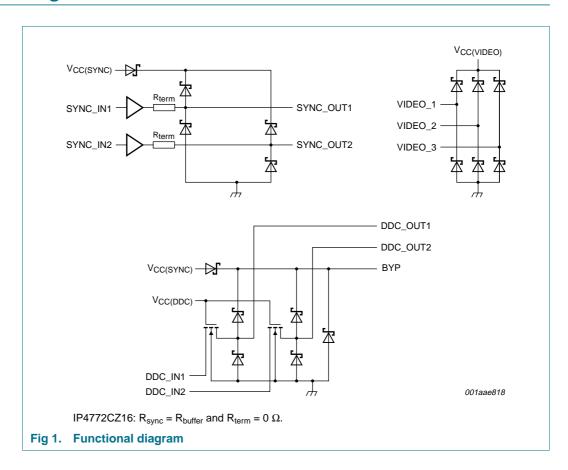
- To terminate and to buffer channels, to reduce EMI/RFI and to provide downstream ESD protection for:
 - ◆ VGA interfaces including DDC channels
 - Desktop and notebooks PCs
 - Graphics cards
 - Set top boxes

4. Ordering information

Table 1. Ordering information

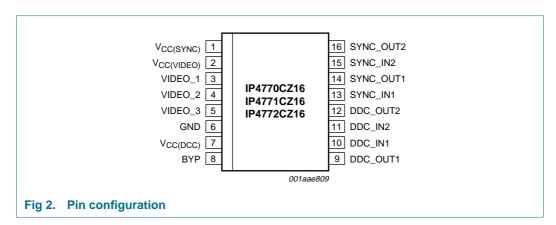
Type number	Package				
	Name	Description	Version		
IP4770CZ16	SSOP16	plastic shrink small outline package; 16 leads; body	SOT519-1		
IP4771CZ16		width 3.9 mm; lead pitch 0.635 mm			
IP4772CZ16					

5. Functional diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V _{CC(SYNC)}	1	supply voltage for SYNC_1 and SYNC_2 level shifter and their connected ESD protections
$V_{CC(VIDEO)}$	2	supply voltage for VIDEO_1, VIDEO_2 and VIDEO_3 protection circuits
VIDEO_1	3	video signal ESD protection channel 1
VIDEO_2	4	video signal ESD protection channel 2
VIDEO_3	5	video signal ESD protection channel 3
GND	6	ground
$V_{CC(DDC)}$	7	supply voltage for DDC_1 and DDC_2 level shifter N-FET gates
ВҮР	8	this input is used to connect an external 0.2 μ F bypass capacitor to increase ESD withstand voltage rating for the DDC outputs (± 8 kV with capacitor or ± 4 kV without capacitor)
DDC_OUT1	9	DDC signal output 1; connected to the video connector side of one of the SYNC lines
DDC_IN1	10	DDC signal input 1; connected to the VGA controller side of one of the SYNC lines
DDC_IN2	11	DDC signal input 2; connected to the VGA controller side of one of the SYNC lines
DDC_OUT2	12	DDC signal output 2; connected to the video connector side of one of the SYNC lines
SYNC_IN1	13	SYNC signal input 1; connected to the VGA controller side of one of the SYNC lines
SYNC_OUT1	14	SYNC signal output 1; connected to the video connector side of one of the SYNC lines
SYNC_IN2	15	SYNC signal input 2; connected to the VGA controller side of one of the SYNC lines
SYNC_OUT2	16	SYNC signal output 2; connected to the video connector side of one of the SYNC lines

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to ground (GND).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; pins VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SYNC_OUT2, DDC_OUT1, DDC_OUT2	<u>(1)</u>		
		level 4; contact	-8	+8	kV
		level 4; air discharge	–15	+15	kV
		IEC 61000-4-2; all other pins			
		level 1; contact	-2	+2	kV
		level 1; air discharge	-2	+2	kV
$V_{\text{CC(VIDEO)}}$	video supply voltage		-0.5	5.5	V
$V_{CC(DDC)}$	data display channel supply voltage		-0.5	5.5	V
$V_{\text{CC}(\text{SYNC})}$	synchronization supply voltage		-0.5	5.5	V
$V_{I(VIDEO_1)} \\$	input voltage on pin VIDEO_1		-0.5	$V_{CC(VIDEO)}$	V
$V_{I(VIDEO_2)}$	input voltage on pin VIDEO_2		-0.5	$V_{CC(VIDEO)}$	V
$V_{I(VIDEO_3)}$	input voltage on pin VIDEO_3		-0.5	$V_{CC(VIDEO)}$	V
$V_{I(DDC_IN1)}$	input voltage on pin DDC_IN1		-0.5	$V_{CC(DDC)}$	V
$V_{I(DDC_IN2)}$	input voltage on pin DDC_IN2		-0.5	$V_{CC(DDC)}$	V
$V_{I(SYNC_IN1)}$	input voltage on pin SYNC_IN1		-0.5	$V_{CC(SYNC)}$	V
$V_{I(SYNC_IN2)}$	input voltage on pin SYNC_IN2		-0.5	$V_{CC(SYNC)}$	V
$V_{O(DDC_OUT1)}$	output voltage on pin DDC_OUT1		-0.5	$V_{CC(DDC)}$	V
V _{O(DDC_OUT2)}	output voltage on pin DDC_OUT2		-0.5	$V_{CC(DDC)}$	V
P _{tot}	total power dissipation	T _{amb} = 25 °C	-	500	mW
T _{stg}	storage temperature		– 55	+125	°C

^[1] Pins BYP, $V_{CC(VIDEO)}$ and $V_{CC(SYNC)}$ must be bypassed to ground (pin GND) via a low-impedance ground plane with 0.22 μ F, low inductance, chip ceramic capacitor at each supply pin.

The bypass capacitor at pin BYP can be omitted. In this case the maximum ESD level for DDC_OUT1 and DDC_OUT2 pins is reduced to ± 4 kV.

ESD pulse is applied between the pins VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SYNC_OUT2, DDC_OUT1, DDC_OUT2 and GND.

8. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{oper}	operating temperature		-40	-	+85	°C

9. Characteristics

Table 5. Sync circuit characteristics

 $V_{CC(SYNC)} = 5 \text{ V; } T_{amb} = 25 \,^{\circ}C; \text{ unless otherwise specified.}$

$\begin{tabular}{l lllllllllllllllllllllllllllllllllll$	Max	Unit
$I_{CC(SYNC)}$ supply current on pin $V_{CC(SYNC)}$ [1]		
	50	μΑ
SYNC input at 3 V [1]	2	mΑ
Input: pins SYNC_IN1 and SYNC_IN2		
V _{IH} HIGH-level input voltage 2.0 -	-	V
V _{IL} LOW-level input voltage	0.6	V
Output: pins SYNC_OUT1 and SYNC_OUT2		
V_{OH} HIGH-level output voltage $I_{OH} = 1 \text{ mA}$ 4.85 -	-	V
IP4772CZ16; I _{OH} = 24 mA 2.0 -	-	V
V_{OL} LOW-level output voltage $I_{OL} = 1 \text{ mA}$	0.15	V
IP4772CZ16; I _{OL} = 24 mA	0.8	V
R _{sync} synchronization resistance IP4770CZ16	-	Ω
IP4771CZ16 [2] - 65	-	Ω
IP4772CZ16 3 - 10	-	Ω
Sync channel		
t_{PLH} LOW-to-HIGH propagation delay $C_L = 50 \ pF; \ t_r \ and \ t_f \le 5 \ ns$ [4]	12	ns
t_{PHL} HIGH-to-LOW propagation delay $C_L = 50 \text{ pF}; t_r \text{ and } t_f \leq 5 \text{ ns}$ [4]	12	ns
$t_{r(o)}$ output rise time $C_L = 50 \; pF; \; t_r \; and \; t_f \leq 5 \; ns$ - 4	-	ns
$C_L = 7 \text{ pF}; t_r \text{ and } t_f \le 5 \text{ ns}$ - 1.5	-	ns
$t_{f(o)} \qquad \qquad \text{output fall time} \qquad \qquad C_L = 50 \text{ pF}; t_r \text{ and } t_f \leq 5 \text{ ns} \qquad \qquad - \qquad 4$	-	ns
$C_L = 7 \text{ pF}; t_r \text{ and } t_f \le 5 \text{ ns}$ - 1.5	-	ns
Protection diode		
$I_{L(r)}$ reverse leakage current per channel; $V = 3.0 \text{ V}$	1	μΑ
V _{BRzd} Zener diode breakdown voltage I = 1 mA 6 -	9	V
V_{Fd} diode forward voltage $I_F = 1 \text{ mA}$ - 0.7	_	V

^[1] SYNC outputs unloaded.

^[2] $R_{sync} = R_{term} + R_{buffer}$.

^[3] $R_{sync} = R_{buffer}$ because $R_{term} = 0 \Omega$.

^[4] This parameter is guaranteed by design and characterization.

Table 6. Video circuit characteristics

 $V_{CC(VIDEO)} = 5 \text{ V; } T_{amb} = 25 \,^{\circ}\text{C; unless otherwise specified.}$

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Supply: pin	V _{CC(VIDEO)}					
I _{CC(VIDEO)}	supply current on pin $V_{\text{CC(VIDEO)}}$	static input signals	-	-	10	μΑ
Video chann	nel: pins VIDEO_1, VIDEO_2 and VID	DEO_3				
C _{ch(video)}	video channel capacitance	$f_i = 1 \text{ MHz}; V_I = 2.5 \text{ V}$	<u>[1]</u> _	-	4	pF
I _{i(video)}	video input current	$V_I = V_{CC(VIDEO)}$ or GND	-1	-	+1	μΑ
Protection of	liode					
V_{Fd}	diode forward voltage	I _F = 1 mA	-	0.7	-	V

^[1] This parameter is guaranteed by design and characterization.

Table 7. Level circuit characteristics

 $V_{CC(DDC)}$ = 5 V; T_{amb} = 25 °C; unless otherwise specified.

(/	· · ·						
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Supply: pin	V _{CC(DDC)}						
I _{CC(DDC)}	supply current on pin $V_{CC(DDC)}$			-	-	10	μΑ
N-MOSFET							
I _{L(off)}	off-state leakage current		<u>[1]</u>	-	-	10	μΑ
ΔV_{on}	on-state voltage drop	$V_{CC(DDC)} = 2.5 \text{ V}; V_S = \text{GND};$ $I_{DS} = 3 \text{ mA}$		-	-	0.18	V
Protection of	diode						
I _{L(r)}	reverse leakage current	per channel; V = 3.0 V		-	-	1	μΑ
V_{BRzd}	Zener diode breakdown voltage	I = 1 mA		6	-	9	V
V_{Fd}	diode forward voltage	I _F = 1 mA		-	0.7	-	V

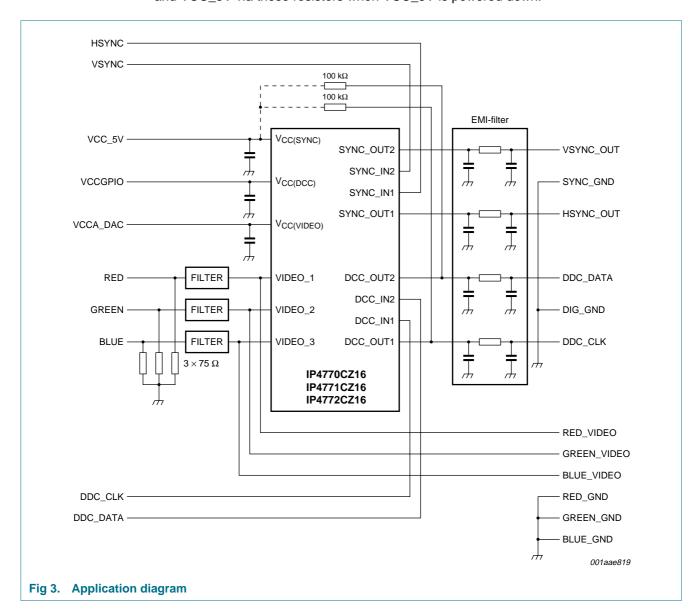
^[1] Input $V_{I(DDC_INx)} \le V_{CC(DDC)} - 0.4 \text{ V}$ and output $V_{O(DDC_OUTx)} = V_{CC(DDC)}$ or input $V_{I(DDC_INx)} = V_{CC(DDC)}$ and output $V_{O(DCC_OUTx)} \le V_{CC(DCC)} - 0.4 \text{ V}$.

10. Application information

The IP4770CZ16, IP4771CZ16, IP4772CZ16 should be placed as close as possible to the VGA/DVI interface connector.

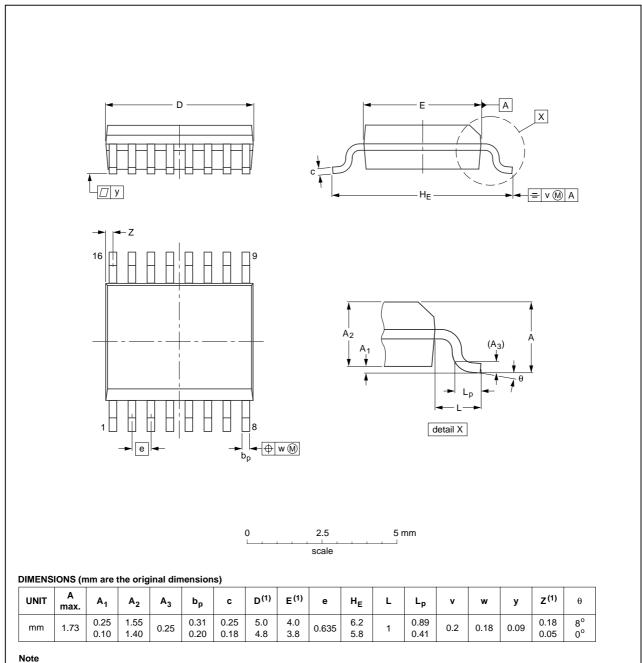
The ESD protection channels VIDEO_1, VIDEO_2 and VIDEO_3 can be connected in any order with RBG signals.

The 100 $k\Omega$ resistors between the DDC_OUTx channels and VCC_5V are optional. They may be used, if required, to pull-up the DDC_OUTx lines to VCC_5V when no monitor is connected to the VGA connector. Backflow current can flow between pins DDC_OUTx and VCC_5V via these resistors when VCC_5V is powered down.



11. Package outline

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1



1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

	OUTLINE		REFER	ENCES		EUROPEAN	ISSUE DATE
	VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
	SOT519-1						-99-05-04- 03-02-18
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Fig 4. Package outline SOT519-1 (SSOP16)

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12. Abbreviations

Table 8. Abbreviations

10010 01	7 (1515) 0 (Tations .
Acronym		Description
CMOS		Complementary Metal Oxide Semiconductor
DDC		Data Display Channel
DVI		Digital Video Interface
EMI		ElectroMagnetic Interference
ESD		ElectroStatic Discharge
FET		Field Effect Transistor
HSYNC		Horizontal SYNChronization
MOSFET		Metal Oxide Semiconductor Field Effect Transistor
PC		Personal Computer
RFI		Radio Frequency Interference
RGB		Red Green Blue
SYNC		SYNChronization
TTL		Transistor-Transistor Logic
VGA		Video Graphics Adapter
VSYNC		Vertical SYNChronization

13. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4770CZ16_4771_4772_1	20061025	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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