CA91C015

VMEbus DATA ADDRESS REGISTER FILE (DARF)

- **Complete VMEbus address and data interface, except buffers**
- **Decoupling of CPU and VMEbus**
- **Sustained 25-30 Megabyte/second VMEbus transfer rate**
- **Selectable atomic or decoupled mode**
- **Programmable A32 and A24 slave image bases and sizes**
- **Programmable access protection**
- **Integral DMA for local RAM to VMEbus transfers**
- **Location monitor with 31-longword deep data FIFO**
- **Low power CMOS implementation**
- **224 Pin Grid Array package**
- **Available in MIL-STD 883C Class B version**

The CA91C015 Data Address Register File (DARF) is one member of the AVICS (Advanced VMEbus Interface Chip Set); the other member being the CA91C014 Advanced System Architecture Control Circuit (ACC). This chip set integrates all the functions commonly required to interface an intelligent card to the VMEbus, while adding features that provide major architectural improvements. The ACC and DARF, while optimized for use together, may also be used individually where appropriate in the system design.

The DARF provides a decoupled address and data path between the VMEbus and the local CPU and memory, and also contains a Location Monitor with an associated message queue.

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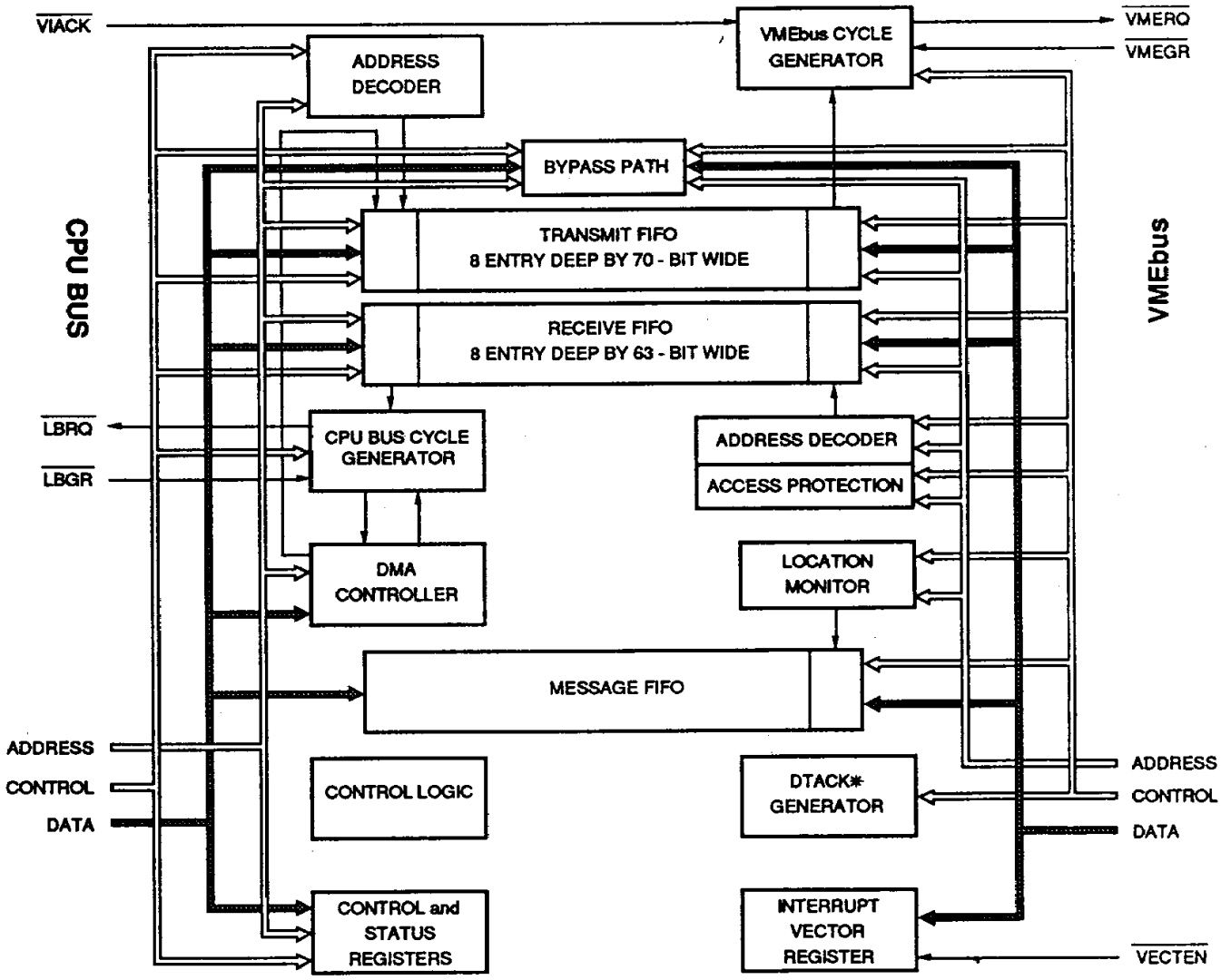

Figure 1 : CA91C015 DARF BLOCK DIAGRAM

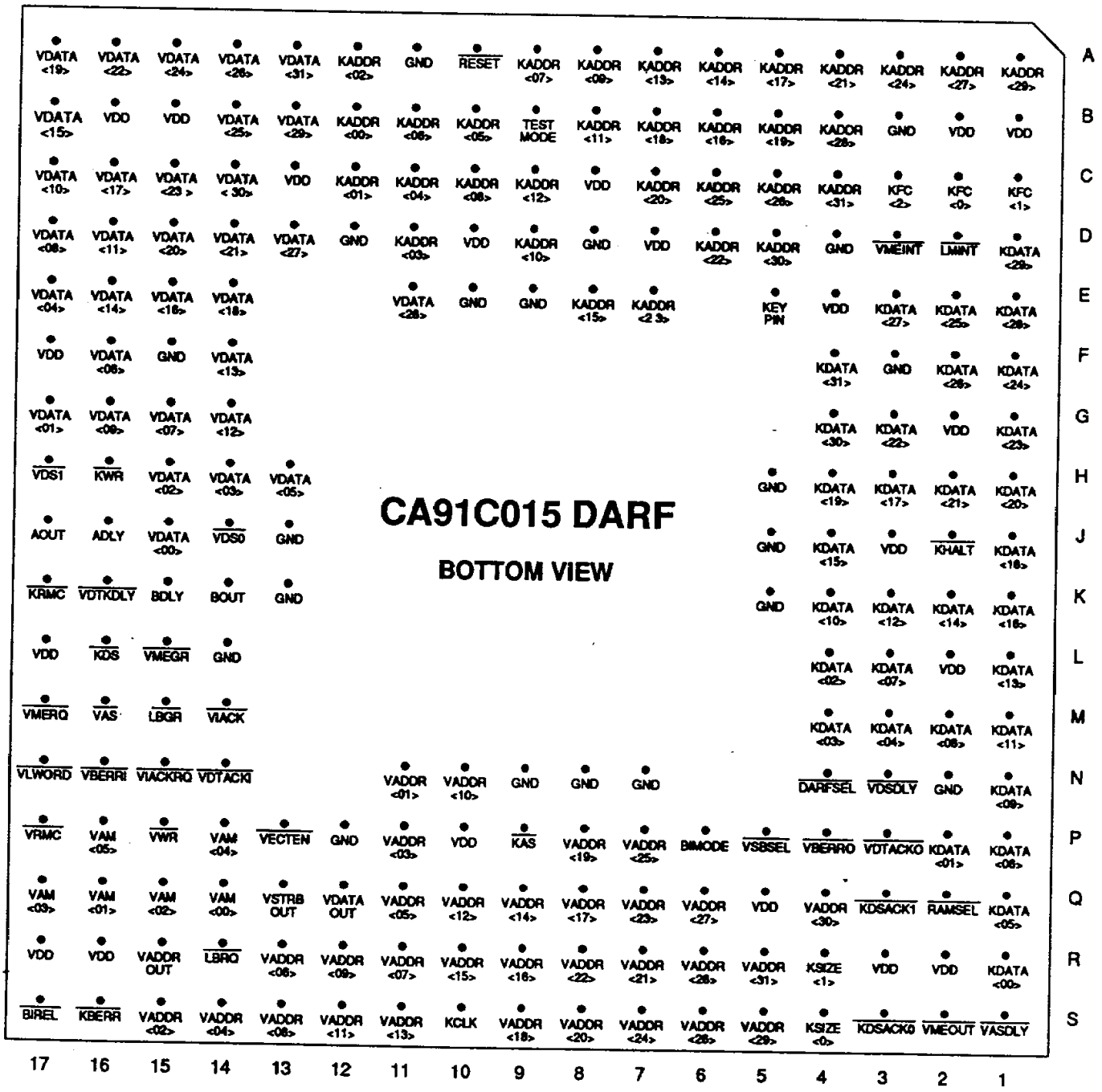

Figure 2 : PIN CONFIGURATION for 224–PIN PGA PACKAGE

Table 1 : DARF PGA PINOUT

Pin	Signal	Signal Group
A1	KADDR 29	Local Bus
A2	KADDR 27	Local Bus
A3	KADDR 24	Local Bus
A4	KADDR 21	Local Bus
A5	KADDR 17	Local Bus
A6	KADDR 14	Local Bus
A7	KADDR 13	Local Bus
A8	KADDR 09	Local Bus
A9	KADDR 07	Local Bus
A10	$\overline{\text{RESET}}$	Reset, Clock & Mode
A11	V_{SS}	
A12	KADDR 02	Local Bus
A13	VDATA 31	VMEbus
A14	VDATA 26	VMEbus
A15	VDATA 24	VMEbus
A16	VDATA 22	VMEbus
A17	VDATA 19	VMEbus
B1	V_{DD}	
B2	V_{DD}	
B3	V_{SS}	
B4	KADDR 28	Local Bus
B5	KADDR 19	Local Bus
B6	KADDR 16	Local Bus
B7	KADDR 18	Local Bus
B8	KADDR 11	Local Bus
B9	TESTMODE	Reset, Clock & Mode
B10	KADDR 05	Local Bus
B11	KADDR 06	Local Bus
B12	KADDR 00	Local Bus
B13	VDATA 29	VMEbus
B14	VDATA 25	VMEbus
B15	V_{DD}	
B16	V_{DD}	
B17	VDATA 15	VMEbus
C1	KFC1	Local Bus
C2	KFC0	Local Bus
C3	KFC2	Local Bus
C4	KADDR 31	Local Bus
C5	KADDR 26	Local Bus
C6	KADDR 25	Local Bus
C7	KADDR 20	Local Bus
C8	V_{DD}	
C9	KADDR 12	Local Bus
C10	KADDR 08	Local Bus
C11	KADDR 04	Local Bus
C12	KADDR 01	Local Bus
C13	V_{DD}	
C14	VDATA 30	VMEbus
C15	VDATA 23	VMEbus
C16	VDATA 17	VMEbus
C17	VDATA 10	VMEbus
D1	KDATA 29	Local Bus
D2	$\overline{\text{LMINT}}$	Reset, Clock & Mode
D3	$\overline{\text{VMEINT}}$	Reset, Clock & Mode
D4	V_{SS}	
D5	KADDR 30	Local Bus
D6	KADDR 22	Local Bus
D7	V_{DD}	
D8	V_{SS}	
D9	KADDR 10	Local Bus
D10	V_{DD}	
D11	KADDR 03	Local Bus
D12	V_{SS}	
D13	VDATA 27	VMEbus
D14	VDATA 21	VMEbus
D15	VDATA 20	VMEbus
D16	VDATA 11	VMEbus
D17	VDATA 08	VMEbus
E1	KDATA 28	Local Bus
E2	KDATA 25	Local Bus
E3	KDATA 27	Local Bus
E4	V_{DD}	
E5	N/C	(Keying Pin)
E7	KADDR 23	Local Bus
E8	KADDR 15	Local Bus
E9	V_{SS}	
E10	V_{SS}	
E11	VDATA 28	VMEbus
E14	VDATA 18	VMEbus
E15	VDATA 16	VMEbus
E16	VDATA 14	VMEbus
E17	VDATA 04	VMEbus
F1	KDATA 24	Local Bus
F2	KDATA 26	Local Bus
F3	V_{SS}	
F4	KDATA 31	Local Bus

Table 1 : DARF PGA PINOUT CON'T

Pin	Signal	Signal Group
F14	VDATA 13	VMEbus
F15	V_{SS}	
F16	VDATA 06	VMEbus
F17	V_{DD}	
G1	KDATA 23	Local Bus
G2	V_{DD}	
G3	KDATA 22	Local Bus
G4	KDATA 30	Local Bus
G14	VDATA 12	VMEbus
G15	VDATA 07	VMEbus
G16	VDATA 09	VMEbus
G17	VDATA 01	VMEbus
H1	KDATA 20	Local Bus
H2	KDATA 21	Local Bus
H3	KDATA 17	Local Bus
H4	KDATA 19	Local Bus
H5	V_{SS}	
H13	VDATA 05	VMEbus
H14	VDATA 03	VMEbus
H15	VDATA 02	VMEbus
H16	$\overline{KWR}$	Local Bus
H17	$\overline{VDS1}$	VMEbus
J1	KDATA 18	Local Bus
J2	$\overline{KHALT}$	Local Bus
J3	V_{DD}	
J4	KDATA 15	Local Bus
J5	V_{SS}	
J13	V_{SS}	
J14	$\overline{VDS0}$	VMEbus
J15	VDATA 00	VMEbus
J16	ADLY	Reset, Clock & Mode
J17	AOUT	Reset, Clock & Mode
K1	KDATA 16	Local Bus
K2	KDATA 14	Local Bus
K3	KDATA 12	Local Bus
K4	KDATA 10	Local Bus
K5	V_{SS}	
K13	V_{SS}	
K14	BOUT	Reset, Clock & Mode
K15	BDLY	Reset, Clock & Mode
K16	$\overline{VDTKDLY}$	VMEbus
K17	$\overline{KRMC}$	Local Bus
L1	KDATA 13	Local Bus
L2	V_{DD}	
L3	KDATA 07	Local Bus
L4	KDATA 02	Local Bus
L14	V_{SS}	
L15	$\overline{VMEGR}$	VMEbus
L16	$\overline{KDS}$	Local Bus
L17	V_{DD}	
M1	KDATA 11	Local Bus
M2	KDATA 08	Local Bus
M3	KDATA 04	Local Bus
M4	KDATA 03	Local Bus
M14	$\overline{VIACK}$	VMEbus
M15	$\overline{LBGR}$	Local Bus
M16	$\overline{VAS}$	VMEbus
M17	$\overline{VMERQ}$	VMEbus
N1	KDATA 09	Local Bus
N2	V_{SS}	
N3	$\overline{VDSDLY}$	VMEbus
N4	$\overline{DARFCS}$	Local Bus
N7	V_{SS}	
N8	V_{SS}	
N9	V_{SS}	
N10	VADDR 10	VMEbus
N11	VADDR 01	VMEbus
N14	$\overline{VDTACKI}$	VMEbus
N15	$\overline{VIACKRQ}$	VMEbus
N16	$\overline{VBERRI}$	VMEbus
N17	$\overline{VLWORD}$	VMEbus
P1	KDATA 06	Local Bus
P2	KDATA 01	Local Bus
P3	$\overline{VDTACKO}$	VMEbus
P4	$\overline{VBERRO}$	VMEbus
P5	$\overline{VSBSEL}$	VMEbus
P6	BIMODE	Reset, Clock & Mode
P7	VADDR 25	VMEbus
P8	VADDR 19	VMEbus
P9	$\overline{KAS}$	Local Bus
P10	V_{DD}	
P11	VADDR 03	VMEbus
P12	V_{SS}	
P13	$\overline{VECTEN}$	VMEbus
P14	VAM 04	VMEbus
P15	$\overline{VWR}$	VMEbus

Table 1 : DARF PGA PINOUT CON'T

Pin	Signal	Signal Group
P16	VAM 05	VMEbus
P17	$\overline{\text{VRMC}}$	VMEbus
Q1	KDATA 05	Local Bus
Q2	$\overline{\text{RAMSEL}}$	Local Bus
Q3	$\overline{\text{KDSACK1}}$	Local Bus
Q4	VADDR 30	VMEbus
Q5	V_{DD}	
Q6	VADDR 27	VMEbus
Q7	VADDR 23	VMEbus
Q8	VADDR 17	VMEbus
Q9	VADDR 14	VMEbus
Q10	VADDR 12	VMEbus
Q11	VADDR 05	VMEbus
Q12	VDATAOUT	VMEbus
Q13	VSTRBOUT	VMEbus
Q14	VAM 00	VMEbus
Q15	VAM 02	VMEbus
Q16	VAM 01	VMEbus
Q17	VAM 03	VMEbus
R1	KDATA 00	Local Bus
R2	V_{DD}	
R3	V_{DD}	
R4	KSIZE1	Local Bus
R5	VADDR 31	VMEbus
R6	VADDR 28	VMEbus
R7	VADDR 21	VMEbus
R8	VADDR 22	VMEbus

Pin	Signal	Signal Group
R9	VADDR 16	VMEbus
R10	VADDR 15	VMEbus
R11	VADDR 07	VMEbus
R12	VADDR 09	VMEbus
R13	VADDR 06	VMEbus
R14	$\overline{\text{LBRQ}}$	Local Bus
R15	VADDROUT	VMEbus
R16	V_{DD}	
R17	V_{DD}	
S1	$\overline{\text{VASDLY}}$	VMEbus
S2	$\overline{\text{VMEOUT}}$	VMEbus
S3	$\overline{\text{KDSACK0}}$	Local Bus
S4	KSIZE0	Local Bus
S5	VADDR 29	VMEbus
S6	VADDR 26	VMEbus
S7	VADDR 24	VMEbus
S8	VADDR 20	VMEbus
S9	VADDR 18	VMEbus
S10	KCLK	Reset, Clock & Mode
S11	VADDR 13	VMEbus
S12	VADDR 11	VMEbus
S13	VADDR 08	VMEbus
S14	VADDR 04	VMEbus
S15	VADDR 02	VMEbus
S16	$\overline{\text{KBERR}}$	Local Bus
S17	$\overline{\text{BIREL}}$	Reset, Clock & Mode

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Table 2a : LOCAL BUS SIGNALS

The local bus signals are those used to gain access to, or perform data transfers on the local CPU bus. The DARF is designed for parallel connection with a 68020 or 68030 CPU.

Symbol	Pin(s)	Type	Name and Function
$\overline{\text{DARFCS}}$	N4	I	DARF internal registers chip select, input
KADDR 31 – 00	C4, D5, A1, B4, A2, C5, C6, A3, E7, D6, A4, C7, B5, B7, A5, B6, E8, A6, A7, C9, B8, D9, A8, C10, A9, B11, B10, C11, D11, A12, C12, B12	I/O	Address bus bits 31 through 00, input/output
$\overline{\text{KAS}}$	P9	I/O	Address strobe, input/output
$\overline{\text{KBERR}}$	S16	I/O	Data transfer failure, input/output
KDATA 31 – 00	F4, G4, D1, E1, E3, F2, E2, F1, G1, G3, H2, H1, H4, J1, H3, K1, J4, K2, L1, K3, M1, K4, N1, M2, L3, P1, Q1, M3, M4, L4, P2, R1	I/O	Data bus bits 31 through 00, input/output
$\overline{\text{KDS}}$	L16	I/O	Data strobe, input/output
$\overline{\text{KDSACK1}}$ – $\overline{\text{KDSACK0}}$	Q3, S3	I/O	Transfer and size acknowledge, input/output
KFC2 – KFC0	C3, C1, C2	I/O	Function code indicator bits, input/output
$\overline{\text{KHALT}}$	J2	I/O	CPU halt or retry, input/output
$\overline{\text{KRMC}}$	K17	I/O	Read-modify-write lock signal, input/output
KSIZE1 – KSIZE0	R4, S4	I/O	Data transfer size bits, input/output
$\overline{\text{KWR}}$	H16	I/O	Write signal, input/output
$\overline{\text{LBGR}}$	M15	I	Local bus grant, input
$\overline{\text{LBRQ}}$	R14	O	Local bus request, output
$\overline{\text{RAMSEL}}$	Q2	O	Local memory enable signal, output

Table 2b : VMEbus SIGNALS

The VMEbus signals are those involved in gaining access to and using the VMEbus. The DARF does not connect directly to the VMEbus; rather, external buffers and transceivers are used for VMEbus control signals and addresses.

Symbol	Pin(s)	Type	Name and Function
VADDR 31 – 01	R5, Q4, S5, R6, Q6, S6 P7, S7, Q7, R8, R7, S8 P8, S9, Q8, R9, R10, Q9 S11, Q10, S12, N10 R12, S13, R11, R13 Q11, S14, P11, S15, N11	I/O	Address bits
VADDROUT	R15	O	Address transciever direction control
VAM 05 – VAM 00	P16, P14, Q17, Q15, Q16, Q14	I/O	Address modifier bits
$\overline{\text{VAS}}$	M16	I/O	Address strobe
$\overline{\text{VASDLY}}$	S1	I	Delayed address strobe
$\overline{\text{VBERRI}}$	N16	I	BERR*
$\overline{\text{VBERRO}}$	P4	O	BERR*
VDATA 31 – 00	A13, C14, B13, E11, D13 A14, B14, A15, C15, A16 D14, D15, A17, E14, C16 E15, B17, E16, F14, G14 D16, C17, G16, D17, G15 F16, H13, E17, H14, H15 G17, J15	I/O	Data bits
VDATAOUT	Q12	O	Data transceiver direction control
$\overline{\text{VDS1}}$ – $\overline{\text{VDS0}}$	H17, J14	I/O	Data strobes
$\overline{\text{VDSDLY}}$	N3	I	Delayed data strobe
$\overline{\text{VDTACKI}}$	N14	I	DTACK*
$\overline{\text{VDTACKO}}$	P3	O	DTACK*
$\overline{\text{VDTKDLY}}$	K16	I	Delayed DTACK*
$\overline{\text{VECTEN}}$	P13	I	Respond to VMEbus IACK cycle request
$\overline{\text{VIACK}}$	M14	I/O	IACK* signal
$\overline{\text{VIACKRQ}}$	N15	I	VMEbus IACK cycle request to DARF
$\overline{\text{VLWORD}}$	N17	I/O	Long-word signal
$\overline{\text{VMEGR}}$	L15	I	VMEbus grant input from the ACC
$\overline{\text{VMEOUT}}$	S2	I	Off-card data transfer bus select
$\overline{\text{VMERQ}}$	M17	O	VMEbus request output to the ACC
$\overline{\text{VRMC}}$	P17	I/O	Read-modify-write signal
$\overline{\text{VSBSEL}}$	P5	O	Auxilliary data transfer bus select
VSTRBOUT	Q13	O	Address and data strobe transceiver direction
$\overline{\text{VWR}}$	P15	I/O	Write signal

Table 2c : RESET, CLOCK and MODE SIGNALS

Symbol	Pin(s)	Type	Name and Function
ADLY	J16	I	Delay circuit A input from delay line
AOUT	J17	O	Delay circuit A output to delay line
BDLY	K15	I	Delay circuit B input from delay line
BIMODE	P6	I	BI-mode™ signal
$\overline{\text{BIREL}}$	S17	O	BI-mode™ release
BOUT	K14	O	Delay circuit B output to delay line
KCLK	S10	I	Clock input, same as the CPU clock
$\overline{\text{LMINT}}$	D2	O	Location Monitor FIFO interrupt
$\overline{\text{RESET}}$	A10	I	Reset input
TESTMODE	B9	I	Chip test mode input; for chip fabrication only
$\overline{\text{VMEINT}}$	D3	O	VMEbus related events interrupt

TERMINOLOGY

Signals on the VMEbus and those within the circuit card may be active high or active low. Active low signals are defined as being true or asserted when they are at a low voltage, and conversely for active high signals. VMEbus active low signals are indicated by the * suffix, while on-card active low signals that do not connect directly to the VMEbus are indicated with $\overline{\text{OVERBARS}}$.

Where there is a need to clarify whether a signal is a VMEbus or local signal, a V may be prefixed for VMEbus signals, an L for general local signals, or a K for signals only connecting to the local CPU.

The output type abbreviations used in Tables 3 and 9 are defined in this section. They have both a letter code and a number suffix which indicates their current rating.

For example, the VDATA 31-00 signals are shown as input type CTTL, which are CMOS inputs with normal TTL voltage thresholds, and output type TS4 SR, which are tristateable 4 mA sink and source current outputs with slew rate limiting.

TP	Totem pole output
TS	Tristate totem pole output
OD	Open drain output
SR	Slew rate limited output
CTTL	CMOS input with TTL thresholds
CTTL PD	CMOS input, TTL thresholds, integral pull down
CTTL PU	CMOS input, TTL thresholds, integral pull up

Table 3 : Input and Output Type General Classification

Signal	Input	Output	Signal	Input	Output
ADLY	CTTL		TESTMODE	CTTL	
AOUT		TP4	VADDR 31-01	CTTL	TS4 SR
BDLY	CTTL		VADDROUT	CTTL	TS4
BIMODE	CTTL		VAM 05 – VAM 00	CTTL	TS4
$\overline{\text{BIREL}}$		TP2	$\overline{\text{VAS}}$	CTTL	TS4
BOUT		TP4	$\overline{\text{VASDLY}}$	CTTL	
$\overline{\text{DARFCS}}$	CTTL		$\overline{\text{VBERRI}}$	CTTL	
$\overline{\text{DTACKDLY}}$	CTTL		$\overline{\text{VBERRO}}$		TP4
KADDR 31 – 00	CTTL	TS6	VDATA 31 – 00	CTTL	TS4 SR
$\overline{\text{KAS}}$	CTTL	TS8	VDATAOUT		TP4
$\overline{\text{KBERR}}$	CTTL	OD8	$\overline{\text{VDS1}}$ – $\overline{\text{VDS0}}$	CTTL	TS4
KCLK	CTTL		$\overline{\text{VDSDLY}}$	CTTL	
KDATA 31 – 00	CTTL PU	TS6	$\overline{\text{VDTACKI}}$	CTTL	
$\overline{\text{KDS}}$		TS8	$\overline{\text{VDTACKO}}$		TP4
$\overline{\text{KDSACK1}}$ – $\overline{\text{KDSACK0}}$	CTTL	TS8	$\overline{\text{VECTEN}}$	CTTL	
$\overline{\text{KFC 1}}$		TS6	$\overline{\text{VIACK}}$	CTTL	TS4
$\overline{\text{KFC 2,0}}$	CTTL	TS6	$\overline{\text{VIACKRQ}}$	CTTL	
$\overline{\text{KHALT}}$		OD12	$\overline{\text{VLWORD}}$	CTTL	TS4
$\overline{\text{KRMC}}$	CTTL	TS8	$\overline{\text{VMEGR}}$	CTTL	
KSIZE1 – KSIZE0	CTTL	TS8	$\overline{\text{VMEINT}}$		TP2
$\overline{\text{KWR}}$	CTTL	TS8	$\overline{\text{VMEOUT}}$	CTTL	
$\overline{\text{LBGR}}$	CTTL		$\overline{\text{VMERQ}}$		TP2
$\overline{\text{LBRQ}}$		TP2	$\overline{\text{VRMC}}$	CTTL	TS4
$\overline{\text{LMINT}}$		TP2	$\overline{\text{VSBSEL}}$		TP4
$\overline{\text{RAMSEL}}$		TP4	VSTRBOUT		TP4
$\overline{\text{RESET}}$	CTTL		$\overline{\text{VWR}}$	CTTL	TS4

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Table 4 : AC CHARACTERISTICS (DARF LOCAL BUS MASTERSHIP)
(Commercial T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = –55° to +125°C, V_{DD} = 5V ± 10%)

Symbol	Description	Clk Count	Limits			Unit
			Min	Max		
				Com	Mil	
	Clock frequency		-	25	20	MHz
t_1	KCLK cycle time	-	40/50			ns
t_2	KCLK pulse width low	-	17/22	-	-	ns
t_3	KCLK pulse width high	-	17/22	-	-	ns
$t_{4,5}$	KCLK rise and fall times	-	-	5	5	ns
t_6	KCLK high to address valid	-	5	40	47	ns
t_7	KCLK high to address tri-state	-	5	30	35	ns
t_8	KCLK high to address invalid	-	5	-	-	ns
t_9	KCLK low to $\overline{KAS}$, $\overline{KDS}$ asserted	-	4	25	30	ns
t_{9A}	$\overline{KAS}$ to $\overline{KDS}$ skew (read) (Note 1)	-	–15	10	15	ns
t_{11}	Address valid to $\overline{KAS}$ asserted	-	4	-	-	ns
t_{12}	KCLK low to $\overline{KAS}$, $\overline{KDS}$ negated	-	4	25	30	ns
t_{13}	$\overline{KAS}$ negated to address invalid (Note 3)	0.5	0	-	-	ns
t_{14}	$\overline{KAS}$ width asserted (Note 3)	2.0	-5	-	-	ns
t_{14A}	$\overline{KDS}$ width asserted (write) (Note 3)	1.0	-5	-	-	ns
t_{15}	$\overline{KAS}$ & $\overline{KDS}$ width negated (Note 3)	1.0	0	-	-	ns
t_{16}	KCLK high to $\overline{KAS}$ tri-state	-	4	25	30	ns
t_{17}	$\overline{KAS}$, $\overline{KDS}$ high to $\overline{KWR}$ invalid (Note 3)	0.5	–2	-	-	ns
t_{18}	KCLK high to $\overline{KWR}$ high	-	4	25	30	ns
t_{20}	KCLK high to $\overline{KWR}$ low	-	4	30	35	ns
t_{21}	$\overline{KWR}$ high to $\overline{KAS}$ asserted (Note 3)	0.5	–5	-	-	ns
t_{22}	$\overline{KWR}$ low to $\overline{KDS}$ asserted (Notes 3 & 6)	1.5	0	-	-	ns
t_{23}	KCLK high to data out valid	-	5	30	36	ns
t_{25}	$\overline{KDS}$ high to data out invalid (Notes 3 & 6)	0.5	0	-	-	ns
t_{26}	Data out valid to $\overline{KDS}$ low (Notes 3 & 6)	0.5	–7	-	-	ns
t_{27}	Data in valid to KCLK low	-	5	-	-	ns
t_{27A}	Late $\overline{KBERR}$ to KCLK high (Notes 5)	-	5	-	-	ns
t_{28}	$\overline{KDSACK}$ high to next S2 low	-	5	-	-	ns
t_{29}	$\overline{KDS}$ high to data hold time	-	0	-	-	ns
t_{31}	$\overline{KDSACK}$ low to data in valid (Notes 2 & 3)	1.0	-	2	5	ns
t_{46}	$\overline{KWR}$ width low (Notes 3)	4.0	–5	-	-	ns

Table 4 : AC CHARACTERISTICS (DARF LOCAL BUS MASTERSHIP) CON'T
(Commercial T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = –55° to +125°C, V_{DD} = 5V ± 10%)

Symbol	Description	Clk Count	Limits			Unit
			Min	Max		
				Com	Mil	
t_{47A}	Asynchronous input setup time (Notes 5)	-	5	-	-	ns
t_{47B}	Asynchronous input hold time	-	5	-	-	ns
t_{48}	$\overline{KDSACK}$ asserted to $\overline{KBERR}$ low (Notes 3, 4)	2.5	-	0	0	ns
t_{53}	Data out hold from KCLK high	-	5	-	-	ns

Notes:
1. This number can be reduced to 2 ns if strobes have equal loads.
2. If the asynchronous setup time (t_{47}) requirements are met, the $\overline{KDSACKn}$ low to data setup time (t_{31}) can be ignored. The data must only satisfy the data-in to clock low setup time (t_{27}) for the following clock cycle, $\overline{KBERR}$ must only satisfy the later KBERR/ low to clock high setup time (t_{27A}) for the following clock cycle.
3. This timing parameter is the sum of the number listed and the product of the CLK COUNT times the period of the CPU clock.
   eg: $t_{21} = -5 + (0.5 \times t_{KCLK})$ ns
4. This specification applies to the first $\overline{KDSACKn}$ signal asserted. In the absence of $\overline{KDSACKn}$, $\overline{KBERR}$ is an asynchronous input using the asynchronous input setup time (t_{47}). Timing paramter t_{27A} must also be met for a late $\overline{KBERR}$.
5. This timing parameter applies for all asynchronous inputs: $\overline{KDSACK0}$, $\overline{KDSACK1}$, $\overline{KBERR}$, $\overline{LBGR}$ and $\overline{VMEGR}$.
6. Actual value depends on the clock input waveform.

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Table 5 : AC CHARACTERISTICS (DARF BUS ARBITRATION)
(Commercial T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = –55° to +125°C, V_{DD} = 5V ± 10%)

Symbol	Description	Clk Count	Limits			Unit
			Min	Max		
				Com	Mil	
t_{90}	KCLK low to $\overline{LBRQ}$ asserted	-	3	20	25	ns
t_{91}	KCLK low to $\overline{LBRQ}$ negated	-	3	20	25	ns
t_{92}	KCLK low to $\overline{VMERQ}$ asserted	-	3	20	25	ns
t_{93}	KCLK low to $\overline{VMERQ}$ negated	-	3	20	25	ns
t_{94}	KCLK high to KADDR, $\overline{KFC}$, $\overline{KSIZE}$ buses driven	-	5	-	-	ns
t_{95}	$\overline{LBGR}$ low to DARF S0 (Note 1)	3.5/4.5	-	-	-	t_{KCLK}

Notes:
1. This timing parameter is the sum of the number listed and product of the CLK COUNT times the period of the CPU clock.
   eg: $t_{21} = -5 + (0.5 \times t_{KCLK})$ ns

Figure 3 : INPUT CLOCK WAVEFORM TIMING

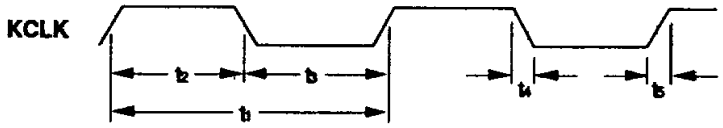


Figure 4a : DARF MASTER INTERFACE, MEMORY READ

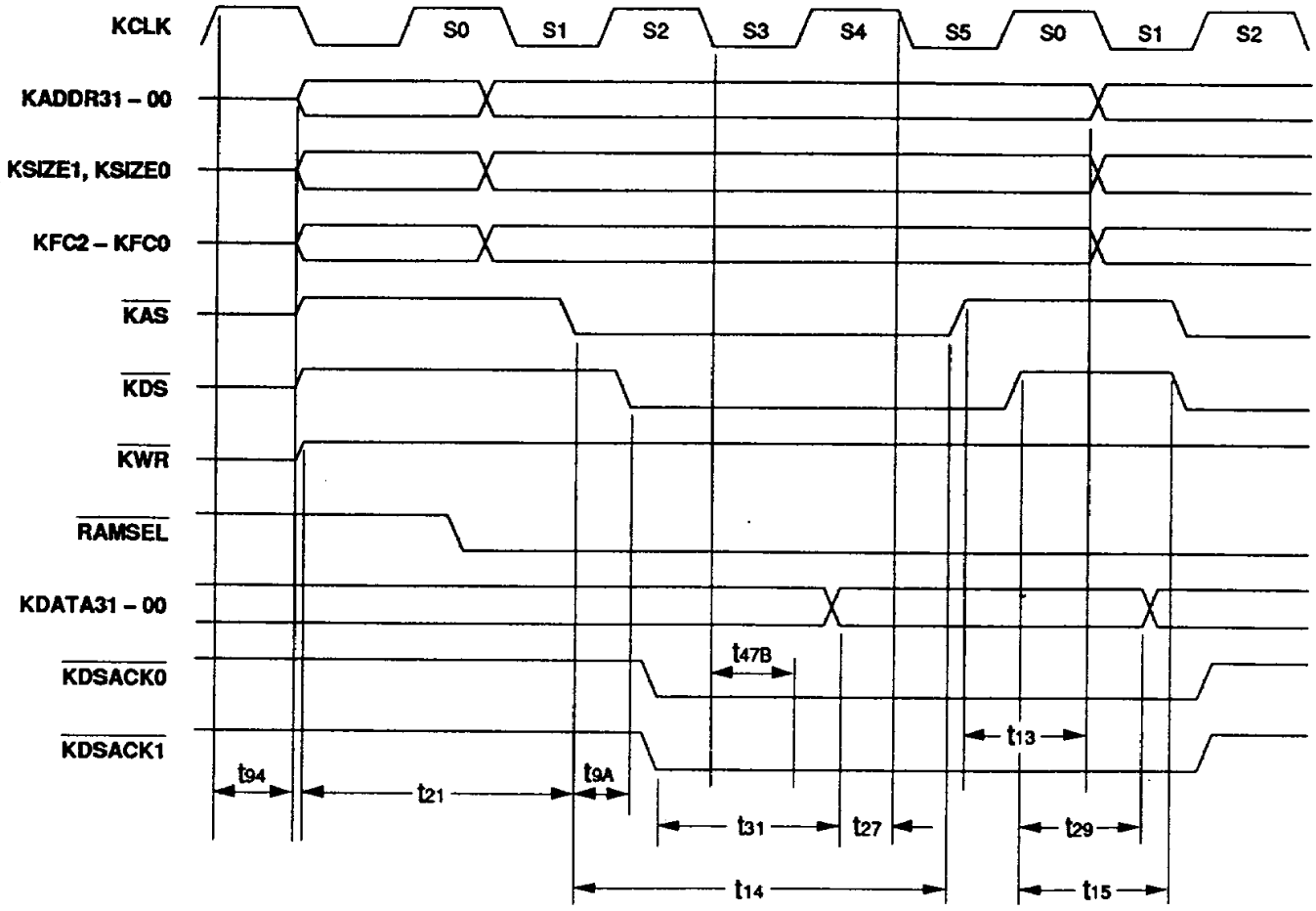


Figure 4b : DARF MASTER INTERFACE, MEMORY WRITE

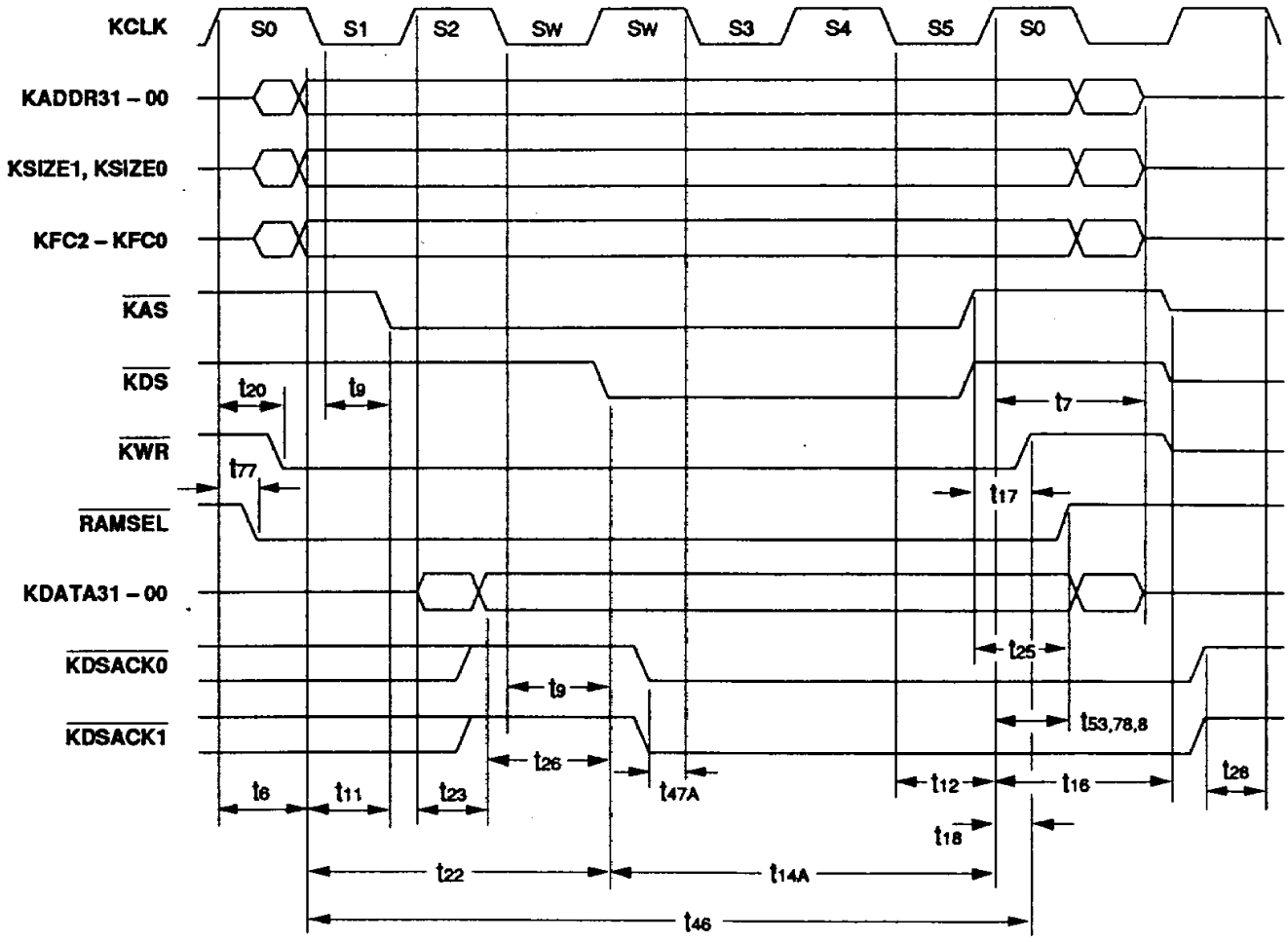
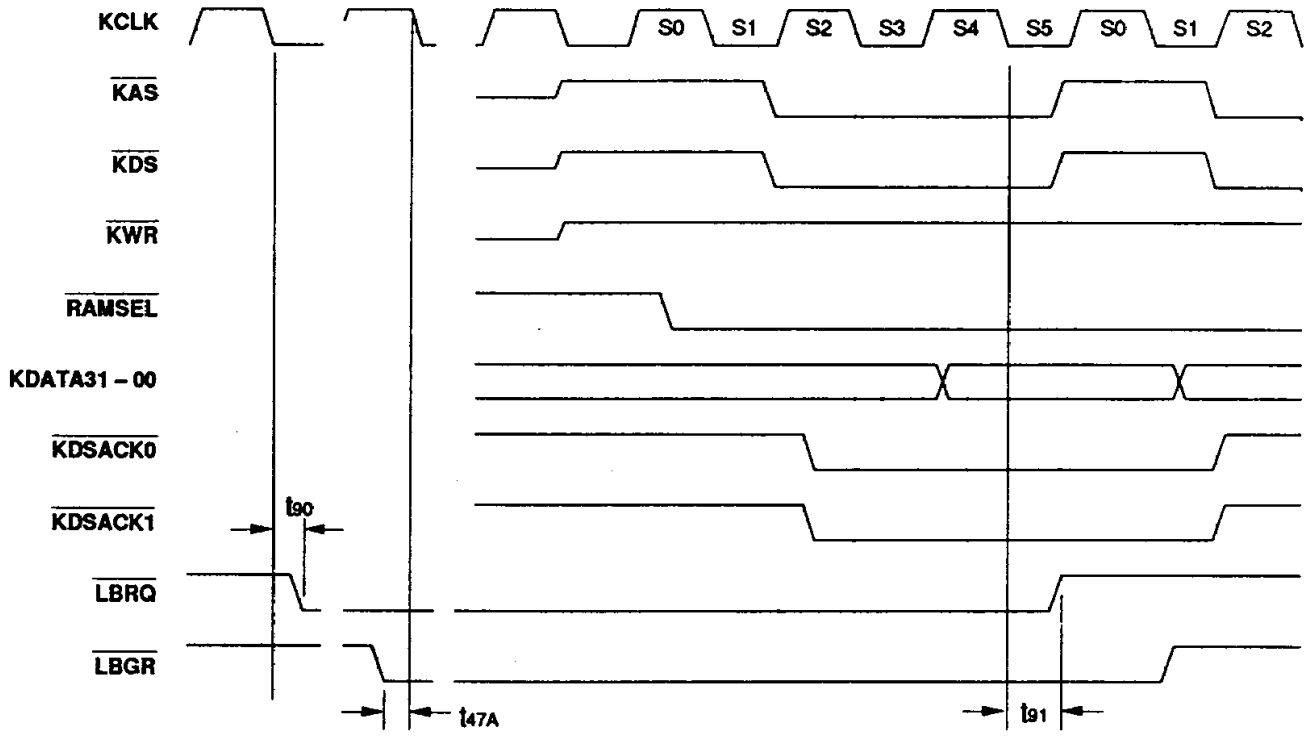
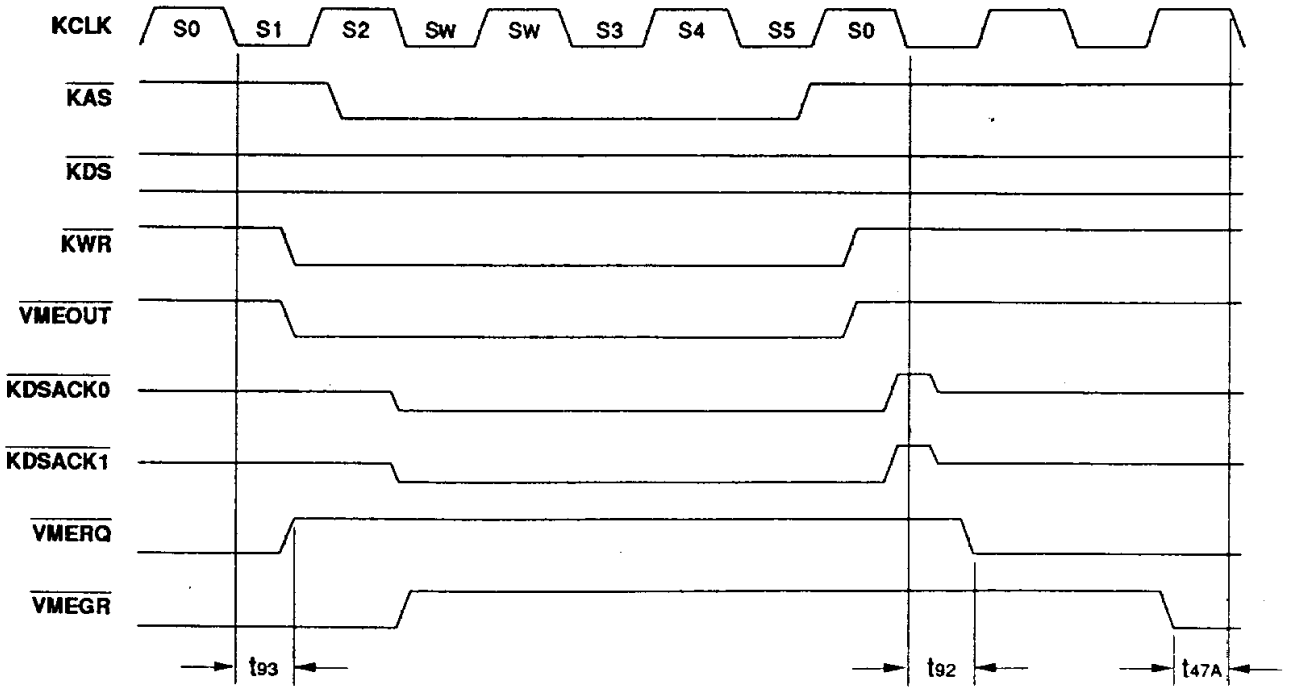


Figure 5 : DARF BUS ARBITRATION, CPU BUS REQUEST



Note: $\overline{\text{LBRQ}}$ is only released if another cycle is not pending. If $\overline{\text{LBRQ}}$ is released early, it is done 2 clocks after $\overline{\text{KAS}}$ is asserted.

Figure 6 : DARF BUS ARBITRATION, CPU BUS REQUEST



Note: $\overline{\text{VMEREQ}}$ is shown negated here for timing purposes only.

Table 6 : AC CHARACTERISTICS (DARF LOCAL BUS SLAVE INTERFACE)
(Commercial T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = –55° to +125°C, V_{DD} = 5V ± 10%)

Symbol	Description	Clk Count	Limits			Unit
			Min	Max		
				Com	Mil	
t_{60}	$\overline{KWR}$, etc valid to S3 low (Note 1)	-	-	26	40	ns
t_{61}	$\overline{KAS}$ setup to S3 low	-	5	-	-	ns
t_{61A}	$\overline{KAS}$ delay from S1 low	-	2	-	-	ns
t_{62}	KCLK low to data valid (read)	-	5	40	80	ns
t_{63}	S3 low to $\overline{KDSACKn}$ asserted	-	5	30	40	ns
t_{64}	S0 high to address invalid	-	0	-	-	ns
t_{65}	Address valid to S3 low (Note 1)	-	-	26	40	ns
t_{66}	S5 low to $\overline{KAS}$ high	-	0	-	-	ns
t_{67}	$\overline{KAS}$ high to $\overline{KDSACKn}$ high	-	3	20	30	ns
t_{68}	S0 low to $\overline{KDSACKn}$ tri-state	-	4	25	35	ns
t_{69}	$\overline{KAS}$ high to data tri-state (read)	-	5	35	40	ns
t_{70}	$\overline{KAS}$ high to $\overline{KWR}$ invalid (Note 1)	-	-	10	12	ns
t_{71}	Data setup time to S4 low	-	5	-	-	ns
t_{72}	$\overline{KAS}$ high to $\overline{KFC[2–0]}$ invalid	-	0	-	-	ns
t_{73}	$\overline{KAS}$ high to $\overline{KSIZE[1–0]}$ invalid (Note 1)	-	-	10	12	ns
t_{74}	$\overline{KAS}$ high to data invalid (read)	-	4	20	25	ns
t_{75}	KCLK low to $\overline{RAMSEL}$ low, VMEout	-	4	25	30	ns
t_{76}	$\overline{KAS}$ high to $\overline{RAMSEL}$ high, VMEout	-	3	20	25	ns
t_{77}	KCLK high to $\overline{RAMSEL}$ low, VMEin	-	4	21	25	ns
t_{78}	KCLK high to $\overline{RAMSEL}$ high, VMEin	-	3	20	25	ns
t_{79}	Address valid to $\overline{VSBSEL}$ low	-	23	40	55	ns
t_{80}	$\overline{KAS}$ high to $\overline{VSBSEL}$ high	-	2	15	20	ns
t_{81}	KCLK low to $\overline{LMINT}$ low	-	7	35	45	ns
t_{82}	KCLK low to $\overline{BIREL}$ low	-	4	25	30	ns
t_{83}	KCLK low to $\overline{BIREL}$ high	-	3	20	25	ns

Note:

1. This timing parameter is actually a *minimum* time which must be provided for the given operation condition.

4

Figure 7a : DARF SLAVE INTERFACE, CPU REGISTER READ

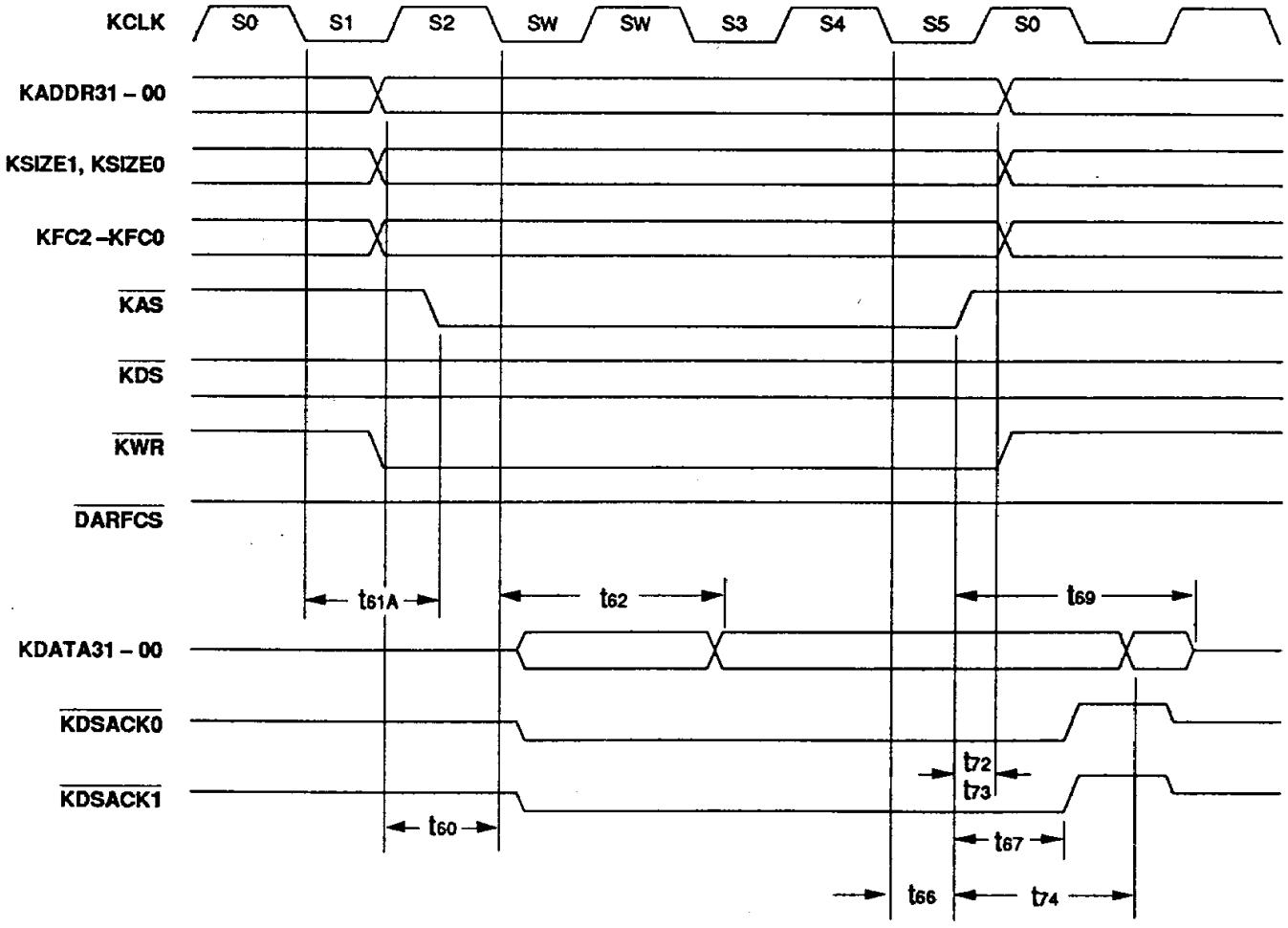


Figure 7B : DARF SLAVE INTERFACE, CPU REGISTER WRITE

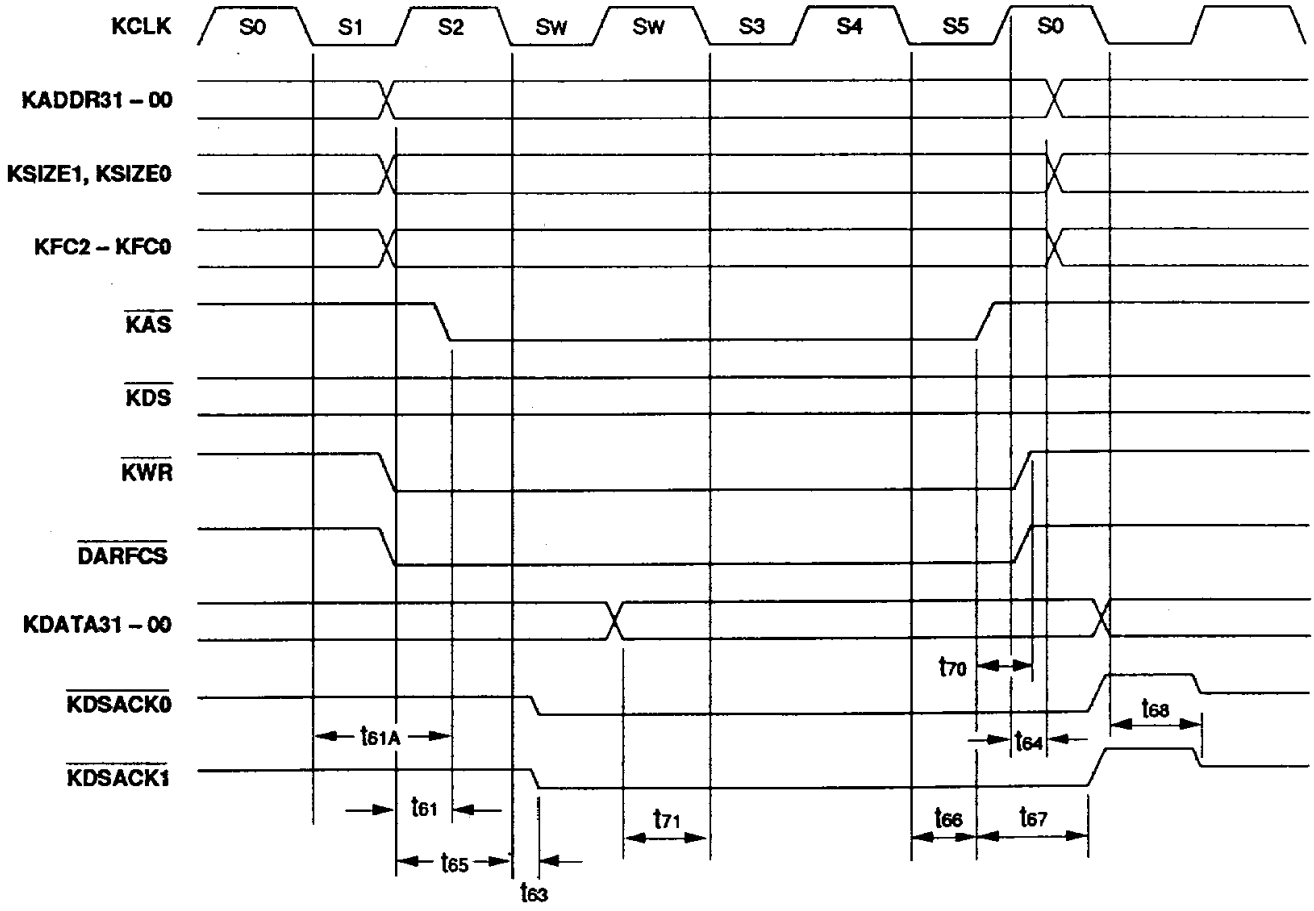
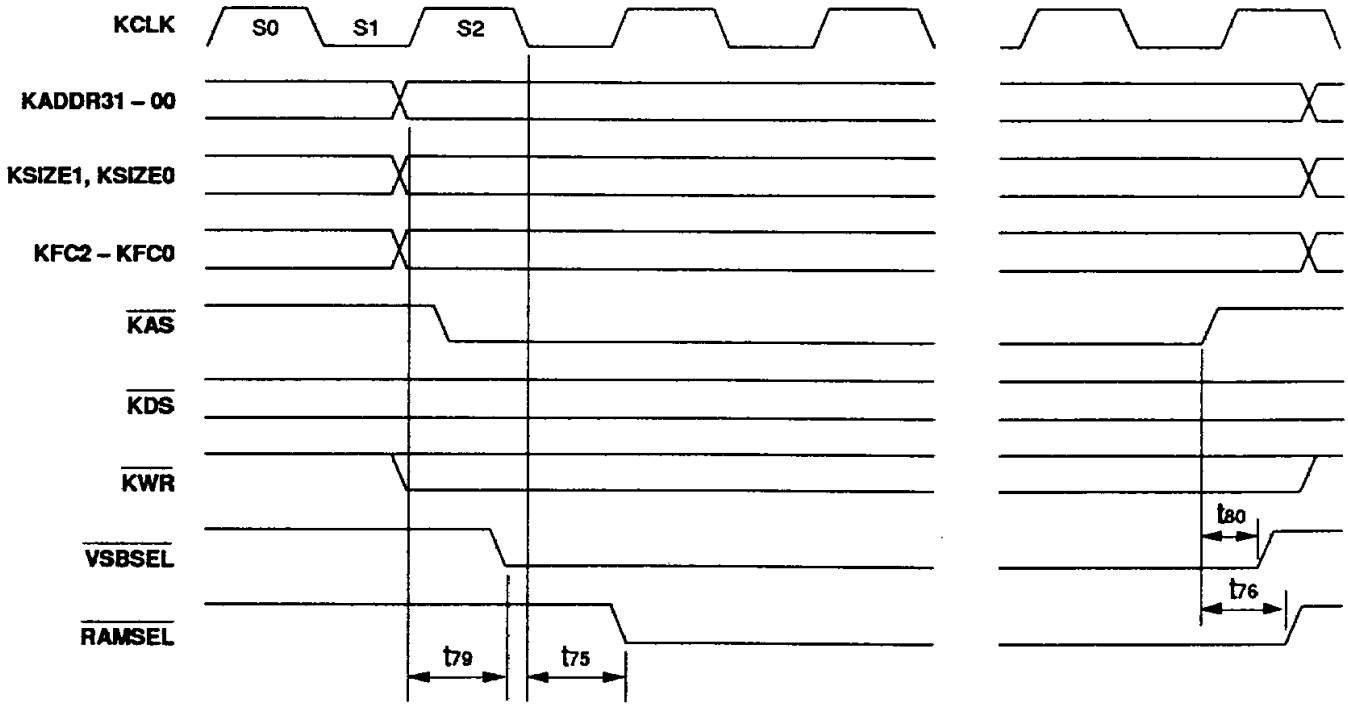
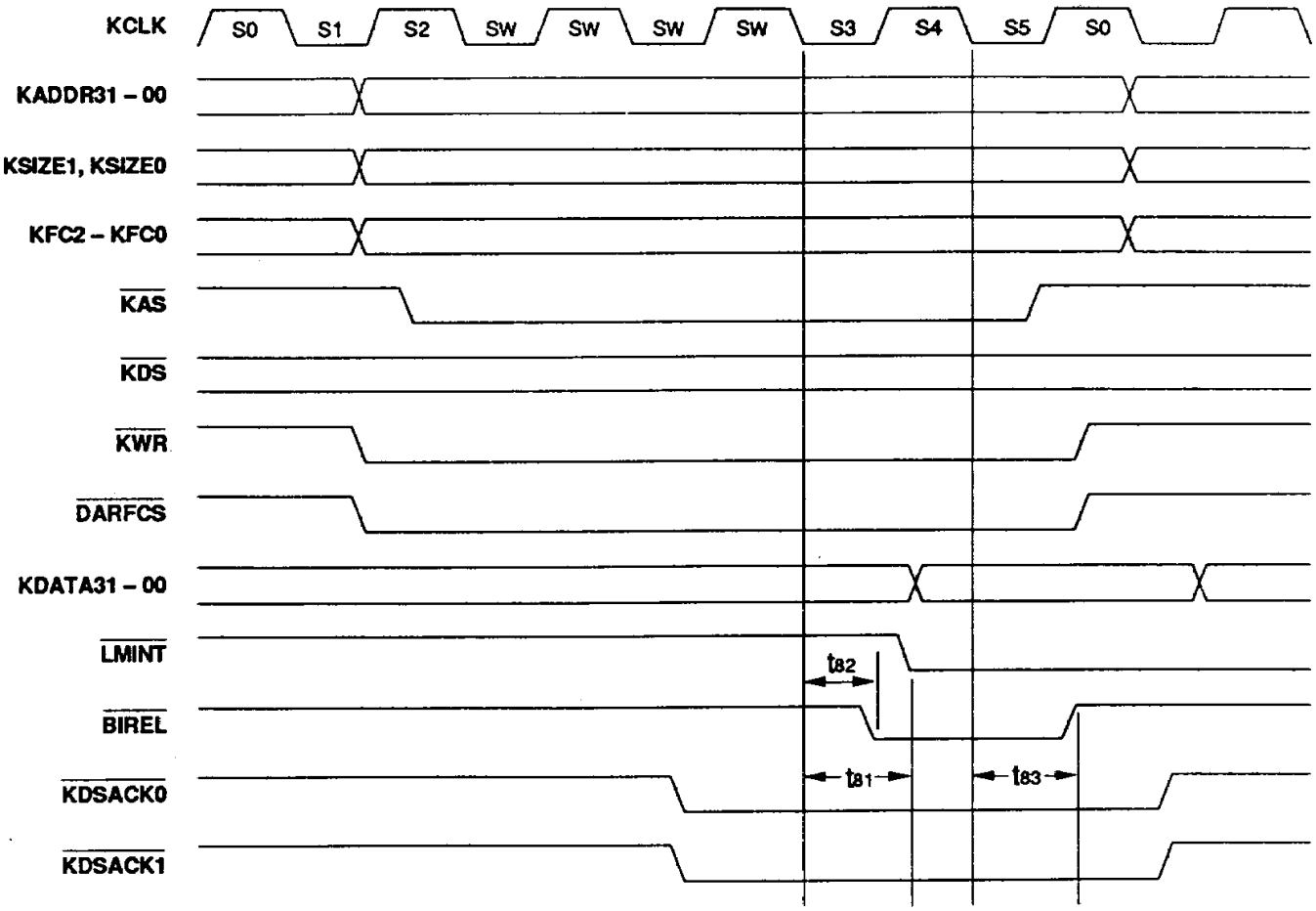


Figure 8 : DARF SLAVE INTERFACE, VSB and DVA DECODING



Note: $\overline{DVA}$ and $\overline{VSBSEL}$ will not be asserted on the same cycle. Both are shown here for illustration only.

Figure 9 : DARF SLAVE INTERFACE, CPU LOCATION MONITOR WRITE



Note:

This diagram assumes that the CPU is allowed access to the Location Monitor without waiting for the VMEbus to finish a write cycle.

If the VMEbus is writing to the FIFO, a minimum of two wait states are added, depending on the DSB* release time of the VME master.

If the LM FIFO is full, wait states are added indefinitely.

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Table 7 : AC CHARACTERISTICS (DARF VMEbus MASTERSHIP)
(Commercial T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = –55° to +125°C, V_{DD} = 5V ± 10%)

Symbol	Description	Clk Count	Limits			Unit
			Min	Max		
				Com	Mil	
t_{100}	S1 clock low to $\overline{\text{VMERQ}}$ asserted (Note 3)	4	3	20	25	ns
t_{101}	VADDR, VAM valid to $\overline{\text{VAS}}$ asserted	-	38	-	-	ns
t_{102}	$\overline{\text{VWR}}$ valid to $\overline{\text{VDSa}}$ asserted (Note 3)	1	30	-	-	ns
t_{103}	VDATA valid to $\overline{\text{VDSa}}$ asserted	-	40	-	-	ns
t_{104}	$\overline{\text{VAS}}$ asserted to $\overline{\text{VDSa}}$ asserted	-	2	-	-	ns
t_{105}	$\overline{\text{VDTACKI}}$ low to VDSb negated, Decoupled VME access	-	5	30	35	ns
t_{105A}	$\overline{\text{VDTACKI}}$ low to $\overline{\text{VDSb}}$ negated, Atomic VME access (Note 4)	-	45	70	75	ns
t_{106}	$\overline{\text{VDTACKI}}$ low to $\overline{\text{VAS}}$ negated, Decoupled VME access with cycle pending	-	5	35	40	ns
t_{107}	$\overline{\text{VDTACKI}}$ low to $\overline{\text{VAS}}$ negated, Decoupled VME access without cycle pending	-	15	85	100	ns
t_{107A}	$\overline{\text{VDTACKI}}$ low to $\overline{\text{VAS}}$ negated, Atomic VME access (Note 4, 5 & 6)	-	55	125		ns
t_{108}	VME buffers tri-state to $\overline{\text{VAS}}$ negated	-	3	20	25	ns
t_{109}	VADDROUT low to VME buffers tri-state	-	0	5	6	ns
t_{110}	VDATAOUT low to VDATA tri-state	-	1	7	9	ns
t_{111}	$\overline{\text{VMEGR}}$ low to VADDROUT, VDATAOUT asserted (Note 3)	2/3	4	25	30	ns
t_{112}	VADDROUT asserted to $\overline{\text{VAS}}$ low (Note 3)	1	45	75	85	ns
t_{113}	$\overline{\text{VAS}}$, $\overline{\text{VDSn}}$ minimum high time (Note 4)	-	45	-	-	ns
t_{114}	VME cycle time, $\overline{\text{VAS}}$ to $\overline{\text{VAS}}$ (Note 1)	-	101	173	194	ns
t_{115}	$\overline{\text{VDTACKI}}$ high to $\overline{\text{VDSa}}$ asserted	-	5	-	-	ns
t_{116}	$\overline{\text{VDSa}}$ low to $\overline{\text{VDTACKI}}$ asserted	-	20	-	-	ns
t_{117}	$\overline{\text{VDSa}}$ low to $\overline{\text{VDSb}}$ low (Note 7)	-	0	5	7	ns
t_{118}	$\overline{\text{VDTACKI}}$ low to $\overline{\text{KDSACKn}}$ asserted (Note 2, 4)	-	45	75	80	ns
t_{119}	$\overline{\text{VMEGR}}$ low to $\overline{\text{VAS}}$ asserted (Note 3, 4 & 8)	3/4	50	100	115	ns
t_{120}	AOUT edge to ADLY edge	-	37	43	43	ns
t_{121}	BOUT high to BDLY high	-	37	43	43	ns
t_{122}	$\overline{\text{VDTACKI}}$ low to $\overline{\text{VDTKDLY}}$ low	-	35	45	45	ns

Notes: see next page

Notes:

1. This cycle time applies only to the DARF operating in loopback mode. This time represents the maximum obtainable transfer rate under *ideal* conditions.
2. This parameter applies to Atomic VME accesses only.
3. This timing parameter is the sum of the number listed and product of the CLK COUNT times the period of the CPU clock.
   eg: $t_{21} = -5 + (0.5 \times t_{KCLK})$ ns
4. This parameter assumes that a 40ns delay line is used to generate ADLY, BDLY, $\overline{\text{VDSDLY}}$, and $\overline{\text{VDTKDLY}}$.
5. In the case of RMW cycles, the release time of $\overline{\text{KRMC}}$ controls the release of $\overline{\text{VAS}}$ when the TASCON bit is set. The release of $\overline{\text{KRMC}}$ controls the release of VADDR, VAM, and $\overline{\text{VRMC}}$ regardless of the state of the TASCON bit.
6. The minimum low time for VAS is $(3 \times t_{KCLK} - 5\text{ns})$ and may override this parameter, depending on the Slave Response time.
7. If the loading on the two outputs is equal, the skew can be reduced to 2ns.
8. This parameter assumes that previous VMEbus cycle is complete and that VMEbus ownership can be taken without further delay.

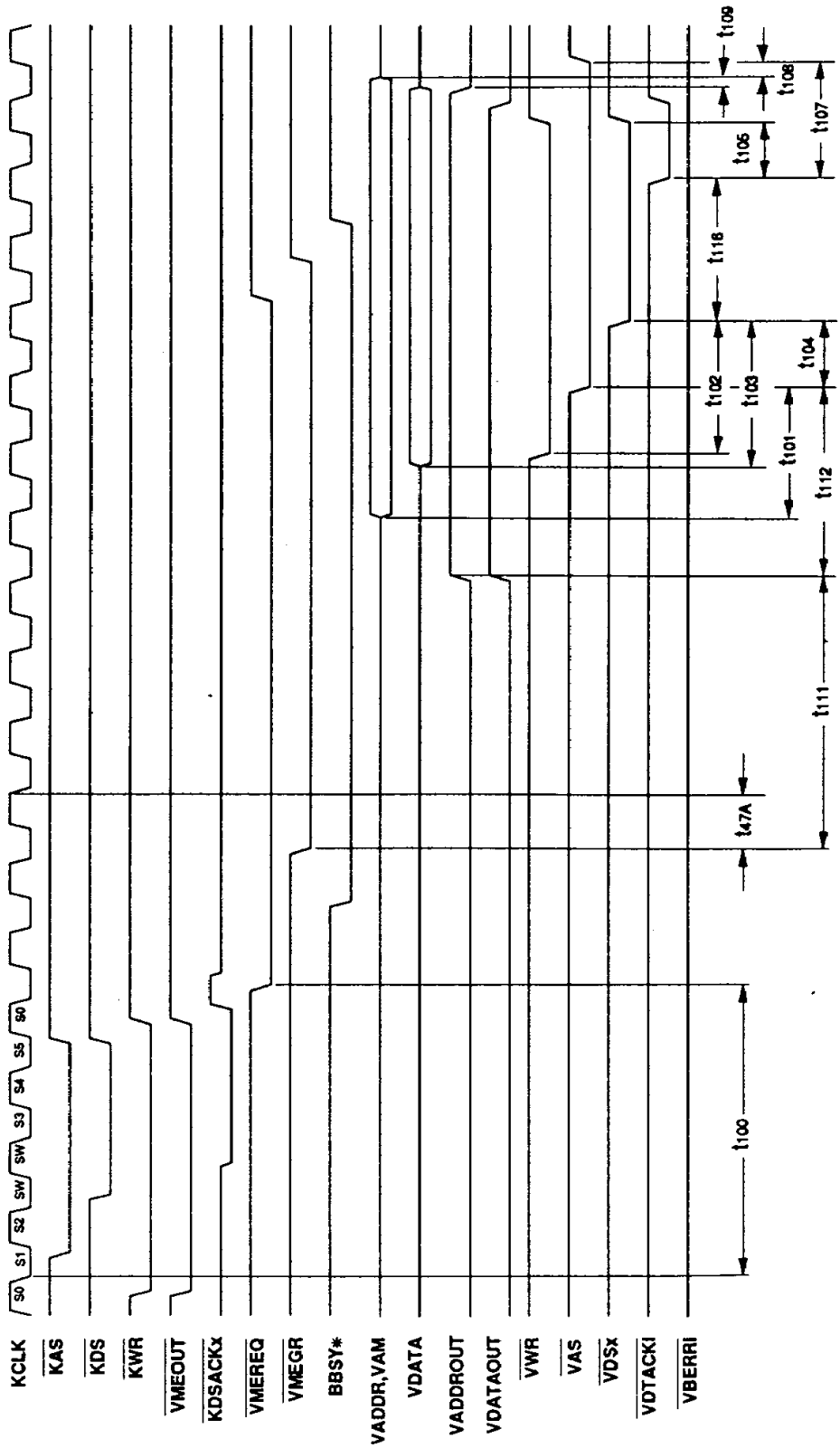

Figure 10a : DARF VME MASTER INTERFACE, SINGLE DECOUPLED WRITE

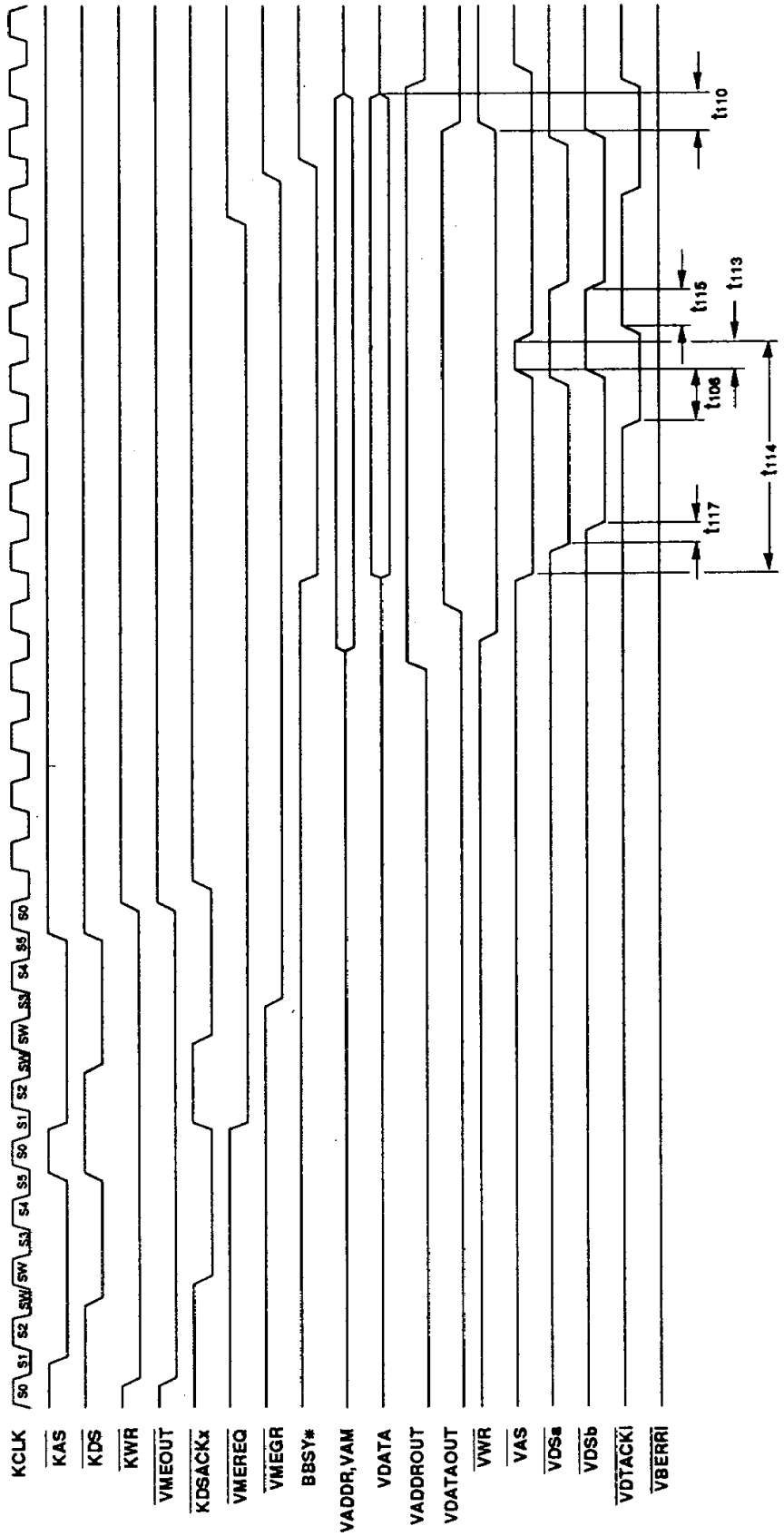

Figure 10a : DARF VME MASTER INTERFACE, MULTIPLE DECOUPLED WRITE

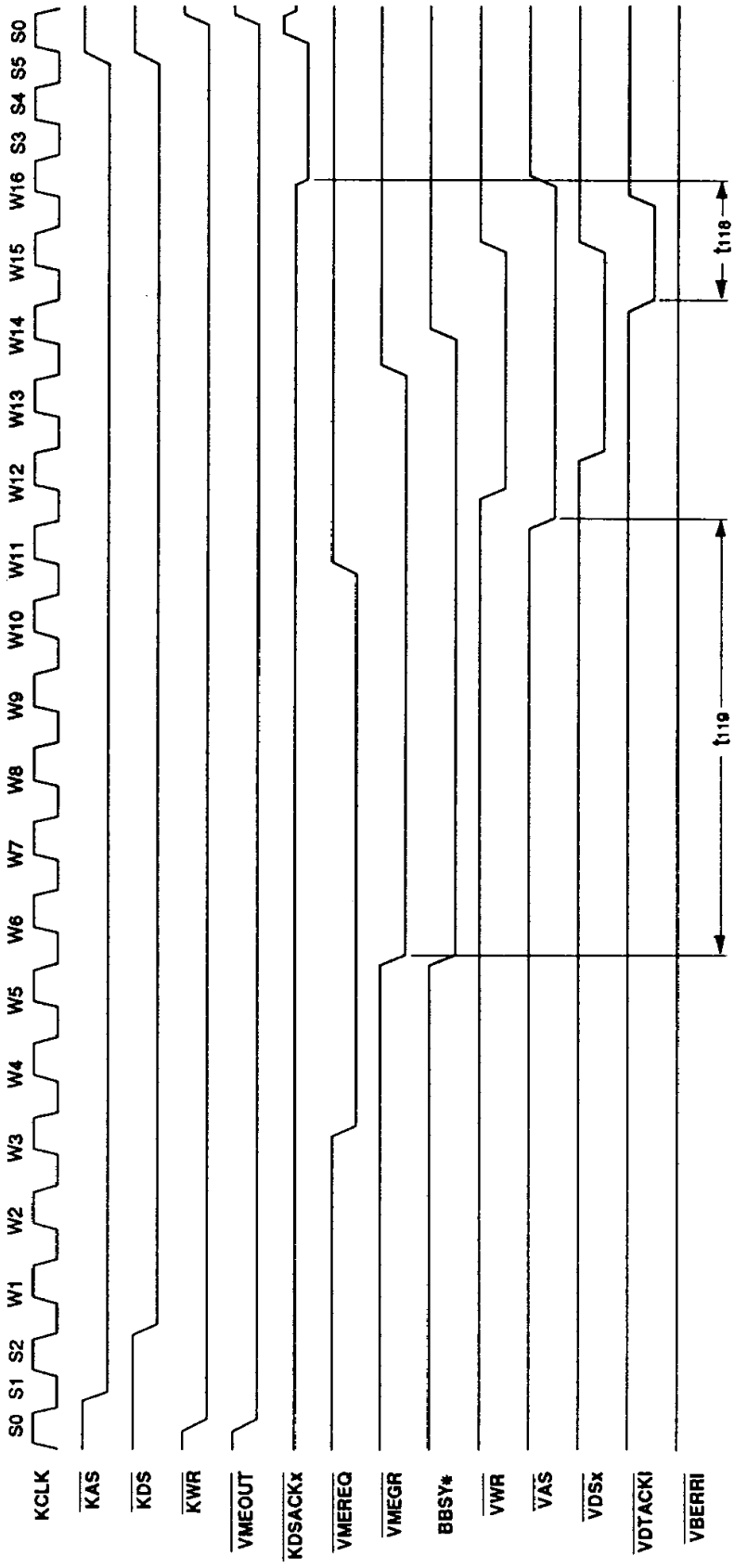

Figure 11 : DARF VME MASTER INTERFACE, ATOMIC WRITE

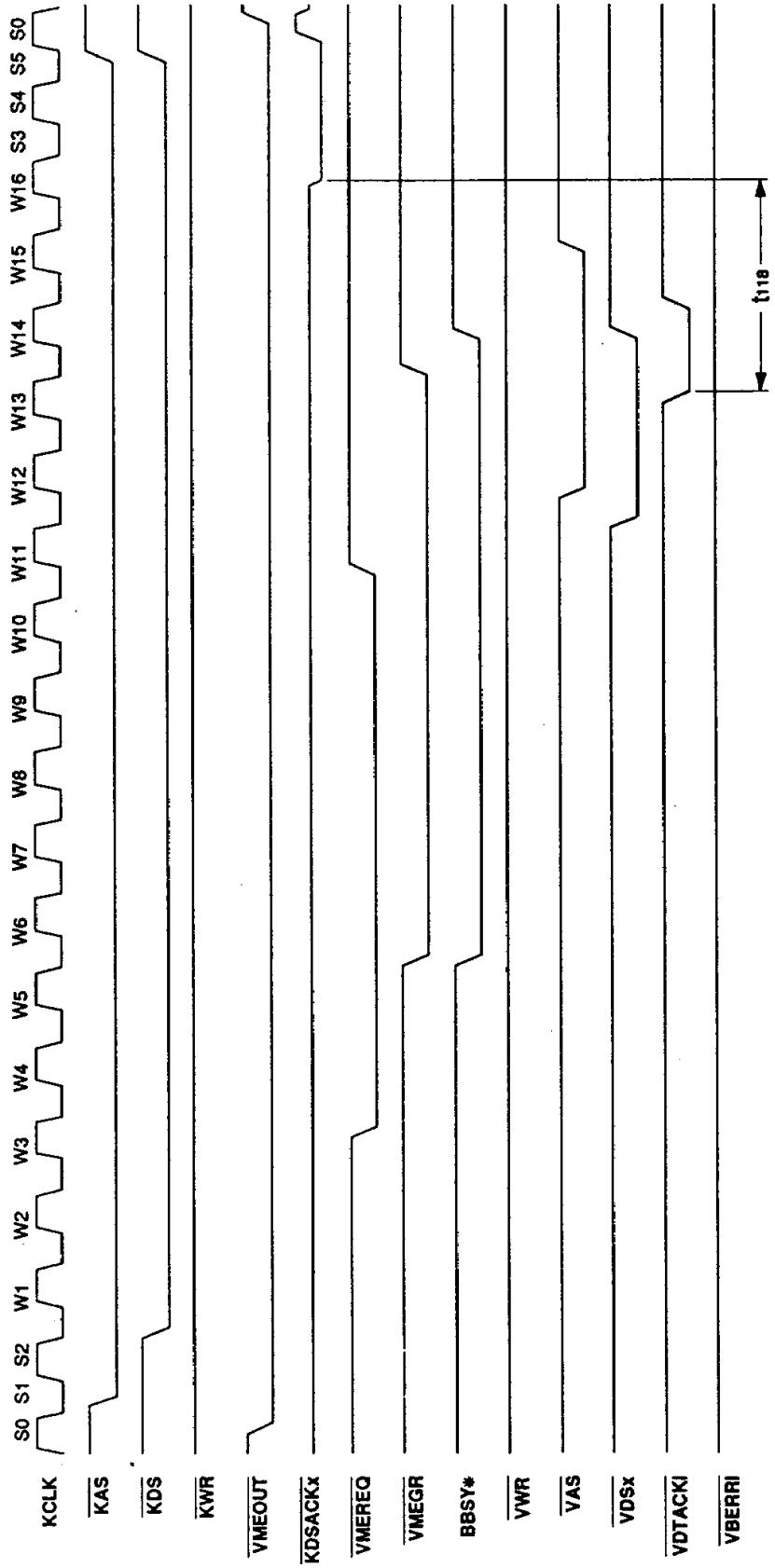

Figure 12 : DARF VME MASTER INTERFACE, SINGLE READ

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Figure 13 : DARF DELAY LINE TIMING, VMEbus MASTER CYCLES

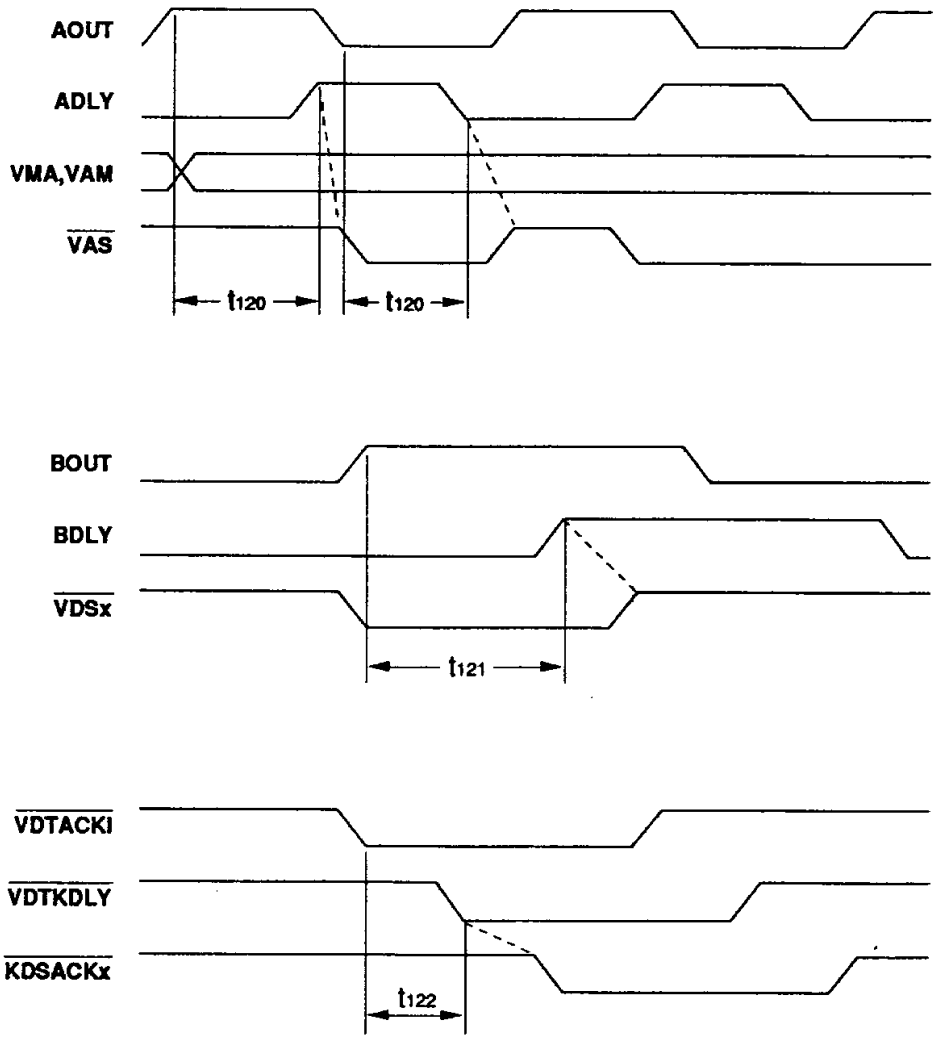

Figure 14 : DARF MASTER INTERFACE, VMEbus Iack CYCLE

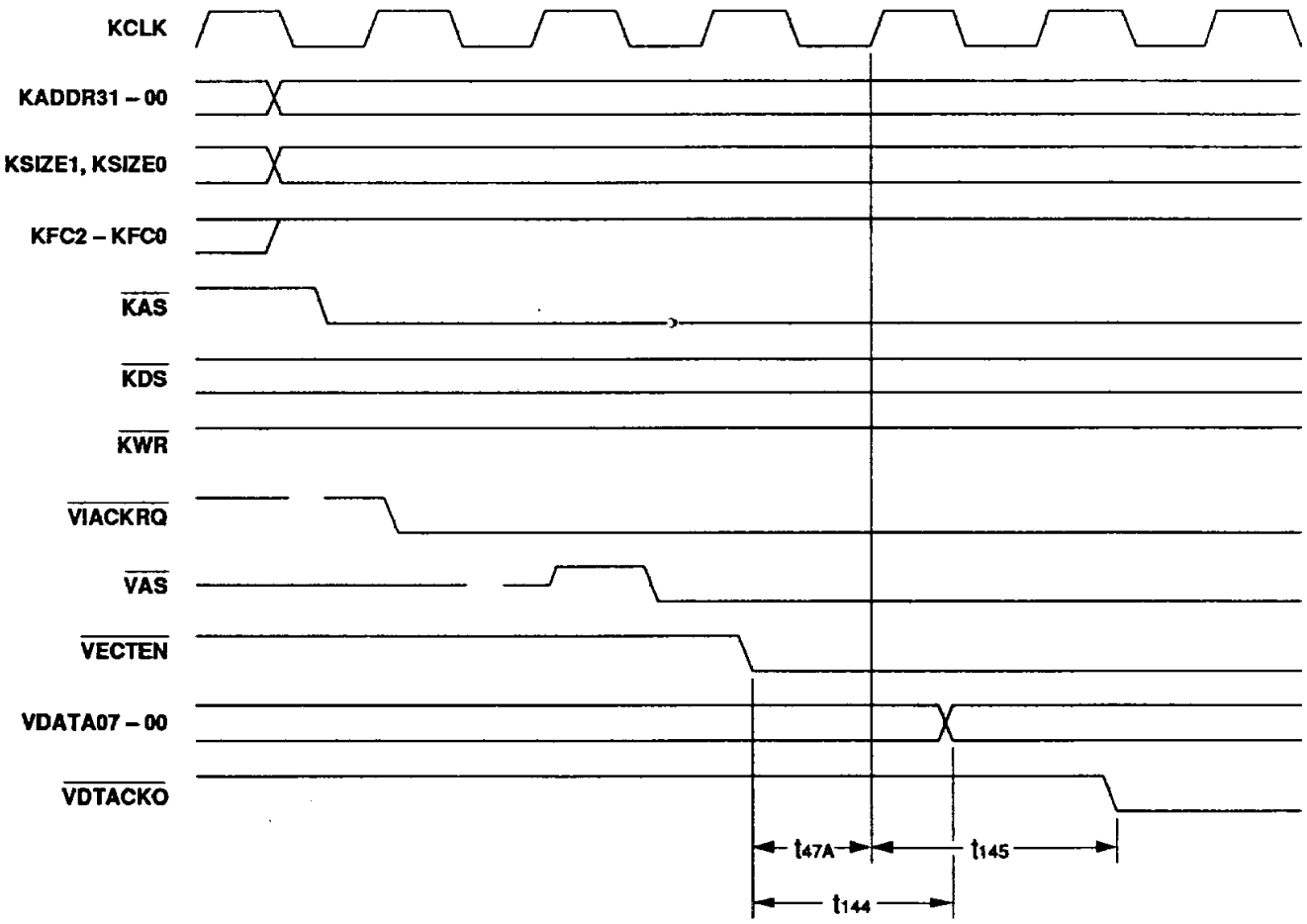

Table 8 : AC CHARACTERISTICS (DARF VMEbus SLAVE INTERFACE)
(Commercial T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = –55° to +125°C, V_{DD} = 5V ± 10%)

Symbol	Description	Clk Count	Limits			Unit
			Min	Max		
				Com	Mil	
t_{130}	VADDR, VAM, $\overline{\text{VLWORD}}$, $\overline{\text{VIACK}}$ setup to $\overline{\text{VAS}}$ low	-	5	-	-	ns
t_{131}	$\overline{\text{VAS}}$ low to $\overline{\text{VASDLY}}$ low	-	15	25	25	ns
t_{132}	VDATA, $\overline{\text{VWR}}$ setup to $\overline{\text{VDSa}}$ low	-	5	-	-	ns
t_{133}	$\overline{\text{VDSn}}$ edge to $\overline{\text{VDSDLY}}$ edge	-	35	45	45	ns
t_{134}	SR, RXFIFO write without holdoff (Note 1 & 4)	-	45	65	70	ns
t_{135}	SR, LM write without holdoff (Note 1 & 4)	3/4	50	75	80	ns
t_{136}	SR, LM write with CPU holdoff (Note 1 & 4)	6/7	50	75	80	ns
t_{137}	SR, Atomic (minimum) (Note 5)	11.5/12.5	4	35	40	ns
t_{138}	$\overline{\text{VDSa}}$ low to $\overline{\text{LMINT}}$ asserted (Note 1 & 4)	1.5/2.5	50	85	90	ns
t_{139}	$\overline{\text{VDSa}}$ low to $\overline{\text{VBERRO}}$ asserted, illegal VMEin cycle (Note 2, 4 & 6)	-	45	65	70	ns
t_{140}	$\overline{\text{VDSb}}$ high to $\overline{\text{VDTACKO}}$ negated, VMEbus write cycle to DARF	-	5	30	35	ns
t_{140A}	$\overline{\text{VDSb}}$ high to $\overline{\text{VDTACKO}}$ negated, VMEbus read cycle to DARF (Note 4)	-	45	70	75	ns
t_{141}	VDATAOUT negated to $\overline{\text{VDTACKO}}$ negated	-	–1	0	1	ns
t_{142}	VADDR, VAM, $\overline{\text{VLWORD}}$, $\overline{\text{VIACK}}$ hold time from $\overline{\text{VDTACKO}}$ low	-	0	-	-	ns
t_{143}	$\overline{\text{VDSn}}$ low to $\overline{\text{LBRQ}}$ asserted, Atomic VMEin cycle	2/3	3	20	25	ns
t_{144}	$\overline{\text{VECTEN}}$ low to VDATA asserted (Note 3)	0.5/1.5	5	35	40	ns
t_{145}	$\overline{\text{VECTEN}}$ low to $\overline{\text{VDTACKO}}$ asserted (Note 3)	2/3	3	20	25	ns
t_{146}	$\overline{\text{VDSDLY}}$ low to $\overline{\text{VDTACKO}}$ asserted, Decoupled VMEin cycle (Note 1)	-	4	25	30	ns
t_{147}	$\overline{\text{KDSACKn}}$ low to $\overline{\text{VDTACKO}}$ asserted BERRCHK = 0 (Note 3)	1.5/2.5	5	35	40	ns
t_{147A}	$\overline{\text{KDSACKn}}$ low to $\overline{\text{VDTACKO}}$ asserted BERRCHK = 1 (Note 3)	2.5/3.5	5	35	40	ns
t_{148}	KCLK high to $\overline{\text{VBERRO}}$ or $\overline{\text{VDTACKO}}$ asserted, Atomic VMEin cycle	-	5	35	40	ns
t_{149}	Pulse width, late $\overline{\text{KBERR}}$ width (Note 7)	-	10	t_{CLK}	t_{CLK}	ns

Notes: see next page

Notes:

1. This parameter assumes that there is space in the Message/Receive FIFO to receive the data.
2. This parameter applies only to accesses to protected memory and Message FIFO read cycles.
3. This timing parameter is the sum of the number listed and product of the CLK COUNT times the period of the CPU clock.

   eg: $t_{21} = -5 + (0.5 \times t_{KCLK})$ ns
4. This parameter assumes that a 40ns delay line is used to generate ADLY, BDLY, $\overline{\text{VDSDLY}}$, and $\overline{\text{VDTKDLY}}$.
5. This slave response parameter assumes that the $\overline{\text{LBGR}}$ is returned in time to be sampled on the next falling edge of KCLK after $\overline{\text{LBRa}}$ is asserted. Additional clocks will have to be added to account for bus arbitration time.
6. This parameter applies when an illegal access to the DARF is attempted by the VMEbus, i.e, read access to the location monitor or illegal access to protected memory.
7. When $\overline{\text{KBERR}}$ is received late, it is latched internally for the DARF's use. $\overline{\text{KBERR}}$ needs to be negated before the next local bus cycle starts.

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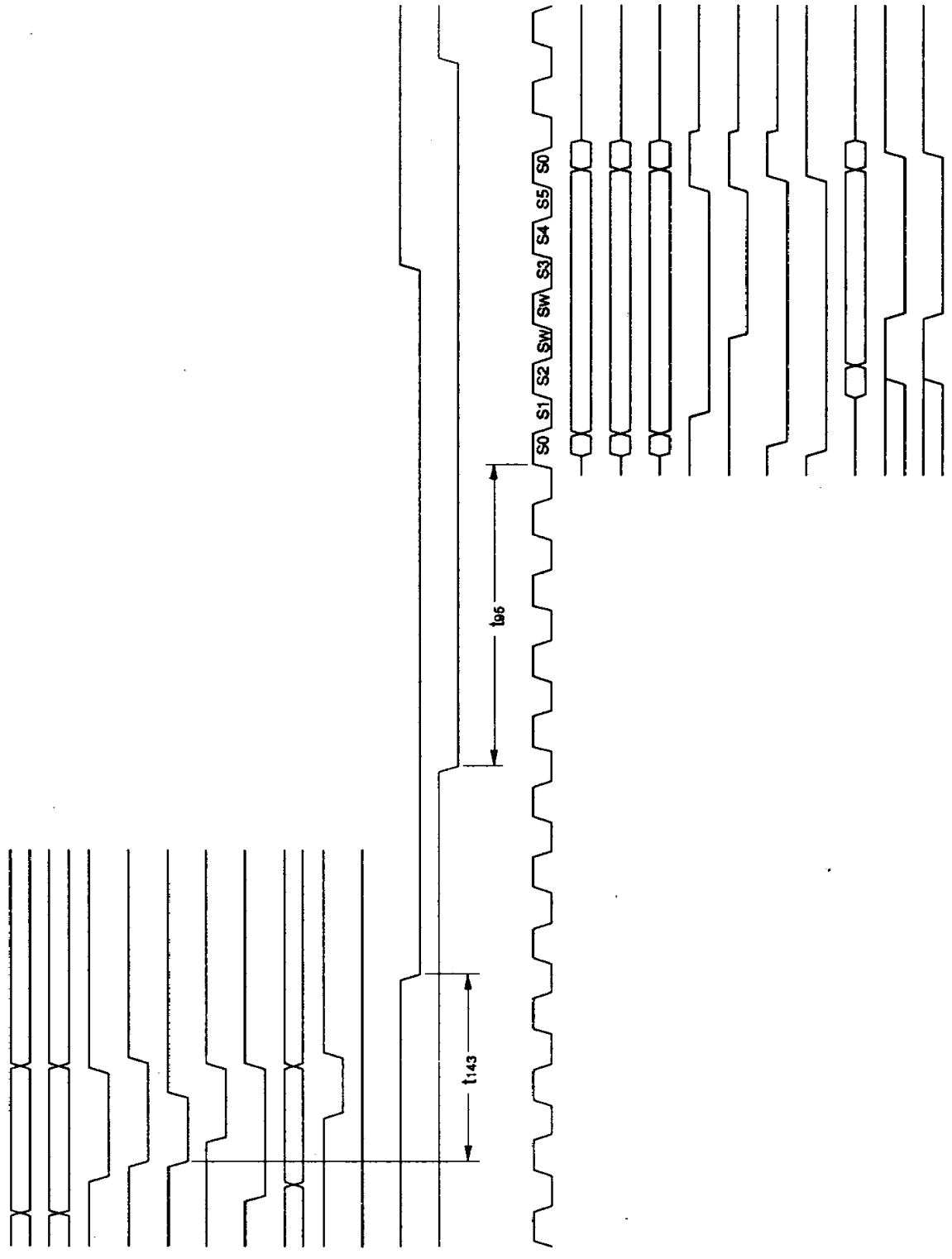


Figure 15 : DARF SLAVE INTERFACE, VME DECOUPLED WRITE

Figure 16 : DARF VME SLAVE INTERFACE, DECOUPLED WRITE

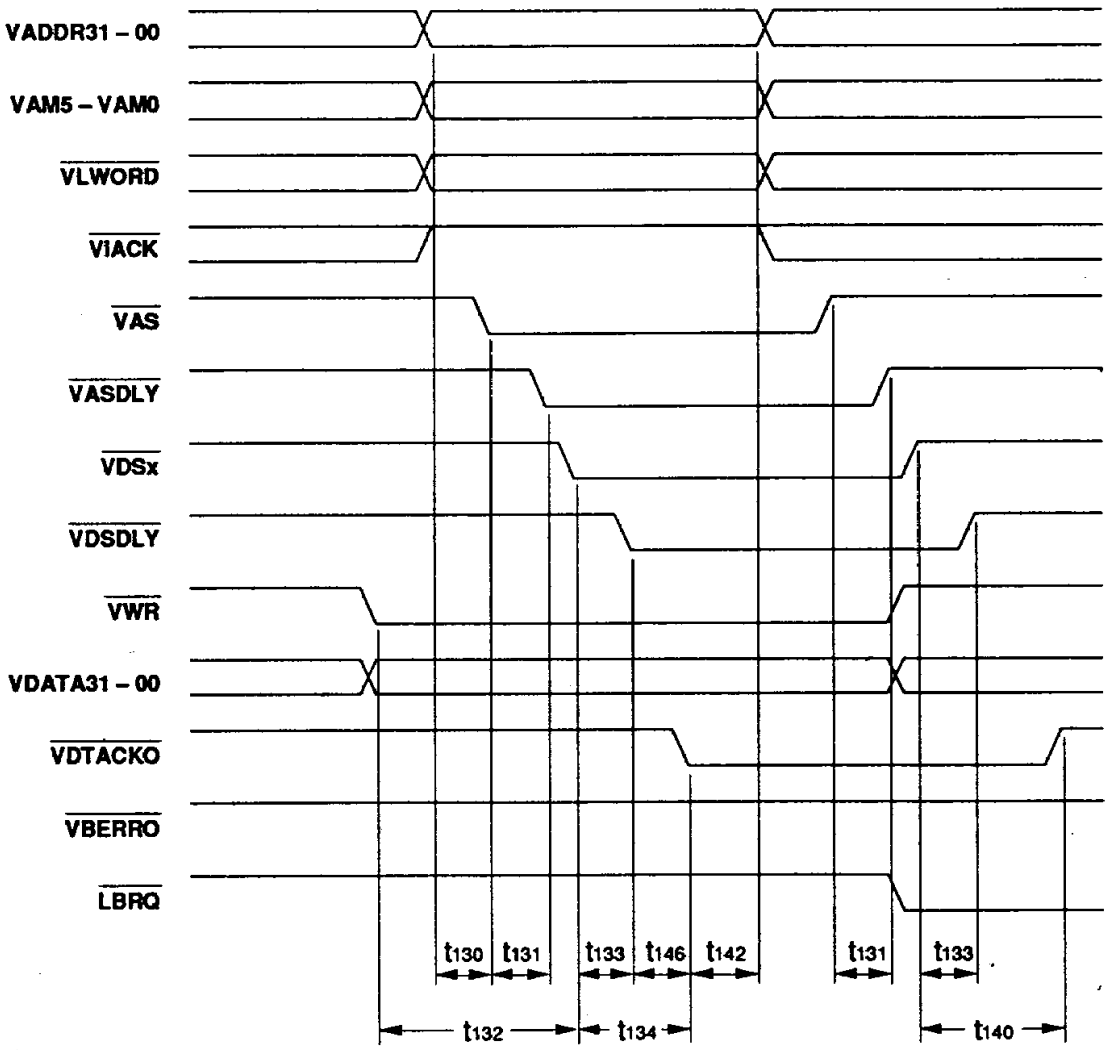
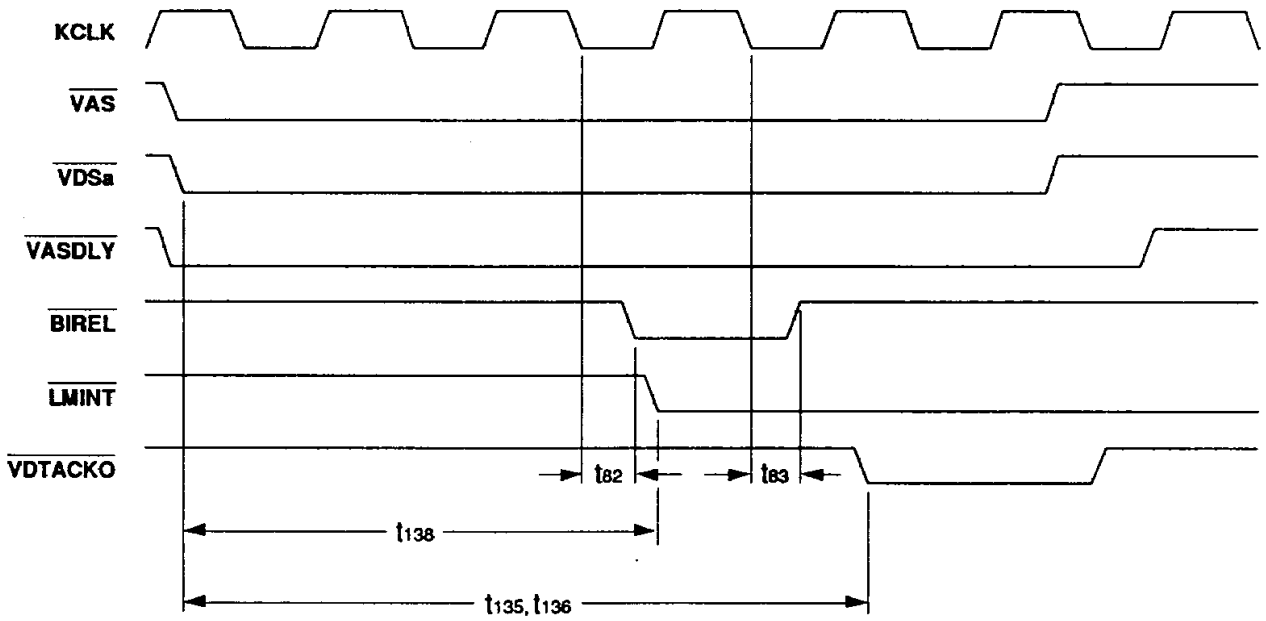


Figure 17 : VMEbus SLAVE INTERFACE, LOCATION MONITOR WRITE



Note:

The Slave Response time for Location Monitor writes is extended an additional 3 clocks if the CPU is writing to the FIFO when the VMEin cycle occurs.

Figure 18a : DARF SLAVE INTERFACE, MEMORY READ with BERRCHK CLEARED

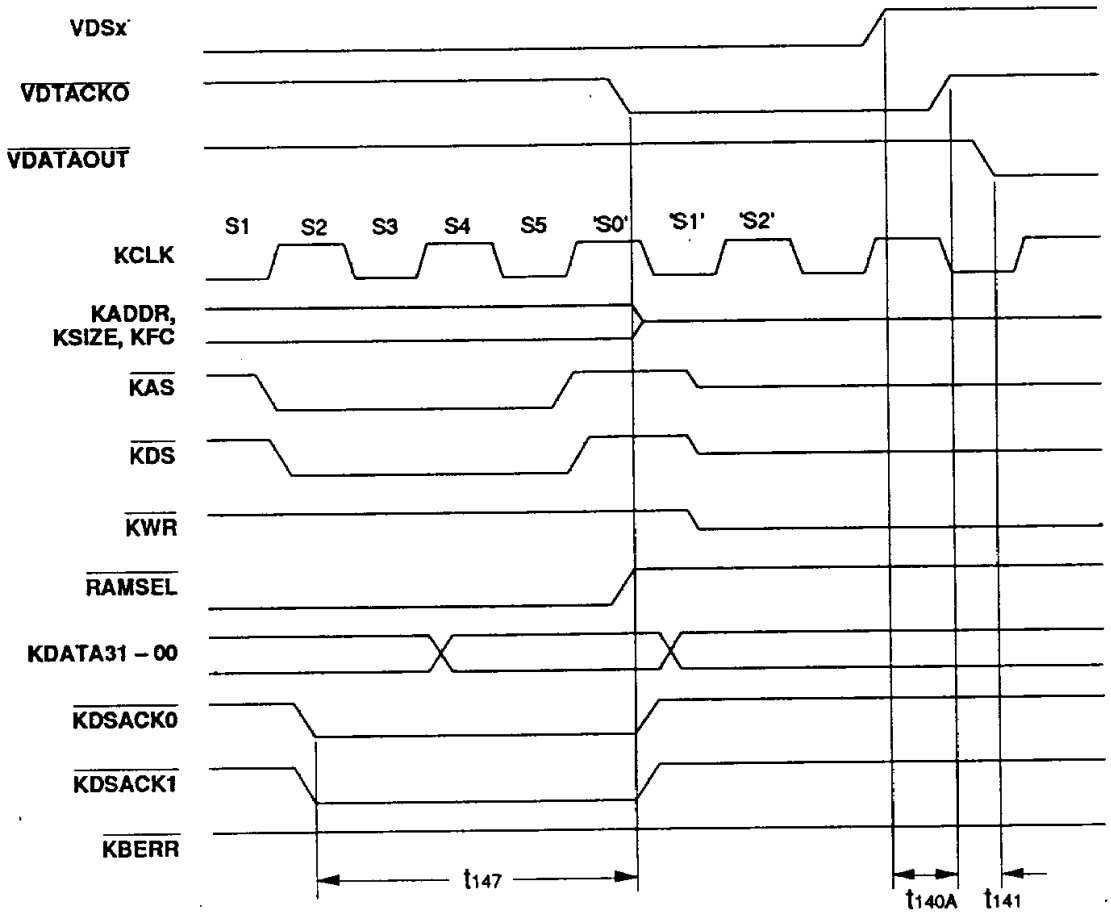


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Figure 18b : DARF SLAVE INTERFACE, MEMORY READ with BERRCHK SET

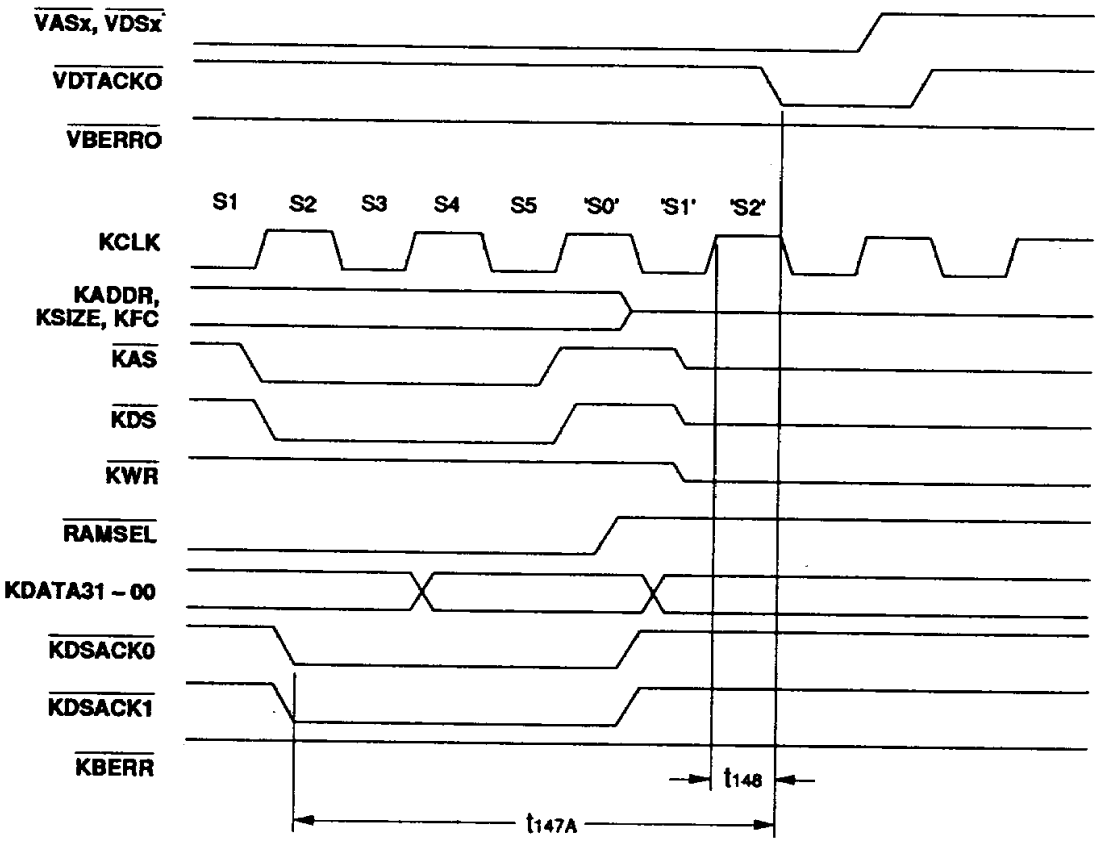

Figure 18b : DARF SLAVE INTERFACE, MEMORY READ with LATE KBERR

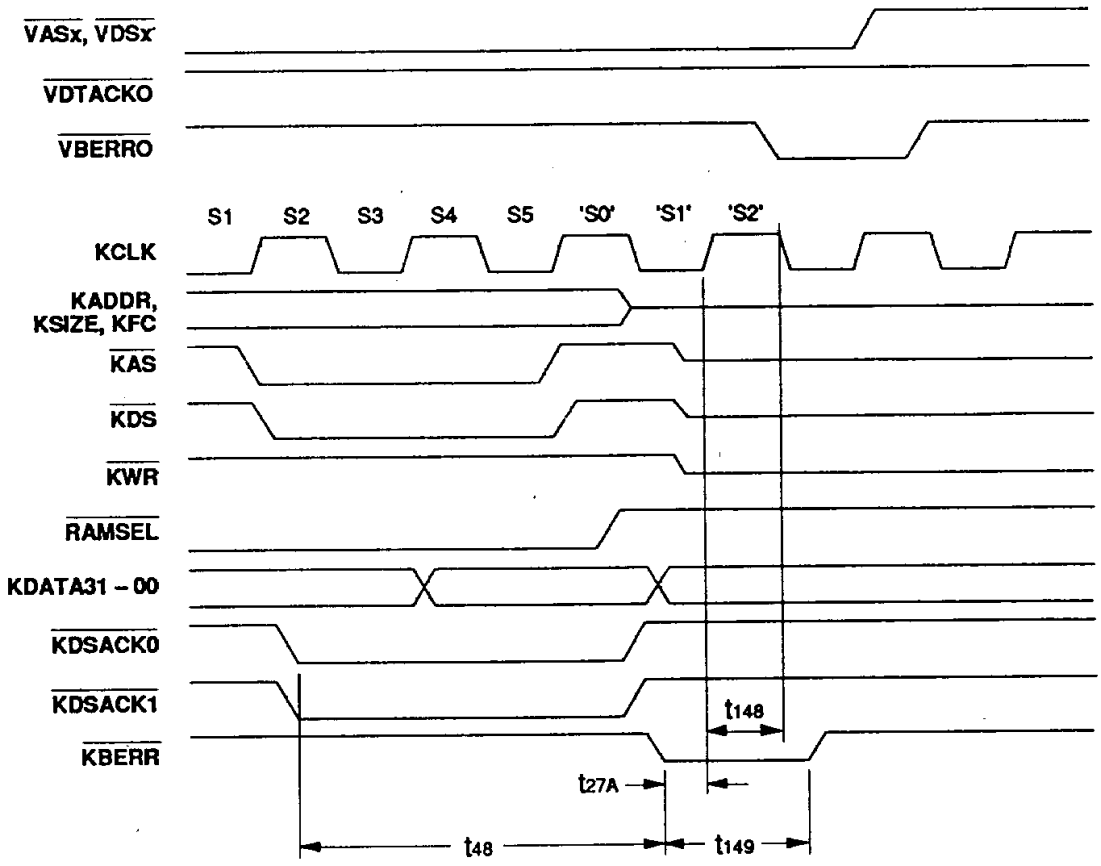

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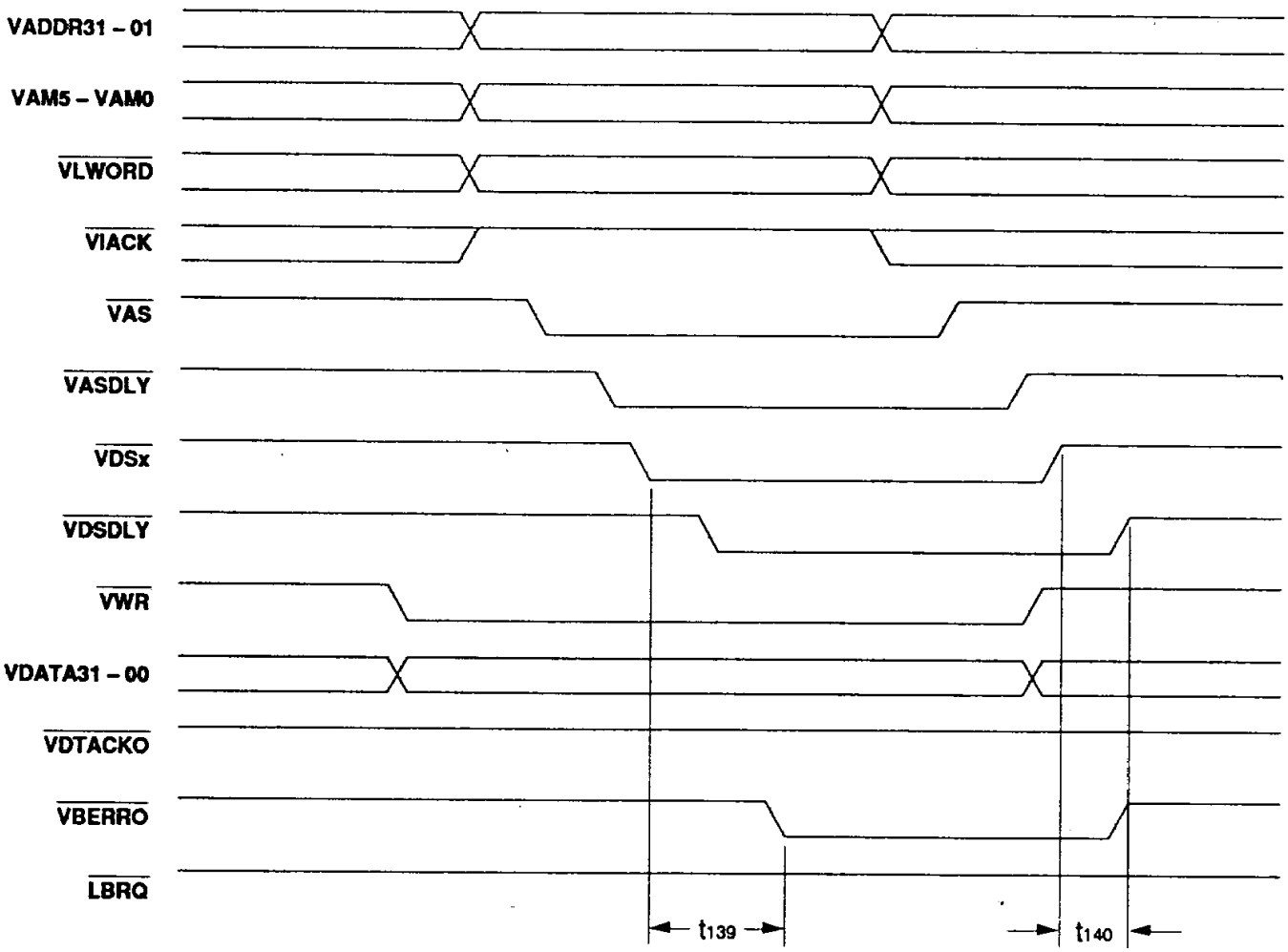
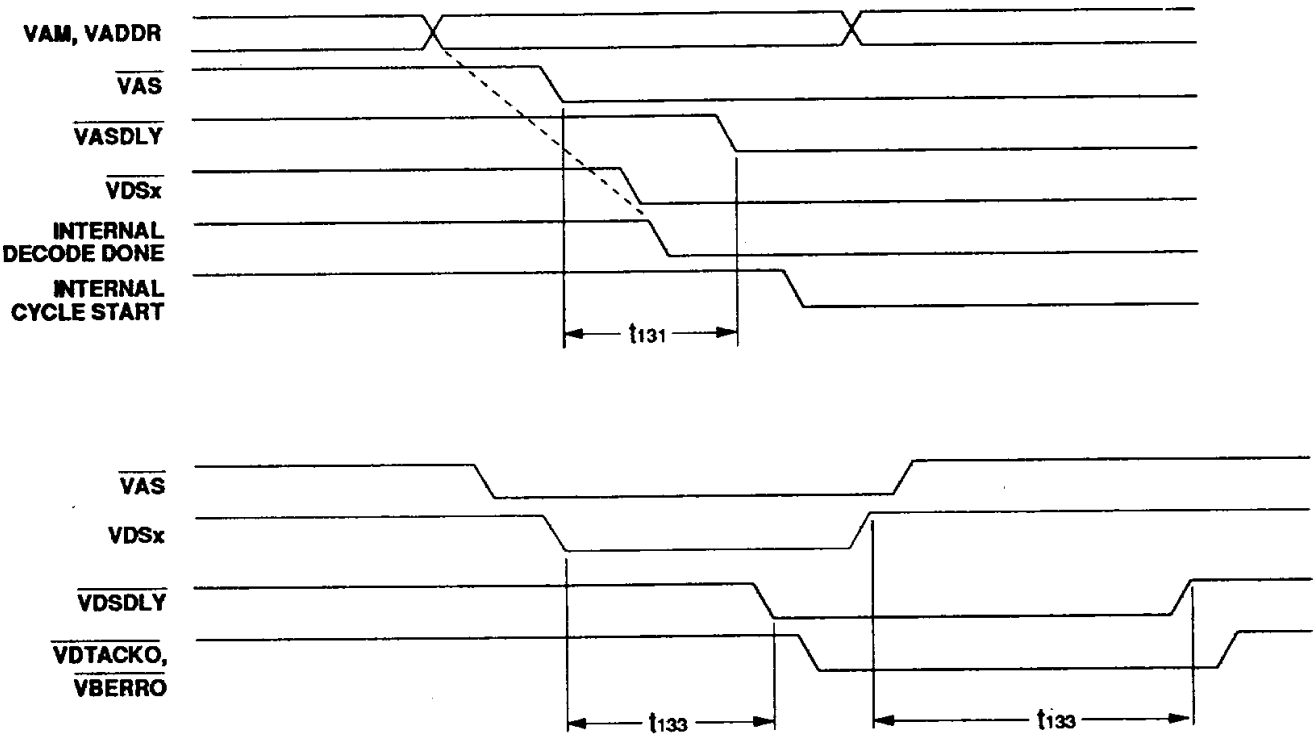
Figure 20 : DARF VME SLAVE INTERFACE, ILLEGAL ACCESS



Note:
This timing applies to VMEbus attempts to read the Location Monitor or to illegally access protected memory.

Figure 21 : DARF DELAY LINE TIMING, VMEbus SLAVE CYCLES



Note:
On VMEbus write cycles to the DARF, VDTACK0 is negated with VDSB instead of VDSDLY.

Table 9 : DC CHARACTERISTICS
(Commercial T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = –55° to +125°C, V_{DD} = 5V ± 10%)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$				
	CTTL		-	1	10	µA
	CTTL PU		-	-	40	µA
I_{IL}	Input LOW Current	$V_{IN}=V_{SS}$				
	CTTL		-	–1	–10	µA
	CTTL PU		–8	–30	–100	µA
I_{OZ}	Tri-state Output Leakage Current		–10	±1	10	µA
V_{IL}	Input LOW Voltage					
	CTTL		-	-	0.8	V
	CTTL PU		-	-	0.8	V
V_{IH}	Input HIGH voltage					
	CTTL	0° to 70°C	2.0	-	-	V
	CTTL PU	0° to 70°C	2.0	-	-	V
	CTTL	–55° to +125°C	2.25	-	-	V
	CTTL PU	–55° to +125°C	2.25	-	-	V
V_{OH}	Voltage Output HIGH	0° to 70°C				
	TP2	I_{OH} = –2 mA	2.4	4.5	-	V
	TP4	I_{OH} = –4 mA	2.4	4.5	-	V
	TS4	I_{OH} = –4 mA	2.4	4.5	-	V
	TS4 SR	I_{OH} = –4 mA	2.4	4.5	-	V
	TS6	I_{OH} = –6 mA	2.4	4.5	-	V
	TS8	I_{OH} = –8 mA	2.4	4.5	-	V
V_{OH}	Voltage Output HIGH	–55° to 125°C				
	TP2	I_{OH} = –1.6 mA	2.4	4.5	-	V
	TP4	I_{OH} = –3.2 mA	2.4	4.5	-	V
	TS4	I_{OH} = –3.2 mA	2.4	4.5	-	V
	TS4 SR	I_{OH} = –3.2 mA	2.4	4.5	-	V
	TS6	I_{OH} = –4.8 mA	2.4	4.5	-	V
	TS8	I_{OH} = –6.4 mA	2.4	4.5	-	V

Table 9 : DC CHARACTERISTICS CON'T
(Commercial T_A = 0° to +70°C, V_{DD} = 5V ± 5%, Military T_A = –55° to +125°C, V_{DD} = 5V ± 10%)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
V_{OL}	Voltage Output LOW	0° to 70°C				
	TP2	I_{OL} = 2 mA	-	0.2	0.4	V
	TP4	I_{OL} = 4 mA	-	0.2	0.4	V
	TS4	I_{OH} = 4 mA	-	0.2	0.4	V
	TS4 SR	I_{OH} = 4 mA	-	0.2	0.4	V
	TS6	I_{OL} = 6 mA	-	0.2	0.4	V
	TS8	I_{OL} = 8 mA	-	0.2	0.4	V
	OD8	I_{OL} = 8 mA	-	0.2	0.4	V
	OD12	I_{OL} = 12 mA	-	0.2	0.4	V
V_{OL}	Voltage Output LOW	–55° to 125°C				
	TP2	I_{OL} = 1.6 mA	-	0.2	0.4	V
	TP4	I_{OL} = 3.2 mA	-	0.2	0.4	V
	TS4	I_{OH} = 3.2 mA	-	0.2	0.4	V
	TS4 SR	I_{OH} = 3.2 mA	-	0.2	0.4	V
	TS6	I_{OL} = 4.8 mA	-	0.2	0.4	V
	TS8	I_{OL} = 6.4 mA	-	0.2	0.4	V
	OD8	I_{OL} = 6.4 mA	-	0.2	0.4	V
	OD8	I_{OL} = 6.4 mA	-	0.2	0.4	V
	OD12	I_{OL} = 9.6 mA	-	0.2	0.4	V

Note that the type abbreviations used above have a number suffix which indicates the current rating. The letter prefixes are defined in the Terminology section, just before Table 3.

Table 10 : CAPACITIVE LOADING

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input Pin Capacitance		-	10	-	pF
C_{IO}	Bidirectional Pin Capacitance TS4, TS4 SR, TS6, TS8, OD12		-	14	-	pF
C_{OUT}	Output Pin Capacitance TP2, TP4, OD8		-	13	-	pF

Note that the maximum capacitive loads under recommended operating conditions for outputs driving the local bus, that is, all signals beginning with K, is 1300pF. The maximum capacitive load for all outputs is 85pF.

Table 16 : RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage (V_{DD})	+4.5 V to +5.5 V
Power Dissipation (P_{DD})	1 W
Ambient Operating Temperature (T_A Commercial)	0° to +70°C
Ambient Operating Temperature (T_A Military)	–55° to +125°C

The power dissipation figure is based on typical internal logic dissipation plus the worst case set of outputs simultaneously active with maximum rated loads.

Table 17 : ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (V_{DD})	–0.3 to +7.0 V
Input Voltage (V_{IN})	–0.3 to V_{DD} +0.3 V
DC Input Current (I_{IN})	–10 to +10 mA
Storage Temperature, ceramic (T_{STG})	–65° to +150°C
Storage Temperature, plastic (T_{STG})	–40° to +125°C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliablility.

FUNCTIONAL DESCRIPTION

The DARF provides an address and data path to link a CPU to a VMEbus, including the logic required to perform data transfers as a master or a slave on local or VMEbus. Transmit and receive paths of the DARF each run in one of two operating modes: atomic or decoupled. In atomic mode, a cycle initiated on one port of the DARF does not finish until the DARF has initiated and completed that cycle on its other port. The decoupled mode allows cycles on one port to be completed and queued within the DARF for later dispatch to the other port. The decoupled mode has inherently higher transfer rates than the atomic mode.

Memory Map

The DARF is a two port device with 32-bit addressing and 32-bit data on each port. The 4 Gbyte memory maps are different for each port. A cycle that is generated to select the VMEbus port of the DARF from a VMEbus master is generated on the local bus as a 68020-like bus cycle, with the data shifted to the byte lanes appropriate for the data size indicated in the VMEbus transfer.

A cycle generated by the local CPU for the VMEbus is signalled to the DARF by having the local logic assert the VMEOUT (device wants bus) input. This cycle is interpreted according to the memory map of Figure 22 to generate the appropriate cycle on the DARF VMEbus port.

The DARF treats the 4 Gbyte space viewed from the local port as 32 – 128 Mbyte pages numbered 0 through 31, starting from address 0. Accesses to VMEbus A24:D16 space are through the lowest 16 Mbytes of page 0 (default) or page 31 as determined by register selection. The same is true of A24:D32 transfers through the second 16 Mbytes of page 0 (default) or page 31. A24 can also be disabled entirely, causing these locations to generate A32:D32 VMEbus cycles in those address ranges.

The upper 64 Kbytes of page 31 causes A16:D16 cycles to be generated, if A16 mode is enabled (default). Otherwise, this area causes A32:D32 cycles.

The BUSSEL register within the DARF allows each of the 32 pages to be individually forced to generate a $\overline{\text{VSBSEL}}$ signal instead of a VMEbus access. This is useful whenever a major peripheral bus, like a VME Subsystem Bus (VSB), is present. The default setting is for all pages to generate VMEbus accesses.

Aside from the areas mentioned above, accesses with $\overline{\text{VMEOUT}}$ asserted generate A32:D32 VMEbus cycles.

Bus Master Operation

Bus master operation implies that the DARF is generating a cycle on its VMEbus port. If the logic within the DARF indicates that the cycle should not be generated on the VMEbus (BUSSEL register), the DARF asserts the $\overline{\text{VSBSEL}}$ signal until the local cycle is terminated. The DARF does not decouple these cycles, and they proceed regardless of the DARF BI-mode™ status.

VMEbus Requesting

Accesses to the VMEbus may be requested by the DARF for any of the following:

- A local read cycle to the VMEbus
- An atomic mode write cycle from the local bus to the VMEbus
- $\overline{\text{VIACKRQ}}$ signal is requesting a VMEbus interrupt acknowledge cycle
- Cycles are queued in the transmit FIFO
- A local cycle with $\overline{\text{KRMC}}$ asserted accesses the VMEbus

Deadlocks

If, while requesting the VMEbus for the first three cases above, an incoming atomic cycle is received from the VMEbus, then the DARF asserts $\overline{\text{KBERR}}$ and $\overline{\text{KHALT}}$ to instruct the local device to relinquish the local bus then retry its cycle. The incoming VMEbus cycle then finishes normally, before the CPU is allowed to retry it's cycle. If an incoming atomic cycle occurs during the last case above, the DARF issues only $\overline{\text{KBERR}}$ locally. This is required to terminate local $\overline{\text{KRMC}}$ cycles which will not otherwise relinquish the local bus.

Transactions Performed

When generating VMEbus cycles in A24 or A16 mode, the DARF sets all unused address lines to logic 1. The address modifier codes generated by the DARF during VMEbus cycles indicate the addressing mode (A32, A24 or A16) and the access type (user/supervisor program/data). Interrupt acknowledge cycles generated by the DARF use AM code 2E if A16 mode is enabled, or code 0E otherwise.

The DARF uses the $\overline{\text{KDSACK0}}$ and $\overline{\text{KDSACK1}}$ signals to indicate to the CPU the size of data being transfered in

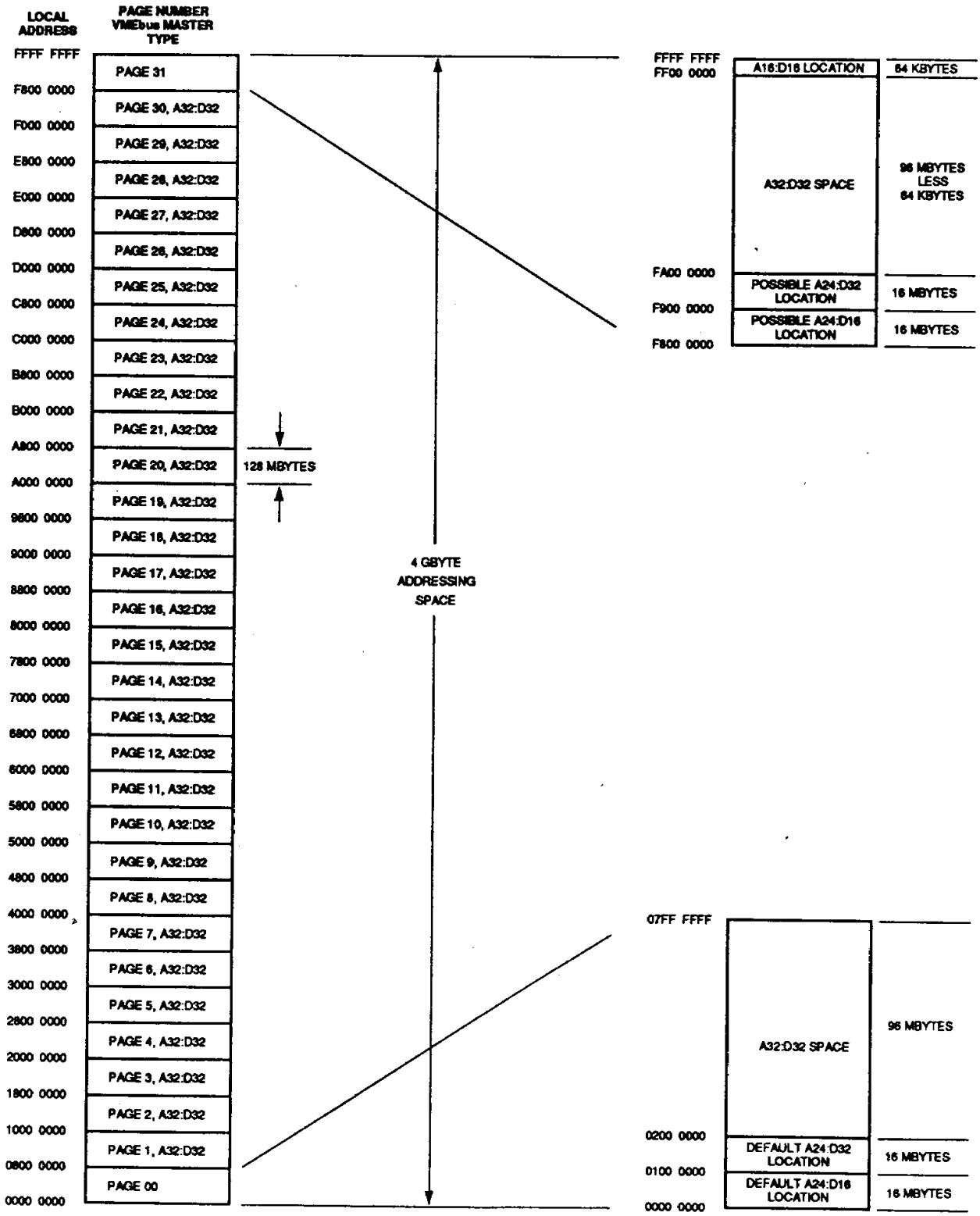


Figure 22 : DARF MEMORY MAP

any given transaction. Accesses to D32 space result in both KDSACK0 and KDSACK1 being asserted if the access is aligned (A01 = A00 = 0). All other VMEbus cycles requested by the CPU result in the assertion of KDSACK1 only. The DARF supports unaligned transfers as generated by Motorola 68020/030 microprocessors.

Locked Transactions

Two classes of locked transactions concern the DARF; single address locked transactions and multi-address locked transactions. These classes correspond to the 68020 TAS and CAS2 instructions respectively.

During cycles where KRMC is asserted (locked cycles) on the local bus, the DARF retains control of the VMEbus, until all cycles making up the locked transaction are complete. Note that this is insufficient to guarantee the indivisibility of a locked transaction, since it may not prevent access by other devices to the memory on the slave module during the locked transaction (though it does if the slave is another DARF).

For single address locked transactions, the VMEbus specification allows AS* to remain asserted for all cycles of the transaction. To enable this feature, the TASCON control bit must be set within the DARF. *Caution:* the use of the TASCON mode with multi-address locked transactions may cause the failure of those transactions.

During all types of locked transactions, the DARF asserts its VRMC output. This output may be routed to the VMEbus P2 Reserved pin for transmission to a similarly equipped slave. It is recommended that this connection be made through a jumper block in case a different use is envisaged for this VMEbus pin. If the slave module(s) participating in the locked transaction are capable of responding to the VRMC/ signal (eg: DARF equipped module), all locked transactions can be made indivisible.

During a locked transaction to the VMEbus, an incoming transaction causes the attempted locked transaction to be terminated, with a bus error, when bus control has not been acquired.

Atomic Mode

In atomic mode accesses, the CPU transfer is *not* queued by the transmit FIFO; the CPU becomes directly linked to the VMEbus once ownership is established. The CPU enters wait states until a DTACK* or BERR* is generated by the VMEbus slave and passed back through the DARF. Only then can the CPU terminate the local cycle and proceed to the next.

If a BERR* is received during a VMEbus transaction, the VBERR flag will be set in the DARF and the VMEINT output asserted. The DARF does not initiate any further cycles on the VMEbus until the VBERR flag is cleared. The VMEINT output remains asserted as long as the VBERR flag is asserted.

Read, locked and interrupt acknowledge cycles are always atomic. Write cycles are atomic if the transmit FIFO is in atomic mode. Atomic cycles are blocked, if cycles are queued in the transmit FIFO, until the FIFO has cleared. This is required to ensure data integrity.

Decoupled Mode

When the CPU writes to the VMEbus with the transmit FIFO in decoupled mode, the local cycle finishes in one wait state. The transmit FIFO is 7 stages deep and contains all queued decoupled writes and DMA writes. When the FIFO becomes non-empty, it causes a request for the VMEbus.

Similar to the atomic mode, a decoupled cycle ending in BERR* during transfer across the VMEbus results in VBERR being set, VMEINT asserted and the transmit FIFO to be frozen. The transmission of data does not resume until the VBERR flag is cleared. The address, data and control information for the failed cycle are saved in DARF registers so that the CPU can determine which access failed. The DARF does not have the capability to retry the failed cycle.

Decoupled writes to a full transmit FIFO are blocked until there is sufficient room to queue the transaction.

Interrupt Acknowledge Cycles

When the VIACKRQ input to the DARF is asserted, the DARF attempts an atomic VMEbus cycle (once the transmit FIFO is clear). The VMEOUT signal should not be asserted during this cycle. The DARF performs a VMEbus 8-bit interrupt acknowledge cycle using address lines VADDR 03 – VADDR 01 to indicate the interrupt level being acknowledged. The 8-bit interrupt vector is presented on local data bits KDATA 31 – KDATA 24 upon successful completion of the interrupt acknowledge.

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Bus Slave Operations

The DARF does not respond to any VMEbus accesses as a slave until its base address, image size and access protection attributes have been initialized by the local CPU. The DARF can present A32 and A24 (but not A16) slave images of different size to the VMEbus. Cycles supported as a slave are reads, writes, interrupt acknowledges and locked transactions. The local CPU can access the slave image of its own DARF, though such accesses would result in the DARF asserting its $\overline{\text{RAMSEL}}$ output only, with no VMEbus signals being affected.

The A32 slave image may be programmed to begin on any 128 Mbyte boundary. The size of the A32 slave image can be any binary increment from 4 Kbytes to 128 Mbytes.

The A24 slave image may have a size of 512 Kbytes, 1, 2 or 4 Mbytes. The base of the slave image may be an integer multiple of the size chosen.

All three methods of addressing local resources; direct access, A24 slave image access and A32 slave image access, should point to the same memory locations. To fulfill this intent, the A24 image should be on a boundary appropriate to the amount of memory available on the module, irrespective of the slave image size selected.

The DARF responds to supervisory and nonprivileged program or data accesses if the address and address modifiers fall within an enabled slave image. Part or all of such a slave image may be protected from write cycles only, or from both read and write cycles from the VMEbus (see Register Description section). Access to a protected location with a protected cycle type results in the termination of the VMEbus cycle in BERR*. Locked cycles to an area that is write protected return BERR* on the write cycles of the transaction only. Note that access protection should be initialized before a slave image is enabled.

Error Checking

A DARF access to the local bus that ends in $\overline{\text{KBERR}}$ or $\overline{\text{KBERR}}$ and $\overline{\text{KDSACK}}$ is interpreted by the DARF to have terminated in error. The DARF sets its internal LBERR flag and asserts the $\overline{\text{VMEINT}}$ output. If the cycle is an atomic access from the VMEbus, then that VMEbus cycle is terminated in BERR*.

Beyond the capabilities outlined above, the DARF is capable of checking for a late bus error indication on local bus accesses. With the BERRCHK control bit set, the DARF interprets a $\overline{\text{KBERR}}$ received up to 2 clock cycles after $\overline{\text{KDSACK}}$ as a signal to terminate the cycle in error, with the consequences outlined above. The DARF therefore waits 2 clock cycles after local completion of an atomic slave access before deciding whether to terminate the VMEbus cycle in BERR* or DTACK*.

The $\overline{\text{KDSACK}}$ encoding used to terminate the local cycle during slave access from the VMEbus is irrelevant since the VMEbus does not support dynamic bus sizing. Any $\overline{\text{KDSACK}}$ encoding successfully terminates a DARF generated local bus cycle.

Decoupled Mode

When changing the receive FIFO between atomic and decoupled modes, incoming VMEbus cycles must be disabled. The VINEN control bit should first be cleared, the RXATOM control bit changed, then VINEN reasserted.

In decoupled mode, the DARF decodes the access to determine if it is a valid access to an enabled slave image. If not, the DARF makes no response to the cycle. If valid, the access protection mechanism is triggered and where access is protected, an immediate BERR* is issued. Unprotected write accesses are queued in the receive FIFO and a DTACK* is issued to terminate the VMEbus cycle. If the FIFO is full, the DARF delays its DTACK* response until there is room to queue the access. *Caution:* in some cases this may exceed the VMEbus data transfer timeout period.

Like bus master operation, slave accesses other than writes always occur in atomic mode. If there are writes queued in the receive FIFO, the slave access is blocked until these FIFO entries are cleared. It is recommended that the VMEbus data transfer timeout be set greater than 4 ms, since eight local bus cycles could be required (7 for the FIFO plus one for the atomic cycle).

If the DARF receives a local bus error while performing an queued write, the LBERR flag is set and the $\overline{\text{VMEINT}}$ output asserted. The DARF does not stop any operations, nor does it save any information about the failed cycle if this error condition occurs. $\overline{\text{VMEINT}}$ remains asserted as long as the LBERR flag is set.

Local Bus Mastership

The DARF requests the local bus for any of the following:

- Cycles are queued in the receive FIFO
- A VMEbus read of local memory
- An atomic write to local memory from the VMEbus
- The DARF internal DMA is reading from local memory
- A VMEbus locked transaction accesses local memory

The DARF asserts its $\overline{\text{LBRQ}}$ output to request the local bus. A local bus arbiter (contained in the ACC) requests the local bus from the CPU. When the local bus has been granted and all buses and control signals have been released, the local bus arbiter completes any required handshakes (such as asserting $\overline{\text{BGACK}}$ to a 680x0 CPU), then asserts the $\overline{\text{LBGR}}$ input of the DARF. The DARF maintains its $\overline{\text{LBRQ}}$ asserted for any of the following:

- Queued cycles are present and $\overline{\text{LBGR}}$ is still asserted
- VMEbus AS* is asserted for an atomic cycle
- The DARF $\overline{\text{VRMC}}$ input is asserted for a VMEbus locked transaction

While using the local bus, DARF signals emulate 68020 timing. In decoupled operation, late bus error checking, if enabled, overlaps the first two clocks of the subsequent access.

In the first case above, the DARF releases $\overline{\text{LBRQ}}$ within 1 or 2 transactions of the negation of $\overline{\text{LBGR}}$. In the second two cases, the DARF does not release $\overline{\text{LBRQ}}$ until the conditions outlined have been cleared.

DMA Controller Operation

The DARF has a built-in DMA function for transfering aligned 32-bit data form local memory to VMEbus A24:D32 or A32:D32 space. The DMA uses the DARF transmit FIFO in decoupled mode to transfer up to 4K longword (16 Kbyte) blocks. Longwords are read singly from the local bus and queued with their destination address in the transmit FIFO. The DMA24 control bit, and not the previously described address map, determines whether the VMEbus transfer will be A24:D32 or A32:D32. In A24, the DARF uses AM code 39 (standard nonprivileged data access) and sets VMEbus A31 - A24 to logic 1s. In A32, the DARF uses AM code 09 (extended nonprivileged data access).

The DARF registers used for DMA operation may be read at any time by the local CPU. *Caution:* the register values may not be stable when DMA is operating during CPU read operations.

The Source Address Register contains the address of the local memory location, which points to the next longword that will be read from local memory.

The Destination Address Register contains the VMEbus address, which represents the next VMEbus address to be queued in the transmit FIFO.

The Transfer Count Register contains the number of longwords remaining to be transferred.

The local CPU must set the DARF transmit FIFO to decoupled mode, set up the DMA parameters and clear the VBERR, DONE and DLBER flags before setting the DMAGO bit to start the DMA. Upon normal completion, the DARF asserts its DONE flag and the $\overline{\text{VMEINT}}$ output.

If the local CPU clears the DMAGO bit during DMA operation, those operations cease within 2 transfers and the DMA asserts the DONE flag and $\overline{\text{VMEINT}}$ output. If a local or VMEbus error is encountered during DMA operation, or a late bus error when BERRCHK is enabled, the DMA stops; DMAGO is cleared, $\overline{\text{DLBER}}$ or VBERR are asserted as appropriate and $\overline{\text{VMEINT}}$ is asserted. The DONE flag is not set in this case. $\overline{\text{VMEINT}}$ remains asserted as long as any of DONE, DLBER or VBERR are asserted for the cases above.

Location Monitor and FIFOs

Aligned write accesses to the top longword or highest even word in either the A24 or A32 slave images of the DARF, from either the local or VMEbus, trigger the DARF location monitor. Location monitor accesses result in the data associated with the write cycle being queued in the 32-bit x 31 entry message FIFO. Even word accesses are stored in the lower 16-bits of the FIFO, with the upper 16-bits set to logic 1s in that entry. The $\overline{\text{LMINT}}$ output of the DARF remains asserted as long as there is data queued in the message FIFO.

Accesses within the top longword of either the A24 or A32 slave images do not result in any local memory activity. If such an access is an aligned longword or an even word write, a DTACK* is given to the VMEbus or a $\overline{\text{KDSACK}}$ to the local bus, as appropriate. Other access types produce

no response. Accesses when the message FIFO is full also produce no response. A register within the DARF, when read by the local CPU, dequeues the top entry in the FIFO. Reads from an empty FIFO are acknowledged with KDSACK, but indeterminate data is returned.

The location monitor is also used to remove the card from BI-mode™. The BIREL output of the DARF pulses each time the LM is written to, which clears the BI-mode™ signal from the ACC.

VMEbus Interrupter

The participation of the DARF in VMEbus interrupt generation is limited to gating an 8-bit interrupt vector from its IVECT register onto VMEbus VDATA 07 – VDATA 00 and asserting DTACK* whenever its VECTEN input is asserted. External logic is required for assertion and negation of IRQ7* – IRQ1* and for recognition of VMEbus interrupt acknowledge cycles leading to the assertion of VECTEN.

Control and Status Registers

The DARF has 16 internal registers accessible through its local port in 1 wait state as aligned longwords only via the assertion of DARFCS.

Caution: the contents of many of these registers may be changing even as they are read.

Test and Diagnostic Modes

The TESTMODE pin of the DARF is used for chip level factory testing only and must be grounded in a system environment.

As described earlier, the information for a transmit FIFO write that receives a VMEbus BERR* is available for local CPU inspection in the DATAO, ADDO and AMO registers. The DARF does not have the capability to retry the cycle.

In addition to the registers described for the transmit FIFO, three similar registers exist for the receive FIFO. Since the receive FIFO does not halt on error, these registers are used to verify receiver operation only. To aid this function, control bits are provided to prevent automatic dequeuing of receive FIFO entries and to dequeue single entries on CPU command.

Loopback Mode

In loopback mode, a local CPU write to one of its own slave images results in a VMEbus cycle occurring, contrary to normal operation. The DARF enables the transceivers to drive all VMEbus address, data and control signals. The DARF captures the receive data at its input pins and queues it in the receive FIFO. DTACK* is generated on the VMEbus to terminate the cycle.

A local CPU read cycle asserts RAMSEL to redirect the access to local memory during loopback operation.

The DARF *must* be in decoupled mode on both FIFOs for correct loopback operation.

Caution: the loopback mode is intended only for testing, as there is the possibility for loss of data integrity.

DARF REGISTERS

All registers are 32 bits wide and are only accessible as longwords, although not all bits are always used. If the value read from a register is different than the value written to, or stored in the register, then read and write values are individually described. Otherwise, no distinction is made. Bits that are not used have defined values, and may be used in future versions of the DARF. It is recommended that such unused bits be set to zero to maximize the probability of future firmware compatibility.

Values written to read only bits have no effect. It is recommended that only zero values be written in such cases, to ensure compatibility with future versions of the DARF which may use these bits to provide additional features.

In the following tables: R = Read only
U = Undefined
R/W = Read/Write

Table 13 : DARF REGISTER DESCRIPTIONS

Offset from DARF Basic Address	Name	Register Function
3CH	MODE	Mode control register
38H	LMFIFO	Location Monitor FIFO read port
34H	TXCTL	Transmit FIFO control bits output latch
30H	TXADDR	Transmit FIFO address output latch
2CH	TXDATA	Transmit FIFO data output latch
28H	APBR	Access protect boundary register
24H	IVECT	VMEbus interrupter vector register
20H	BUSSEL	VMEbus/VSB select register
1CH	RXCTL	Receive FIFO control bits, for self tests
18H	RXADDR	Recieve FIFO address bits, for self tests
14H	RXDATA	Recieve FIFO data bits, for self tests
10H	VMEBAR	VMEbus slave base address register
0CH	DCSR	Control and status register
08H	DMATC	DMA transfer count register
04H	DMADAR	DMA destination address register
00H	DMASAR	DMA source address register

Table 14 : DARF MODE CONTROL REGISTER

Register Name: MODE	Register Offset: 3CH

Bits	Function							
31 – 24	Not Used							
23 – 16	Not Used							
15 – 08	Not Used			RXATOM	TXATOM	A24SLVEN	DMA24	BERRCHK
07 – 00	TASCON	A24P0	LPBK	DISRX	A24DI	A16DI	PROT	VINEN

Name	Type	Condition after Reset	State	Function
RXATOM	R/W	0		Receive FIFO Atomic/Decoupled
			0	RX FIFOs used in decoupled mode
			1	RX FIFOs bypassed (Atomic mode)
TXATOM	R/W	0		Transmit FIFO Atomic/Decoupled
			0	TX FIFOs used in decoupled mode
			1	TX FIFOs bypassed (Atomic mode)
A24SLVEN	R/W	0		A24 slave image enable
			0	Image will not respond
			1	Image is enabled
DMA24	R/W	0		DMA destination address size
			0	DMA operates as A32 master
			1	DMA operates as A24 master
BERRCHK	R/W	1		Local late bus error enable
			0	No extra delay inserted.
			1	1 clock local delay inserted to check for late BERR from RAM
TASCON	R/W	0		AS* modifier for RMW cycles
			0	AS* negated between every VMEbus cycle
			1	AS* not negated between cycles while CPU RMC is asserted
A24P0	R/W	1		VMEbus A24 space address
			0	A24 space located at F800.0000
			1	A24 space located at 0000.0000
LPBK	R/W	0		Loopback enable bit
			0	No loopback
			1	Loopback through FIFOs enabled

Table 14 : DARF MODE CONTROL REGISTER CON'T

Name	Type	Condition after Reset	State	Function
DISRX	R/W	0		Receive FIFO disable bit
			0	Normal operation
			1	FIFO emptied by CPU reads only
A24DI	R/W	0		Page 0 Master VMEbus A24 disable bit
			0	A24 responds per A24P0 bit
			1	A24 disabled
A16DI	R/W	0		VMEbus Master A16 disable bit
			0	VMEbus A16 located at FFFF.000
			1	A16 space disabled
PROT	R/W	0		Access protection type
			0	Write protection only
			1	Read and write protection.
VINEN	R/W	0		Slave images enabling
			R 0	All slave images are disabled
			R 1	All programmed images enabled
			W 0	Disable all slave images
			W 1	Enable all programmed images

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Table 15 : LOCATION MONITOR FIFO READ PORT

Register Name: LMFIFO	Register Number: 38H

Bits	Function
31 – 24	LM (Location Monitor FIFO Output Stage Data) – Byte 3
23 – 16	LM (Location Monitor FIFO Output Stage Data) – Byte 2
15 – 08	LM (Location Monitor FIFO Output Stage Data) – Byte 1
07 – 00	LM (Location Monitor FIFO Output Stage Data) – Byte 0

Name	Type	Condition after Reset	State	Function
LM 31 – 00	R	U		Data at output stage of Location Monitor FIFO.

Table 16 : TRANSMIT FIFO AM Code and CONTROL BIT LATCH

Register Name: AMC	Register Number: 34H

Bits	Function							
31 – 24	Not Used							
23 – 16	Not Used							
15 – 08	Not Used							
07 – 00	Not Used	Not Used	SIZ1	SIZ0	SPC1	SPC0	TC1	TC0

Name	Type	Condition after Reset	State	Function
SIZ1, 0	R	U		Transfer size bits
			0, 0	Longword
			0, 1	Byte
			1, 0	Word
			1, 1	Tri-byte
SPC1, 0	R	U		Address space bits
			0, 0	A32
			0, 1	Reserved
			1, 0	A16
			1, 1	A24
TC1, 0	R	U		Type code
			0, 0	User program space
			0, 1	User data space
			1, 0	Supervisor program space
			1, 1	Supervisor data space

Table 17 : TRANSMIT FIFO ADDRESS OUTPUT LATCH

Register Name: ADDO	Register Number: 30H

Bits	Function
31 – 24	TXA (Transmit FIFO Output Address) – Byte 3
23 – 16	TXA (Transmit FIFO Output Address) – Byte 2
15 – 08	TXA (Transmit FIFO Output Address) – Byte 1
07 – 00	TXA (Transmit FIFO Output Address) – Byte 0

Name	Type	Condition after Reset	State	Function
TXA 31 – 00	R	U		Address at transmit FIFO output stage

Table 18 : TRANSMIT FIFO DATA OUTPUT LATCH

Register Name: DATAO	Register Number: 2CH

Bits	Function
31 – 24	TXD (Transmit FIFO Output Data) – Byte 3
23 – 16	TXD (Transmit FIFO Output Data) – Byte 2
15 – 08	TXD (Transmit FIFO Output Data) – Byte 1
07 – 00	TXD (Transmit FIFO Output Data) – Byte 0

Name	Type	Condition after Reset	State	Function
TXD 31 – 00	R	U		Data at transmit FIFO output stage

Table 19 : ACCESS PROTECT BOUNDARY REGISTER

Register Name: APBR	Register Number: 28H

Bits	Function				
31 – 24	Not Used				
23 – 16	Not Used				
15 – 08	Not Used				
07 – 00	Not Used *(4 bits)*	APB03	APB02	APB01	APB00

Name	Type	Condition after Reset	State	Function
APB03 – 00	R/W	U		Access protection boundary; protection enforced below this boundary on slave VMEbus image
			0	No protection
			1	Lower 64 KB
			2	Lower 128 KB
			3	Lower 256 KB
			4	Lower 512 KB
			5	Lower 1 MB
			6	Lower 2 MB
			7	Lower 4 MB
			8	Lower 8 MB
			9	Lower 16 MB
			A	Lower 32 MB
			B	Lower 64 MB
			C	Lower 128 MB
			D	Lower 128 MB
			E	Lower 128 MB
			F	Lower 128 MB

Table 20 : VMEbus INTERRUPTER VECTOR REGISTER

Register Name: IVECT	Register Number: 24H

Bits	Function
31 – 24	Not Used
23 – 16	Not Used
15 – 08	Not Used
07 – 00	IVECT (Interrupt Vector)

Name	Type	Condition after Reset	State	Function
IVECT07 – 00	R/W	U		VMEbus Interrupter Vector bits

Table 21 : VMEbus/VSB BUS SELECT REGISTER

Register Name: BUSSEL	Register Number: 20H

Bits	Function
31 – 24	VSBEN (VMEbus/VSB Select Bits) – Byte 3
23 – 16	VSBEN (VMEbus/VSB Select Bits) – Byte 2
15 – 08	VSBEN (VMEbus/VSB Select Bits) – Byte 1
07 – 00	VSBEN (VMEbus/VSB Select Bits) – Byte 0

Name	Type	Condition after Reset	State	Function
VSBEN31 – 00	R/W	0		VMEbus/VSB select bits, one for each of the 32 by 128 Mbyte pages (refer to Address Range Map below)
			0	VMEbus selected
			1	VSB selected

Bit	Address Range Mapped	Bit	Address Range Mapped
0	0000.0000 - 07FF.FFFF	16	8000.0000 - 87FF.FFFF
1	0800.0000 - 0FFF.FFFF	17	8800.0000 - 8FFF.FFFF
2	1000.0000 - 17FF.FFFF	18	9000.0000 - 97FF.FFFF
3	1800.0000 - 1FFF.FFFF	19	9800.0000 - 9FFF.FFFF
4	2000.0000 - 27FF.FFFF	20	A000.0000 - A7FF.FFFF
5	2800.0000 - 2FFF.FFFF	21	A800.0000 - AFFF.FFFF
6	3000.0000 - 37FF.FFFF	22	B000.0000 - B7FF.FFFF
7	3800.0000 - 3FFF.FFFF	23	B800.0000 - BFFF.FFFF
8	4000.0000 - 47FF.FFFF	24	C000.0000 - C7FF.FFFF
9	4800.0000 - 4FFF.FFFF	25	C800.0000 - CFFF.FFFF
10	5000.0000 - 57FF.FFFF	26	D000.0000 - D7FF.FFFF
11	5800.0000 - 5FFF.FFFF	27	D800.0000 - DFFF.FFFF
12	6000.0000 - 67FF.FFFF	28	E000.0000 - E7FF.FFFF
13	6800.0000 - 6FFF.FFFF	29	E800.0000 - EFFF.FFFF
14	7000.0000 - 77FF.FFFF	30	F000.0000 - F7FF.FFFF
15	7800.0000 - 7FFF.FFFF	31	F800.0000 - FFFF.FFFF

Table 22 : RECEIVE FIFO CONTROL REGISTER

Register Name: RXCTL	Register Number: 1CH

Bits	Function				
31 – 24	Not Used				
23 – 16	Not Used				
15 – 08	Not Used				
07 – 00	Not Used *(4 bits)*	SIZ1	SIZ0	TC1	TC0

Name	Type	Condition after Reset	State	Function
SIZ1, 0	R	U		Receive FIFO SIZ1, 0 output bits
			0, 0	Longword
			0, 1	Byte
			1, 0	Word
			1, 1	Tri-byte
TC1, 0	R	U		Receive FIFO TC1, 0 output bits
			0, 0	User program space
			0, 1	User data space
			1, 0	Supervisor program space
			1, 1	Supervisor data space

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Table 23 : RECEIVE FIFO ADDRESS REGISTER

Register Name: RXADD	Register Number: 18H

Bits	Function
31 – 24	RADDR (Address at Output Stage of Receive FIFO) – Byte 3
23 – 16	RADDR (Address at Output Stage of Receive FIFO) – Byte 2
15 – 08	RADDR (Address at Output Stage of Receive FIFO) – Byte 1
07 – 00	RADDR (Address at Output Stage of Receive FIFO) – Byte 0

Name	Type	Condition after Reset	State	Function
RADDR31 – 00	R	U		Receive FIFO output address. Upper address bits are zeroed according to the size of slave image for which the transfer was accepted

Table 24 : RECEIVE FIFO DATA REGISTER

Register Name: RXDATA	Register Number: 14H

Bits	Function
31 – 24	RDATA (Data at Output Stage of Receive FIFO) – Byte 3
23 – 16	RDATA (Data at Output Stage of Receive FIFO) – Byte 2
15 – 08	RDATA (Data at Output Stage of Receive FIFO) – Byte 1
07 – 00	RDATA (Data at Output Stage of Receive FIFO) – Byte 0

Name	Type	Condition after Reset	State	Function
RDATA	R	U		Receive FIFO output data

Table 25 : VMEbus BASE ADDRESS REGISTER

Register Name: VMEBAR	Register Number: 10H

Bits	Function			
31 – 24	Not Used			
23 – 16	Not Used	A24SIZ *(2 bits)*	A24BA *(5 bits)*	
15 – 08	Not Used *(7 bits)*			A32SIZ
07 – 00	A32SIZ *continued (4 bits)*		A32BA *(5 bits)*	

Name	Type	Condition after Reset	State	Function
A24SIZ	R/W	U		Sets size of A24 slave image
			0	512K
			1	1M
			2	2M
			3	4M
A24BA	R/W	U		Sets base address of A24 image; size set via A24SIZ can change lower bits to 0. Resulting bits match VME address bits A23 – A19.
A32SIZ	R/W	U		Sets size of A32 slave image
			0	4K
			1	8K
			2	16K
			3	32K
			4	64K
			5	128K
			6	256K
			7	512K
			8	1M
			9	2M
			A	4M
			B	8M
			C	16M
			D	32M
			E	64M
			F	128M

Table 25 : VMEbus BASE ADDRESS REGISTER CON'T

Name	Type	Condition after Reset	State	Function
A32BA	R/W	U		Sets base address of A32 image
			0	0000.0000
			1	0800.0000
			2	1000.0000
			3	1800.0000
			4	2000.0000
			5	2800.0000
			6	3000.0000
			7	3800.0000
			8	4000.0000
			9	4800.0000
			A	5000.0000
			B	5800.0000
			C	6000.0000
			D	6800.0000
			E	7000.0000
			F	7800.0000
			10	8000.0000
			11	8800.0000
			12	9000.0000
			13	9800.0000
			14	A000.0000
			15	A800.0000
			16	B000.0000
			17	B800.0000
			18	C000.0000
			19	C800.0000
			1A	D000.0000
			1B	D800.0000
			1C	E000.0000
			1D	E800.0000
			1E	F000.0000
			1F	F800.0000

Table 26 : CONTROL and STATUS REGISTER

Register Name: DCSR	Register Number: 0CH

Bits	Function							
31 – 24	Not Used							
23 – 16	Not Used							
15 – 08	Not Used *(4 bits)*				BARDY	RXSHFT	RXRST	TXRST
07 – 00	RXHD	TXHD	DLBER	LMHD	LBERR	VBERR	DONE	DMAGO

Name	Type	Condition after Reset	State	Function
BARDY	R	0		VMEbus Base Address Ready
			0	BAR not programmed yet
			1	BAR ready
RXSHFT	R/W	0		Receive FIFO shift
			R	Clears self; always reads zero
			W 0	No effect
			W 1	Rx FIFO shifts one forward
RXRST	R/W	0		Receive FIFO reset
			R	Clears self; always reads zero
			W 0	No effect
			W 1	Resets entire receive FIFO
TXRST	R/W	0		Transmit FIFO reset
			R	Clears self; always reads zero
			W 0	No effect
			W 1	Resets entire transmit FIFO and any VME-out cycle in progress
RXHD	R	0		Receive FIFO status
			0	Receive FIFO is empty
			1	Receive FIFO has entries
TXHD	R	0		Transmit FIFO status
			0	Transmit FIFO is empty
			1	Transmit FIFO has entries
DLBER	R/W	0		DMA Local Bus Error indicator; asserts $\overline{\text{VMEINT}}$ pin while 1
			R 0	No error indicated
			R 1	DMA received a local bus error
			W 0	Clears DLBER indicator
			W 1	No effect

Table 26 : CONTROL and STATUS REGISTER CON'T

Name	Type	Condition after Reset	State	Function
LMHD	R	0		Location Monitor FIFO status; asserts $\overline{\text{LMINT}}$ pin while 1
			0	LM FIFO is empty
			1	LM FIFO has entries
LBERR	R/W	0		Local $\overline{\text{KBERR}}$ received while in decoupled mode; asserts $\overline{\text{VMEINT}}$ pin while 1
			R 0	No error indicated
			R 1	Local bus error received
			W 0	Clears LBERR indicator
			W 1	No effect.
VBERR	R/W	0		VMEbus BERR* received while in decoupled mode; freezes TxFIFO and asserts $\overline{\text{VMEINT}}$ pin while 1
			R 0	No error indicated
			R 1	VMEbus BERR* received
			W 0	Clears VBERR indicator
			W 1	No effect.
DONE	R/W	0		DMA Done indicator; asserts $\overline{\text{VMEINT}}$ pin while 1
			R 0	DMA not done yet
			R 1	DMA finished or stopped by CPU; not set if stopped due to BERR*
			W 0	Clear DONE bit
			W 1	No effect
DMAGO	R/W	0		DMA Go bit
			R 0	DMA is stopped, by self or CPU
			R 1	DMA is running
			W 0	DMA stop request
			W 1	Starts DMA

Table 27 : DMA TRANSFER COUNT REGISTER

Register Name: DMATC	Register Number: 08H

Bits	Function	
31 – 24	Not Used	
23 – 16	Not Used	
15 – 08	Not Used *(4 bits)*	DTC (DMA Transfer Count)
07 – 00	DTC (DMA Transfer Count) *continued (12 bits)*	

Name	Type	Condition after Reset	State	Function
DTC11 – 00	R/W	U	0	DMA transfer count, in number of longwords Zero indicates 4096 longwords

Table 28 : DMA DESTINATION ADDRESS REGISTER

Register Name: DMADAR	Register Number: 04H

Bits	Function		
31 – 24	DDA (Destination Address Bits) – Byte 3		
23 – 16	DDA (Destination Address Bits) – Byte 2		
15 – 08	DDA (Destination Address Bits) – Byte 1		
07 – 00	DDA (Destination Address Bits) – Byte 0	0	0

Name	Type	Condition after Reset	State	Function
DDA31 – 03	R/W	U		Destination address bits 31 – 03
DDA01 – 00	R	0	0	Destination address bits 01 & 00 are always 0

Table 29 : DMA SOURCE ADDRESS REGISTER

Register Name: DMASAR	Register Number: 00H

Bits	Function		
31 – 24	Not Used *(5 bits)*	DSA (DMA Source Address)	
23 – 16	DSA (DMA Source Address) – Byte 2		
15 – 08	DSA (DMA Source Address) – Byte 1		
07 – 00	DSA (DMA Source Address) – Byte 0	0	0

Name	Type	Condition after Reset	State	Function
DSA26 – 02	R/W	U		Source address bits 26 to 02
DSA01 – 00	R	0	0	Source address bits 01 & 00 are always 0

DARF CONNECTIONS to VMEbus, LOCAL BUS and CA91C014 ACC

Table 30 : DARF to VMEbus CONNECTIONS

The DARF VMEbus signals connect via buffers to the VMEbus. These signals correspond to (or are derived from) the VMEbus signals shown below.

DARF	VMEbus
VADDR 31 – 01	A31 – 01
VAM 5 – 0	AM5 – 0
$\overline{\text{VAS}}$	AS*
$\overline{\text{VASDLY}}$	AS*
$\overline{\text{VBERRI}}$	BERR*
$\overline{\text{VBERRO}}$	BERR*
VDATA 31 – 00	D31 – 00
$\overline{\text{VDS0}}$	DS0*
$\overline{\text{VDS1}}$	DS1*
$\overline{\text{VDSDLY}}$	DS0* & DS1*
$\overline{\text{VDTACKI}}$	DTACK*
$\overline{\text{VDTACKO}}$	DTACK*
$\overline{\text{VDTKDLY}}$	DTACK*
$\overline{\text{VIACK}}$	IACK*
$\overline{\text{VLWORD}}$	LWORD*
$\overline{\text{VRMC}}$	RMC*
$\overline{\text{VWR}}$	WRITE*

Table 31 : DARF to LOCAL BUS CONNECTIONS

The DARF local bus signals connect in parallel with the same signals on the local CPU, usually a 68020 or 68030.

KADDR 31 – 00	$\overline{\text{KDSACK1}}$
$\overline{\text{KAS}}$	KFC 2-0
$\overline{\text{KBERR}}$	$\overline{\text{KHALT}}$
KCLK	$\overline{\text{KRMC}}$
KDATA 31 – 00	KSIZE 1 – 0
$\overline{\text{KDS}}$	$\overline{\text{KWR}}$
$\overline{\text{KDSACK0}}$	

Table 32 : DARF to ACC CONNECTIONS

ACC	PGA	DARF	PGA
BIMODE	B7	BIMODE	P6
$\overline{\text{BIREL}}$	Q11	$\overline{\text{BIREL}}$	S17
$\overline{\text{LBGR0}}$	Q7	$\overline{\text{LBGR}}$	M15
$\overline{\text{LBRQ0}}$	N10	$\overline{\text{LBRQ}}$	R14
$\overline{\text{VECTEN}}$	P8	$\overline{\text{VECTEN}}$	P13
$\overline{\text{VIACK}}$	Q8	$\overline{\text{VIACKRQ}}$	N15
$\overline{\text{VMEGR}}$	N8	$\overline{\text{VMEGR}}$	L15
$\overline{\text{VMERQ}}$	P11	$\overline{\text{VMERQ}}$	M17

Note: In addition to the above signals, the DARF may also connect to any two of the ACC local autovectored interrupt inputs, except for $\overline{\text{L7INMI}}$ and $\overline{\text{L7IMEM}}$. The DARF uses the two interrupts to signal location monitor accesses and general DARF service requests.

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APPLICATION NOTES

System Configuration

In order to force the CPU to retry a VME-out cycle, the DARF must have already requested the VMEbus from the ACC. The DARF waits for the VMEbus grant, then immediately negates its request without using it so that spurious bus requests do not disrupt VMEbus operation. The DARF is then be ready for a new VME-out cycle.

However, if the ACC is programmed into FAIR and ROR mode, and some other card is using the bus on the same bus request level, the CPU and DARF may thrash, forever requesting and throwing away the bus grant. Avoid this configuration by using either different request levels, or by not using both FAIR and ROR modes.

DARF Initialization

Until the local CPU needs to use either the VMEbus or it's slave image of memory, the DARF does not need to be programmed. Before the DARF will perform a VMEbus cycle for the CPU, its BIMODE BI-mode™ signal must be deasserted. On cards using the ACC and DARF, this is accomplished by creating a VMEbus slave image using the VMEBAR register, then writing to the location monitor that exists at the top of that slave image. The DARF will assert $\overline{\text{BIREL}}$ to the ACC, which will then negate BIMODE if all other BI-mode™ initiator signals are negated.

For VMEbus to access dual ported memory on the card, the VMEBAR and APBR registers must be programmed, to create the slave image and initialize the access protection. The DARF must also be out of BI-mode™.

The DARF defaults to decoupled mode. If the DARF receives a VMEbus BERR*, software on the card must clear the VBERR flag in the Control and Status register before further VMEbus master accesses are possible.

BI-mode™ is a trademark of DY-4 Systems Inc, denoting the Bus Isolation mode.