DATA SHEET

CBTU4411

11-bit DDR2 SDRAM mux/bus switch with 12 Ω on-resistance

Product data sheet
Supersedes data of 2005 Jan 07

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Philips
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11-bit DDR2 SDRAM mux/bus switch with 12 Ω on-resistance

CBTU4411

FEATURES

- Enable and select signals are SSTL_18 compatible
- Optimized for use in Double Data Rate 2 (DDR2) SDRAM applications
- Designed to be used with 400 to 667 Mbps/200 to 333 MHz DDR2 data bus
- Switch on resistance is designed to eliminate the need for series resistor to DDR2 SDRAM
- 12 Ω on resistance
- Controlled enable/disable times support fast bus turnaround
- Pseudo-differential select inputs support accurate and low–skew control of switching times
- Selectable built-in termination resistors on the Sn inputs
- Internal 400 Ω pull-down resistors on B port
- V_{BIAS} input for optimal DIMM-port pull-down when disabled
- Configurable to support differential strobe with pull-up to $^3/_4$ of V_{DD} on Channel 10 when idle
- Low differential skew
- Matched rise/fall slew rate
- Low cross-talk data-data/data-DQM
- Simplified 1:4 switch position control by 2-bit encoded input
- Single input pin puts all bus switches in off (high-Z) position
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 1500 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 750 V CDM per JESD22-C101

DESCRIPTION

This 11-bit bus switch is designed for 1.7 V to 1.9 V V_{DD} operation and SSTL_18 select input levels.

Each Host port pin is multiplexed to one of four DIMM port pins. The selection of the DIMM port to be connected to the Host port is controlled by a decoder driven by 3 hardware select pins, S[1:0] and $\overline{EN}$. Driving pin $\overline{EN}$ HIGH disconnects all DIMM ports from their respective host ports. When $\overline{EN}$ is driven LOW, pins S0 and S1 select one of four DIMM ports to be connected to their respective host port. When disconnected, any DIMM port is terminated to the externally supplied voltage V_{BIAS} by means of an on-chip pull-down resistor of typically 400 Ω. The on-state connects the Host port to the DIMM port through a 12 Ω nominal series resistance. The design is intended to have only one DIMM port active at any time.

The CBTU4411 can also be configured to support a differential strobe signal on channels 10 (TRUE) and 9 (complementary Strobe). When its LVCMOS configuration input STRobe ENable is HIGH, Channel 10 is pulled up to $^3/_4$ of V_{DD} internally by a resistive divider when the DIMM port is idle. When the CBTU4411 is disabled ($\overline{EN}$ = HIGH in Strobe mode, the pull-down on Channel 10 is disabled for current savings, pulling Channel 10 to V_{DD}. When STRobe ENable is LOW, Channel 10 behaves the same as all other channels.

The select inputs (S0, S1) are pseudo-differential type SSTL_18. A reference voltage should be provided to input pin V_{REF} at nominally $V_{DD}/2$. This topology provides accurate control of switching times by reducing dependency on select signal slew rates. S0 and S1 are provided with selectable input termination to $V_{DD}/2$ (active when LVCMOS input TERM is HIGH). When the CBTU4411 is disabled ($\overline{EN}$ = HIGH), both S0 and S1 inputs are pulled LOW.

The part incorporates a very low cross-talk design. It has a very low skew between outputs (< 30 ps) and low skew (< 30 ps) for rising and falling edges. The part has optimal performance in DDR2 data bus applications.

Each switch has been optimized for connection to 1 or 2-rank DIMMs.

The low internal RC time constant of the switch allows data transfer to be made with minimal propagation delay.

The CBTU4411 is characterized for operation from 0 °C to +85 °C.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Host to DIMM or v.v.	Figures 5, 7; V_{DD} = 1.8 V; input slew rate = 2.5 V/ns	50	ps
C_{IN}	Input capacitance – control pins	V_I = 0 V or V_{DD}	3	pF
C_{ON}	Channel on capacitance	V_{in} = 0.9 V	4	pF
I_{DD}	Quiescent supply current	V_{DD} = 1.8 V; I_O = 0; V_I = V_{DD} or GND	6	mA

ORDERING INFORMATION

T_{amb} = 0 °C to +85 °C

Type number	Topside mark	Package		
		Name	Description	Version
CBTU4411EE		LFBGA72	plastic low profile fine-pitch ball grid array package; 72 balls; body 7 × 7 × 1.05 mm	SOT856-1

72-BALL BGA CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11
A	S1	STREN	V_{DD}	0DP0	1DP0	2DP0	1DP1	2DP1	3DP1	0DP2	1DP2
B	TERM	S0	V_{DD}	GND	HP0	3DP0	0DP1	HP1	GND	HP2	2DP2
C	V_{REF}	$\overline{EN}$								0DP3	3DP2
D	V_{BIAS}	GND								HP3	1DP3
E	2DP10	3DP10								2DP3	3DP3
F	1DP10	HP10								GND	0DP4
G	0DP10	GND								HP4	1DP4
H	3DP9	2DP9								2DP4	3DP4
J	1DP9	HP9								1DP5	0DP5
K	0DP9	GND	HP8	0DP8	HP7	0DP7	GND	HP6	0DP6	HP5	2DP5
L	3DP8	2DP8	1DP8	3DP7	2DP7	1DP7	3DP6	2DP6	1DP6	V_{DD}	3DP5

NOTE: BLANK SPACE INDICATES NO BALL

SA00655

Figure 1. Ball configuration (transparent top view)

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
B5, B8, B10, D10, F2, G10, J2, K3, K5, K8, K10	HP0–HP10	Host ports
C2	$\overline{EN}$	LVCMOS level Enable input (active LOW). When connected HIGH, all DIMM ports will be disconnected (show a high-impedance path) from the Host ports
A2	STREN	STRobe ENable. LVCMOS level STRobe ENable input (active HIGH). When tied LOW, Channel 10 (HP10 and its DP ports) functions identically to all other channels. When tied HIGH, Channel 10 is designated as the STROBE channel (see Function Table and Simplified Schematic).
B2, A1	S0, S1	Select inputs, type SSTL_18. See Function Table.
C1	V_{REF}	Reference voltage for the pseudo-differential SSTL_18 select inputs (S0, S1)
D1	V_{BIAS}	Voltage bias for the DIMM-port pull-down resistor (R_{pd})
B1	TERM	LVCMOS level input pin activates termination resistance on Sn inputs when HIGH; high-impedance when LOW.
A[4:11], B6, B7, B11, C10, C11, D11, E1, E2, E10, E11, F1, F11, G1, G11, H1, H2, H10, H11, J1, J10, J11, K1, K4, K6, K9, K11, L[1:9], L11	0DP0–3DP0 0DP1–3DP1 0DP2–3DP2 0DP3–3DP3 0DP4–3DP4 0DP5–3DP5 0DP6–3DP6 0DP7–3DP7 0DP8–3DP8 0DP9–3DP9 0DP10–3DP10	DIMM ports
B4, B9, D2, F10, G2, K2, K7	GND	Ground
A3, B3, L10	V_{DD}	Positive supply voltage

FUNCTION TABLE, CHANNELS 0–9

INPUTS			FUNCTION							
			0DPn		1DPn		2DPn		3DPn	
$\overline{EN}$	S1	S0	HPn	V_{BIAS}	HPn	V_{BIAS}	HPn	V_{BIAS}	HPn	V_{BIAS}
L	L	L	R_{on}	high-Z	high-Z	R_{PD}	high-Z	R_{pd}	high-Z	R_{pd}
L	L	H	high-Z	R_{pd}	R_{on}	high-Z	high-Z	R_{pd}	high-Z	R_{pd}
L	H	L	high-Z	R_{pd}	high-Z	R_{pd}	R_{on}	high-Z	high-Z	R_{pd}
L	H	H	high-Z	R_{pd}	high-Z	R_{pd}	high-Z	R_{pd}	R_{on}	high-Z
H	X	X	high-Z	R_{pd}	high-Z	R_{pd}	high-Z	R_{pd}	high-Z	R_{pd}

H = HIGH voltage level
L = LOW voltage level
high-Z = high-impedance

FUNCTION TABLE, CHANNEL 10

INPUTS				FUNCTION									
$\overline{EN}$	S1	S0	STREN	0DP10			1DP10			2DP10			3DP10		
				HP10	V_{BIAS}	V_{DD}	HP10	V_{BIAS}	V_{DD}	HP10	V_{BIAS}	V_{DD}	HP10	V_{BIAS}	V_{DD}
L	L	L	L	R_{on}	high-Z	high-Z	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z
L	L	L	H	R_{on}	high-Z	high-Z	high-Z	R_{pd}	R_{pu}	high-Z	R_{pd}	R_{pu}	high-Z	R_{pd}	R_{pu}
L	L	H	L	high-Z	R_{pd}	high-Z	R_{on}	high-Z	high-Z	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z
L	L	H	H	high-Z	R_{pd}	R_{pu}	R_{on}	high-Z	high-Z	high-Z	R_{pd}	R_{pu}	high-Z	R_{pd}	R_{pu}
L	H	L	L	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z	R_{on}	high-Z	high-Z	high-Z	R_{pd}	high-Z
L	H	L	H	high-Z	R_{pd}	R_{pu}	high-Z	R_{pd}	R_{pu}	R_{on}	high-Z	high-Z	high-Z	R_{pd}	R_{pu}
L	H	H	L	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z	R_{on}	high-Z	high-Z
L	H	H	H	high-Z	R_{pd}	R_{pu}	high-Z	R_{pd}	R_{pu}	high-Z	R_{pd}	R_{pu}	R_{on}	high-Z	high-Z
H	X	X	L	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z	high-Z	R_{pd}	high-Z
H	X	X	H	high-Z	high-Z	R_{pu}	high-Z	high-Z	R_{pu}	high-Z	high-Z	R_{pu}	high-Z	high-Z	R_{pu}

$\overline{EN}$	TERM	Sn input termination
L	L	Termination resistors on Sn inputs disconnected (high-impedance).
L	H	Termination resistors on Sn inputs active.
H	X	Pull-down to GND via RTT × 2. Also disables the Sn input receivers for power savings.

I_{DDQ} TEST MODE

Condition	Description
$V_{BIAS} = V_{DD}$	All DIMM ports are disconnected (high-impedance) from their Host ports, and disconnected (high-impedance) from V_{BIAS} and R_{pu}. Used for production testing only.
$V_{BIAS} < 0.5 \times V_{DD}$	Normal operation. See Function Table above.

SIMPLIFIED SCHEMATIC, CHANNELS 0–9

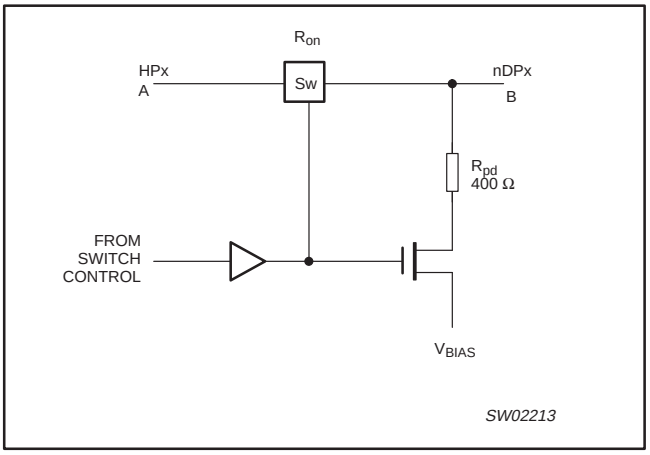


Figure 2. Channels 0-9 simplified schematic

SIMPLIFIED SCHEMATIC, CHANNEL 10

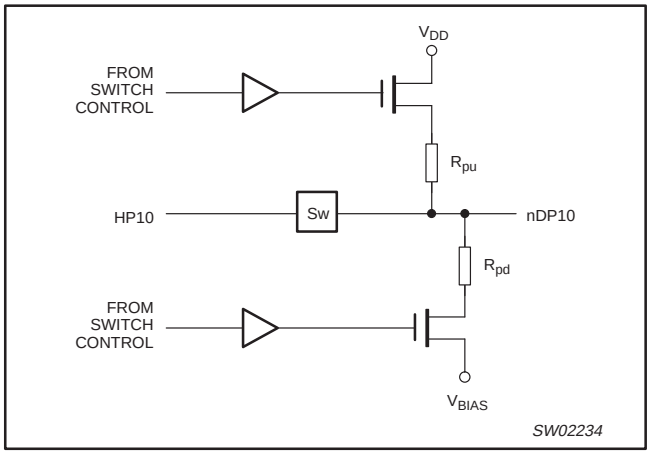
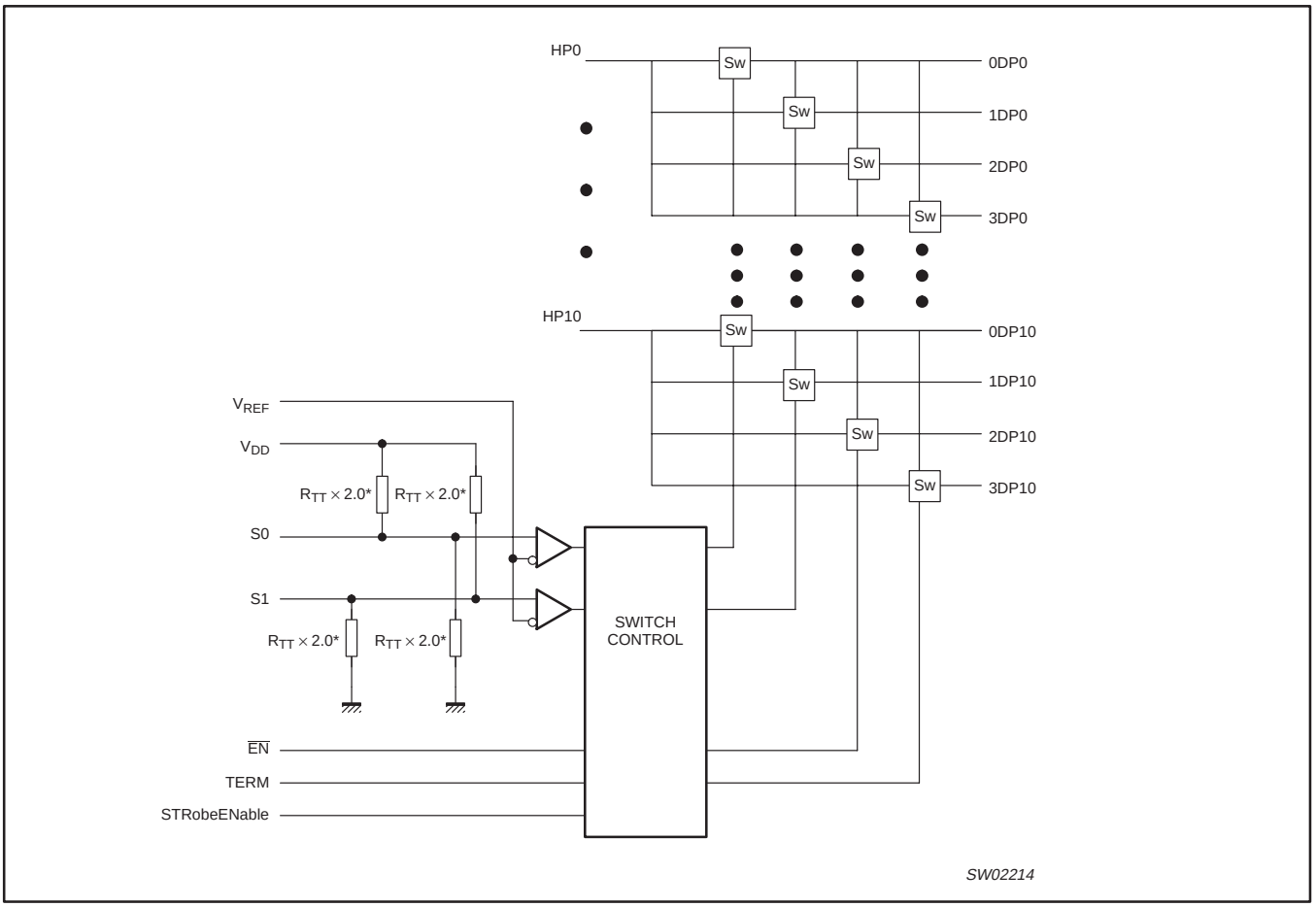


Figure 3. Channel 10 simplified schematic

LOGIC DIAGRAM (POSITIVE LOGIC)



NOTE: * = SELECTABLE

Figure 4. Positive logic diagram

ABSOLUTE MAXIMUM RATINGS[1, 3]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{DD}	DC supply voltage		–0.5 to +2.5	V
I_{IK}	DC input clamp current	$V_{I/O} < 0$ V	–50	mA
V_I	DC input voltage range (S pin only)[2]		V_{DD} + 0.3	V
T_{stg}	Storage temperature range		–65 to 150	°C
V_I	DC input voltage range (except S pin)[2]		–0.5 to +2.5	V

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	DC supply voltage	1.7	—	1.9	V
V_{REF}	Reference voltage	$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V_{BIAS}	Pull-down resistor input bias voltage[2]	0	$0.30 \times V_{DD}$	$0.33 \times V_{DD}$	V
V_{TT}	Termination voltage at DRAM inputs	V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
V_i	Input voltage	0	—	V_{DD}	V
V_{IH}	AC HIGH-level input voltage, Sn inputs	V_{REF} + 250 mV	—	—	V
V_{IL}	AC LOW-level input voltage, Sn inputs	—	—	V_{REF} – 250 mV	V
V_{IH}	DC HIGH-level input voltage, Sn inputs	V_{REF} + 125 mV	—	—	V
V_{IL}	DC LOW-level input voltage, Sn inputs	—	—	V_{REF} – 125 mV	V
V_{IH}	HIGH-level input voltage, $\overline{EN}$, STREN, and TERM pins	$0.65 \times V_{DD}$	—	—	V
V_{IL}	LOW-level Input voltage, $\overline{EN}$, STREN, and TERM pins	—	—	$0.35 \times V_{DD}$	V
T_{amb}	Operating free-air temperature range	0	—	+85	°C

NOTES:
1. All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation.
2. $V_{BIAS} > 0.5 \times V_{DD}$ is reserved for test purposes only.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = 0 °C to +85 °C Min	Typ[1]	Max	UNIT
V_{IK}	Input clamp voltage	V_{DD} = 1.7 V; I_I = –18 mA		—	—	–1.2	V
V_{TTSn}	Sn inputs termination voltage	Sn inputs = open circuit; TERM = HIGH		$0.5 \times V_{DD}$ – 40 mV	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$ + 40 mV	V
$V_{DP10strobe}$	Channel 10 DIMM port pull-up voltage	$\overline{EN}$ = LOW; V_{bias} = 0.54 V; V_{DD} = 1.8 V; STREN = HIGH; unselected DIMM port		$V_{DD}/2$ + 0.25	$0.75 \times V_{DD}$	$0.75 \times V_{DD}$ + 0.25	V
I_I	Input leakage current	V_{DD} = 1.8 V; V_I = V_{DD} or GND; S = V_{DD}; V_{BIAS} = V_{DD}; TERM = LOW	S0, S1	—	—	±100	µA
			Host port	—	—	±100	µA
			DIMM port	—	—	±100	µA
I_{DD}	Quiescent supply current	V_{DD} = 1.8 V; I_O = 0, V_I = V_{DD} or GND, $\overline{EN}$ = LOW		—	6	9	mA
		V_{DD} = 1.8 V; I_O = 0, V_I = V_{DD} or GND, $\overline{EN}$ = HIGH		—	5	100	µA
C_{in}	Sn pin capacitance	V_I= 1.8 V or 0		—	3	—	pF
C_{on}	Switch on capacitance	V_{in}= 0.9 V		—	4	6	pF
r_{on}[2]	On-resistance	V_{DD} = 1.8 V; V_A = V_{REF}; V_B = V_{REF} ± 250 mV		7	12	17	Ω
		V_{DD} = 1.8 V; V_A = V_{REF}; V_B = V_{REF} ± 500 mV		7	12	17	Ω
Δr_{on}	Variation in r_{on} over channel voltage	$\overline{EN}$ = LOW; V_{bias} = 0.54 V; V_{DD} = 1.8 V; STREN = LOW; selected DIMM port V_{HPn} = $V_{DD}/2$ + 250 mV and V_{xDPn} = $V_{DD}/2$ – 250 mV		–	1.8	2.5	Ω
r_{pd}	Pull-down resistance	$\overline{EN}$ = HIGH; V_{BIAS} = 0.54 V; V_{DD} = 1.8 V		280	400	520	Ω
$r_{pd, channel\ 10}$	Pull-down resistor, channel 10	$\overline{EN}$ = HIGH; V_{BIAS} = 0.54 V; V_{DD} = 1.8 V; STREN = LOW		280	400	520	Ω
		$\overline{EN}$ = HIGH; V_{BIAS} = 0.54 V; V_{DD} = 1.8 V; STREN = HIGH		780	1120	1460	Ω
$r_{pu, channel\ 10}$	Pull-up resistor, channel 10	$\overline{EN}$ = HIGH; V_{BIAS} = 0.54 V; V_{DD} = 1.8 V; STREN = HIGH		430	622	810	Ω
r_{TT}	Sn-input termination resistor value. Thevenin equivalent (see Figure 4).	Input voltage sweep 0 < $V_{in(S)}$ < V_{DD}; TERM = HIGH		55	80	105	Ω

NOTES:
1. All typical values are at V_{DD} = 1.8 V, T_{amb} = 25 °C
2. Measured by the current between the Host and the DIMM terminals at the indicated voltages on each side of the switch.

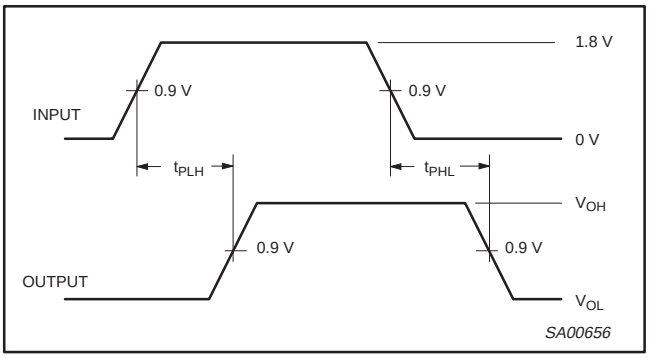
AC CHARACTERISTICS

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{DD} = +1.8 V ± 0.1 V Min	Typ	Max	UNIT
t_{pd}	Propagation delay[1] (see Figures 5 and 7)	HPx or xDPx	xDPx or HPx	—	50	100	ps
t_{PZH}, t_{PZL}	Enable time	Sn	HPx or xDPx	0.75	—	1.75	ns
t_{PHZ}, t_{PLZ}	Disable time	Sn	HPx or xDPx	0.75	—	1.75	ns
t_{osk}	Output skew Any output to any output, Waveform 5 (see note 2)			—	25	30	ps
t_{esk}	Edge skew Difference of rising edge propagation delay to falling edge propagation delay, Waveform 4 (see note 2)			—	25	30	ps

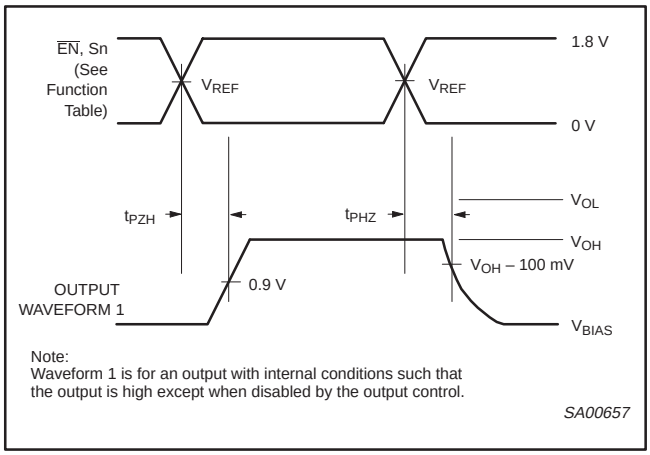
NOTES:
1. This parameter is not production tested.
2. Skew is not production tested.

HPx to xDPx AC WAVEFORMS AND TEST CIRCUIT

AC WAVEFORMS

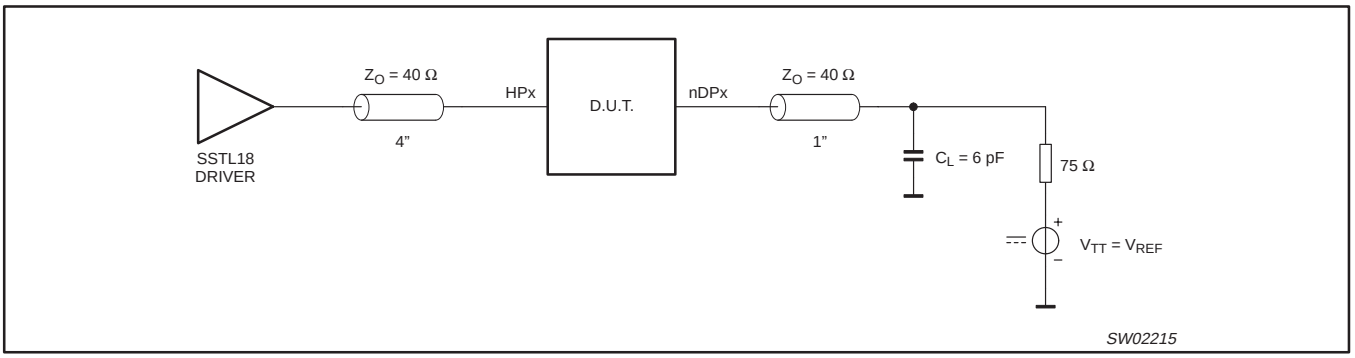


Waveform 1. Input (An) to Output (Yn) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT HPx to xDPx



NOTES:
1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate = 2.5 V/ns.
2. The outputs are measured one at a time with one transition per measurement.

Figure 5. Test circuit — HPx to xDPx

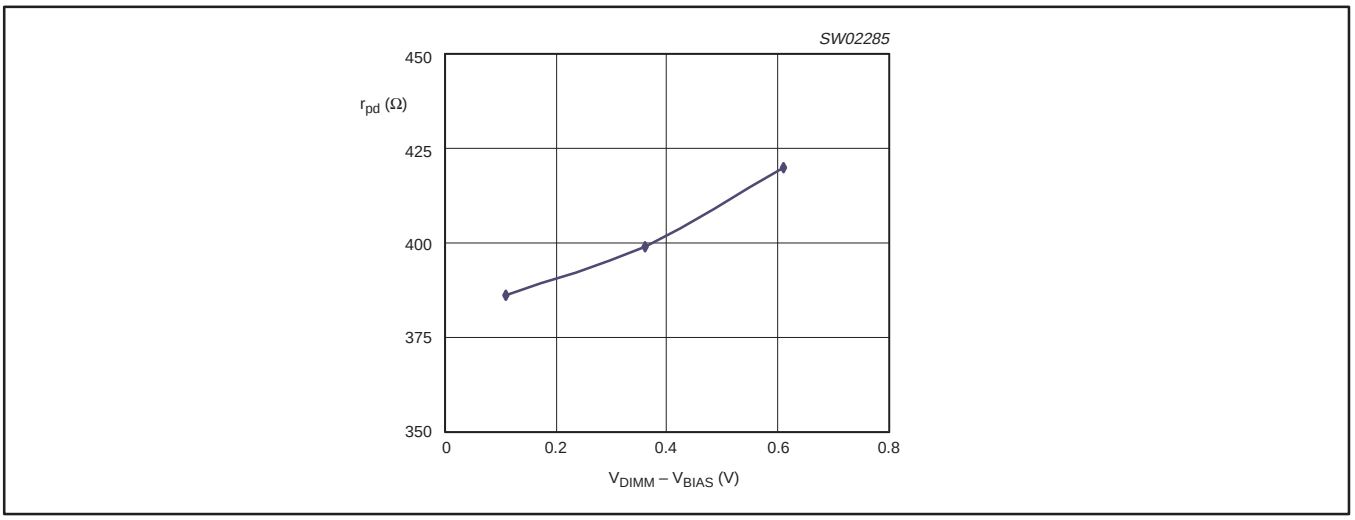
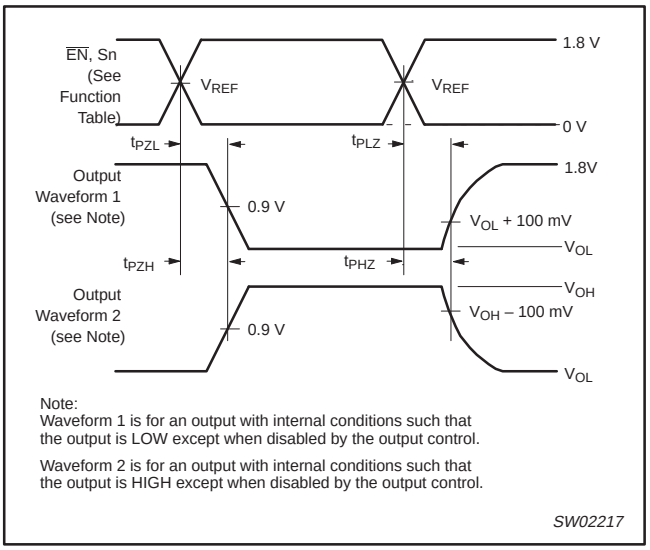


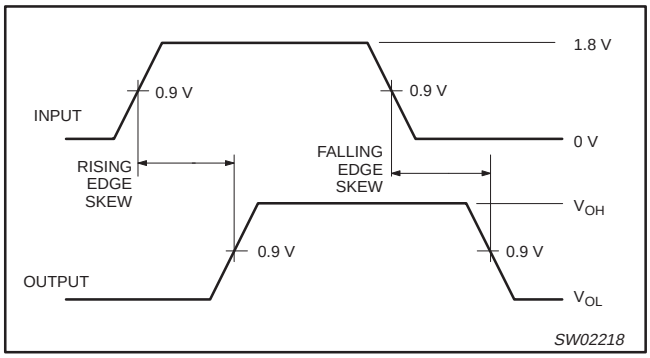
Figure 6. Pull-down resistance versus voltage.

xDPx to HPx AC WAVEFORMS AND TEST CIRCUIT

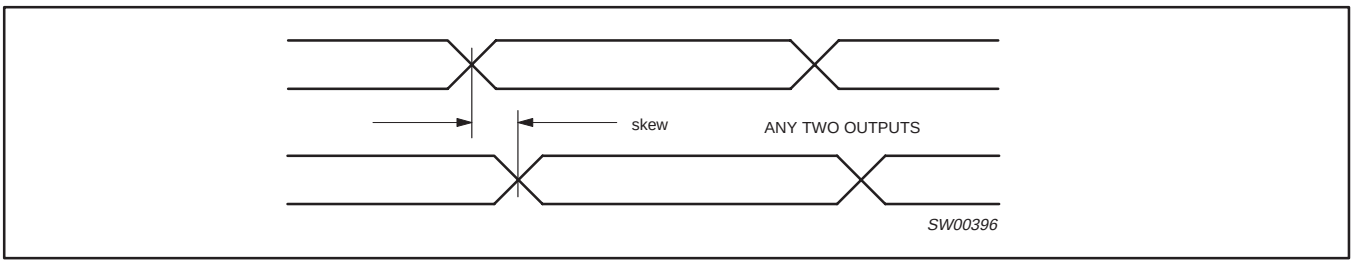
AC WAVEFORM



Waveform 3. 3-State Output Enable and Disable Times

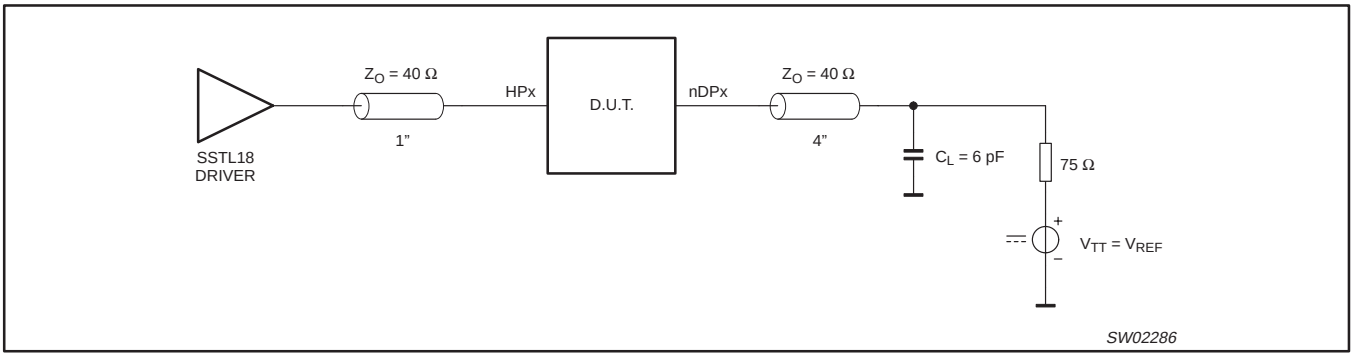


Waveform 4. Rising and Falling Edge Skew



Waveform 5. Skew Between Any Two Outputs

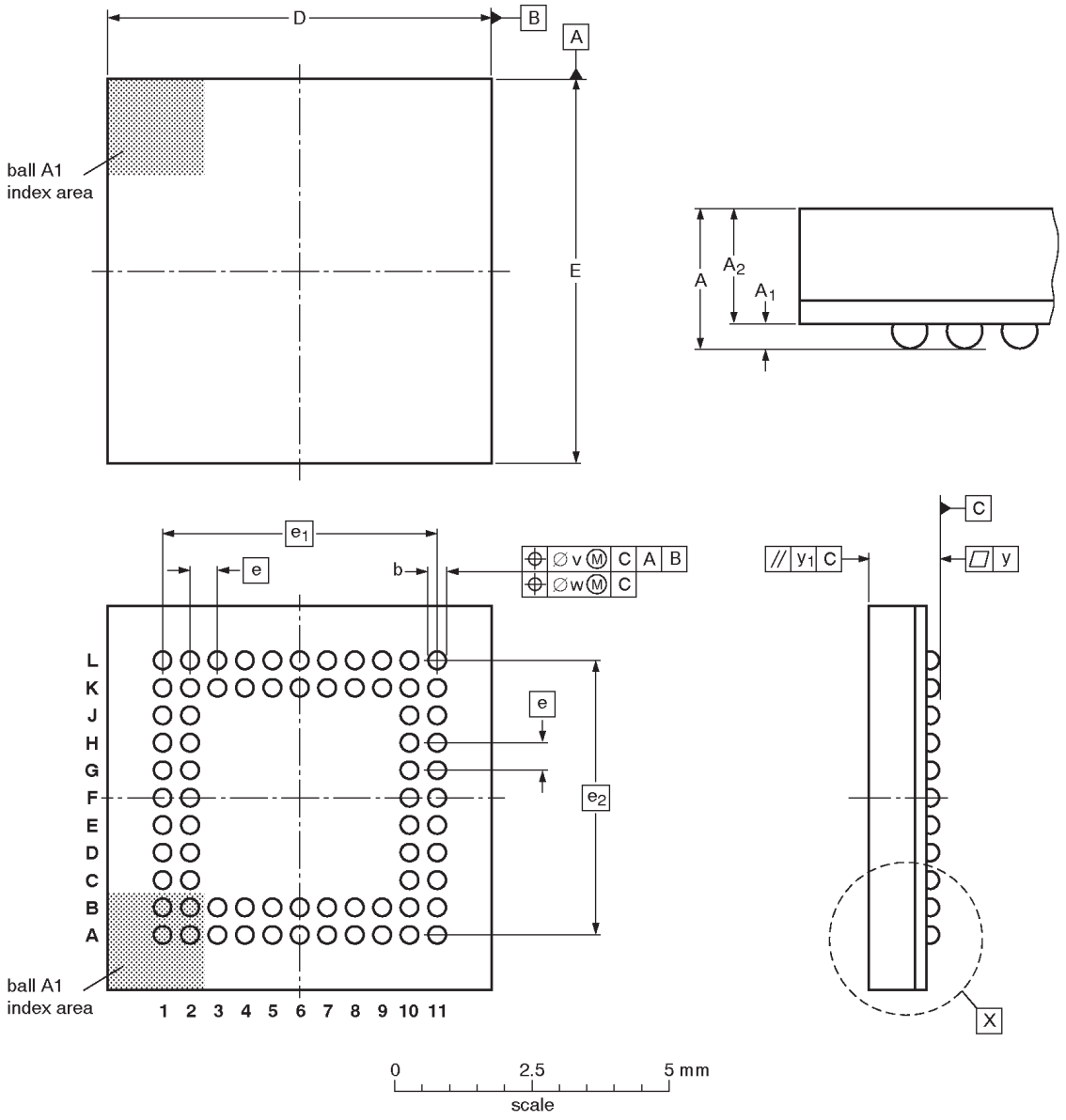
TEST CIRCUIT xDPx to HPx



NOTES:
1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate = 2.5 V/ns.
2. The outputs are measured one at a time with one transition per measurement.

Figure 7. Test circuit — xDPx to HPx

LFBGA72: plastic low profile fine-pitch ball grid array package; 72 balls; body 7 x 7 x 1.05 mm **SOT856-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.3 0.2	1.20 0.95	0.35 0.25	7.2 6.8	7.2 6.8	0.5	5	5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT856-1						~~04-04-27~~ 04-05-12

REVISION HISTORY

Rev	Date	Description
_2	20060922	**Product data sheet. Supersedes data of 2005 Jan 07.** Modifications: • data sheet released for public distribution
_1	20050107	**Product data sheet (9397 750 12977).**

Legal Information

Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this data sheet was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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