PI3PCIE2415-A

3.3V PCI Express® 2.0, 2-Lane, 2:1 Mux/DeMux Switch

Features

- 4 Differential Channel, 2:1 Mux/DeMux
- PCI Express® 2.0 Performance, 5.0Gbps
- Pinout optimized for placement between two PCIe slots
- Bi-directional operation
- Low Bit-to-Bit Skew, 7ps max
- Low Crosstalk: -26dB@5 GHz
- Low Off Isolation: -20dB@5 GHz
- V_{DD} Operating Range: +3.3V
- ESD Tolerance: 2kV HBM
- Low channel-to-channel skew, 35ps max
- Packaging (Pb-free & Green):
  - 42-contact, TQFN (ZH42)

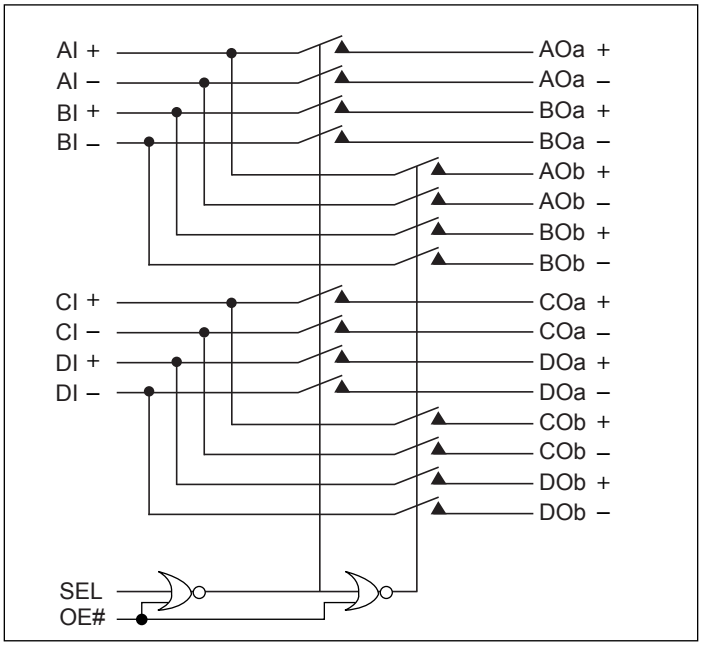
Description

Pericom Semiconductor's PI3PCIE2415-A is an 8 to 4 differential channel multiplexer/demultiplexer switch. This solution can switch 2 full PCI Express® 2.0, lanes to one of two locations. Using a unique design technique, Pericom has been able to minimize the impedance of the switch such that the attenuation observed through the switch is negligible. The unique design technique also offers a layout targeted for PCI Express signals, which minimizes the channel to channel skew as well as channel to channel crosstalk as required by the PCI Express specification.

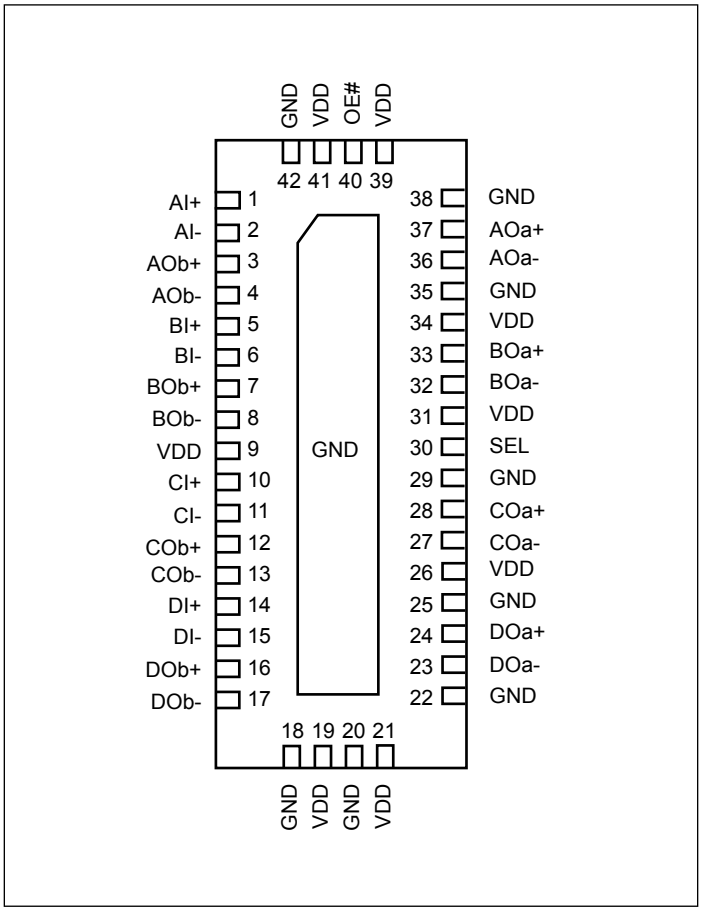
Application

Routing of PCIe® 2.0, signals with low signal attenuation.

Block Diagram



Pin Description (Top-Side View)



Truth Table

Function	SEL	OE#
xIy to xOay	L	L
xIy to xOby	H	L
All differential data pins = Hi-Z (disconnect)	X	H

Signal Descriptions

Pin Number	Pin Name	Type	Description
1, 2	AI+, AI-	Differential input	Differential input pair from PCIE signal source. Signal is passed through to the AOa+, AOa- pin respectively when SEL=0. Signal is passed through to the AOb+, AOb- pin respectively when SEL = 1.
37, 36	AOa+, AOa-	Differential pass-through input	Differential analog pass-through output. Signal from AI+ and AI- is passed through AOa+ and AOa- respectively when SEL=0.
3, 4	AOb+, AOb-	Differential pass-through input	Differential analog pass-through output. Signal from AI+ and AI- is passed through AOb+ and AOb- respectively when SEL=1.
5, 6	BI+, BI-	Differential input	Differential input pair from PCIE signal source. Signal is passed through to the BOa+, BOa- pin respectively when SEL=0. Signal is passed through to the BOb+, BOb- pin respectively when SEL = 1.
33, 32	BOa+, BOa-	Differential pass-through input	Differential analog pass-through output. Signal from BI+ and BI- is passed through BOa+ and BOa- respectively when SEL=0.
7, 8	BOb+, BOb-	Differential pass-through input	Differential analog pass-through output. Signal from BI+ and BI- is passed through BOb+ and BOb- respectively when SEL=1.
10, 11	CI+, CI-	Differential input	Differential input pair from PCIE signal source. Signal is passed through the COa+, COa- pin respectively When SEL=0. Signal is passed through to the COb+, COb- pin respectively when SEL = 1.
28, 27	COa+, COa-	Differential pass-through input	Differential analog pass-through output. Signal from CI+ and CI- is passed through COa+, COa- pin respectively when SEL = 0.
12, 13	COb+, COb-	Differential pass-through input	Differential analog pass-through output. Signal from CI+ and CI- is passed through COb+, COb- pin respectively when SEL = 1.
14, 15	DI+, DI-	Differential input	Differential input pair from PCIE signal source. Signal is passed through the DOa+, DOa- pin respectively When SEL=0. Signal is passed through to the DOb+, DOb- pin respectively when SEL = 1.
24, 23	DOa+, DOa-	Differential pass-through input	Differential analog pass-through output. Signal from DI+ and DI- is passed through DOa+, DOa- pin respectively when SEL = 0.
16, 17	DOb+, DOb-	Differential pass-through input	Differential analog pass-through output. Signal from DI+ and DI- is passed through DOb+, DOb- pin respectively when SEL = 1.
18, 20, 22, 25, 29, 35, 38, 42	GND	Ground input	Ground
30	SEL	3.6V tolerant low-voltage single-ended input	SEL controls the mux through a flow-through latch.
9, 19, 21, 26, 31, 34, 39, 41	V_{DD}	Power supply	Power, 3.3V ±10%
40	OE#	Input	Output Enable, active low. When OE# = 0, the device I/O is active. When OE# = 1, all I/O are high-impedance.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C
Supply Voltage to Ground Potential .....–0.5V to +4.6V
DC Input Voltage .....–0.5V to VDD
DC Output Current 120mA
Power Dissipation 0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	3.3V Power Supply		3.0	3.3	3.6	V
I_{DD}	Total current from V_{DD} 3.3V supply		0		2.5	mA
T_{CASE}	Case temperature range for operation within spec.		-40		85	Celsius

DC Electrical Characteristics (T_A = –40°C to +85°C, V_{DD} = 3.3V ± 10%)

Parameter	Description	Test Conditions	Min	Typ(1)	Max	Units
$V_{IH\text{-}SEL}$ / $V_{IH\text{-}OE\#}$ (2)	Input high level, SEL & OE# input		2.0		3.6	V
$V_{IL\text{-}SEL}$ / $V_{IL\text{-}OE\#}$(2)	Input low level, SEL & OE# input		0		0.8	V
I_{IN_SEL} / $V_{IN\text{-}OE\#}$(2)	Input leakage Current, SEL/OE# input	Measured with input at $V_{IH\text{-}SEL}$/$V_{IH\_OE\#}$ max and $V_{IL\text{-}SEL}$/$V_{IL\_OE\#}$ min	–10		10	uA
R_{ON}	On Resistance	V_{DD} = Min., V_{IN} = 1.3V, I_{IN} = 40mA			12	Ohm
C_{ON}	On Channel Capacitance	V_{IN} = 0, V_{DD} = 3.3V		2.0		pF

Note:

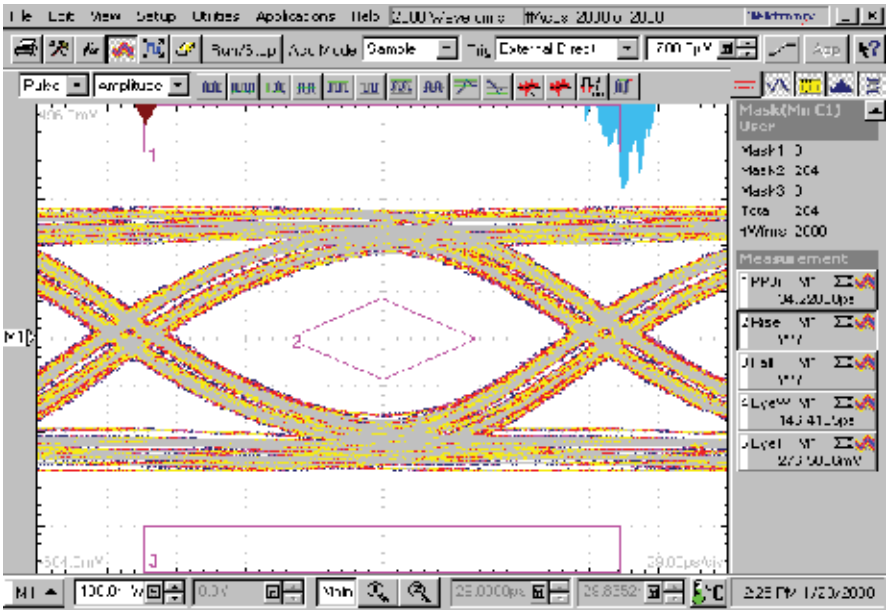
1. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Dynamic Electrical Characteristics for xI±, xOy±

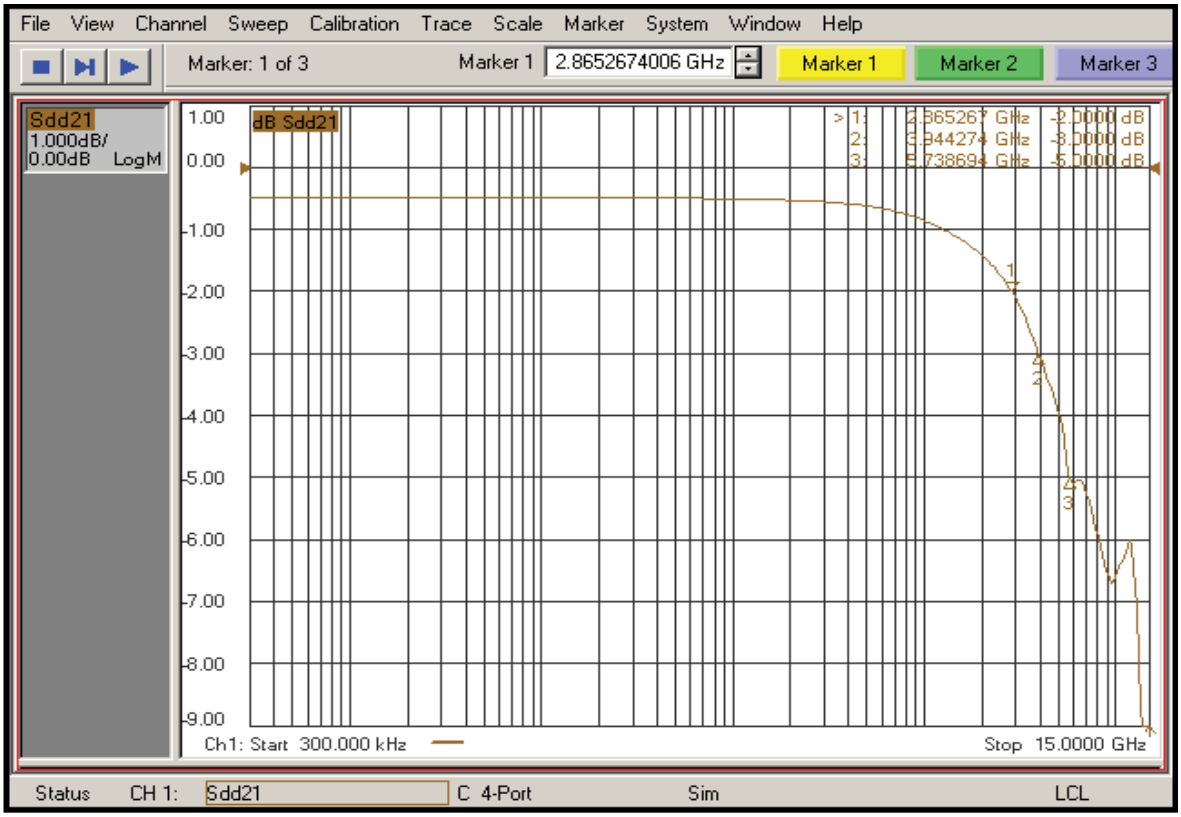
Parameter	Description	Test Conditions	Min.	Typ.(1)	Max.	Units
DDIL	Differential Insertion Loss	f=1.2GHz f=2.5GHz f=5.0GHz f=7.5GHz	-1.5 -2.0 -5.0 -9.0			dB
$DDIL_{OFF}$	Differential Off Isolation	f= 0 to 3.0GHz			-20.0	
DDRL	Differential Return Loss	f= 0 to 2.8GHz f= 2.8 to 5.0GHz f= 5.0 to 7.5GHz		-14.0 -8.0 -4.0		
DDNEXT	Near End Crosstalk	f= 0 to 2.5GHz f= 2.5 to 5.0GHz f= 5.0 to 7.5GHz			-32.0 -26.0 -20.0	

Switching Characteristics (T_A= -40° to +85°C, V_{DD} = 3.3V±10%)

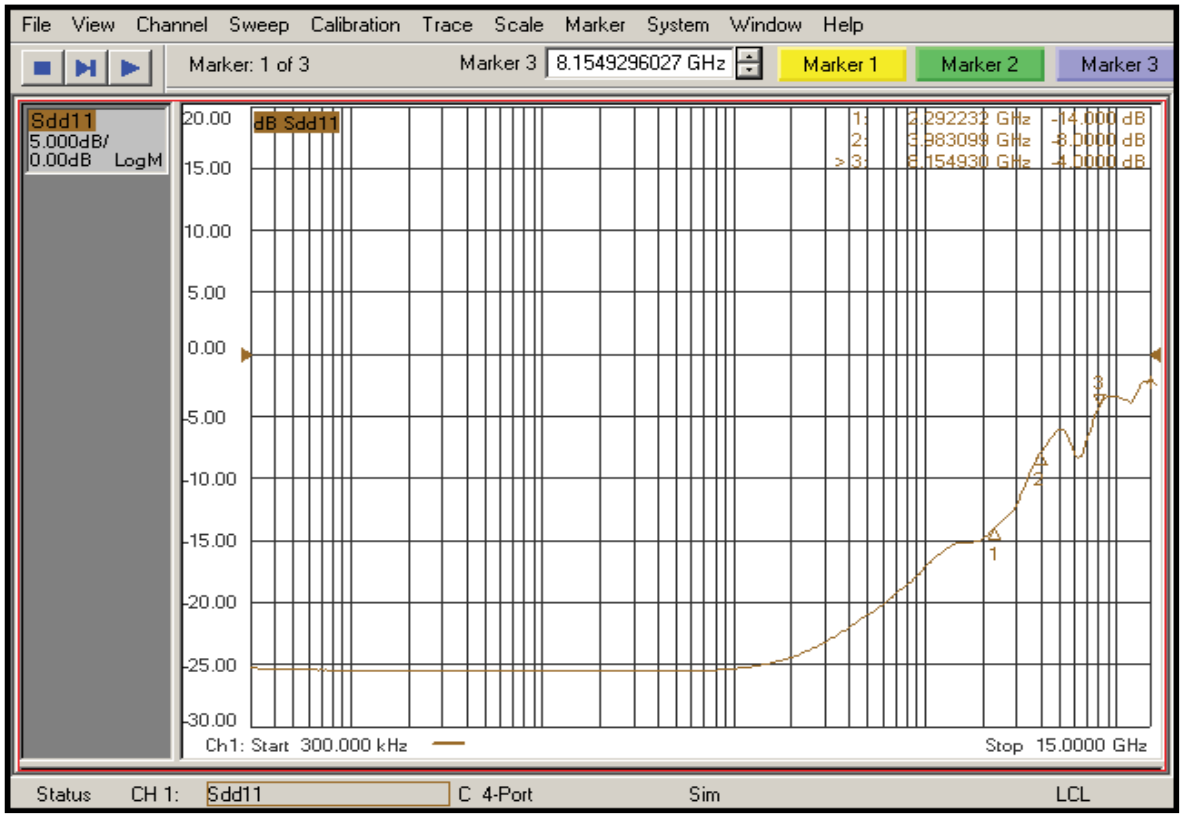
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PZH}, t_{PZL}	Line Enable Time - SEL to xI±, xOy±	See "Test Circuit for Electrical Characteristics"	0.5		12.0	ns
t_{PHZ}, t_{PLZ}	Line Disable Time - SEL to xI±, xOy±	See "Test Circuit for Electrical Characteristics"	0.5		12.0	ns
t_{b-b}	Bit-to-bit skew within the same differential pair	See "Test Circuit for Electrical Characteristics"			7	ps
t_{ch-ch}	Channel-to-channel skew	See "Test Circuit for Electrical Characteristics"			35	ps



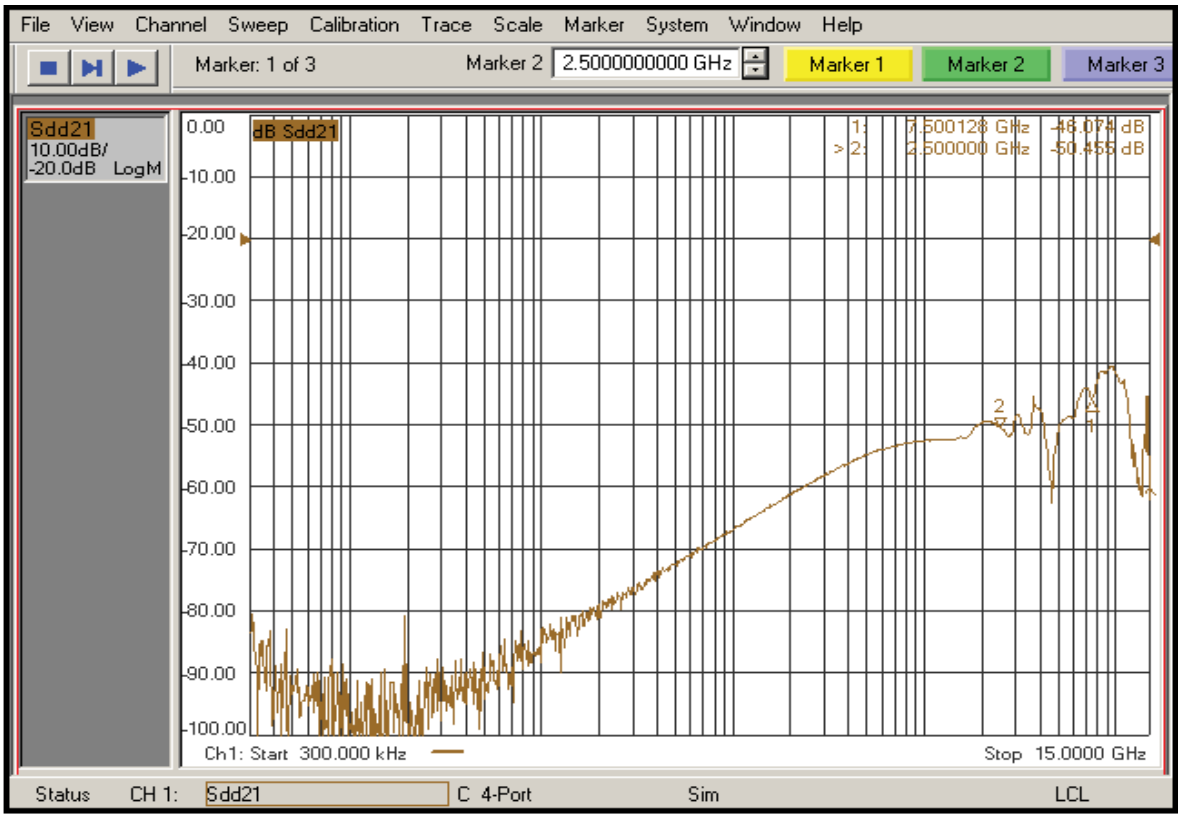
5.0 Gbps Receive Eye Mask -3.5dB WITH the Switch



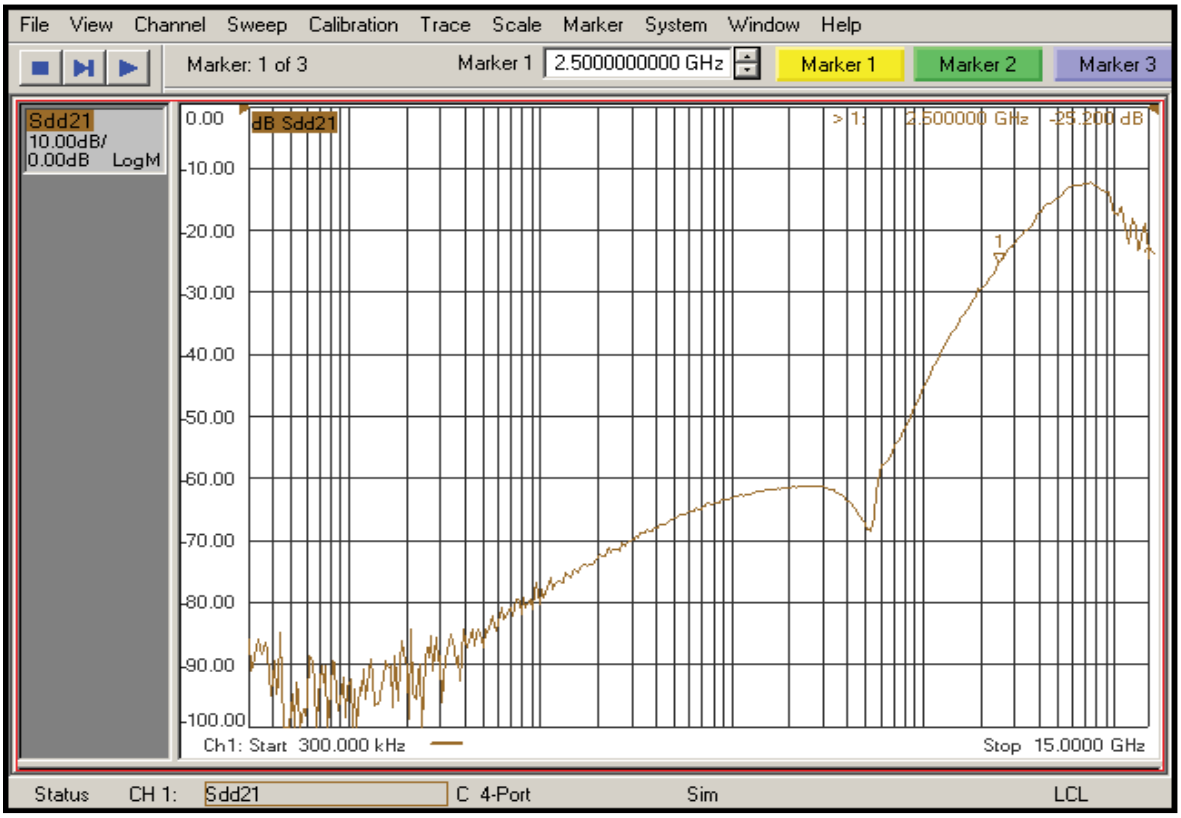
Differential Insertion Loss



Differential Return Loss

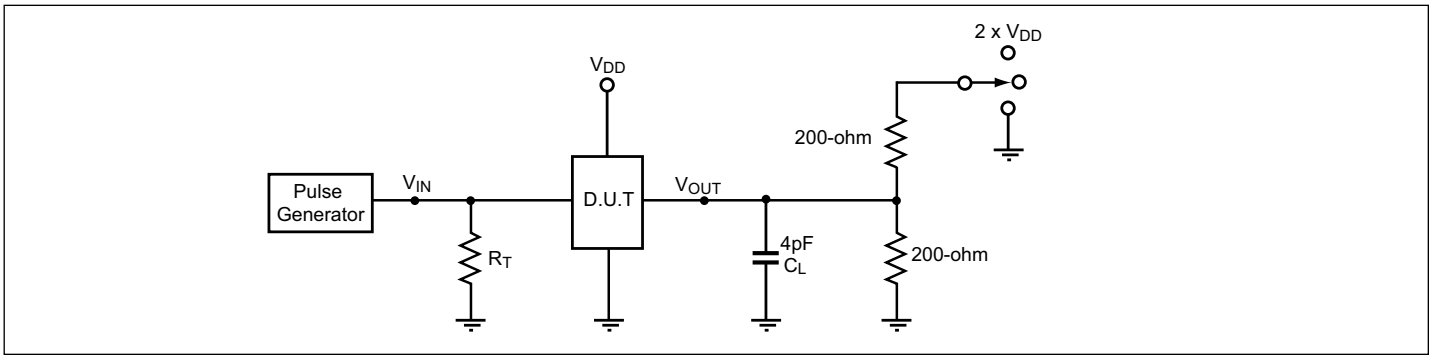


Differential Off Isolation



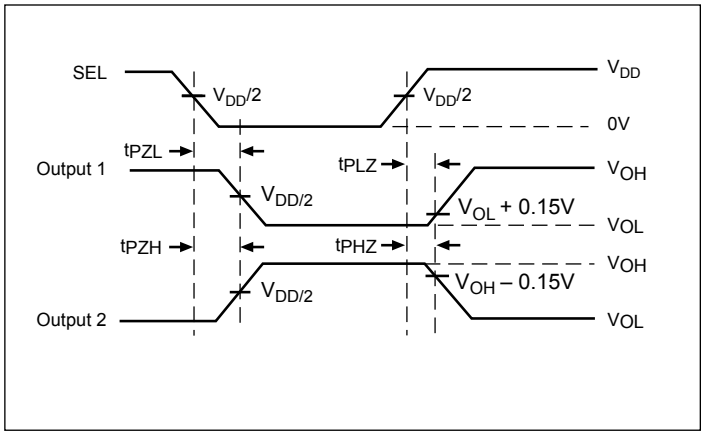
Differential Crosstalk

Test Circuit for Electrical Characteristics(1-5)



Notes:
1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, $Z_O = 50\Omega$, $t_R \leq 2.5$ns, $t_F \leq 2.5$ns.
5. The outputs are measured one at a time with one transition per measurement.

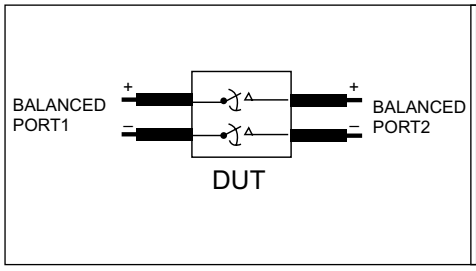
Switching Waveforms



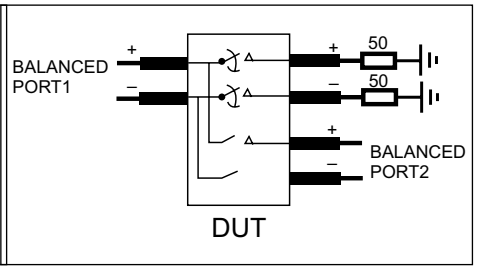
Voltage Waveforms Enable and Disable Times

Switch Positions

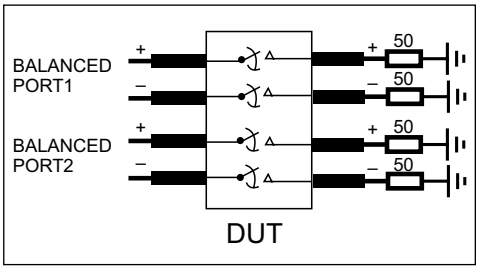
Test	Switch
t_{PLZ}, t_{PZL}	2 x V_{DD}
t_{PHZ}, t_{PZH}	GND
Prop Delay	Open



Diff. Insertion Loss and Return Test Circuit



Diff. Off Isolation Test Circuit



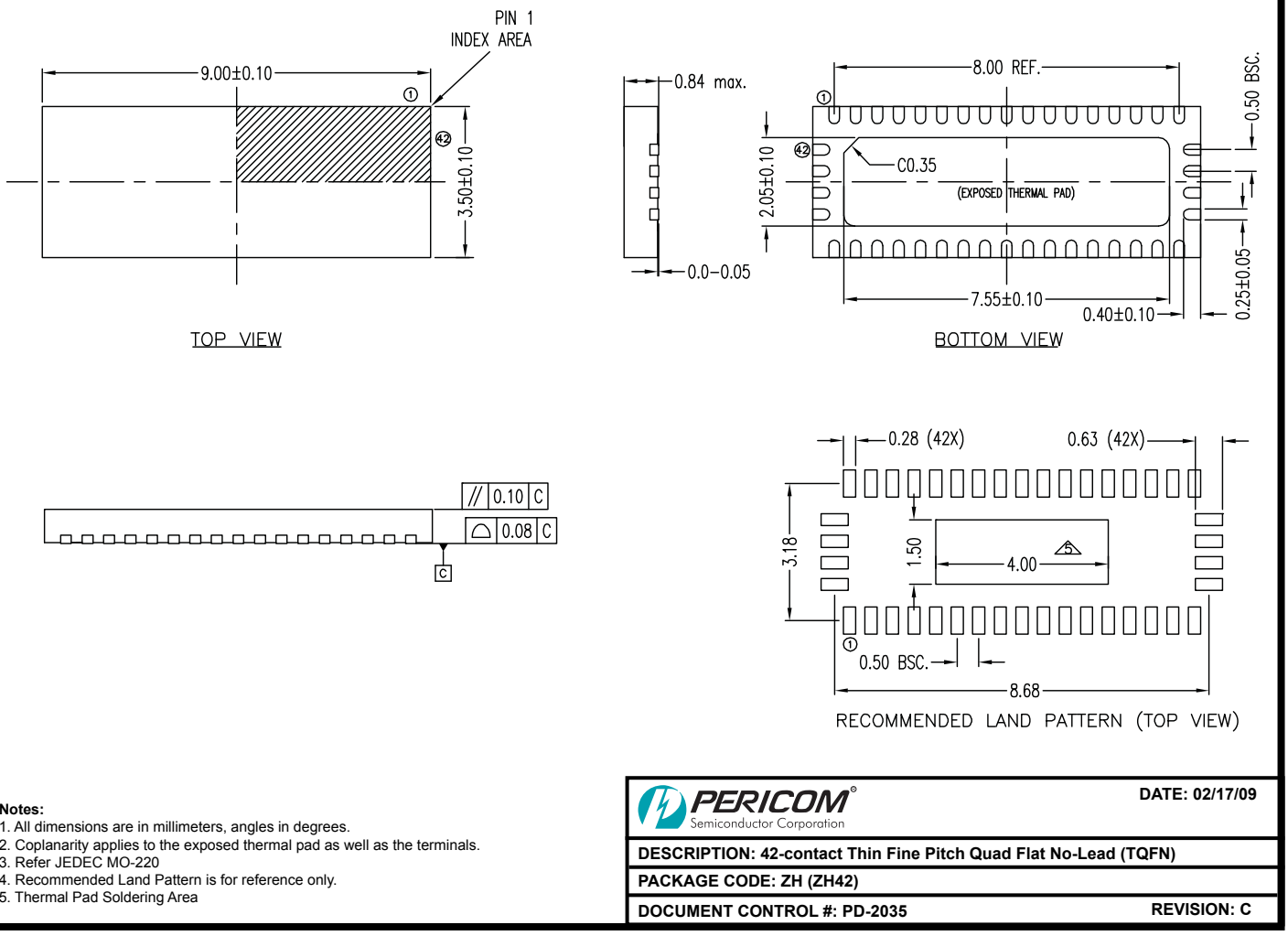
Diff. Near End Xtalk Test Circuit

Application Information

Differential Inputs/Output Characteristics for PCIe® 2.0 speeds

Symbol	Parameter	Min	Nom	Max	Units	Comments
Tbit	Unit Interval	199.94	200.00	200.06	ps	Defined by PCIe 2.0 spec.
$V_{RX-Diffp-p}$	Differential Input Peak-to-Peak Voltage	TBD		1.200	V	VRX-DIFFp-p = 2*|VRX-D+ - VRX-D-|. Applies to IN_S and RX_IN signals.
T_{RX-EYE}	Minimum Eye Width at IN_D input pair.	TBD			Tbit	
$V_{CM-AC-pp}$	AC Peak Common-Mode Input Voltage			100	mV	VCM-AC-pp = |VRX-D+ + VRX-D-|/2 - VRX-CM-DC. VRX-CM-DC = DC(avg) of |VRX-D++VRX-D-|/2 VCM-AC-pp includes all frequencies above 30kHz.
$Z_{RX-DIFF-DC}$	Dc Differential Input Impedance	80	100	120	Ω	Rx DC Differential Mode impedance
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required IN_D+ as well as IN_D- DC impedance (50 Ω ± 20% tolerance). Includes mux resistance.
$V_{RX-Bias}$	Rx input termination voltage	0		2.0	V	Intended to limit power-up stress on PCIe output buffers.

Packaging Mechanical: 42-Contact TQFN (ZH)



Notes:
1. All dimensions are in millimeters, angles in degrees.
2. Coplanarity applies to the exposed thermal pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended Land Pattern is for reference only.
5. Thermal Pad Soldering Area

PERICOM Semiconductor Corporation — DATE: 02/17/09

DESCRIPTION: 42-contact Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH (ZH42)

DOCUMENT CONTROL #: PD-2035 — REVISION: C

09-0116

Note: For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description
PI3PCIE2415-AZHE	ZH	Pb-free & Green, 42-contact TQFN

Notes:

• Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

• "E" denotes Pb-free and Green

• Adding an "X" at the end of the ordering code denotes tape and reel packaging