5.0Gbps 4-Lane PCIe® 2.0 ReDriver™ with Equalization, Emphasis, & I²C Control

Features

- Up to 5.0Gbps PCI Express® 2.0 Serial ReDriver
- Supporting 8 differential channels or 4 lanes of PCIe Interface
- I²C configuration controls (3.3V tolerant)
- Adjustable receiver equalization and transmitter de-emphasis and output levels
- Variable input an output termination
- 1:2 channel broadcast
- Channel loop-back
- Electrical Idle fully supported
- Receiver detect and individual output control
- Single supply voltage, 1.2V ± 0.05V
- Power down modes
- Packaging: 56-contact TQFN, Pb-free & Green

Description

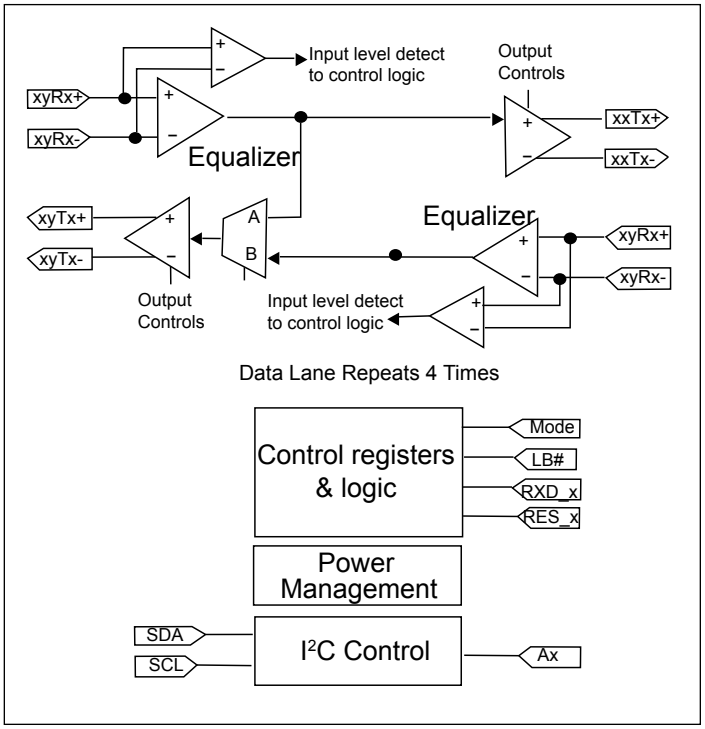
Pericom Semiconductor's PI2EQX5864D is a low power, PCIe® compliant signal redriver. The device provides programmable equalization, amplification, and de-emphasis by using 8 select bits, to optimize performance over a variety of physical mediums by reducing Inter-symbol interference.

PI2EQX5864D supports eight 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or extends the signals across other distant data pathways on the user's platform.

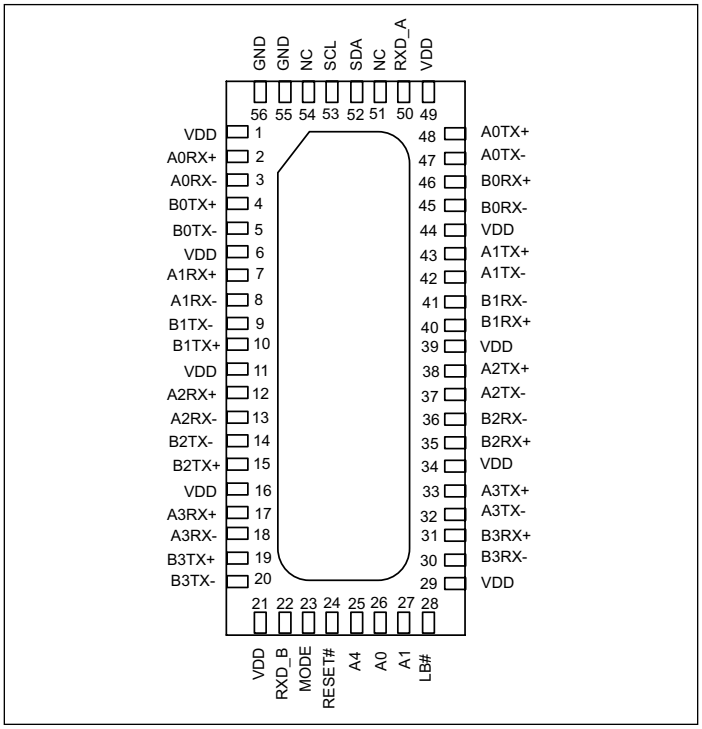
The integrated equalization circuitry provides flexibility with signal integrity of the PCI Express signal before the ReDriver™, whereas the integrated de-emphasis circuitry provides flexibility with signal integrity of the signal after the redriver.

In addition to providing signal re-conditioning, Pericom's PI2EQX5864D also provides power management Stand-by mode operated by a Bus Enable pin.

Block Diagram



Pin Configuration



Pin Description

Pin #	Pin Name	Type	Description
Data Signals			
2 3	A0RX+, A0RX-	I I	CML inputs for Channel A0, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
48 47	A0TX+, A0TX-	O O	CML outputs for Channel A0, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
7 8	A1RX+, A1RX-	I I	CML inputs for Channel A1, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
43 42	A1TX+, A1TX-	O O	CML outputs for Channel A1, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
12 13	A2RX+, A2RX-	I I	CML inputs for Channel A2, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
38 47	A2TX+, A2TX-	O O	CML outputs for Channel A2, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
17 18	A3RX+, A3RX-	I I	CML inputs for Channel A3 with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
33 32	A3TX+, A3TX-	O O	CML outputs for Channel A3, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
46 45	B0RX+, B0RX-	I I	CML inputs for Channel B0, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
4 5	B0TX+, B0TX-	O O	CML outputs for Channel B0, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
41 40	B1RX-, B1RX+	I I	CML inputs for Channel B1, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
9 10	B1TX-, B1TX+	O O	CML outputs for Channel B1, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
36 35	B2RX-, B2RX+	I I	CML inputs for Channel B2, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
14 15	B2TX-, B2TX+	O O	CML outputs for Channel B2, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.
31 30	B3RX+, B3RX-	I I	CML inputs for Channel B3, with internal 50-Ohm pull down during normal operation, and >200K-Ohm otherwise.
19 20	B3TX+, B3TX-	O O	CML outputs for Channel B3, with internal 50-Ohm pull up during normal operation and 2K-Ohm pull up otherwise.

(continued on next page)

Pin Description (continued)

Pin #	Pin Name	Type	Description
Control Signals			
26, 27, 25	A0, A1, A4	I	I^2C programmable address bit A0, A1 and A4.
28	LB#	I	Loopback control input. Input with internal 100K-Ohm pull-up resistor. LB# = High or open for normal operation. LB# = Low for loopback connection of A_RX to A_TX and B_TX.
23	Mode	I	Enables I^2C control when LOW. Has internal 100K-Ohm pull-up resistor. A LVCMOS high level selects input pins control, and disables I^2C operation. Note, during startup, input status of the control pin (LB#, RES_A/B#, RXD_A/B) will be latched to set the initial register state.
51	NC		No Connect
54	NC		No Connect
24	RESET#	I	RESET# is an active low channel reset input for Channel A0, B0, A1, B1, A2, B2, A3 and B3 with internal 100K-Ohm pull-up resistor. When low, receiver detection cycle is reset, and normal detection cycle is carry on after the pin goes high.
50	RXD_A	I	Receiver detect enable input for Channel A0, A1, A2 and A3 with internal 100K-Ohm pull-up resistor.
22	RXD_B	I	Receiver detect enable input for Channel B0, B1, B2 and B3 with internal 100K-Ohm pull-up resistor.
53	SCL	I/O	I^2C SCL clock input.
52	SDA	I/O	I^2C SDA data input.
55, 56, Center Pad	GND	PWR	Supply Ground
1, 6, 11, 16, 21, 29, 34, 39, 44, 49	V_{DD}	PWR	1.2V Supply Voltage

Description of Operation:

Configuration Modes

Device configuration can be performed in two ways depending on the state of the MODE input. MODE determines whether IC configuration status is from the input pins or via I^2C control. When MODE is set high, the configuration input pins set the configuration operating state as stored in configuration registers. While MODE is set high, changes to these control registers are disabled and the initial condition is protected from any changes to insuring a known operating state. When the MODE pin is low, reprogramming of these control registers via I^2C is allowed. Note that the MODE pin is not latched, and is always active to enable or disable I^2C access.

During initial power-on, the value at the configuration input pins: LB#, RESET#,RXD_A and RXD_B, will be latched to the configuration registers as initial startup states.

Equalizer Configuration

The PI2EQX5864D input equalizer compensates for signal attenuation and Inter-Symbol Interference (ISI) resulting from long signal traces or cables, vias, signal crosstalk and other factors, by boosting the gain of high-frequency signal components. Because either too little, or too much, signal compensation may be non-optimal eight levels are provided to adjust for any application.

Equalizer configuration can be programmed via I^2C when the mode pin is low. Each group of four channels, A and B, has separate equalization control, and all four channels within the group are assigned the same configuration state. The Equalizer Selection table below describes the register state and associated operation of the equalizer.

Equalizer Selection

SEL2_[A:B]	SEL1_[A:B]	SEL0_[A:B]	@1.25GHz	@2.5GHz
0	0	0	0.5dB	1.2dB
0	0	1	0.6dB	1.5dB
0	1	0	1.0dB	2.6dB
0	1	1	1.9dB	4.3dB
1	0	0	2.8dB	5.8dB
1	0	1	3.6dB	7.1dB
1	1	0	5.0dB	9.0dB
1	1	1	7.7dB	12.3dB

Output Configuration

The PI2EQX5864D provides flexible output strength and emphasis controls to provide the optimum signal to pre-compensate for losses across long trace or noisy environments so that the receiver gets a clean with good eye opening. Control of output configuration is grouped for the A and B channels, so that each channel within the group has the same setting.

Output configuration can be set via I^2C when the mode pin is LOW. The Output Swing Control table shows available configuration settings for output level control, as specified by the SELx_y registers.

Output Swing Control

S1_[A:B]	S0_[A:B]	Swing (Diff. VPP)
0	0	1V
0	1	0.5V
1	0	0.7V
1	1	0.9V

Emphasis settings are determined by the state of the Dx_y input pins and configuration registers, as shown below. De-Emphasis is selected as the default power-on mode in following the PCI Express specification, but can be changed to Pre-emphasis via reprogramming the Loopback and Emphasis Control register using the I^2C interface.

Output De-Emphasis Adjustment

D2_[A:B]	D1_[A:B]	D0_[A:B]	De-emphasis
0	0	0	0dB
0	0	1	-2.5dB
0	1	0	-3.5dB
0	1	1	-4.5dB
1	0	0	-5.5dB
1	0	1	-6.5dB
1	1	0	-7.5dB
1	1	1	-8.5dB

Input Level Detect

An input level detect and output squelch function is provided on each channel to eliminate re-transmission of input noise. A continuous signal level below the V_{th-} threshold causes the output driver to go to a high-impredance state, so that both the positive and negative output signal are pulled to V_{DD} by the internal pull-up resistors. This feature supports L0S PCI Express Electrical Idle state.

Receiver Detect

Automatic Receiver Detection is a feature that can set the number of active channels. By sensing the presence of a load device on the output, the channel can be automatically enabled for operation. This allows the PI2EQX5864D to configure itself properly depending on the devices it is communicating with, whether it is a 4-lane, 3-lane, 2-lane or just 1-lane device or adapter card.

Receiver Detect is enabled by the RXD_A, or RXD_B pins, or alternatively via I^2C programming. When RXD_A or RXD_B is set to low, the Receiver Detect operation for that group of channels is disabled, and those channels go directly to 50-Ohm input termination to ground and 50-Ohm output termination to V_{DD} (for a valid differential channel input level) or to 2K-Ohm (if the signal level is less than the threshold level).

The RESET# input is used to reset the receiver detect state machine to its initial state. The start of the receiver detect cycle starts when RESET# transitions from low to high.

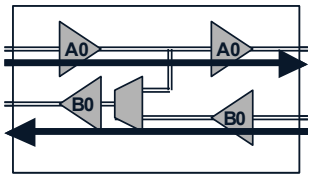
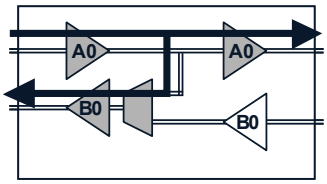
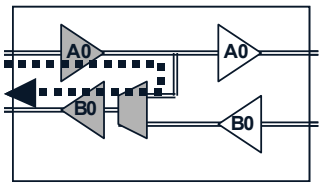
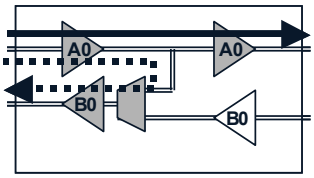
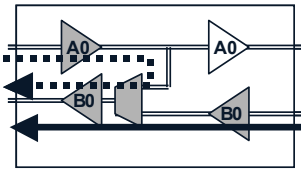
When a Receiver Detect cycle begins the differential channel pins are enabled with a 2K-Ohm pull-up to V_{DD}. A 50-Ohm Receiver termination will change the pin level. This pin level is evaluated after a fixed time-out, and the channel is then set into the proper operating state. The register bits RX50_Ax and RX50_Bx represent the receiver detect result for their specific channels.

The I/O operation table summarizes the relationships and operation of receiver detect and other signals involved with I/O control.

I/O Operation Control

Control Inputs		Detection States		Data Channel I/O		
RXD_x	RESET#	RX50	SIG_x	Input Termination	Output Termination	Mode
0	0	X	X	Hi-Z	2K-Ohm pull-up	Channel disabled, output pulls to V_{DD}. Receiver detect reset
0	1	X	0	50-Ohm pull-down	2K-Ohm pull-up	Channel enabled, no input signal, output pulls to V_{DD}. Receiver detect disabled
0	1	X	1	50-Ohm pull-down	50-Ohm pull-up	Channel enabled, valid input signal detected, output driving. Receiver detect disabled.
1	0	X	X	Hi-Z	2K-Ohm pull-up	Channel disabled. Receiver detect reset.
1	1	0	X	Hi-Z	2K-Ohm pull-up	Channel disabled, output pulls to V_{DD}. Receiver detect enabled, no receiver detected.
1	1	1	0	50-Ohm pull-down	2K-Ohm pull-up	Channel inactive, output pulls to V_{DD}. Receiver detect enabled, receiver detected. No input signal
1	1	1	1	50-Ohm pull-down	50-Ohm pull-up	Channel active, valid input signal detected, output driving. Receiver detect enabled, load detected.

Loopback Operation

Loopback Modes		CONDITIONS
	NORMAL MODE A0Rx to A0Tx, B0Rx to B0Tx	LB_A0B0# = 1 INDIS_A0 = 0 OUTDIS_A0 = 0 INDIS_B0 = 0 OUTDIS_B0 = 0
	BROADCAST MODE A0Rx to A0Tx and B0Tx	LB_A0B0# = 0 INDIS_A0 =0 INDIS_B0 = 1 OUTDIS_B0 = 0
	LOOPBACK MODE A0Rx to B0Tx	LB_A0B0# = 0 INDIS_A0 = 0 OUT_DIS_A0 = 1 INDIS_B0 = 1 OUTDIS_B0 = 0
	DEMUX MODE Solid Line A0Rx to A0Tx	LB_A0B0# = 1 INDIS_A0 = 0 OUTDIS_A0 = 0 INDIS_B0 = 1 OUTDIS_B0 = 0
	DEMUX MODE Dashed Line A0Rx to B0Tx	LB_A0B0# = 0 INDIS_A0 = 0 OUTDIS_A0 = 0 INDIS_B0 = 1 OUTDIS_B0 = 0
	MUX MODE Solid Line B0Rx to B0Tx	LB_A0B0# = 1 INDIS_A0 = 0 OUTDIS_A0 = 1 INDIS_B0 = 0 OUTDIS_B0 = 0
	MUX MODE Dasked Line A0Rx to B0Tx	LB_A0B0# = 0 INDIS_A0 = 0 OUTDIS_A0 = 1 INDIS_B0 = 0 OUTDIS_B0 = 0

Each lane provides a loopback mode for test purposes which is controlled by a strapping pin and I^2C register bit. The LB# pin controls all lanes together. When this pin is high normal data mode is enabled. When LB# is low the loopfeature mode is enabled. The adjacent figure diagrams this operation. Loopback is not intended to be dynamically switched, and the normal system application is to initialize to one configuration or the other.

The Loopback mode can also support mux/demux operation. Using I^2C configuration, unused inputs and outputs can be disabled to minimize power and noise.

I²C Operation

The PI2EQX5864D I²C controller operates as a slave device, supporting standard rate operation of 100Kbps, with 7-bit addressing mode. The data byte format is 8 bit bytes. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred. Address bits A4, A1 and A0 are programmable to support multiple chips environment. The data is loaded until a Stop sequence is issued.

Configuration Register Summary

Byte	Mnemonic	Function
0	SIG	Signal Detect, indicates valid input signal level
1	RX50	Receiver Detect Output, indicates whether a receiver load was detected
2	LBEC	Loopback and Emphasis Control, provides for control of the loopback function and emphasis mode (pre-emphasis or de-emphasis)
3	INDIS	Channel Input Disable, controls whether a channels input buffer is enabled or disabled
4	OUTDIS	Channel Output Disable: Controls whether a channels output buffer is enabled or disabled
5	RESET	Channel Reset
6	PWR	Power Down Control, enables power down for each channel individually
7	RXDE	Receiver Detect Enable, controls the receiver detect operation
8	AEOC	A-Channels Equalizer and Output Control
9	BEOC	B-Channels Equalizer and Output Control
10	RSVD	Reserved
11	RSVD	Reserved

Transferring Data

Every byte put on the SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I²C Data Transfer diagram). The PI2EQX5864D will never hold the clock line SCL LOW to force the master into a wait state.

Note: Byte-write and byte-read transfers have a fixed offset of 0x00, because of the very small number of configuration bytes. An offset byte presented by a host to the PI2EQX5864D is not used.

Addressing

Up to eight PI2EQX5864D devices can be connected to a single I²C bus. The PI2EQX5864D supports 7-bit addressing, with the LSB indicating either a read or write operation. The address for a specific device is determined by the A0, A1 and A4 input pins.

Address Assignment							
A6	A5	A4	A3	A2	A1	A0	R/W
1	1	Program	0	0	Programmable		1=R, 0=W

Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, the PI2EQX5864D will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I^2C Data Transfer diagram. The PI2EQX5864D will generate an acknowledge after each byte has been received.

Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, the PI2EQX5864D will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. For a write cycle, the first data byte following the address byte is a dummy or fill byte that is not used by the PI2EQX5864D. This byte is provided to provided compatibility with systems implementing 10-bit addressing. Data is transferred with the most significant bit (MSB) first. After each block write, address pointer will reset to byte 0.

Register Description

Byte 0 - Signal Detect (SIG)

SIG_xy=0=low input signal, SIG_xy=1=valid input signal

Bit	7	6	5	4	3	2	1	0
Name	**SIG_A0**	**SIG_B0**	**SIG_A1**	**SIG_B1**	**SIG_A2**	**SIG_B2**	**SIG_A3**	**SIG_B3**
Type	R	R	R	R	R	R	R	R
Power-on State	X	X	X	X	X	X	X	X

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Signal Detect register provides information on the instantaneous status of the channel input from the Input Level Threshold Detect circuit. If the input level falls below the Vth- level the relevant SIG_xy bit will be 0, indicating a low-level noise or electrical idle input, resulting in the outputs going to the high-impedance off state or squelch mode. If the input level is above Vth-, then SIG_xy is 1, indicating a valid input signal, and active signal recovery operation.

BYTE 1 - Receiver Detect Output Register (RX50)

RX50_xy = 1 = load detected, RX50_xy = 0 = No receiver found

Bit	7	6	5	4	3	2	1	0
Name	**RX50_A0**	**RX50_B0**	**RX50_A1**	**RX50_B1**	**RX50_A2**	**RX50_B2**	**RX50_A3**	**RX50_B3**
Type	R	R	R	R	R	R	R	R
Power-on State	X	X	X	X	X	X	X	X

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The RX50_xy bits report the result of a receiver detection cycle. One bit is assigned for each channel of the device. RX50_xy is at a logic 1 level indicating a load and receiver was detected. When RX50_xy is 0 then a load device was not detected. The RX50 register is read-only, and is undefined after power-up until a Receiver Detection cycle completes.

BYTE 2 - Loopback and Emphasis Control Register (LBEC)

LB_xyxy#=0=loopback mode, LB_xyxy#=1=normal mode, DE_x=0=pre-emphasis, DE_x=1=de-emphasis

Bit	7	6	5	4	3	2	1	0
Name	**LB_A0B0#**	**LB_A1B1#**	**LB_A2B2#**	**LB_A3B3#**	**DE_A**	**DE_B**	**rsvd**	**rsvd**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Power-on State	LB#	LB#	LB#	LB#	1	1	X	X

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

Individual control for each lane is provided for the loopback function via this register.

BYTE 3 - Channel Input Disable (INDIS)

INDIS_xy=0=enable input, INDIS_xy=1=disable input

Bit	7	6	5	4	3	2	1	0
Name	**INDIS_A0**	**INDIS_B0**	**INDIS_A1**	**INDIS_B1**	**INDIS_A2**	**INDIS_B2**	**INDIS_A3**	**INDIS_B3**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	0	0	0	0	0	0	0	0

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Channel Input Disable register, provides control over the input buffer of each channel independently. When and INDIS_xy bit is logic 1, then the input buffer is switched off and the input termination is high impedance. This feature can be used for PCB testing, and when only one input is used during Loopback as a demux function. When INDIS_xy is at a logic 0 state then the input buffer is enabled (normal operating mode).

BYTE 4 - Channel Output Disable (OUTDIS)

ODIS_xy=0=enable output, ODIS_xy=1=disable output

Bit	7	6	5	4	3	2	1	0
Name	**ODIS_A0**	**ODIS_B0**	**ODIS_A1**	**ODIS_B1**	**ODIS_A2**	**ODIS_B2**	**ODIS_A3**	**ODIS_B3**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	0	0	0	0	0	0	0	0

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Channel Output Disable register, allows control over the output buffer of each channel independently. When and OUTDIS_xy bit is logic 1, then the output buffer is switched off and the termination is high impedance. This feature can be used for PCB testing, and when only one output is used during Loopback as a mux function. When INDIS_xy is at a logic 0 state then the input buffer is enabled (normal operating mode).

BYTE 5 - Channel Reset (RESET)

RESET# =0=reset, RESET# =1=normal operation. Latch from RESET# input at startup

Bit	7	6	5	4	3	2	1	0
Name	**RESET_A0#**	**RESET_B0#**	**RESET_A1#**	**RESET_B1#**	**RESET_A2#**	**RESET_B2#**	**RESET_A3#**	**RESET_B3#**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	Latch from RESET# inputs at startup							

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Channel Reset register allows for restart of an individual channels Receiver Detect function. A transition from 0 to 1 initiates a new Receiver Detect cycle (if the channel is enabled and receiver detect is enabled). While static at 0 or 1, the RESET# bit will have no effect on operation. The Channel Reset bits are read/write allowing the current state to be checked.

BYTE 6 - Power Down Control (PWR)

PD_xy# =0=channel off/power down, PD_xy# =1=normal operation, Latch from PD# input at startup

Bit	7	6	5	4	3	2	1	0
Name	**PD_A0#**	**PD_B0#**	**PD_A1#**	**PD_B1#**	**PD_A2#**	**PD_B2#**	**PD_A3#**	**PD_B3#**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	1	1	1	1	1	1	1	1

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Power Down Control register allows for individual control over each channel for power savings. When PD_xy# is logic 0 the channel is turned off. When PD_xy# is 1 then the channel is enabled for normal operation.

BYTE 7 - Receiver Detect Enable (RXDETEN)

RXD_xy =0=channel off/power down, RXD_xy =1=normal operation, Latch from PD# input at startup

Bit	7	6	5	4	3	2	1	0
Name	**RXDETEN_A0**	**RXDETEN_B0**	**RXDETEN_A1**	**RXDETEN_B1**	**RXDETEN_A2**	**RXDETEN_B2**	**RXDETEN_A3**	**RXDETEN_B3**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	Latch from RXD_A & RXD_B inputs at startup							

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Receiver Detect Enable register allows for control of the receiver detect state machine for each individual channel. When RXD_xy is set to 0, then the receiver detect function is disabled. When RXD_xy is logic 1, then the receiver detect state machine is enabled for operation. The initial state of the register bits are determined by the RXD_A and RXD_B input pins during power-up.

BYTE 8 - A-Channels Equalizer and Output Control (AEOC)

SELx_A: Equalizer configuration, Dx_A: Emphasis control, Sx_A: Output level control (see Configuration Table)

Bit	7	6	5	4	3	2	1	0
Name	**SEL0_A**	**SEL1_A**	**SEL2_A**	**D0_A**	**D1_A**	**D2_A**	**S0_A**	**S1_A**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	**1**	**1**	1	1	1	1	1	1

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The A-Channels Equalizer and Output Control register is used to control the configuration of the input equalizer and output emphasis and levels of the four A channels. These register bits are loaded from the input configuration pins of the same name at power-on. These bits may be changed if the MODE# input is set to allow I^2C configuration. Please refer to the tables (1) Equalizer Configuration, (2) Output Swing Configuration and (3) Output Emphasis Configuration earlier in this document for setting information. All four A channels get the same configuration settings.

BYTE 9 - B-Channels Equalizer and Output Control (BEOC)

SELx_B: Equalizer configuration, Dx_B: Emphasis control, Sx_B: Output level control (see Configuration Table)

Bit	7	6	5	4	3	2	1	0
Name	**SEL0_B**	**SEL1_B**	**SEL2_B**	**D0_B**	**D1_B**	**D2_B**	**S0_B**	**S1_B**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	**1**	**1**	1	1	1	1	1	1

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The B-Channels Equalizer and Output Control register is used to control the configuration of the input equalizer and output emphasis and levels of the four B channels. These register bits are loaded from the input configuration pins of the same name at power-on. These bits may be changed if the MODE# input is set to allow I^2C configuration. Please refer to the tables (1) Equalizer Configuration, (2) Output Swing Configuration and (3) Output Emphasis Configuration earlier in this document for setting information. All four B channels get the same configuration settings.

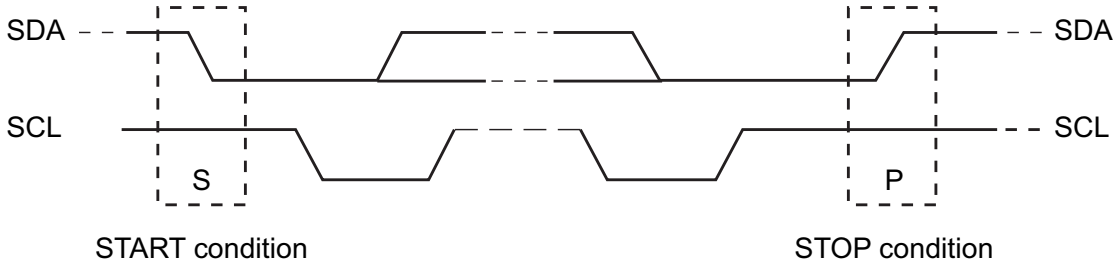
BYTE 10 - Reserved

BYTE 11 - Reserved

Reserved Bytes 10 and 11 are also visible via the I^2C interface. These bytes are R/W, byte 10 is initialized to 00000000 and byte 11 is initialized to 11101111 at power up. These bytes are used for IC manufacturing test purposes and should not be changed for normal operation.

Start & Stop Conditions

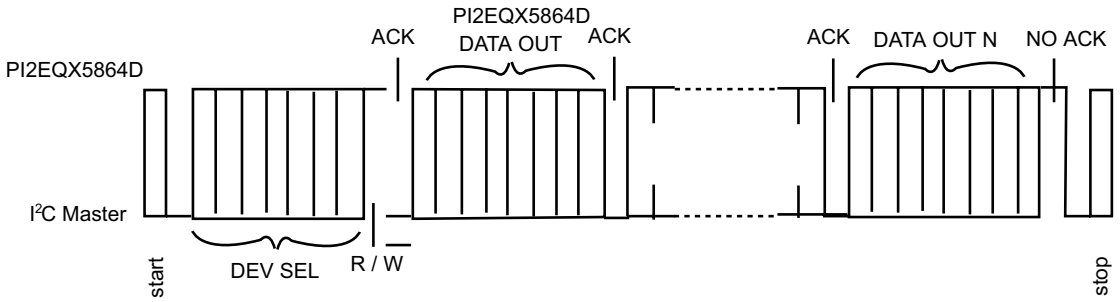
A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below.



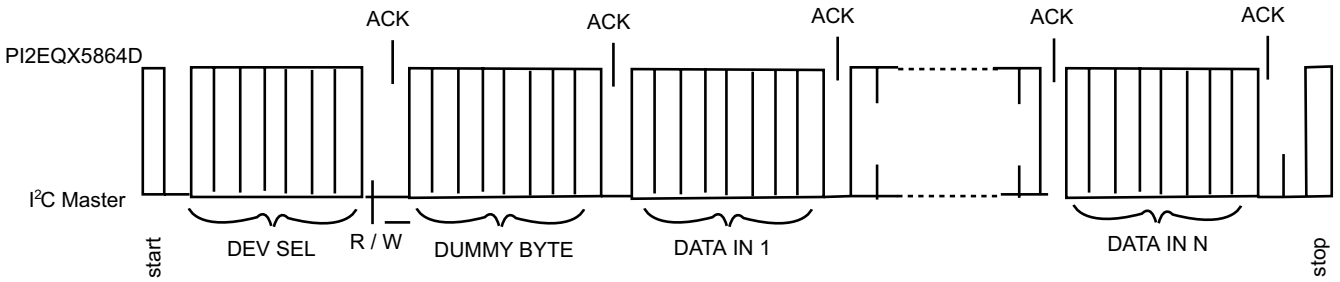
I^2C START and STOP conditions.

I²C Data Transfer

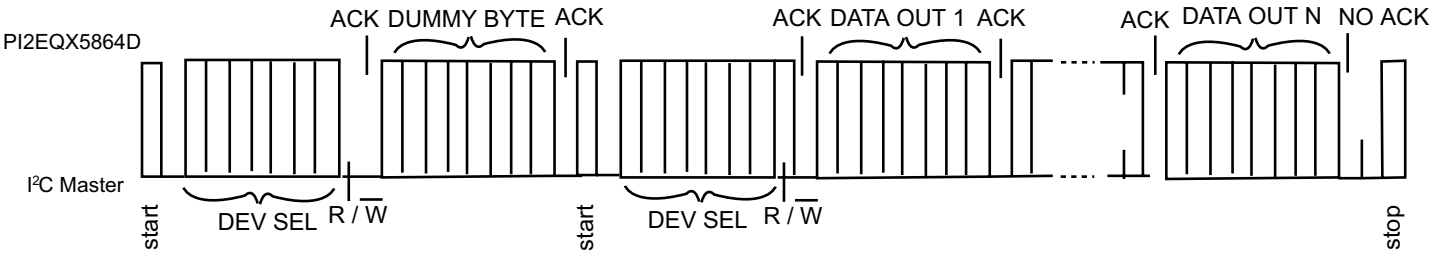
1. Read sequence



2. Write sequence



3. Combined sequence



Notes:
1. only block read and block write from the lowest byte are supported for this application.
2. for some I²C application, an offset address byte will be presented at the second byte in write command, which is called dummy byte here and will be simply ignored in this application for correct interoperation.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature . . . . . –65°C to +150°C
Supply Voltage to Ground Potential . . . . . –0.5V to +2.5V
DC SIG Voltage . . . . . –0.5V to VDD +0.5V
I^2C DC SIG Voltage . . . . . –0.5V to +3.6V
Current Output . . . . . –25mA to +25mA
Power Dissipation Continuous 1W
Operating Temperature . . . . . 0 to +70°C
ESD, HBM: I^2C pins . . . . . –1kV to +1kV
ESD, HBM: All other pins . . . . . –2kV to +2kV

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics

Power Supply Characteristics (V_{DD} = 1.2 ±0.05V, T_A = 0 TO 70°C)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
$I_{DDactive}$	Power supply current - active	All channels switching			800	mA
$I_{DDstandby}$	Power supply current - standby	PD_xy# all 0		5	10	
$I_{DD\text{-}channel}$	Power supply current - per channel, Active			50		

AC Performance Characteristics (V_{DD} = 1.2 ±0.05V, T_A = 0 TO 70°C)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
T_{pd}	Channel latency from input to output			750		ps

CML Receiver Input (V_{DD} = 1.2 ±0.05V, T_A = 0 TO 70°C)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
ZRX-DIFF-DC	DC Differential Input Impedance		80	100	120	Ohms
ZRX-DC	DC Input Impedance		40	50	60	
VRX-DIFFP-P	Differential Input Peak-to-peak Voltage		0.120		1.200	V
VRX-CM-ACP	AC Peak Common Mode Input Voltage				150	mV
Vth-	Signal detect threshold voltage			100	150	

Equalizer

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
J_{RS-T}	Residual jitter	Total			0.3	Ulp-p
J_{RS-D}	Residual jitter	Deterministic			0.2	Ulp-p
J_{RM}	Random jitter	Note 2		1.5		psrms

Notes

1. K28.7 pattern is applied differentially at point A as shown in AC test circuit (see figure).

2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. Jitter is measured at 0V at point C of the AC test circuit (see figure).

CML Transmitter Output (V_{DD} = 1.2V ± 0.05V, T_A = 0 to 70°C)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
Z_{OUT}	Output resistance	Single ended	40	50	60	Ohms
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	
V_{DIFFP}	Output Voltage Swing, Differential	|VTX-D+ - VTX-D-|	200		1000	mVp-p
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Ouput Voltage	VTX-DIFFP-P = 2 * | VTX-D+ - VTX-D- |	0.4		2.0	V
V_{TX-C}	Common-Mode Voltage	| VTX-D+ + VTX-D- | / 2		V_{DD}- 0.3		
t_F, t_R	Transition Time	20% to 80% (3)			150	ps
C_{TX}(1)	AC Coupling Capacitor		75		200	nF

Notes:

1. Recommended external coupling capacitor.

Digital I/O DC Specifications (V_{DD} = 1.2V ± 0.05V, T_A = 0 to 70°C)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC input logic high		V_{DD}/2 +0.2		V_{DD}+0.3	V
V_{IL}	DC input logic low		-0.3		V_{DD}/2 -0.2	
V_{OH}	DC output logic high	I_{OH} = 4mA	V_{DD}-0.4			
V_{OL}	DC output logic low	I_{OL} = 4mA			0.4	
V_{hys}	Hysteresis of Schmitt trigger input		0.2			
I_{IH}(1)	Input high current				100	µA
I_{IL1}(2)	Input low current		-20			
I_{IL2}(3)	Input low current		-20			

Notes:

1. Includes input signals A1, A2, A4, LB#, MODE#, RESET#, RXD_[A:B], SCL, SDA

2. For control inputs without pullups: A1, A2, A4, SCL, SDA

3. Control inputs with pull-ups include: LB#, MODE#, RESET#, RXD_[A:B]

SDA and SCL I/O for I²C-bus (V_{DD} = 1.2 ± 0.05v, T_A = 0 to 70°C)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC input logic high		1.1		3.6	V
V_{IL}	DC input logic low		-0.3		0.7	
V_{OL}	DC output logic low	I_{OL} = 3mA			0.4	
V_{hys}	Hysteresis of Schmitt trigger input		0.2			

Characteristics of the SDA and SCL bus lines for F/S-mode I²C-bus devices(1)

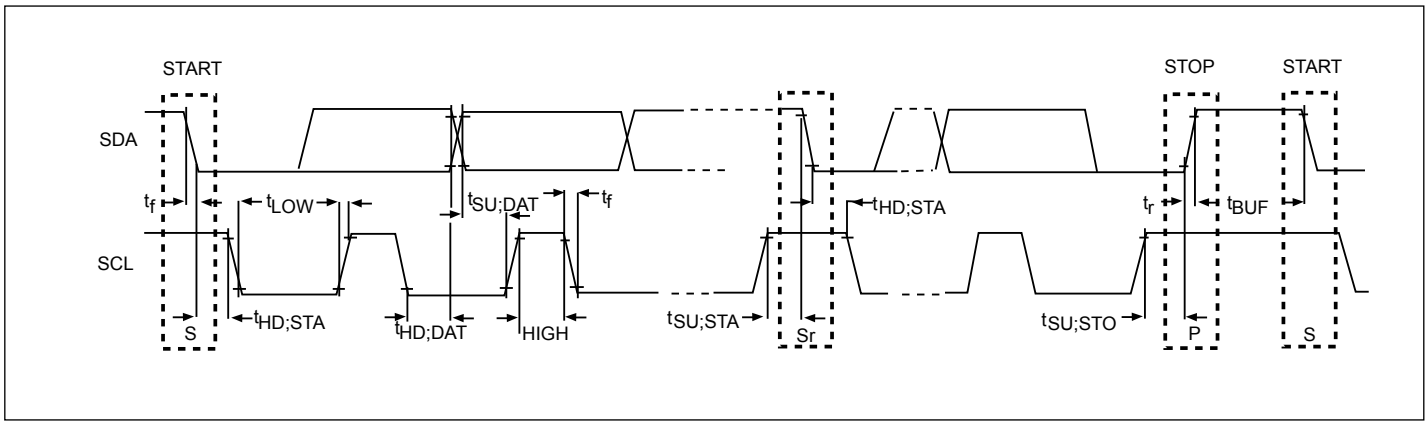
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency		0		100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated		4.0		–	µs
t_{LOW}	LOW period of the SCL clock		4.7		–	
t_{HIGH}	HIGH period of the SCL clock		4.0		–	
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7		–	
$t_{HD;DAT}$	Data hold time		5.0		–	
$t_{SU;DAT}$	Data set-up time		250		–	ns
t_r	Rise time of both SDA and SCL signals		–		1000	
t_f	Fall time of both SDA and SCL signals				300	
$t_{SU;STO}$	Set-up time for STOP condition		4.0		–	µs
t_{BUF}	Buss free time between a STOP and STOP condition		4.7		–	
C_b	Capacitive load for each bus line		–		400	pF

Notes:

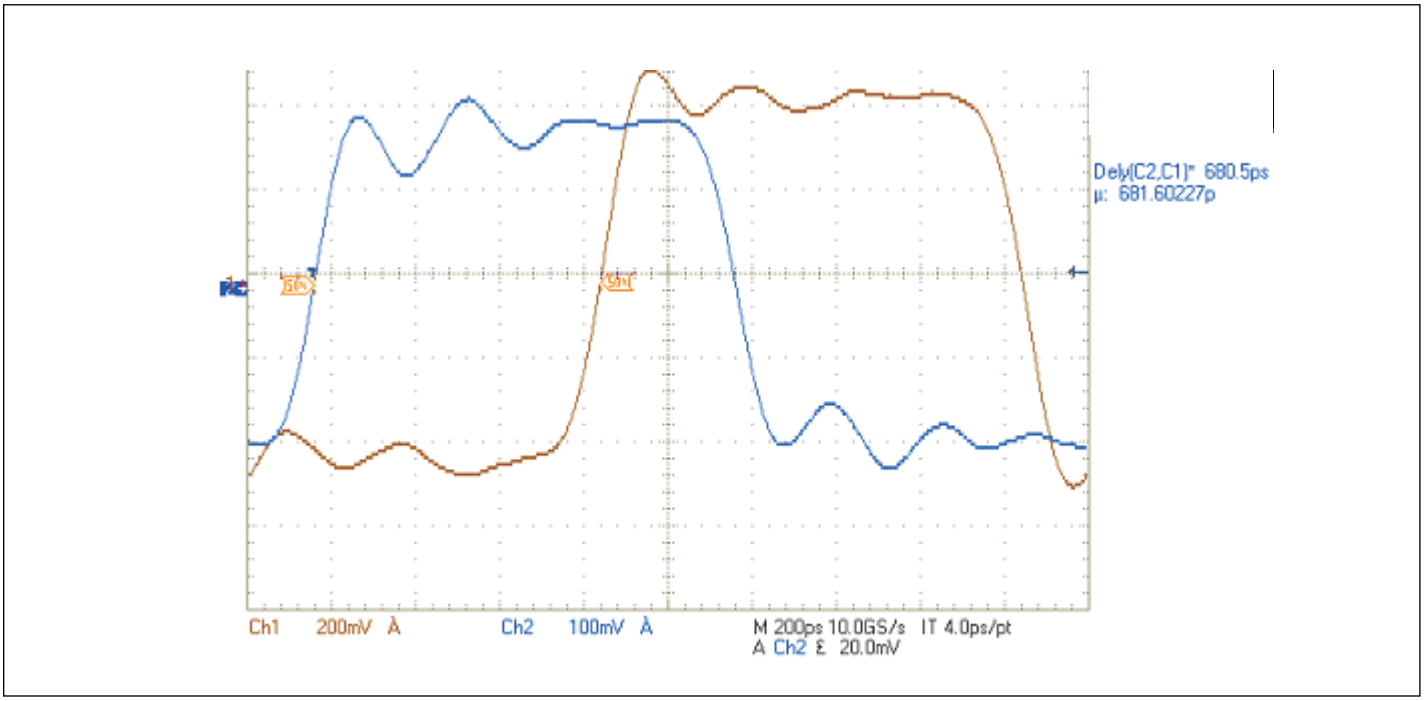
1. All values referred to VIHmin and VILmax levels.

2. A device must initially provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.

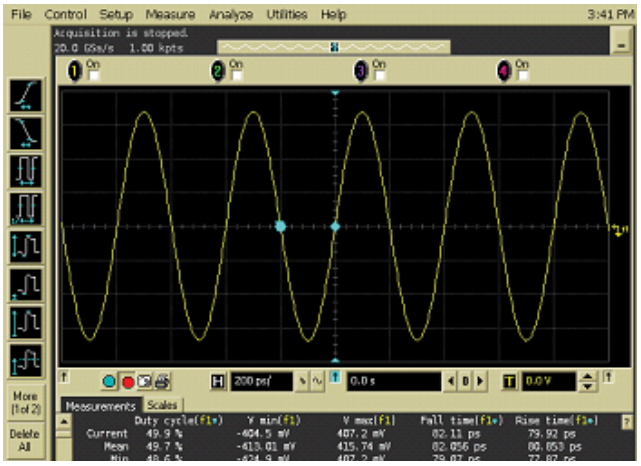
I²C Timing

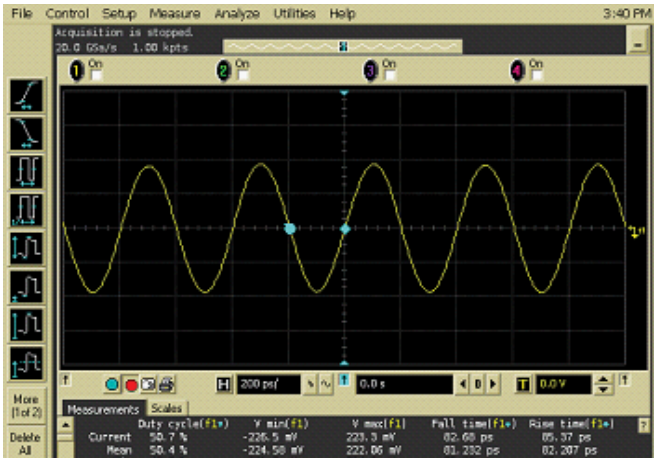


Channel Latency, 5.0 Gbps

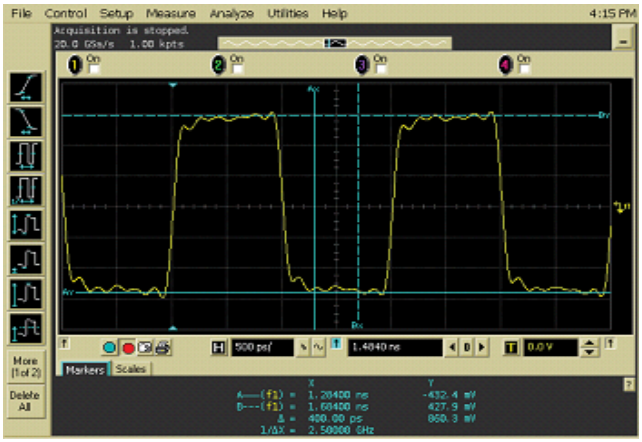


Output Level Settings (1V left, and 0.5V right at 5.0 Gbps)

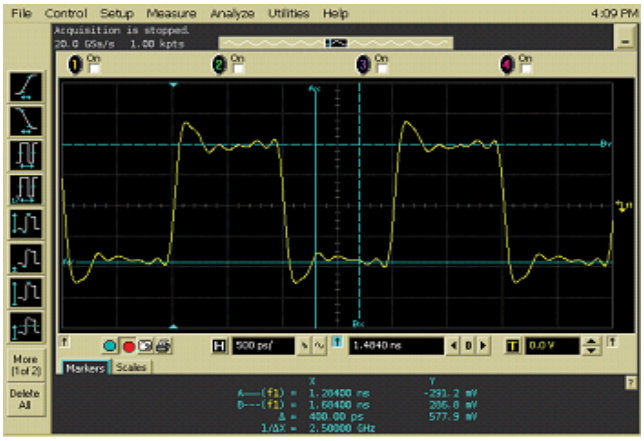




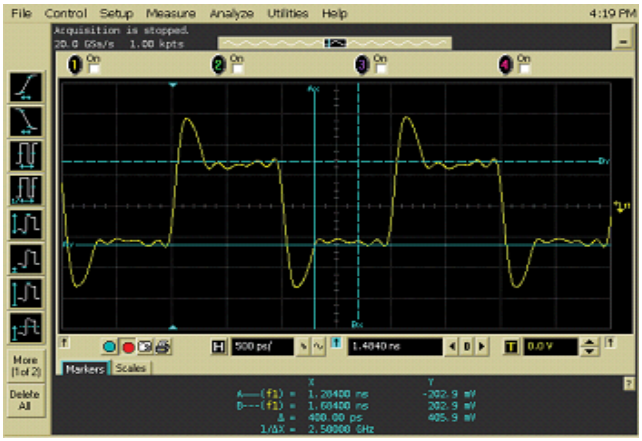
Output De-Emphasis Characteristics



0.0 dB (Dx = 000)



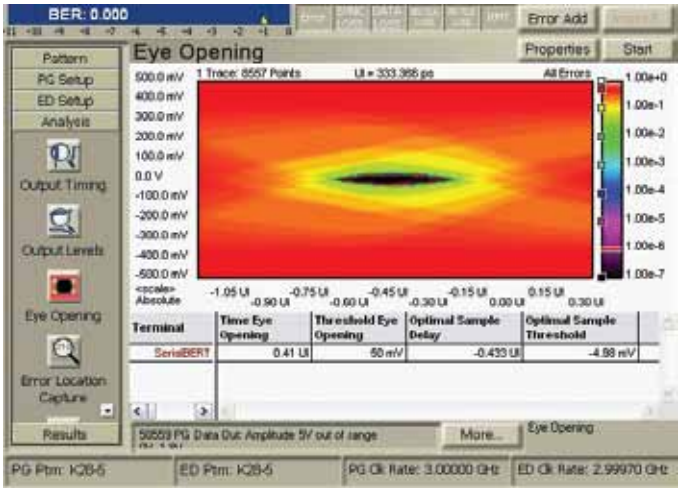
–3.5 dB (Dx = 010)

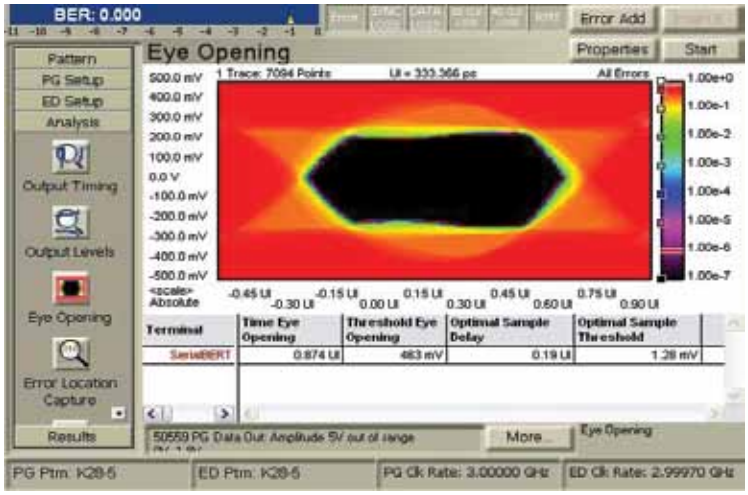


–6.5 dB (Dx = 101)

–8.5 dB (Dx = 111)

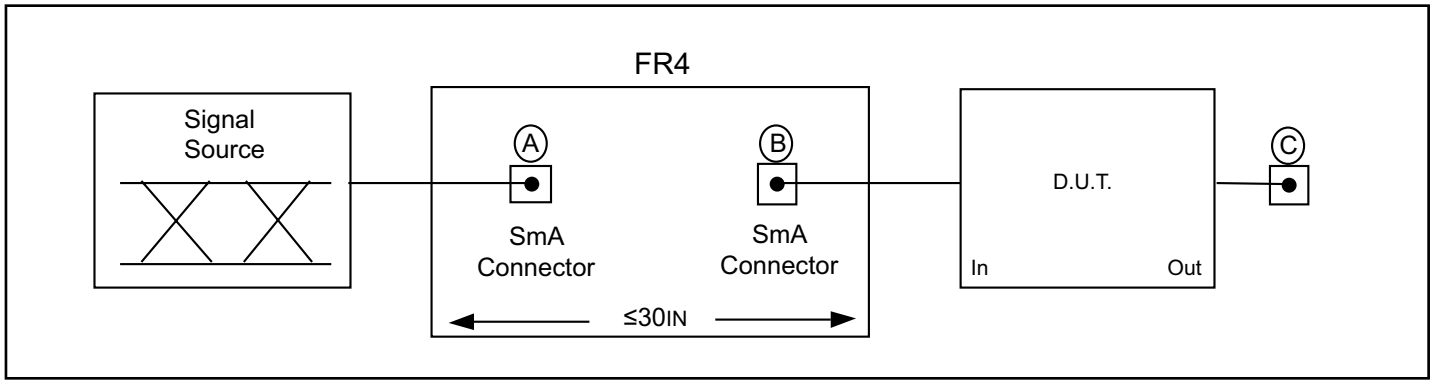
Eye Diagrams 5.0Gbps (input left, output right)

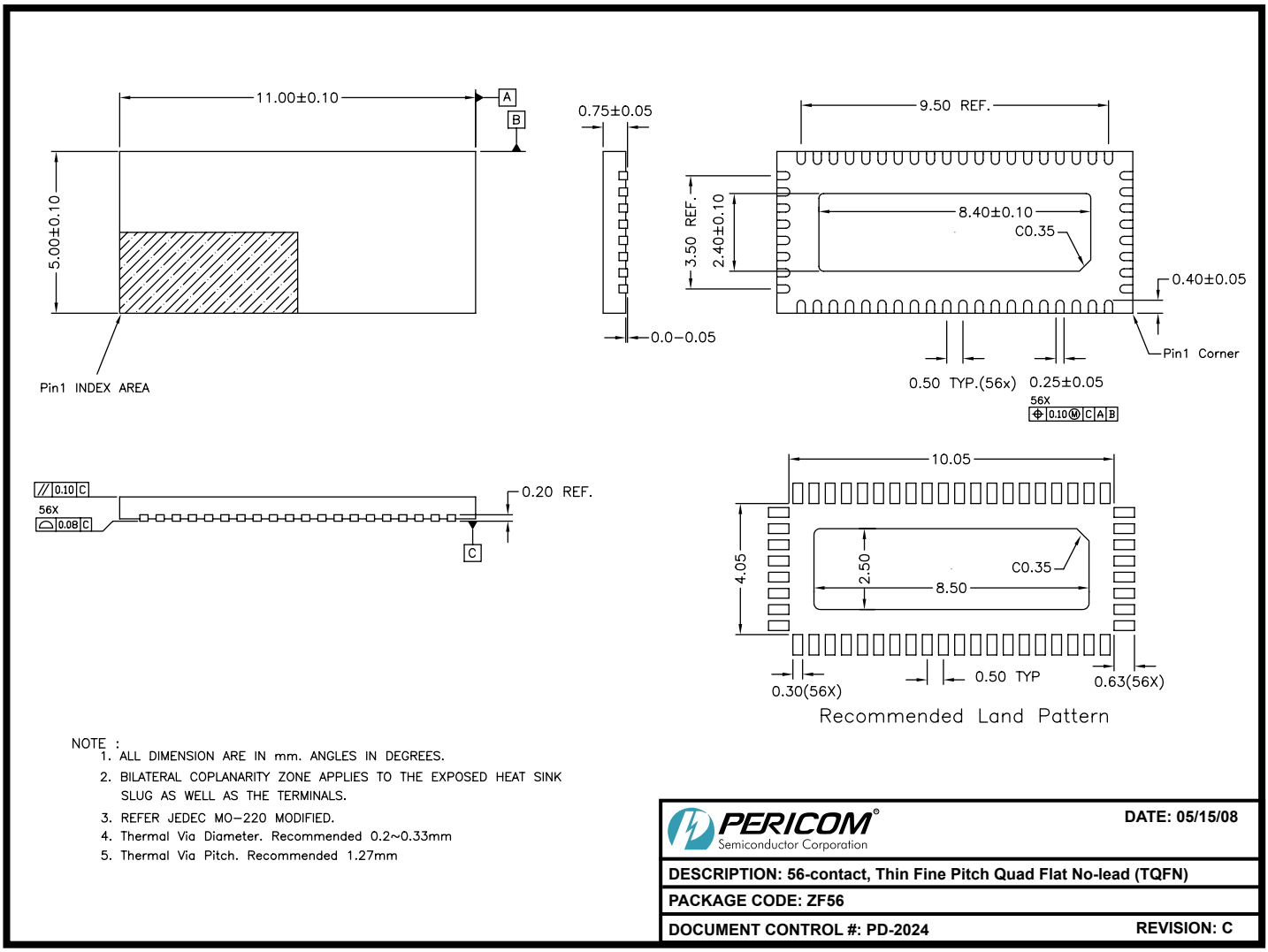




Data Waveforms, 2.5Gbps (left) & 5.0Gbps (right)

AC Test Circuit Referenced in the Electrical Characteristic Table





08-0208

Note:

For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX5864DZFE	ZF	Pb-free & Green 56-Contact TQFN

Notes:

- **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**
- **E = Pb-free and Green**
- **X suffix = Tape/Reel**