2.5 Gbps x2 Lane PCI Express Repeater/Equalizer with Signal Detect and Flow-Through Pinout

Features

- Two High Speed PCI Express lanes
- Supports PCI Express data rates (2.5 Gbps) on each lane
- Adjustable Receiver Equalization
- Input Signal Level Detect & Output Squelch on all Channels
- Output De-emphasis = -3.5dB
- 100–Ohm Differential CML I/O's
- Low Power (100mW per Channel)
- Standby Mode – Power Down State
- V_{DD} Operating Range: 1.8V +/-0.1V
- Packaging (Pb-free & Green): 48-contact TQFN

Description

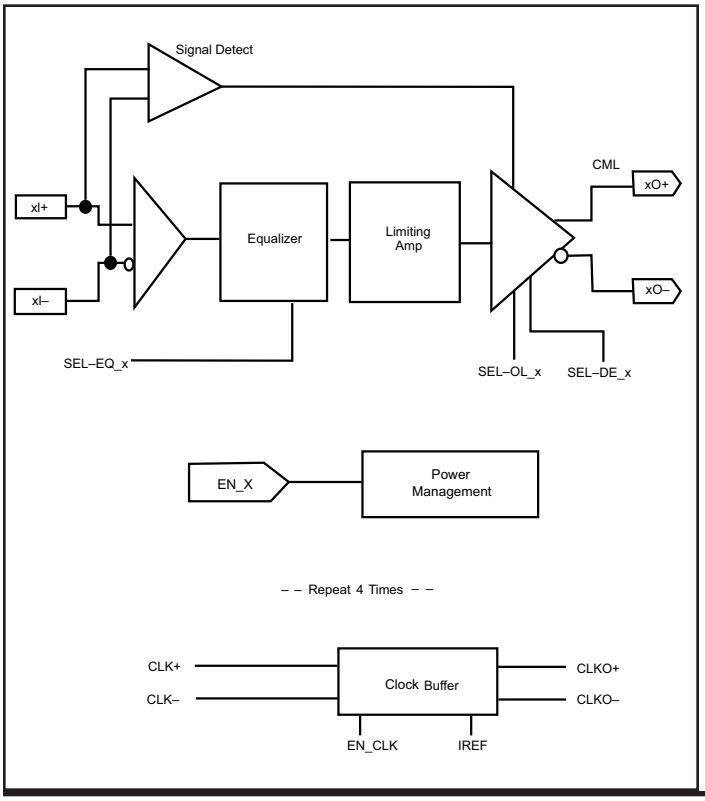
Pericom Semiconductor's PI2EQX4432D is a low power, PCI Express compliant signal Re-Driver. The device provides programmable equalization, to optimize performance by reducing Inter-Symbol Interference (ISI). PI2EQX4432D supports two 100–Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or extends the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the PCI Express signal before the Re-Driver. Whereas the integrated de-emphasis circuitry provides flexibility with signal integrity of the PCI Express signal after the Re-Driver.

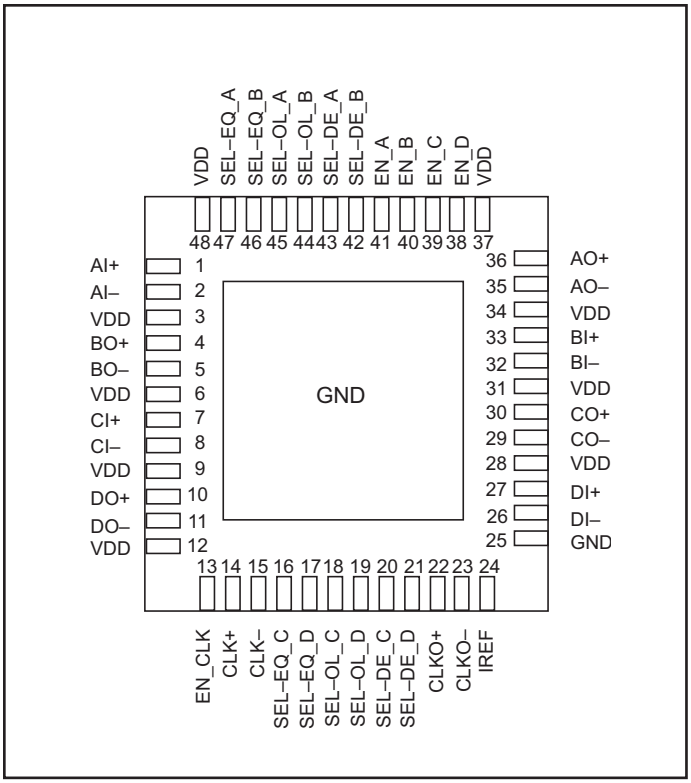
A low-level input signal detection and output squelch function is provided for all four channels. Each channel operates fully independantly. When a channel is enabled (EN_x=1) and operating, that channels input signal level (on xI+/-) determines whether the output is enabled. If the input level of the channel falls below the active threshold level (Vth-) then the output driver switches off, and the pin is pulled to VDD via a high impedance resistor.

In addition to providing serial re-conditioning, Pericom's PIEQX4432D also provides a power management Stand-by mode operated by the enable pins.

Block Diagram



Pin Description (Top View)



Pin Description

Pin #	Pin Name	I/O	Description
1	AI+	I	Positive CML Input Channel A with internal 50 Ohm pull down during normal operation (EN_A = 1). When EN_A = 0, this pin is a high-impedance.
2	AI-	I	Negative CML Input Channel A with internal 50 Ohm pull down during normal operation (EN_A = 1). When EN_A =0, this pin is a high-impedance.
36	AO+	O	Positive CML Output Channel A internal 50 Ohm pull up during normal operation and 2KΩ pull up otherwise.
35	AO-	O	Negative CML Output Channel A with internal 50 Ohm pull up during normal operation and 2K-ohm pull up otherwise.
33	BI+		Posite CML Input Channel B with internal 50 Ohm pull down during normal operation (EN_B = 1). When EN_B = 0, this pin is a high-impedance.
32	BI-	I	Negative CML Input Channel B with internal 50 Ohm pull down during normal operation (EN_B = 1). When EN_B = 0, this pin is a high-impedance.
4	BO+	O	Positive CML Output Channel B with internal 50 Ohm pull up during normal operation and 2k–Ohm pull up otherwise.
5	BO-	O	Negative CMLOutput Channel B with internal 50 Ohm pull up during normal operation and 2k–Ohm pull up otherwise.
7	CI+	I	Positive CML Input Channel C with internal 50 Ohm pull down during normal operation (EN_C = 1). When EN_C = 0, this pin is a high-impedance.
8	CI-	I	Negative CML Input Channel C with internal 50 Ohm pull down during normal operation (EN_C = 1). When EN_C = 0, this pin is a high-impedance.
30	CO+	O	Positive CMLOutput Channel C with internal 50 Ohm pull up during normal operation and 2K-ohm pull up otherwise.
29	CO-	O	Negative CMLOutput Channel C with internal 50 Ohm pull up during normal operation and 2k–Ohm pull up otherwise.
27	DI+	I	Positive CML Input Channel D with internal 50 Ohm pull down during normal operation (EN_D = 1). When EN_D = 0, this pin is a high-impedance.
26	DI-	I	Negative CML Input Channel D with internal 50 Ohm pull down during normal operation (EN_D = 1). When EN_D = 0, this pin is a high-impedance.
10	DO+	O	Positive CML Output Channel D with internal 50 Ohm pull up during normal operation and 2k–Ohm pull up otherwise.
11	DO-	O	Negative CML Output Channel D with internal 50Ω pull up during normal operation and 2k–Ohm pull up otherwise.
41, 40, 39, 38	EN_[A, B, C, D]	I	EN_[A:D] is a channel enable pin with internal 50k–Ohm pull-up resistor. ALVCMOS high provides normal operation. ALVCMOS low selects a low power down mode.
43, 42, 20, 21	SEL–DE_ [A:D]	I	Output De–Emphasis configuration input for channels A, B, C and D, with internal 50k–Ohm pull up.Refer to table for modes.
47, 46, 16, 17	SEL–EQ_ [A:D]	I	Equalizer configuration input for channels A, B, C and D, with internal 50k–Ohm pull-up. Refer to table for modes.
45, 44, 18, 19	SEL–OL_ [A:D]	I	Output Level configuration input for channels A, B, C, and D, with internal 50k–Ohm pull–up. Refer to table for modes.
14, 15	CLK+, CLK–	I	Differential input reference clock, typically 100MHz
22, 23	CLKO, CLKO–	O	Differential reference clock output
13	EN_CLK	I	Enable Clock input with 50K–Ohm pull-up. When EN_CLK is LVCMOS high level, the clock output operates normally. When EN_CLK = low, the clock outputs are turned off for power savings. A clock is not required bt the data channels for operation.

24	IREF	I	Connect to 475-Ohm resistor to ground when the reference clock is used. Otherwise do not connect.
3, 6, 9, 12, 28, 31, 34, 37, 48	VDD	PWR	1.8V Supply Voltage
25, Center Pad	GND	PWR	Supply Ground, Center pad must be connected

Output Swing Control

SEL–OL_[A:D]	Output Swing
0	1x
1	1.2x

Output De-emphasis Adjustment

SEL–DE_[A:D]	De-emphasis
0	0dB
1	–3.5dB

Equalizer Selection

SEL–EQ_[A:D]	Compliance Channel
0	[0:2.5dB] @ 1.25 GHz
1	[0:6.5dB] @ 1.25 GHz

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Supply Voltage to Ground Potential ..... –0.5V to +2.5V
DC SIG Voltage ..... –0.5V to V_{DD} +0.5V
Current Output ..... -25mA to +25mA
Power Dissipation Continous 800mW
Operating Temperature ..... 0 to +70°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics (V_{DD} = 1.8 ±0.1V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Ps	Supply Power	All Enables = LVCMOS High			0.1	W
		All Enables = LVCMOS Low			0.6	
	Latency	From input to output		2.0		ns
CML Receiver Input						
RL_{RX}	Return Loss	50 MHz to 1.25 GHz		12		dB
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		0.175		1.200	V
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	mV
V_{TH}-	Signal Detect Threshold	EN_x = High		120	175	mV
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	Ω
Z_{RX-DC}	DC Input Impedance		40	50	60	
Equalization						
J_{RS}	Residual Jitter(1,2)	Total Jitter			0.3	Ulp-p
		Deterministic jitter			0.2	
J_{RM}	Random Jitter(1,2)			1.5		psrms

Notes

1. K28.7 pattern is applied differentially at point A as shown in Figure 1.
2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. Jitter is measured at 0V at point C of Figure 1.

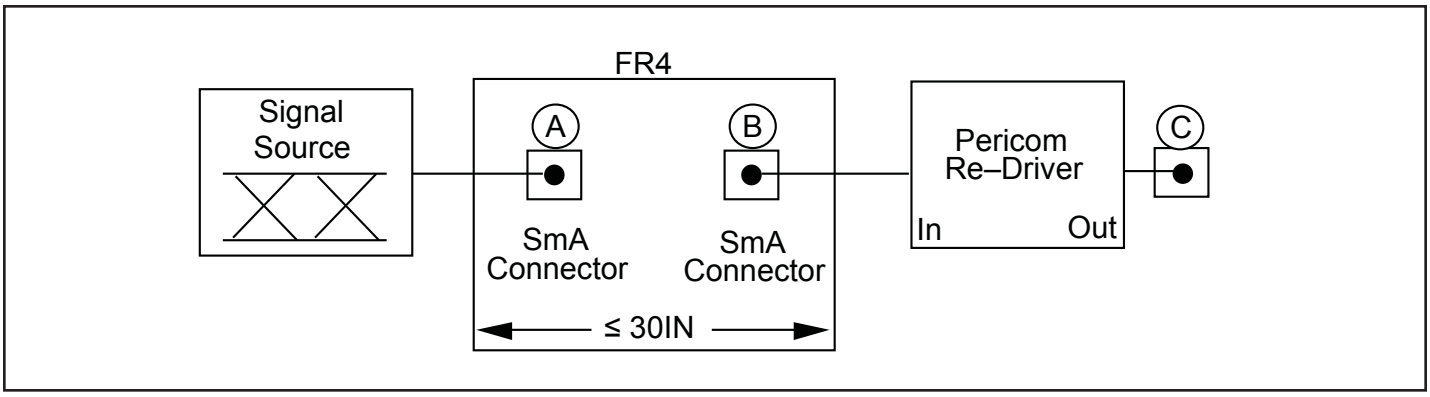


Figure 1. Test Condition Referenced in the Electrical Characteristic Table

AC/DC Electrical Characteristics (TA = 0 to 70˚C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Transmitter Output (100Ω differential)						
V_{DIFFP}	Output Voltage Swing	Differential Swing $\lvert V_{TX-D+} - V_{TX-D-} \rvert$	400		900	mVp-p
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert / 2$		V_{DD}-0.3		
t_F, t_R	Transition Time	20% to 80% (1)			150	ps
Z_{OUT}	Output resistance	Single ended	40	50	60	Ω
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	Ω
C_{TX}	AC Coupling Capacitor		75		200	nF
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Ouput Voltage	$V_{TX-DIFFP-P} = 2 * \lvert V_{TX-D+} - V_{TX-D-} \rvert$	0.8		1.8	V
LVCMOS Control Pins						
V_{IH}	Input High Voltage		0.65 × V_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage				0.35 × V_{DD}	
I_{IH}	Input High Current				250	µA
I_{IL}	Input Low Current				500	

AC Switching Characteristics for Clock Buffer (V_{DD} = 1.8 ±0.1V, AV_{DD} = 1.8 ±0.1V) (3)

Symbol	Parameters	Min	Max.	Units	Notes
T_{rise} / T_{fall}	Rise and Fall Time (measured between 0.175V to 0.525V) (1)	125	525	ps	1
ΔT_{rise} / ΔT_{fall}	Rise and Fall Time Variation		75		1
V_{HIGH}	Voltage High including overshoot	660	900	mV	1
V_{LOW}	Voltage Low including undershoot	-200			1
V_{CROSS}	Absolute crossing point voltages	200	550		1
ΔV_{CROSS}	Total Variation of Vcross over all edges		250		1
T_{DC}	Duty Cycle (input duty cycle = 50%) (2)	45	55	%	2

Notes:
1. Measurement taken from Single Ended waveform.
2. Measurement taken from Differential waveform.
3. Test configuration is R_S = 33.2Ω, Rp = 49.9Ω, and 2pF.

Configuration Test Load Board Termination

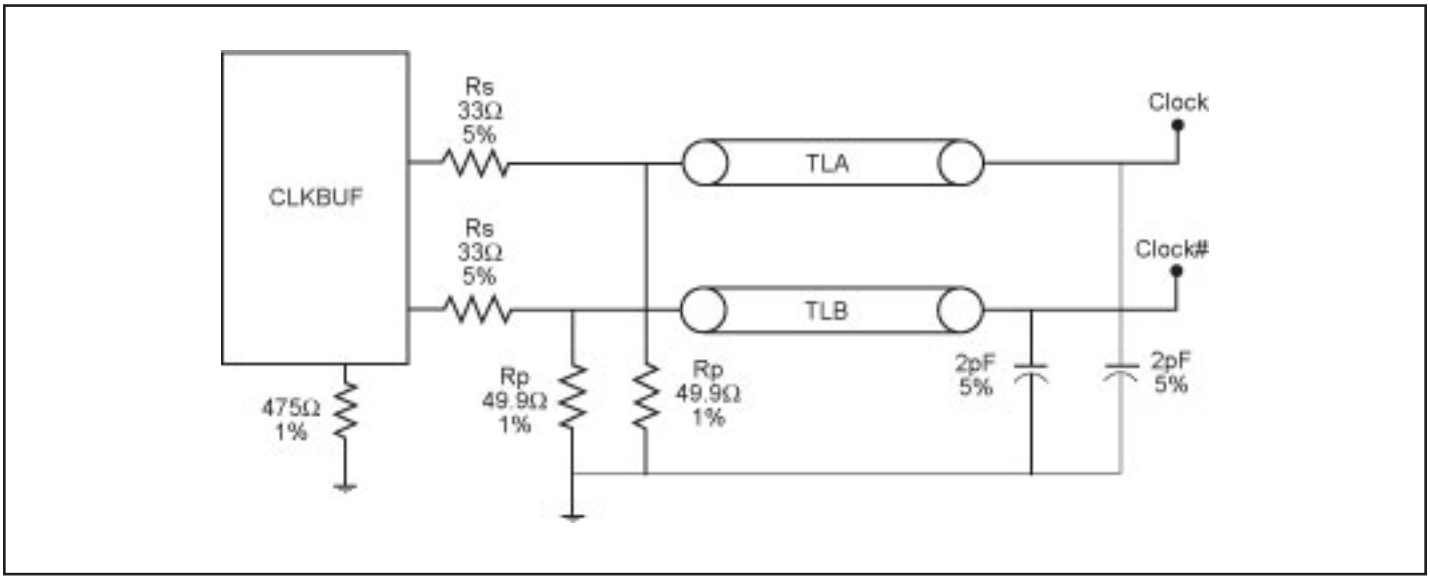
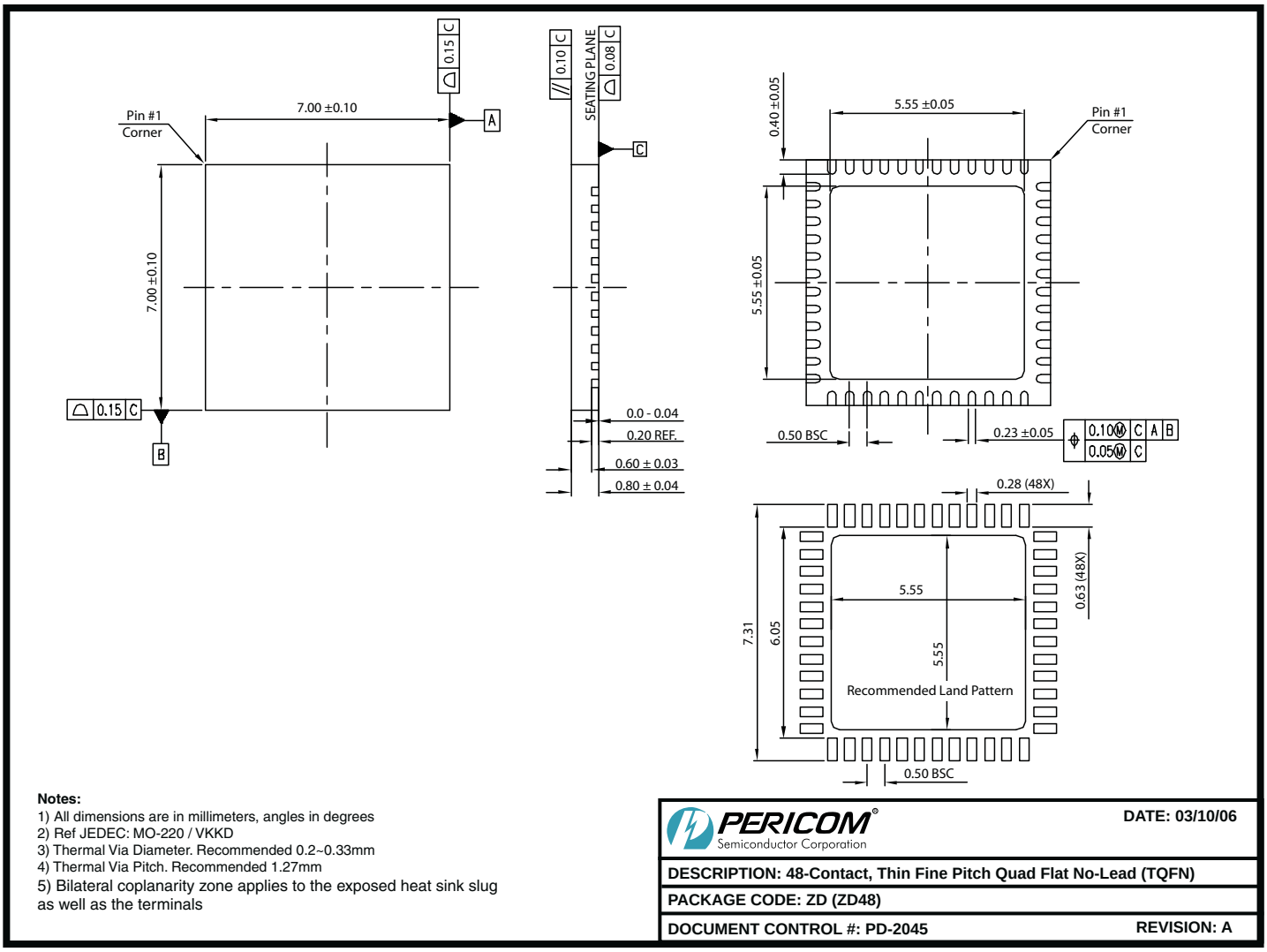


Figure 2. Configuration test load board termination

Note:
• TLA and TLB are 3” transmission lines.

Packaging Mechanical: 48-contact TQFN (ZD48)



Notes:
1) All dimensions are in millimeters, angles in degrees
2) Ref JEDEC: MO-220 / VKKD
3) Thermal Via Diameter. Recommended 0.2~0.33mm
4) Thermal Via Pitch. Recommended 1.27mm
5) Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals

PERICOM Semiconductor Corporation — DATE: 03/10/06

DESCRIPTION: 48-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD (ZD48)

DOCUMENT CONTROL #: PD-2045 — REVISION: A

Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX4432DZDE	ZD	Pb-free & Green 48-contact TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free & Green
- X suffix = Tape/Reel