PI2EQX3231BL

3.0Gbps, 1-port, SATA2 *i/m* Re-Driver

Features

- SATA2 *i, m*; external SATA2
- Two 3.0Gbps differential signal pairs
- Adjustable Receiver Equalization
- 100-Ohm Differential CML I/O's
- Independent Output Emphasis Control
- Input signal level detect and squelch for each channel
- OOB Support
- Low Power (100mW per Channel)
- Stand-by Mode – Power Down State
- V_{DD} Operating Range: 1.5V to 1.8V
- Packaging: — 20-TQFN (3.5x 4.5mm)

Description

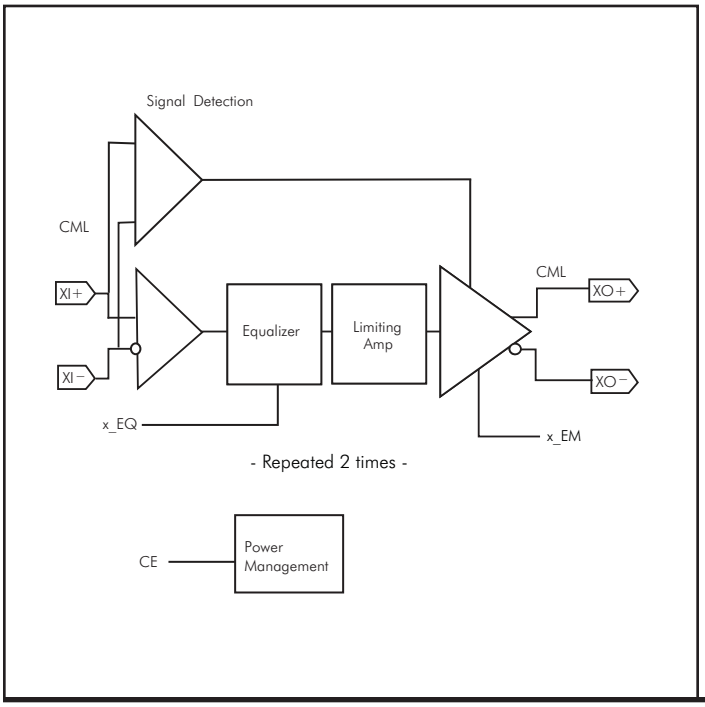
Pericom Semiconductor's PI2EQX3231BL is a low power, signal Re-Driver. The device provides programmable equalization, to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI2EQX3231BL supports two 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the re-driver.

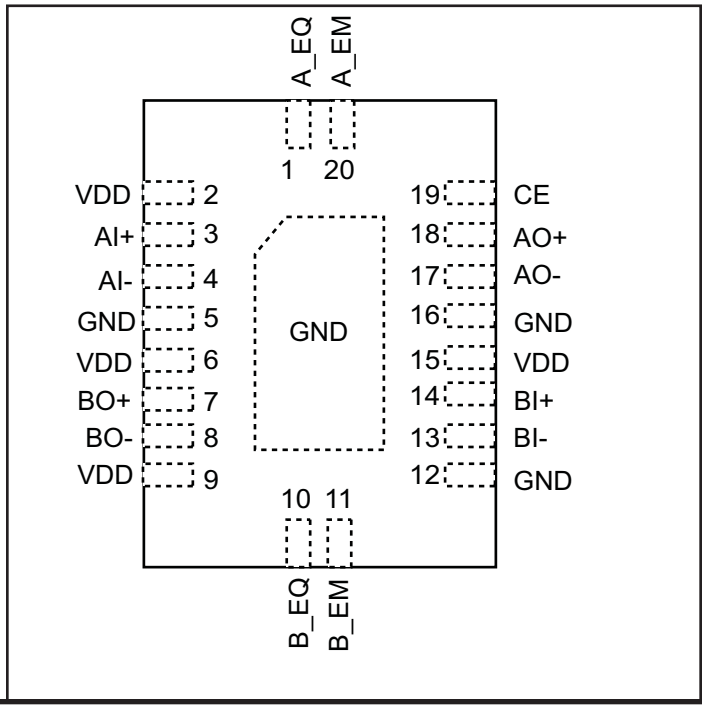
A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independantly. When the channels are enabled (CE=1) and operating, that channels input signal level (on xI+/-) determines whether the output is active. If the input signal level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage.

In addition to signal conditioning, when CE = 0, the device enters a low power standby mode.

Block Diagram



Pin Diagram (Top Side View)



Pin Description

Pin #	Pin Name	Type	Description
20	A_EM	Input	Selection pin for channel A output Emphasis adjustment. (See output Emphasis Adjustment table). With internal 50K-Ohm pull-up resistor.
1	A_EQ	Input	Selection pin for equalizer of Ain. (See Input Equalizer Adjustment table.) With internal 50K-Ohm pull-up resistor.
3 4	AI+ AI-	Input	CML input forward channel A with internal 50-Ohm pull down.
18 17	AO+ AO-	Output	CML output channel A with internal 50-Ohm pull up.
10	B_EQ	Input	Selection pin for equalizer of B_IN. (See Input Equalizer Adjustment table.) With internal 50K-Ohm pull-up resistor.
11	B_EM	Input	Selection pin for channel B output Emphasis adjustment. (See output Emphasis Adjustment table). With internal 50K-Ohm pull-up resistor.
14 13	BI+ BI-	Input	CML input return channel B with internal 50-Ohm pull down.
7 8	BO+ BO-	Output	Positive CML output channel B with internal 50-Ohm pull up.
19	CE	Input	Chip Enable "high" provides normal operation. "Low" for power down mode. With internal 50K-Ohm pull-up resistor.
5, 12, 16, Center Pad	GND	GND	Supply ground.
2,6, 9,15	VDD	Power	1.5V to 1.8V supply voltage (±0.1V)

Input Equalizer Adjustment

x_EQ	Compliance Channel @ 1.5 GHz
0	1.5dB ± 1.0dB
1	5.5dB ± 1.0dB

Output Emphasis Adjustment

x_EM	Compliance Channel @ 1.5GHz
0	0dB
1	-3.5dB

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +2.5V
DC SIG Voltage	–0.5V to V_{DD} +0.5V
Current Output	-25mA to +25mA
Power Dissipation Continous	500mW
Operating Temperature	0 to +70°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics (V_{DD} = 1.4V to 1.9V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current				90	mA
$P_{standby}$	Power, standby	EN_[A:B] = 0			1	mW
$P_{active18}$	Power, active @ 1.8V	VDD=1.8V, EN_[A:B] = 1, Vrx-diff-p >= Vth-sd		125	160	
P_{idle18}	Power, idle @ 1.8V	VDD=1.8V, EN_[A:B] = 1, Vrx-diff-p < Vth-sd		100		mW
$P_{active15}$	Power, active @ 1.5V	VDD=1.5V, EN_[A:B] = 1, Vrx-diff-p >= Vth-sd		100	130	mW
P_{idle15}	Power, idle @ 1.5V	VDD=1.5V, EN_[A:B] = 1, Vrx-diff-p < Vth-sd		80		mW
tpd	Latency	From differential input to differential output		2.0		ns
CML Receiver Input						
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		0.200			V
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	mV
V_{TH-SD}	Signal detect Threshold	CE = 1	50(2)		200 (3)	mVppd
Z_{RX-DC}	DC Input Impedance		40	50	60	Ohm
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	
Equalization						
J_{RS}	Residual Jitter(1,2)	Total Jitter			0.3	Ulp-p
J_{RM}	Random Jitter(1,2)			1.5		psrms

Notes

1. K28.7 pattern is applied differentially at point A as shown in Figure 1.
2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. JItter is measured at 0V at point C of Figure 1.
3. Using Compliance test at 1.5Gbps and 3Gbps. Also using OOB (OOB is formed by ALIGNp primitive or D24.3) test patterns at 1.5Gbps. The ALIGN primitive (K28.5+D10.2+D27.3 = 0011111010+0101010101+0010011100). The D24.3 = 00110011001100110011

AC/DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Transmitter Output (100Ω differential)						
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Ouput Voltage	$V_{TX-DIFFP-P} = 2 * \lvert V_{TX-D+} - V_{TX-D-} \rvert$	400		600	mV
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert /2$		V_{DD} - 0.3		V
t_F, t_R	Transition Time	20% to 80%(1)			150	ps
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	Ohm
LVCMOS Control Pins						
V_{IH}	Input High Voltage		0.65 × V_{DD}			V
V_{IL}	Input Low Voltage				0.35 × V_{DD}	
I_{IH}	Input High Current				5	µA
I_{IL}	Input Low Current				100	

Note:
1. When S_ES=0 select SATAx standard, When S_ES=1 select SATAi/m standard

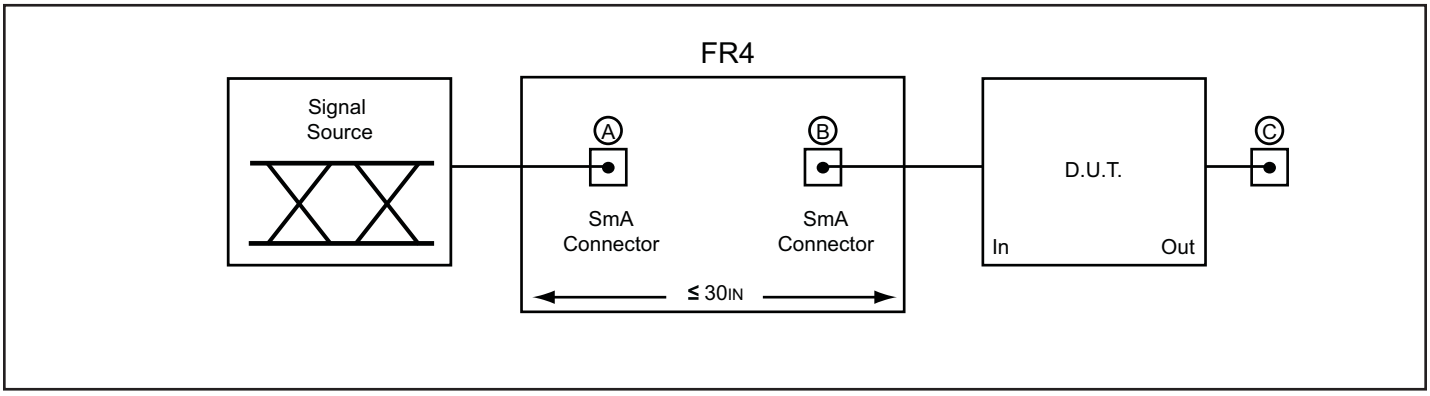
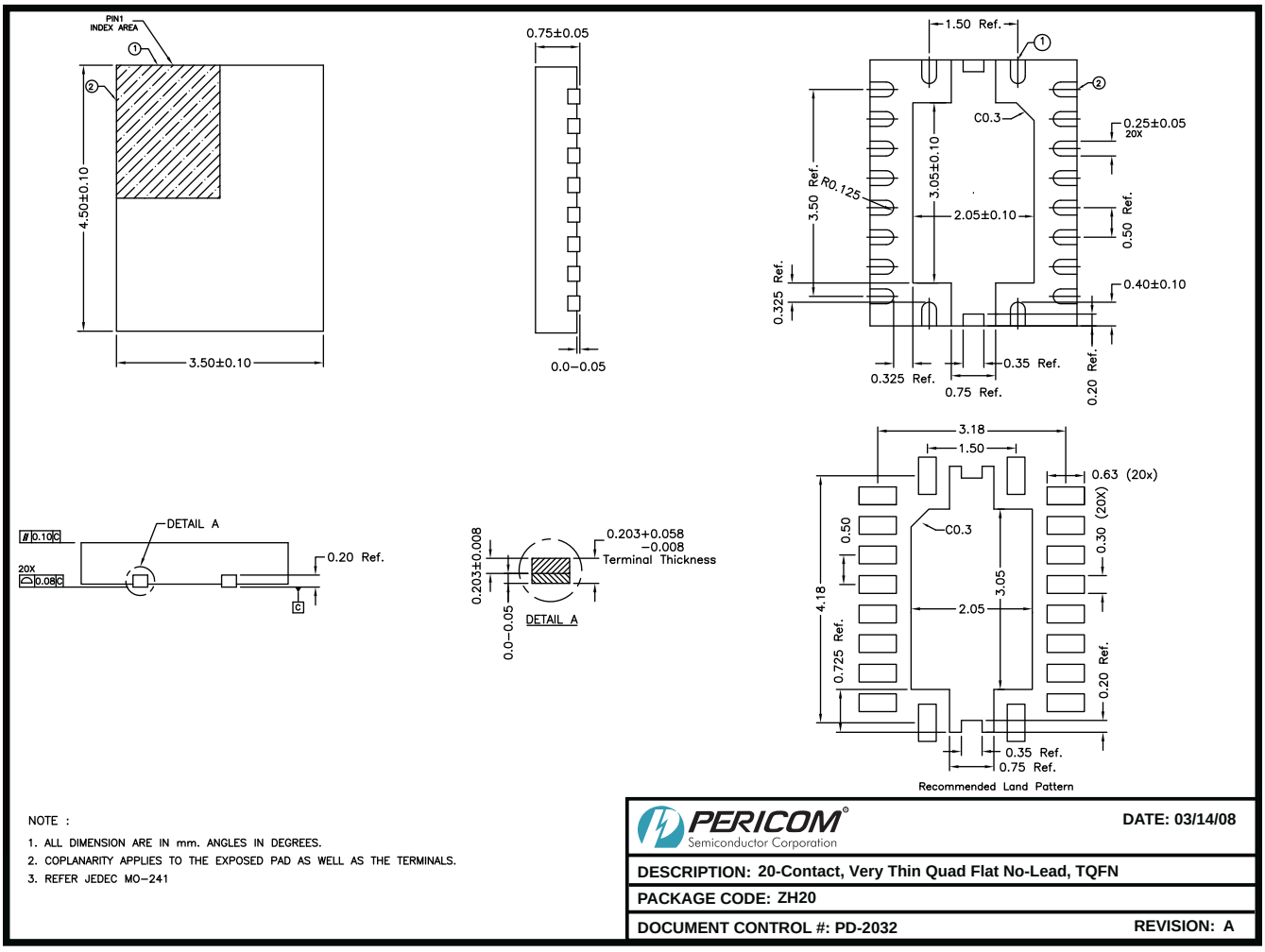


Figure 1. Test Condition Referenced in the Electrical Characteristic Table

Packaging Mechanical: 20-contact TQFN (ZH)



Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX3231BLZHE	ZH	Pb-Free and Green 20-contact TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel