PI2EQX3201B

3.2Gbps 2 Differential Channel Serial Re-driver with Equalization, De-emphasis and Squelch

Features

- Two Pairs of 3.2Gbps differential signal
- Adjustable Transmitter De-Emphasis & Amplitude
- Adjustable Receiver Equalization
- One Spread Spectrum Capable Clock Buffer Output
- 100Ω Differential CML I/O's
- Input signal level detect and squelch for each channel
- Low Power (100mW per Channel)
- Stand-by Mode – Power Down State
- V_{CC} Operating Range: 1.5V to 1.8V
- Built in Clock Buffer
- Packaging (Pb-free & Green):
  — 36-pad TQFN (ZF36)

Description

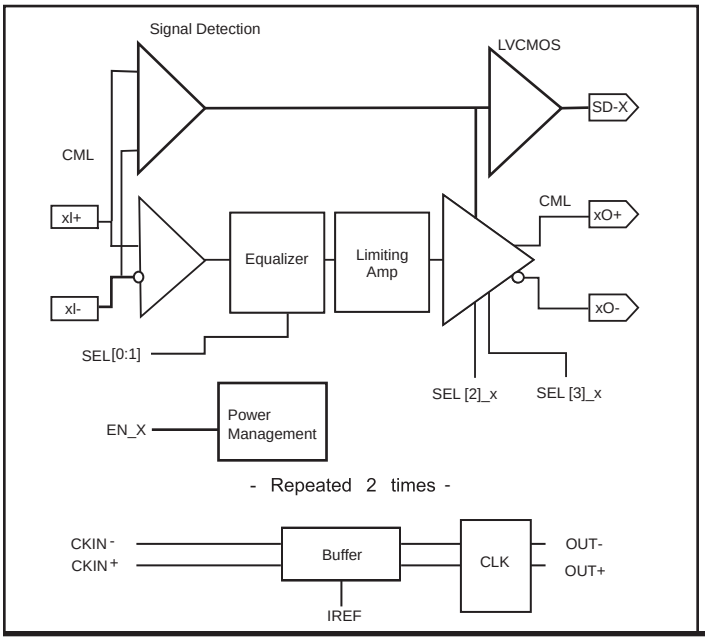
Pericom Semiconductor's PI2EQX3201B is a low power, signal re-driver. The device provides programmable equalization, amplification, and de-emphasis by using 4 select bits, SEL[0:3], to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI2EQX3201B supports two 100 Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the re-driver. Whereas the integrated de-emphasis circuitry provides flexibility with signal integrity of the signal after the re-driver.

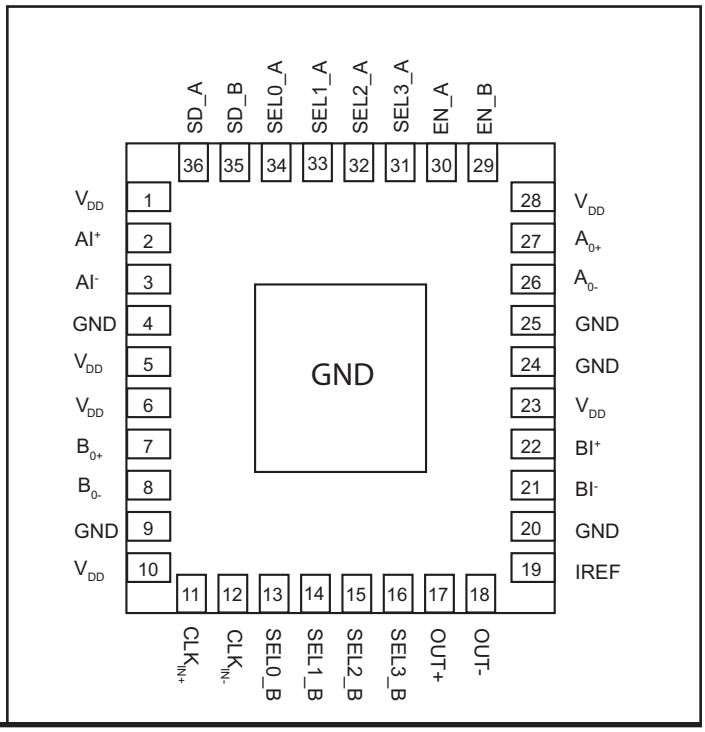
A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independantly. When a channel is enabled (EN_x=1) and operating, that channels input signal level (on xI+/-) determines whether the output is enabled. If the input level of the channel falls below the active threshold level then the output driver switches off, and the pin is pulled to VDD via a high impedance resistor. If the input level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage.

In addition to providing signal re-conditioning, Pericom's PI2EQX3201B also provides power management Stand-by mode operated by a Bus Enable pin.

Block Diagram



Pin Description



Pin Description

Pin #	Pin Name	I/O	Description
2	AI+	I	Positive CML Input Channel A with internal 50Ω pull down
3	AI-	I	Negative CML Input Channel A with internal 50Ω pull down
27	AO+	O	Positive CML Output Channel A internal 50Ω pull up during normal operation and 2KΩ when EN_A=0. Drives to output common mode voltage when input is $<V_{TH-}$.
26	AO-	O	Negative CML Output Channel A with internal 50Ω pull up during normal operation and 2KΩ when EN_A=0. Drives to output common mode voltage when input is $<V_{TH-}$.
22	BI+	I	Positive CML Input Channel B with internal 50Ω pull down
21	BI-	I	Negative CML Input Channel B with internal 50Ω pull down
7	BO+	O	Positive CML Output Channel B with internal 50Ω pull up during normal operation and 2KΩ when EN_B=0. Drives to output common mode voltage when input is $<V_{TH-}$.
8	BO-	O	Negative CMLOutput Channel B with internal 50Ω pull up during normal operation and 2KΩ when EN_B=0. Drives to output common mode voltage when input is $<V_{TH-}$.
11	CLKIN+	I	Differential Input Reference Clock
12	CLKIN-	I	
30, 29	EN_[A,B]	I	EN_[A:B] is the enable pin. A LVCMOS high provides normal operation. A LVCMOS low selects a low power down mode.
4, 9, 20, 24, 25	GND	PWR	Supply Ground
19	IREF	O	External 475Ω resistor connection to set the differential output current
17, 18	OUT+, OUT-	O	Differential Reference Clock Output
36, 35	SD_A, SD_B	O	Signal Detect, output for channels A and B. Provides a LVCMOS high output when a valid input signal is detected. When low, SD_X indicates that the input signal level is below the signal detect threshold level.
34, 33	SEL[0:1]_A	I	Selection pins for equalizer (see Amplifier Configuration Table) w/ 50KΩ internal pull up
13, 14	SEL[0:1]_B	I	
32	SEL[2]_A	I	Selection pins for amplifier (see Amplifier Configuration Table) w/ 50KΩ internal pull up
15	SEL[2]_B	I	
31	SEL[3]_A	I	Selection pins for De-Emphasis (See De-Emphasis Configuration Table) w/ 50KΩ internal pull up
16	SEL[3]_B	I	
1, 5, 6, 10, 23, 28	V_{DD}	PWR	1.5 to 1.8V Supply Voltage

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +2.5V
DC SIG Voltage	–0.5V to V_{CC} +0.5V
Current Output	-25mA to +25mA
Power Dissipation Continous	500mW
Operating Temperature	0 to +70°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Output Swing Control

SEL2_[A:B]	Swing
0	1x
1	1.2x

Output De-emphasis Adjustment

SEL3_[A:B]	De-emphasis
0	0dB
1	-3.5dB

Equalizer Selection

SEL0_[A:B]	SEL1_[A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz

AC/DC Electrical Characteristics (V_{DD} = 1.5 to 1.8V, ±0.1v)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Ps	Supply Power	EN = LVCMOS Low			0.1	W
		EN = LVCMOS High			0.3	
	Latency	From input to output		2.0		ns
CML Receiver Input						
RL_{RX}	Return Loss	50 MHz to 1.25 GHz		12		dB
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		0.200			V
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	mV
V_{TH-SD}	Signal Detect Threshold	EN_X = High	50		200	
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	Ω
Z_{RX-DC}	DC Input Impedance		40	50	60	
Equalization						
J_{RS}	Residual Jitter(1,2)	Total Jitter			0.3	Ulp-p
		Deterministic jitter			0.2	
J_{RM}	Random Jitter(1,2)			1.5		psrms

Notes

1. K28.7 pattern is applied differentially at point A as shown in Figure 1.
2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. JItter is measured at 0V at point C of Figure 1.

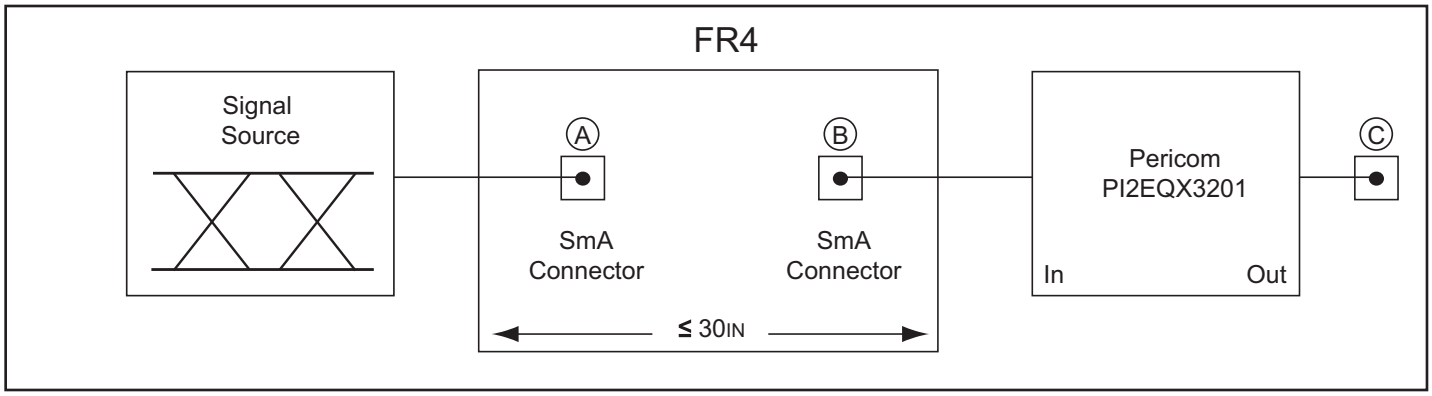


Figure 1. Test Condition Referenced in the Electrical Characteristic Table

AC/DC Electrical Characteristics (T_A = 0 to 70˚C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Transmitter Output (100Ω differential)						
V_{DIFFP}	Output Voltage Swing	Differential Swing | V_{TX-D+} - V_{TX-D-} |	300		425	mVp-p
V_{TX-C}	Common-Mode Voltage	| V_{TX-D+} + V_{TX-D-} | / 2		V_{CC}-0.3		
t_F, t_R	Transition Time	20% to 80% (1)			150	ps
Z_{OUT}	Output resistance	Single ended	40	50	60	Ω
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	Ω
C_{TX}	AC Coupling Capacitor		75		200	nF
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Ouput Voltage	$V_{TX-DIFFP-P}$ = 2 * | V_{TX-D+} - V_{TX-D-} |	600		850	mV
V_{OCM}(2)	Output Common Mode Voltage		1.2(3)		1.6(2)	V
LVCMOS Control Pins						
V_{IH}	Input High Voltage		0.65 × V_{DD}			V
V_{IL}	Input Low Voltage				0.35 × V_{DD}	
I_{IH}	Input High Current				250	µA
I_{IL}	Input Low Current				500	

Note:
1. Using K28.7 (0011111000) pattern)
2. The parameter is determined by device characterization, and is not production tested

AC Switching Characteristics for Clock Buffer (V_{DD} = 1.5V to 1.8V, ±0.1V) [3]

Symbol	Parameters	Min	Max.	Units	Notes
T_{rise} / T_{fall}	Rise and Fall Time (measured between 0.175V to 0.525V) [1]	125	525	ps	1
ΔT_{rise} / ΔT_{fall}	Rise and Fall Time Variation		75		1
V_{HIGH}	Voltage High including overshoot	660	900	mV	1
V_{LOW}	Voltage Low including undershoot	-150			1
V_{CROSS}	Absolute crossing point voltages	200	550		1
ΔV_{CROSS}	Total Variation of Vcross over all edges	200	250		1
T_{DC}	Duty Cycle (input duty cycle = 50%) [2]	45	55	%	2

Notes:
1. Measurement taken from Single Ended waveform.
2. Measurement taken from Differential waveform.
3. Test configuration is R_S = 33.2Ω, Rp = 49.9Ω, and 2pF.

Configuration Test Load Board Termination

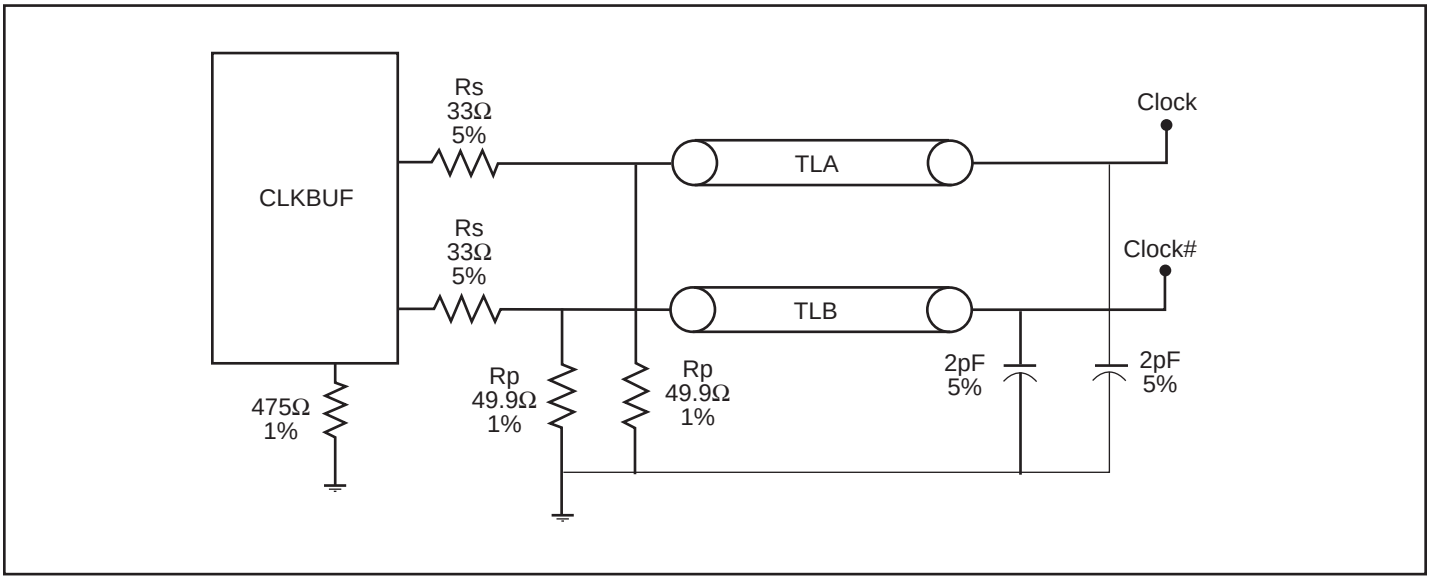
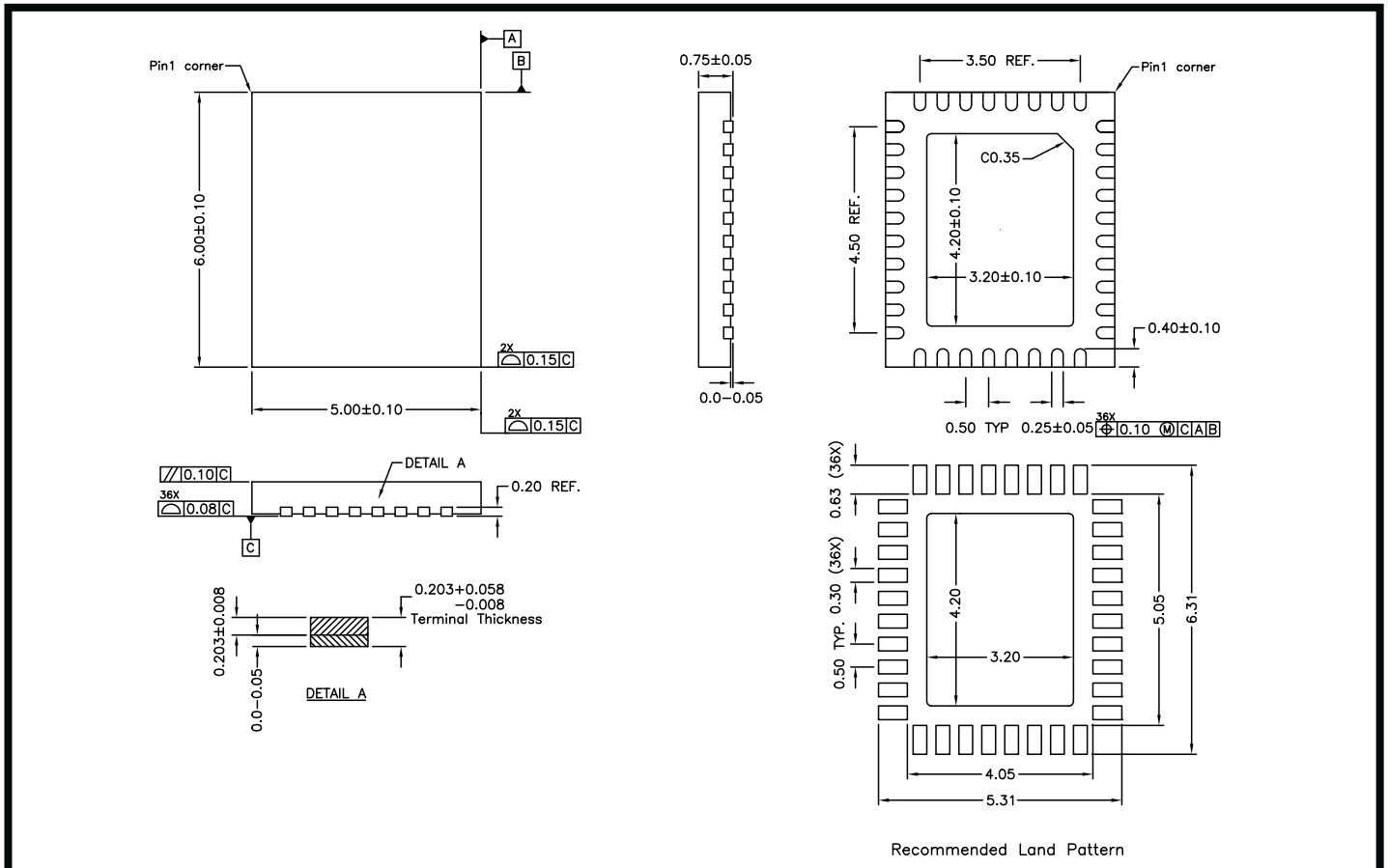


Figure 2. Configuration test load board termination

Note:
• TLA and TLB are 3” transmission lines.

Packaging Mechanical: 36-pad TQFN (ZF36)



Notes:
1) All dimensions are in millimeters, angles in degrees
2) Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
3) Ref JEDEC: MO-220I/WJHD
4) Thermal Via Diameter. Recommended 0.2~0.33mm
5) Thermal Pitch. Recommended 1.27mm

PERICOM Semiconductor Corporation — DATE: 4/28/06

DESCRIPTION: 36-contact, Very Thin Fine Pitch Quad Flat No-Lead (TQFN)	
PACKAGE CODE: ZF36	
DOCUMENT CONTROL #: PD-2023	REVISION: B

Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX3201BZFE	ZF	Pb-Free and Green 36-pad TQFN

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel