National Semiconductor

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LM4310
Mobile Pixel Link Two (MPL-2), RGB Display Differential Interface Deserializer

General Description

The LM4310 deserializes a Two Data + Clock Mobile Pixel Link (MPL-2) RGB serial link. Two operating modes are supported: 24-bit RGB and also 18-bit RGB.

The video interconnect is reduced from 28 signals to 3 differential signals with the LM4312 SER and companion LM4310 DES device, easing flex interconnect design, size constraints and cost.

Bufferless displays from QVGA (320 x 240) up to >VGA (640 x 480) pixels are supported.

The Deserializer also provides a glitch filter on the three control signals (DE, VS and HS). Glitches of 1 or 2 PCLKs wide are filtered out by the Deserializer to prevent flicker on the display.

Performance of the serial link can be checked by use of the parity/packet error reporting pin that monitors the serial payload odd parity bit and reports errors.

The LM4310 DES and LM4312 SER implements the physical layer of the MPL-2 Interface and features robust common-mode noise rejection.

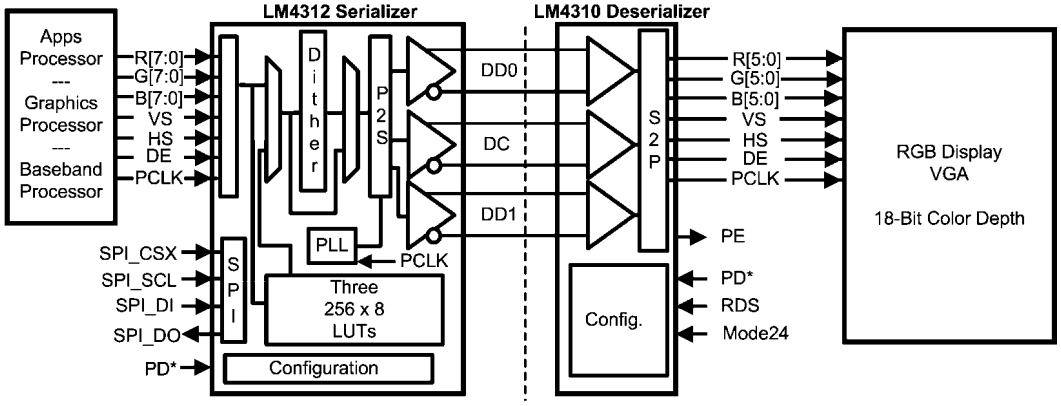
Features

- 24-bit or 18-bit RGB Display Interface
- Supports QVGA to > 640 x 480 VGA Resolutions
- MPL-2 Differential Physical Layer
- Internal 100 Ω Termination and CM Filter
- Glitch filter on control signals (DE, VS & HS)
- Parity / Payload error reporting pin and data re-circulator
- Low Power Consumption
- Receiver output drive strength control (RDS)
- Frame Sequence bits automatically resync upon data or clock error
- Power down mode reduces power to < 10 µA

System Benefits

- Small Robust Interface
- Low Power and Low EMI
- 24-bit Color Transport

Typical Application Diagram - Bridge Chips - 24-bit to 18-bit RGB Interface



[Supply, all Configuration pins, and bypass caps. and grounding not shown]

20203201

Ordering Information

NSID	Package Type	Package ID
LM4310	48L LLP, 6mm x 6mm x 0.4mm, 0.4mm pitch	TBD

Pin Descriptions

Pin Name	No. of Pins	I/O, Type	Description RGB Deserializer
MPL-2 SERIAL BUS PINS			
DD0P, DD0M, DD1P, DD1M	4	I, MPL-2	MPL-2 Differential Data Receiver True (Plus) and Compliment (Minus) Inputs Channel 0 and 1
DCP, DCM	2	I, MPL-2	MPL-2 Differential Clock Receiver True (Plus) and Compliment (Minus) Inputs
CONFIGURATION PINS			
PD*	1	I, LVCMOS	Power Down Mode Input PD* = Low, DES is in SLEEP mode PD* = High, DES is Enabled
TM	1	I LVCMOS	Test Mode **L = Normal Mode, tie to GND** H = Test Mode (Reserved)
RES0	2	I LVCMOS	**Tie to GND**
RDS	1	I LVCMOS	Receiver Drive Strength Control L = Low Drive Strength --- Use for < 10 MHz operations to reduce EMI H = Increased Drive Strength — Recommended
Mode24	1	I LVCMOS	Mode 24 bit Select L = 18-bit RGB H = 24-bit RGB
PE	1	O LVCMOS	Parity / Packet Error Reporting Pin L = no error (Pass) H = Packet or Parity Error detected, last known good Pixel Data is re-circulated.
VIDEO INTERFACE PINS			
PCLK	1	O, LVCMOS	Pixel Clock Output Video Signals are latched on the **RISING** edge.
R[7:0] G[7:0] B[7:0]	24	O, LVCMOS	RGB Data Bus Outputs 24-bit Mode - use RGB[7:0, Bit 7 is MSB] 18-bit Mode - **use RGB[5:0], RGB[7:6] = NC, LSB aligned.**
VS	1	O, LVCMOS	Vertical Sync. Output Signal must be greater than 2 PCLKs wide to pass.
HS	1	O, LVCMOS	Horizontal Sync. Output Signal must be greater than 2 PCLKs wide to pass.
DE	1	O, LVCMOS	Data Enable Output Signal must be greater than 2 PCLKs wide to pass.
POWER/GROUND PINS			
V_{DD}	7	Power	Power Supply Pins. All VDD pins must be connect to power supply. 1.6V to 2.0V
V_{SS}	DAP	Ground	Ground Pin

Note:
I = Input, O = Output, IO = Input/Output. **Do not float unused input pins.**

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.3V to +2.2V
LVCMOS Input/Output Voltage	−0.3V to (V_{DD} +0.3V)
MPL Input Voltage	−0.3V to V_{DD}
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature Soldering, 40 Seconds	+260°C
ESD Ratings:	
HBM, 1.5 kΩ, 100 pF	≥±2 kV
EIAJ, 0Ω, 200 pF	≥±200V

Maximum Package Power Dissipation Capacity at 25°C	
LLP Package	2.25 W
Derate LLP Package above 25°C	22.57 mW/°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
V_{DD} to GND	1.6	1.8	2.0	V
Pixel Clock Frequency, 6X	5		30	MHz
Pixel Clock Frequency, 8X	5		30	MHz
DC Frequency	30		240	MHz
Ambient Temperature	−40	25	85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
MPL-2							
V_{TH}	Differential Threshold High				0	+50	mV
V_{TL}	Differential Threshold Low				0	−50	mV
I_{IN}	Input Current			−1	0	+1	µA
R_T	Termination Resistance	(Note 7)		80	100	125	Ohm
V_{IN}	Input Voltage Range			0		400	mV
LVCMOS (1.6V to 2.0V Operation)							
V_{IH}	Input Voltage High Level	LVCMOS Inputs		0.7 V_{DD}		V_{DD}	V
V_{IL}	Input Voltage Low Level			GND		0.3 V_{DD}	V
V_{HY}	Input Hysteresis				100		mV
I_{IN}	Input Current (includes I_{OZ})			−1	0	+1	µA
V_{OH}	Output Voltage High Level	I_{OH} = −1 mA, RDS = H		0.8 V_{DD}		V_{DD}	V
		I_{OH} = −500 µA, RDS = L					
V_{OL}	Output Voltage Low Level	I_{OL} = 1 mA, RDS = H		V_{SS}		0.2 V_{DD}	V
		I_{OL} = 500 µA, RDS = L					
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{DD} = 1.8 V			6		mA
SUPPLY CURRENT							
I_{DD}	Total Supply Current—Enabled, RGB24	DC = 240 MHz, Checkerboard, RDS = H	(Note 4)		17	27	mA
		DC = 160 MHz, Checkerboard, RDS = H			12		mA
	Total Supply Current—Enabled, RGB18	DC = 180 MHz, Checkerboard, RDS = H			13		mA
		DC = 120 MHz, Checkerboard, RDS = H			9		mA
I_{DDZ}	Supply Current—Disable Power Down Mode	PD* = L	T_A = 25°C		1	10	µA
PD	Power Dissipation	RDS = H , V_{DD} = 1.8 V			22		mW

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
PARALLEL BUS OUTPUT TIMING							
t_{RISE}	Rise Time	PCLK output C_L = 15 pF, *Figure 2*	RDS = H		4		ns
			RDS = L		8		ns
t_{FALL}	Fall Time		RDS = H		4		ns
			RDS = L		8		ns
t_{DVBC}	Data Valid before PCLK (rise)	PCLK = 30 MHz (Note 7) *Figure 4*		.3	.5		UI
t_{DVAC}	Data Valid after PCLK (rise)			.3	.5		UI
SERIAL BUS INPUT TIMING							
t_{DVBC}	Serial Data Valid before Clock (Set Time)	DES Input (Note 7) *Figure 1*	RDS = H	400			ps
t_{DVAC}	Serial Data Valid after Clock (Hold Time)			400			ps
POWER UP TIMING							
t_{ON}		*Figure 7*	PD* L-to-H		1024		PCLK cycles
MPL POWER OFF TIMING							
t_{PAZ}	Disable Time to Power Down	(Note 6) *Figure 8*			0.1	2	µs

Recommended Input Timing Requirements

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL SIGNALS (DE, VS & HS)						
C_{PW}	Control Signal Minimum Pulse Width	DE, VS and HS	3			PCLK cycles

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{DD} = 1.8V and T_A = 25°C.

Note 3: Current into a device pin is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to Ground unless otherwise specified.

Note 4: Total Supply Current Conditions: DES C_L = 15pF, TYP V_{DD} = 1.8V, MAX VDD = 2.0V.

Note 5: Maximum transition time is a function of clock rate and should be less than 30% of the clock period to preserve signal quality.

Note 6: Guaranteed functionally by the I_{DDZ} parameter. See also *Figure 8*.

Note 7: Specification is guaranteed by characterization or design, and is not tested in production.

Timing Diagrams

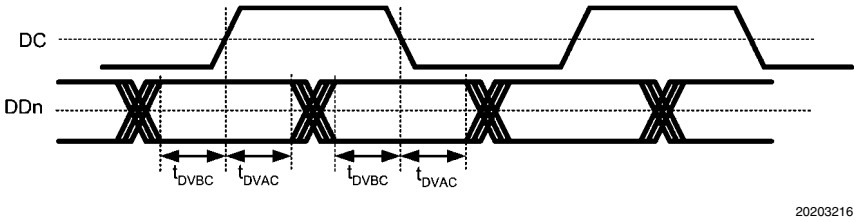


FIGURE 1. Serial Data Valid

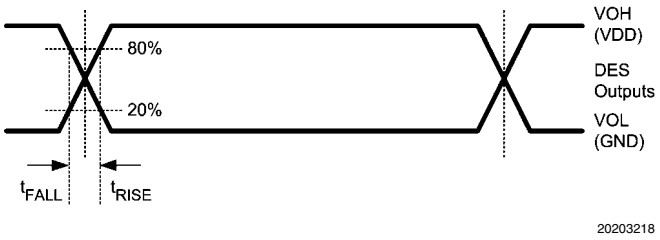


FIGURE 2. PCLK Output Rise and Fall Time

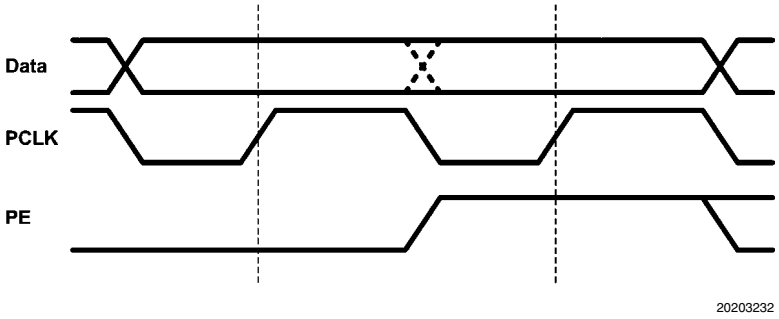


FIGURE 3. PE Output Flag Timing

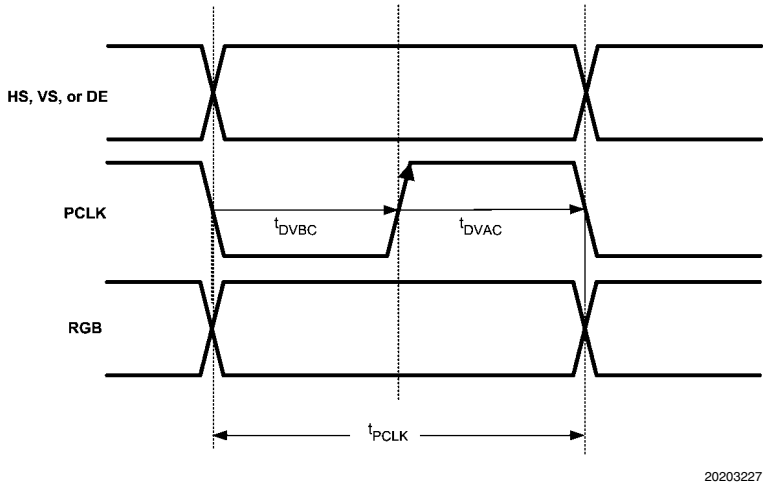


FIGURE 4. LVCMOS RGB Output Timing

Functional Description

The LM4310 is a Mobile Pixel Link 2 DES that deserializes a Two Data + Clock MPL-2 Interface to a 24-bit or 18-bit Parallel RGB Interface depending upon configuration. The LM4310 is compatible with the LM4312 Serializer.

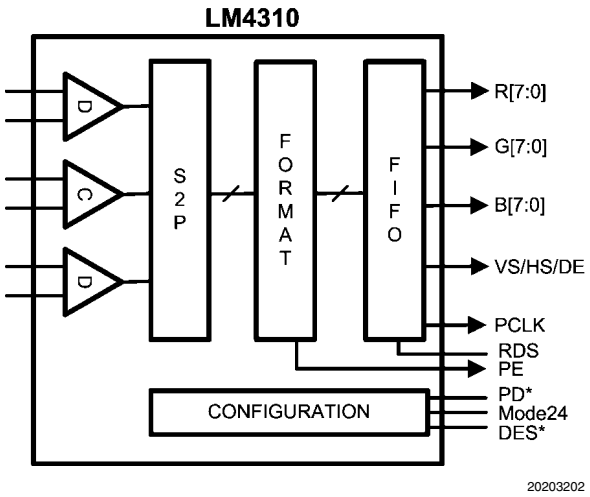


FIGURE 5. LM4310 Block Diagram

SERIAL BUS TIMING

Data valid is relative to both edges of a RGB transaction as shown in *Figure 6*. Data valid is specified as: Data Valid before Clock, Data Valid after Clock, and Skew between data lines should be less than 500 ps.

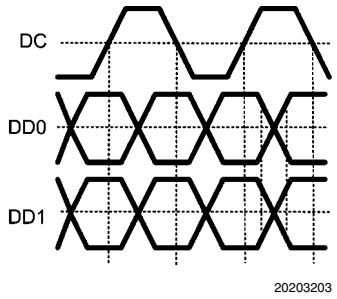


FIGURE 6. MPL-2 Link Timing

SERIAL BUS PHASES

There are three bus phases on the MPL serial bus. These are determined by the state of the DC and DD lines. When the Link is OFF, all signal lines are driven to Ground. When the Link is active, the DC is running and streaming data is sent on the DD Lines. During Link Up, the lines are first driven to a static level and then start to transition. The MPL-2 bus phases are shown in *Table 1*.

TABLE 1. Link Phases

Name	DC State	DDn State	Phase Description	Pre-Phase	Post-Phase
OFF (O)	GND	GND	Link is Off	A, or LU	LU
LINK-UP (LU)	L	L	Start Up	O	A
ACTIVE	A	X	Streaming Data	LU	O

SERIAL BUS START UP TIMING

When the Link is enabled the MPL-2 signals are driven to a static differential Low voltage, this is held for a fixed count to allow for the SER PLL to lock to the PCLK. Next the MPL-2 Lines are driven with actual data. Once the DES is enabled, it will sync up to the serial signals by detecting the Frame Sequence (FS) bits and output correct data. This LINK-UP sequence applies to the MPL-2 RGB Streaming Interface (LM4312/LM4310).

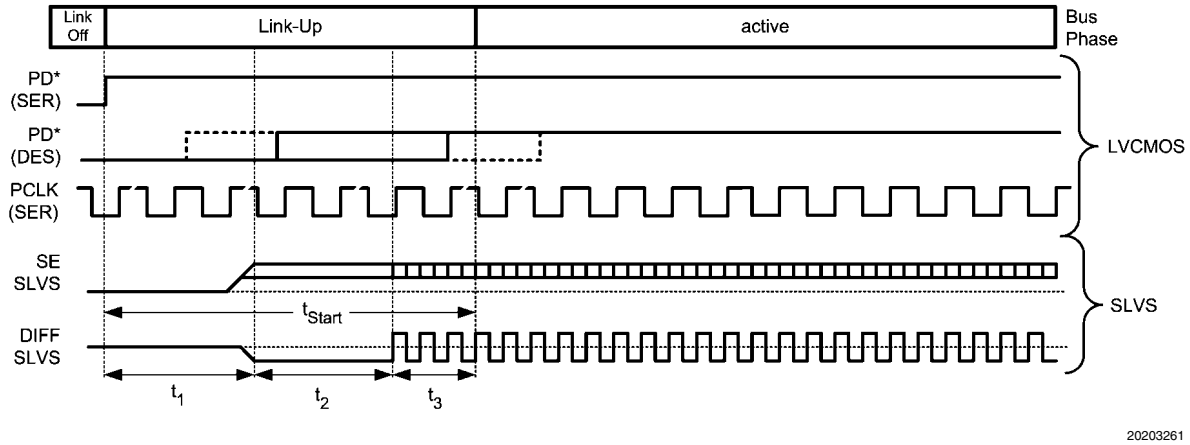


FIGURE 7. MPL Power Up Timing

OFF PHASE

When the Link is turned off, the MPL-2 lines are actively driven to ground. *Figure 8* shows both the differential waveform and single-ended waveforms.

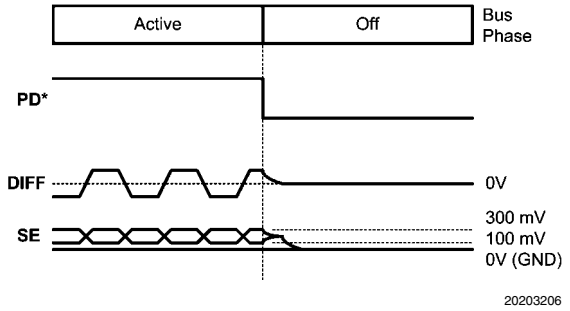


FIGURE 8. Bus Power Down Timing

RGB VIDEO INTERFACE

The LM4310 is transparent to data format and control signal polarity. On each **rising** edge of the PCLK, RGB inputs, HS, VS and DE are sampled. A PCLK by PCLK representation of these signals is duplicated on the RGB Video Interface of the LM4310 device.

24-bit Color Depth Support

The 24-bit RGB (R0-7, G0-7, B0-7) color information are sent first, followed by the control bits VS (VSYNC), HS (HSYNC), DE (Data Enable) and PE (Parity Error) and Frame Sequence (F[1:0]) bits. The bit PE is parity calculated on the full data payload including HS, VS, DE, and F0 and F1 bits. The 24-bit mode is selected by setting the **Mode24** configuration input to a High (V_{DD}). 24–bit RGB mode DC is 8X the PCLK.

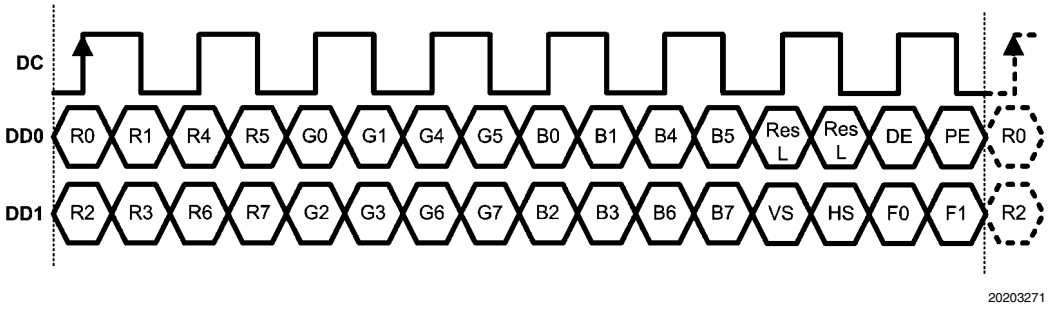


FIGURE 9. 24-bit RGB, 2 DD + DC Lane Serial Payload (8X)

18-bit Color Depth Support

The 18-bit RGB (R0-5, G0-5, B0-5) color information are sent first, followed by the control bits VS (VSYNC), HS (HSYNC), DE (Data Enable) , PE (Parity Error) and Frame Sequence (F[1:0]) bits. The bit PE is parity calculated on the full data payload including HS, VS, DE, and F0 and F1 bits. The 18-bit mode is selected by setting the **Mode24** configuration input to a Low (Ground). 18–bit RGB mode DC is 6X the PCLK.

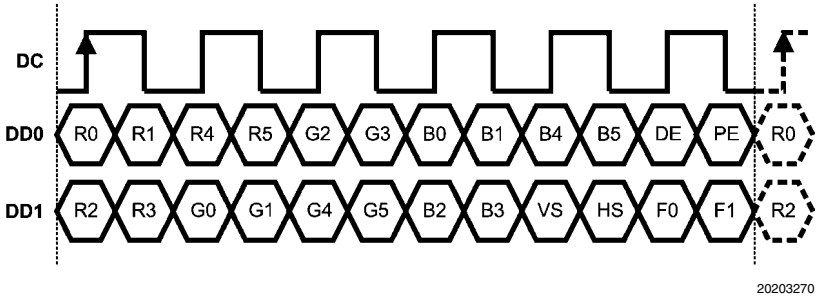


FIGURE 10. 18-bit RGB, 2 DD + DC Lane Serial Payload (6X)

FRAME SEQUENCE — SYNC DETECT AND RECOVERY

If a data error or clock slip error occurs over the MPL-2 link, the LM4310 can detect this condition and quickly recover from it. The method chosen is a data transparent method, and has very little overhead because it does not use a data expansion coding method. For the 18-bit color transaction, it uses two bits that are already required in the 6 DC cycle transaction. Total overhead for each pixel is 2/24 or 12% in the 6X configuration.

FS - SER SIDE FUNCTION

The LM4312 SER simply increments the two bit field F[1:0] on every pixel or frame transmitted. Therefore every four frames, the pattern will repeat. It is very unlikely that this pattern would be found within the payload data, and if it were found, the probability that it would repeat for many frames becomes infinitely small.

FS - DES SIDE FUNCTION

The LM4310 DES, upon a normal power up sequence, detects synchronization and outputs the correct pixel data. It looks for the incrementing pattern for N (N = 4 or 8) pixels (frames) and finding it, starts to output the pixel gray scale data and timing signals.

If a random bit error occurs in the F[1:0] field, the hysteresis counter decrements by one, but the chip continues to output data normally. The next frame will likely recover, incrementing the hysteresis counter back to the maximum and operation will continue normally.

If however, a clock slip or error occurs, the next N frames will be bad and the F[1:0] field will not be detected properly for each frame after the clock error. In this case, the hysteresis counter will decrement to zero quickly. This action causes the DES output to re-circulate the last known good pixel data, and initiates a search function for the incrementing sequence. Once the DES is back in bit alignment (proper frame sequence), then the received good payloads are sent to its output.

DETECTING THE INCREMENTING SEQUENCE

Acquiring synchronization from a random position requires looking only at one DD line, as this line contains the incrementing sequence F[1:0]. This is done by examining six two-bit pairs and comparing each pair to an incrementing sequence. A snapshot of the data is first taken and loaded into six two-bit adders. The adders increment by one and then compare the same bit positions in the next 12-bits. If a match is found, a flag is set for that bit pair. This same procedure is followed until there is only one flag set. After only one flag is set, the synchronization is tested for the full count of the hysteresis counter (4 or 8 pixels) and then a valid synchronization is declared and pixel data and control signals are again output to the display.

In the best case, this parallel method of detecting sync is very fast. If only one flag exists on the first frame tested, then resynchronization can occur in as little as 6 pixel times (assuming no new errors). If however, random data emulates an incrementing sequence for several pixels of time, the process can take longer, as it is data dependant.

It is important to note that a pathological case exists, as it does for most pattern detection methods, where the data can forever emulate this incrementing sequence, when in fact the true F[1:0] is not detected. This F'[1:0] (F prime) may occur for several pixels, but becomes linearly less probable as more and more data passes through the system.

SERIAL PAYLOAD PARITY BIT & DATA RE-CIRCULATION

Under normal operating conditions link errors are not expected as shown in *Figure 11*. However, Odd Parity is calculated on the RGB and control (VS, HS, DE and F0 and F1 bits) signals and is sent from the SER to the DES via the serial PE bit.

The LM4310 DES monitors the PE bit and if a parity error is detected, it **prevents** the output of the known bad pixel payload. The last payload (Pixel data and control) is re-circulated to the DES outputs until the next valid payload is received and Frame Sequence is re-validated as shown in *Figure 3*. Typically a payload with a Parity Error, will take 4 to 5 PCLKs to clear and be re-validated. Thus, the PE pin pulse high will be 4 or more PCLKs wide depending upon the error duration. The PE pin also flags Frame Sequence errors.

Note that Odd Parity by definition can only capture 50% of the possible errors. The PE output can be monitored to determine link performance.

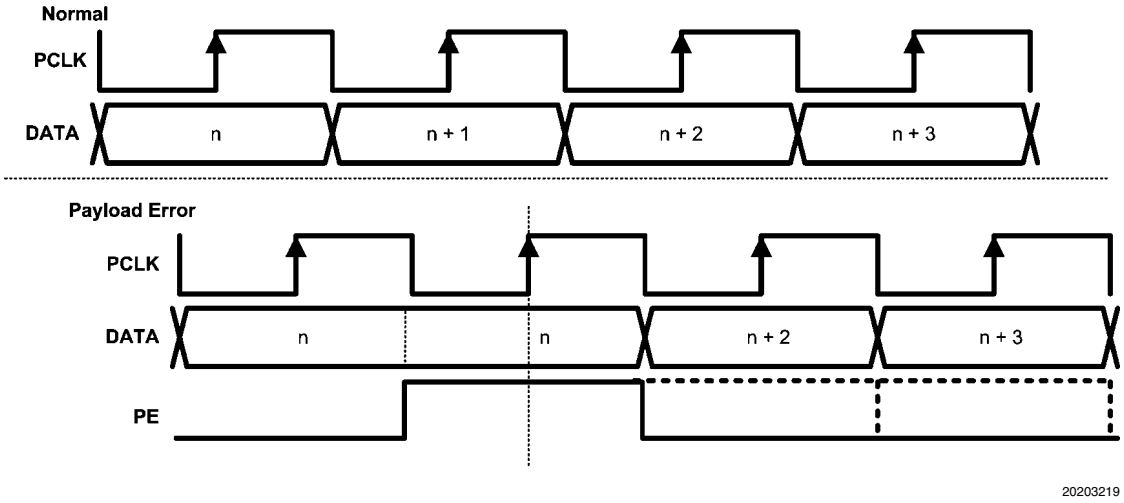


FIGURE 11. Parity Error Flag and Data Recirculation

CONTROL SIGNAL FILTER

The Deserializer provides a noise glitch filter on the control signals (DE, VS and HS). Pulse widths of 1 or 2 PCLKs wide are filtered out preventing flickering on the display. Valid signals on the DE, VS and HS pins must be at least three PCLKs wide in duration.

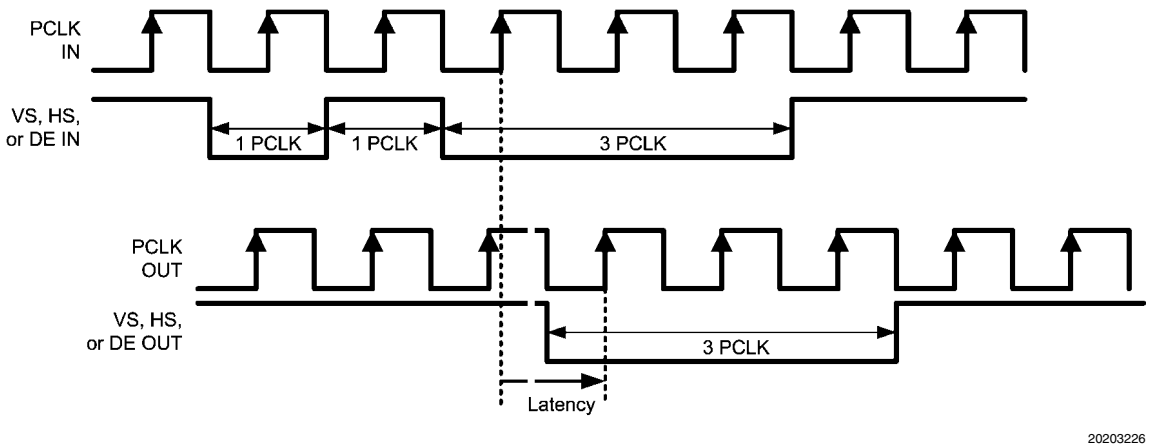


FIGURE 12. Control Signal (HS, VS, DE) Filter

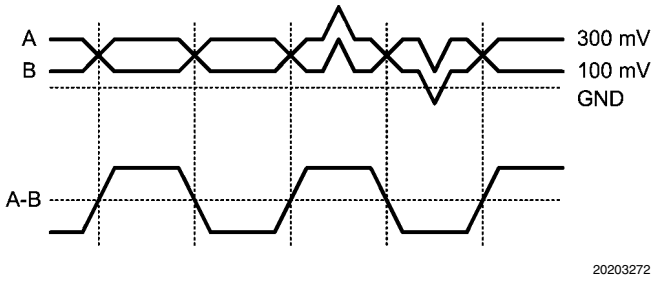


FIGURE 13. Single-ended and Differential SLVS Waveforms

MPL-2 Interface

The Physical Layer of the MPL-2 serial interface is based on the JEDEC SLVS standard. This defines a source and load terminated interface for use in point-to-point applications. The default signal swing is a 200mV signal, which generates a 400mVpp signal across the receiver inputs. The 200mV signal is offset by 200mV. The differential signal magnitude may be adjusted by the Line Driver depending upon Application requirements. A low noise, short distance application may utilize a smaller VOD to reduce power dissipation and noise generation. An application in a high noise environment or longer length, may choose to utilize the maximum signal swing. *Figure 13* illustrates the single-ended and resulting differential waveforms of the serial signals. Noise that is picked up common to both lines is rejected.

LM4310 Features and Operation

POWER SUPPLIES & BYPASS RECOMMENDATIONS

The V_{DD} pins should be connected all together to a common power plane.

Bypass capacitors should be placed near the power supply pins of the device. Use high frequency ceramic (surface mount recommended) 0.1 µF capacitors. Connect bypass capacitors with wide traces and use dual or larger via to reduce resistance and inductance of the via. Utilizing a thin spacing between power and ground planes will provide good high frequency bypass above the frequency range where most typical surface mount capacitors are less effective. To gain the maximum benefit from this, low inductance feed points are important. Also, adjacent signal layers can be filled to create additional capacitance. Minimize loops in the ground returns also for improved signal fidelity and lowest emissions.

UNUSED/OPEN PINS

Unused outputs should be left open to minimize power dissipation. For example in the 18–bit RGB mode, RGB[7:6] will be unused and driven to a static Low level. Unused inputs **must** be tied to the proper input level—do not float.

POWER DOWN (SLEEP)

When the DES is in SLEEP mode, its outputs are in the following states:

All RGB Outputs = Low

VS = HS = DE = Low

PCLK = Low

PE = Low

Application Information

FLEX CIRCUIT RECOMMENDATIONS

The MPL-2 lines should run together to minimize any trace length differences (skew). For impedance control and also noise isolation (crosstalk), guard ground traces are recommended in between the signals. Commonly a Ground-Signal-Signal-Ground (GSSGSSG) layout is used. Locate fast edge rate and large swing signals further away to also minimize any coupling (unwanted crosstalk). In a stacked flex interconnect, crosstalk also needs to be taken into account in the above and below layers (vertical direction). To minimize any coupling locate MPL-2 traces next to a ground layer. Power rails also tend to generate less noise than LVCMOS signals, so they are also good candidates for use as isolation and separation.

The interconnect from the SER to the DES typically acts like a transmission line (length / transition time dependant). Thus impedance control and ground returns are an important part of system design. Differential impedance should be in the 80 to 100 Ohm nominal range for the MPL-2 Link. Skew should be less than 500ps to maximize timing margins.

GROUNDING

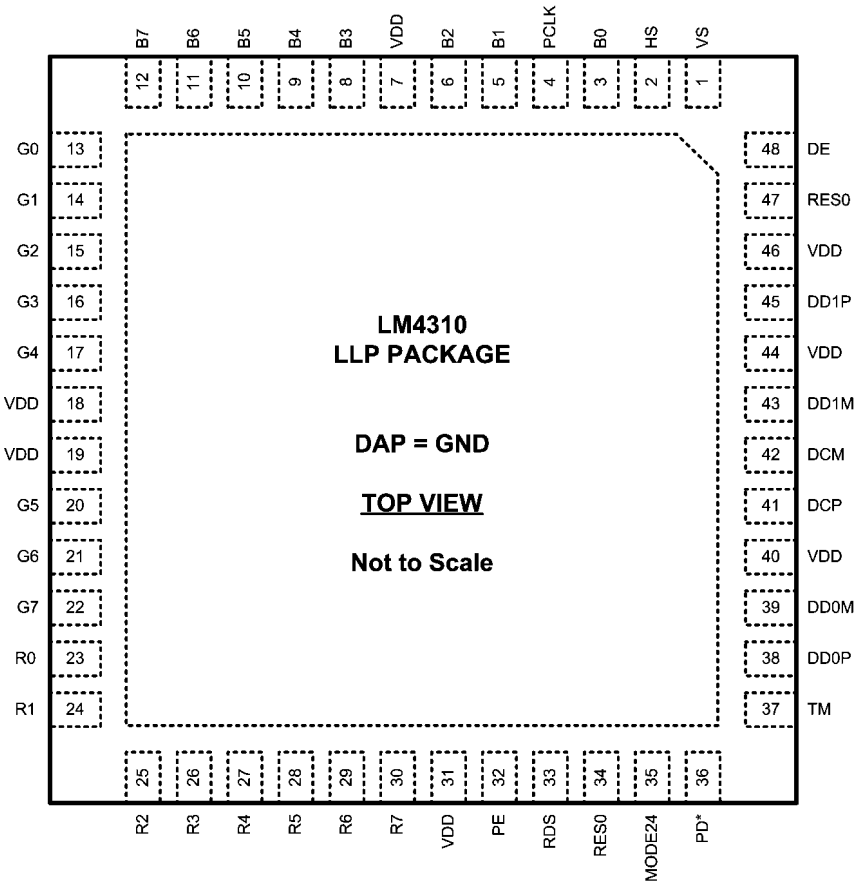
While the LM4310 uses a common ground connection to the center DAP PAD. For proper operation, this DAP **MUST** be connected to the system ground plane.

PCB RECOMMENDATIONS

General guidelines for the PCB design:

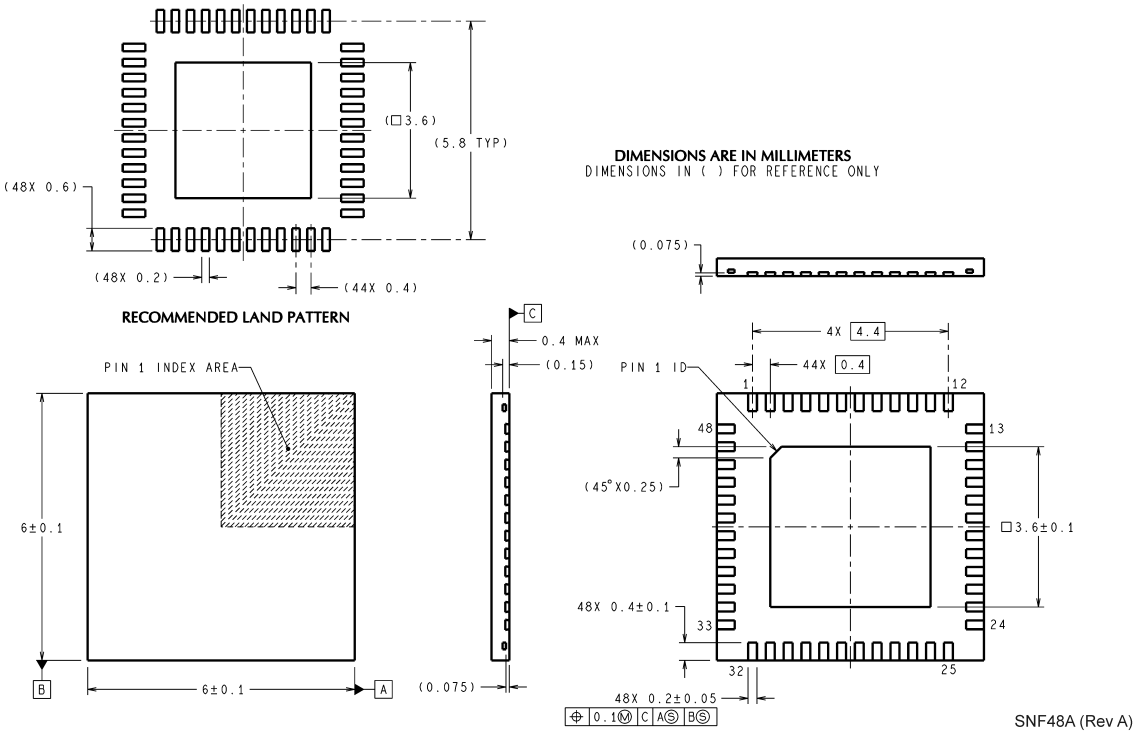
- Floor plan, locate MPL-2 SER near the connector to limit chance of cross talk to high speed serial signals.
- Route serial traces together, minimize the number of layer changes to reduce loading.
- Use ground lines are guards to minimize any noise coupling (guarantees distance).
- Avoid parallel runs with fast edge, large LVCMOS swings.
- Use a GSSG pinout in connectors (Board to Board or ZIF).
- Bypass the device with MLC surface mount devices and thinly separated power and ground planes with low inductance feeds.
- High current returns should have a separate path with a width proportional to the amount of current carried to minimize any resulting IR effects.
- AN-1187 LLP Package Application Note for SMT Assembly Recommendations

Connection Diagram LLP Package



TOP VIEW
(not to scale)

Physical Dimensions inches (millimeters) unless otherwise noted



48L LLP, 0.4mm pitch
Order Number LM4310SM
NS Package Number SNF48A

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
Audio	www.national.com/audio	Analog University	www.national.com/AU
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adc	Distributors	www.national.com/contacts
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