National Semiconductor

September 28, 2010

LM25119

Wide Input Range Dual Synchronous Buck Controller

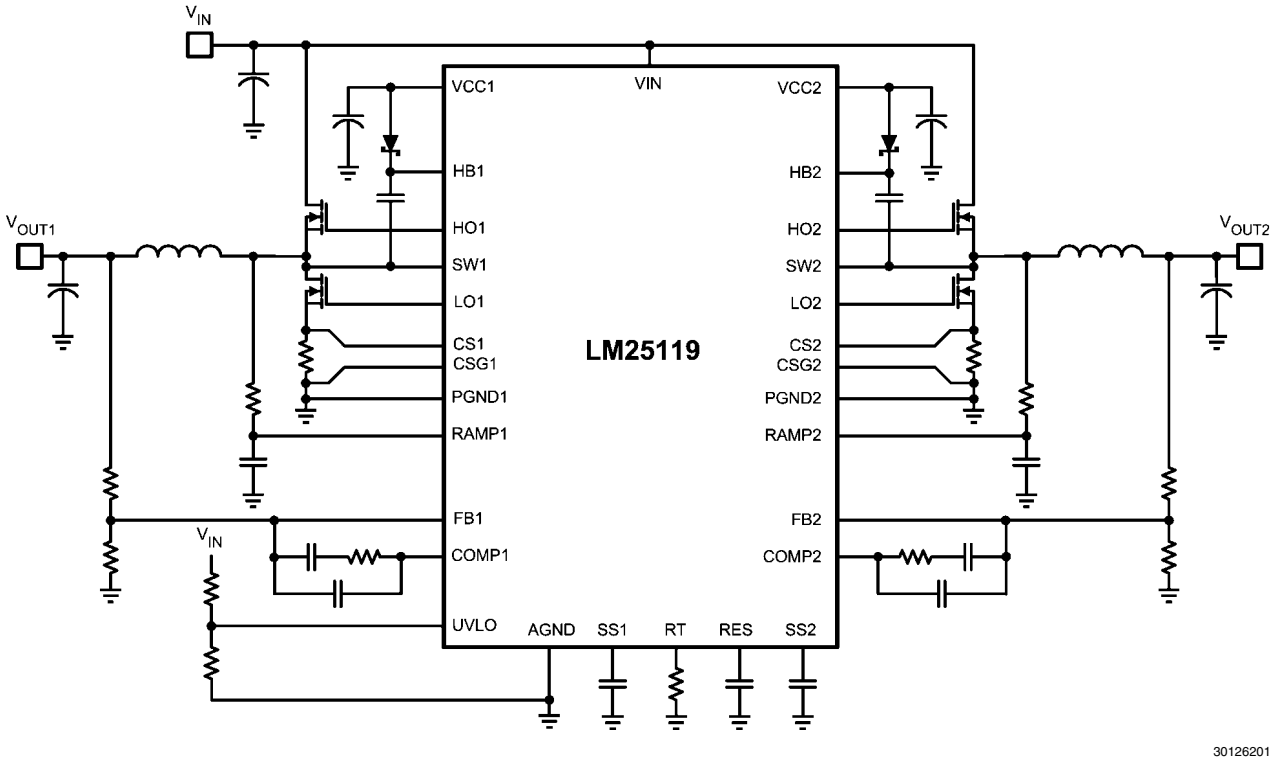
General Description

The LM25119 is a dual synchronous buck controller intended for step-down regulator applications from a high voltage or widely varying input supply. The control method is based upon current mode control utilizing an emulated current ramp. Current mode control provides inherent line feed-forward, cycle-by-cycle current limiting and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable control of very small duty cycles necessary in high input voltage applications. The switching frequency is programmable from 50kHz to 750kHz. The LM25119 drives external high-side and low-side NMOS power switches with adaptive dead-time control. A user-selectable diode emulation mode enables discontinuous mode operation for improved efficiency at light load conditions. A high voltage bias regulator with automatic switch-over to external bias further improves efficiency. Additional features include thermal shutdown, frequency synchronization, cycle-by-cycle and hiccup mode current limit and adjustable line under-voltage lockout. The device is available in a power enhanced leadless LLP-32 package featuring an exposed die attach pad to aid thermal dissipation.

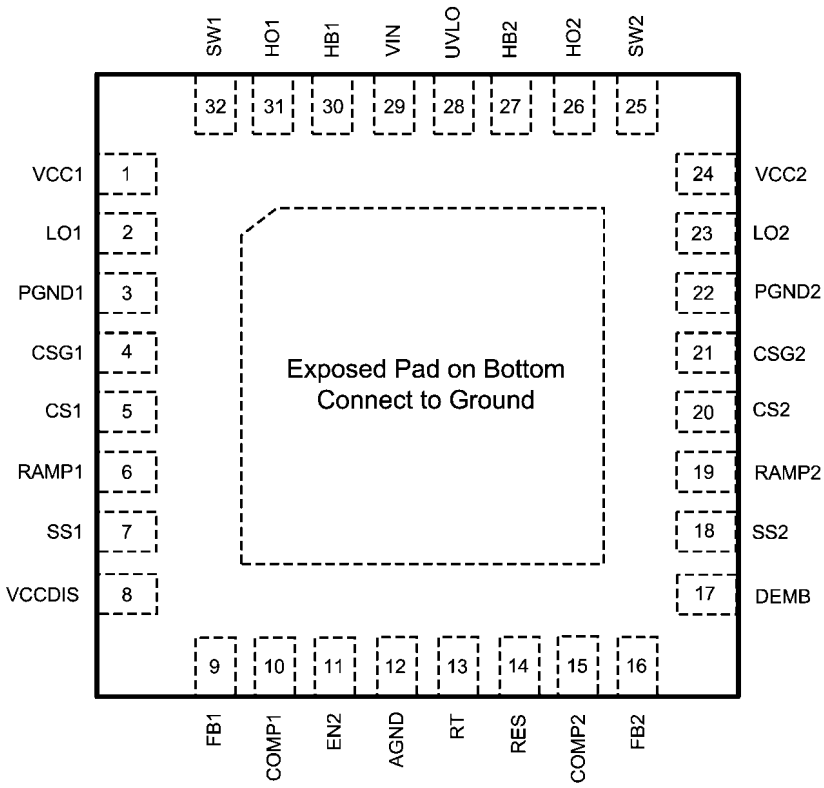
Features

- Emulated peak current mode control
- Wide operating range from 4.5V to 42V
- Easily configurable for dual outputs or interleaved single output
- Robust 3.3A peak gate drive
- Switching frequency programmable to 750kHz
- Optional diode emulation mode
- Programmable output from 0.8V
- Precision 1.5% voltage reference
- Programmable current limit
- Hiccup mode overload protection
- Programmable soft-start
- Programmable line under-voltage lockout
- Automatic switch-over to external bias supply
- Channel2 enable logic input
- Thermal Shutdown
- Leadless LLP32 (5mm x 5mm) package

Typical Application



Connection Diagram



Top View
32–Lead LLP

Order Number	Package Type	NSC Package Drawing	Supplied As
LM25119PSQ	LLP-32	SQA32A	1000 Units on Tape and Reel
LM25119PSQX	LLP-32	SQA32A	4500 Units on Tape and Reel
LM25119PSQE	LLP-32	SQA32A	250 Units on Tape and Reel

Pin Descriptions

Pin	Name	Description
1	VCC1	Bias supply pin. Locally decouple to PGND1 using a low ESR/ESL capacitor located as close to controller as possible.
2	LO1	Low side MOSFET gate drive output. Connect to the gate of the channel1 low-side synchronous MOSFET through a short, low inductance path.
3	PGND1	Power ground return pin for low side MOSFET gate driver. Connect directly to the low side of the channel1 current sense resistor.
4	CSG1	Kelvin ground connection to the external current sense resistor. Connect directly to the low side of the channel1 current sense resistor.
5	CS1	Current sense amplifier input. Connect to the high side of the channel1 current sense resistor.
6	RAMP1	PWM ramp signal. An external resistor and capacitor connected between the SW1 pin, the RAMP1 pin and the AGND pin sets the channel1 PWM ramp slope. Proper selection of component values produces a RAMP1 signal that emulates the current in the buck inductor.
7	SS1	An external capacitor and an internal 10µA current source set the ramp rate of the channel1 error amp reference. The SS1 pin is held low when VCC1 or VCC2 < 4V, UVLO < 1.25V or during thermal shutdown.
8	VCCDIS	Optional input that disables the internal VCC regulators when external biasing is supplied. If VCCDIS >1.25V, the internal VCC regulators are disabled. The externally supplied bias should be coupled to the VCC pins through a diode. VCCDIS has a 500kΩ pull-down resistor to ground to enable the VCC regulators when the pin is left floating. The pull-down resistor can be overridden by pulling VCCDIS above 1.25V with a resistor divider connected to the external bias supply.
9	FB1	Feedback input and inverting input of the channel1 internal error amplifier. A resistor divider from the channel1 output to this pin sets the output voltage level. The regulation threshold at the FB1 pin is 0.8V.
10	COMP1	Output of the channel1 internal error amplifier. The loop compensation network should be connected between this pin and the FB1 pin.
11	EN2	If the EN2 pin is low, channel2 will be disabled. Channel1 and all other functions remain active. The EN2 has a 50kΩ pull-up resistor to enable channel2 when the pin is left floating.
12	AGND	Analog ground. Return for the internal 0.8V voltage reference and analog circuits.
13	RT	The internal oscillator is set with a single resistor between RT and AGND. The recommended maximum oscillator frequency is 1.5MHz which corresponds to a maximum switching frequency of 750kHz for either channel. The internal oscillator can be synchronized to an external clock by coupling a positive pulse into RT through a small coupling capacitor.
14	RES	The restart timer pin for an external capacitor that configures the hiccup mode current limiting. A capacitor on the RES pin determines the time the controller will remain off before automatically restarting in hiccup mode. The two regulator channels operate independently. One channel may operate in normal mode while the other is in hiccup mode overload protection. The hiccup mode commences when either channel experiences 256 consecutive PWM cycles with cycle-by-cycle current limiting. After this occurs, a 10µA current source charges the RES pin capacitor to the 1.25V threshold which restarts the overloaded channel.
15	COMP2	Output of the channel2 internal error amplifier. The loop compensation network should be connected between this pin and the FB2 pin.
16	FB2	Feedback input and inverting input of the channel2 internal error amplifier. A resistor divider from the channel2 output to this pin sets the output voltage level. The regulation threshold at the FB2 pin is 0.8V.
17	DEMB	Logic input that enables diode emulation when in the low state. In diode emulation mode, the low side MOSFET is latched off for the remainder of the PWM cycle when the buck inductor current reverses direction (current flow from output to ground). When DEMB is high, diode emulation is disabled allowing current to flow in either direction through the low side MOSFET. A 50kΩ pull-down resistor internal to the LM25119 holds DEMB pin low and enables diode emulation if the pin is left floating.
18	SS2	An external capacitor and an internal 10µA current source set the ramp rate of the channel2 error amp reference. The SS2 pin is held low when VCC1 or VCC2 < 4V, UVLO < 1.25V or during thermal shutdown.

Pin	Name	Description
19	RAMP2	PWM ramp signal. An external resistor and capacitor connected between the SW2 pin, the RAMP2 pin and the AGND pin sets the channel2 PWM ramp slope. Proper selection of component values produces a RAMP2 signal that emulates the current in the buck inductor.
20	CS2	Current sense amplifier input. Connect to the high side of the channel2 current sense resistor.
21	CSG2	Kelvin ground connection to the external current sense resistor. Connect directly to the low side of the channel2 current sense resistor.
22	PGND2	Power ground return pin for low side MOSFET gate driver. Connect directly to the low side of the channel2 current sense resistor.
23	LO2	Low side MOSFET gate drive output. Connect to the gate of the channel2 low-side synchronous MOSFET through a short, low inductance path.
24	VCC2	Bias supply pin. Locally decouple to PGND2 using a low ESR/ESL capacitor located as close to controller as possible.
25	SW2	Switching node of the buck regulator. Connect to channel2 bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET.
26	HO2	High side MOSFET gate drive output. Connect to the gate of the channel2 high-side MOSFET through a short, low inductance path.
27	HB2	High-side driver supply for bootstrap gate drive. Connect to the cathode of the channel2 external bootstrap diode and to the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high side MOSFET gate and should be placed as close to the controller as possible.
28	UVLO	Under-voltage lockout programming pin. If the UVLO pin is below 0.4V, the regulator will be in the shutdown mode with all function disabled. If the UVLO pin is greater than 0.4V and below 1.25V, the regulator will be in standby mode with the VCC regulators operational, the SS pins grounded and no switching at the HO and LO outputs. If the UVLO pin voltage is above 1.25V, the SS pins are allowed to ramp and pulse width modulated gate drive signals are delivered at the LO and HO pins. A 20µA current source is enabled when UVLO exceeds 1.25V and flows through the external UVLO resistors to provide hysteresis.
29	VIN	Supply voltage input source for the VCC regulators.
30	HB1	High-side driver supply for bootstrap gate drive. Connect to the cathode of the channel1 external bootstrap diode and to the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high side MOSFET gate and should be placed as close to controller as possible.
31	HO1	High side MOSFET gate drive output. Connect to the gate of the channel1 high-side MOSFET through a short, low inductance path.
32	SW1	Switching node of the buck regulator. Connect to channel1 bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET.
EP	EP	Exposed pad of LLP package. No internal electrical connections. Solder to the ground plane to reduce thermal resistance.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN to AGND	-0.3 to 45V
SW1, SW2 to AGND	-3.0 to 45V
HB1 to SW1, HB2 to SW2	-0.3 to 15V
VCC1, VCC2 to AGND (*Note 2*)	-0.3 to 15V
FB1, FB2, DEMB, RES, VCCDIS, UVLO to AGND	-0.3 to 15V
HO1 to SW1, HO2 to SW2	-0.3 to HB+0.3V
LO1, LO2 to AGND	-0.3 to VCC+0.3V
SS1, SS2 to AGND	-0.3 to 7V
EN2, RT to AGND	-0.3 to 7V
CS1, CS2, CSG1, CSG2 to AGND	-0.3V to 0.3V
PGND to AGND	-0.3V to 0.3V
ESD Rating HBM (*Note 3*)	2kV
Storage Temperature	-55°C to +150°C
Junction Temperature	+150°C

Operating Ratings (*Note 1*)

VIN	4.5V to 42V
VCC	4.5V to 14V
HB to SW	4.5V to 14V
Junction Temperature	-40°C to +125°C

Note: COMP1, COMP2, RAMP1, and RAMP2 are output pins. As such they are not specified to have an external voltage applied.

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature range of -40°C to +125°C. Unless otherwise specified, the following conditions apply: VIN = 12V, VCC = 8V, VCCDIS = 0V, EN2 = 5V, R_T = 25kΩ, no load on LO and HO. Electrical characteristics are per channel where applicable. See (*Note 4*) and (*Note 5*).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN Supply						
I_{BIAS}	VIN Operating Current	SS1 = SS2 = 0V		6	**7.3**	mA
		VCCDIS = 2V, SS1 = SS2 = 0V		340	**500**	µA
I_{VCC}	VCC1 Operating Current	VCCDIS = 2V, SS1 = SS2 = 0V		3.9	**4.5**	mA
	VCC2 Operating Current	VCCDIS = 2V, SS1 = SS2 = 0V		1.4	**2.0**	mA
$I_{SHUTDOWN}$	VIN Shutdown Current	UVLO = 0V, SS1 = SS2 = 0V		15	**33**	µA
VCC Regulator (*Note 6*)						
$V_{CC(REG)}$	VCC Regulation		**6.77**	7.6	**8.34**	V
	VCC Regulation	VIN = 4.5V, No external load	**4.4**	4.46		V
	VCC Sourcing Current Limit	VCC = 0V	**25**	40		mA
	VCCDIS Switch Threshold	VCCDIS Rising	**1.19**	1.25	**1.29**	V
	VCCDIS Switch Hysteresis			0.07		V
	VCCDIS Input Current	VCCDIS = 0V		-20		nA
	VCC Under-voltage Threshold	Positive going VCC	**3.8**	4.0	**4.2**	V
	VCC Under-voltage Hysteresis			0.2		V
EN2 Input						
V_{IL}	EN2 Input Low Threshold			2.0	**1.5**	V
V_{IH}	EN2 Input High Threshold		**2.9**	2.5		V
	EN2 Input pull-up resistor			50		kΩ
UVLO						
	UVLO Threshold	UVLO Rising	**1.20**	1.25	**1.29**	V
	UVLO Hysterisis Current	UVLO = 1.4V	**15**	20	**25**	µA
	UVLO Shutdown Threshold			0.4		V
	UVLO Shutdown Hysterisis Voltage			0.1		V
Soft Start						
	SS Current Source	SS = 0V	**7**	10	**13**	µA
	SS Pull Down R_{DSON}			10		Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Error Amplifier						
V_{REF}	FB Reference Voltage	Measured at FB pin, FB = COMP	**0.788**	0.8	**0.812**	V
	FB Input Bias Current	FB = 0.8V		1		nA
	FB Disable Threshold	Interleaved Threshold		2.5		V
	COMP VOH	Isource = 3mA	**2.8**			V
	COMP VOL	Isink = 3mA			**0.31**	V
A_{OL}	DC Gain			80		dB
f_{BW}	Unity Gain Bandwidth			3		MHz
PWM Comparators						
$t_{HO(OFF)}$	Forced HO Off-time		**220**	320	**430**	ns
$t_{ON(min)}$	Minimum HO On-time	C_{RAMP} = 50pF		100		ns
Oscillator						
f_{SW1}	Frequency 1	R_T = 25kΩ	**180**	200	**220**	kHz
f_{SW2}	Frequency 2	R_T = 10kΩ	**430**	480	**530**	kHz
	RT Output Voltage			1.25		V
	RT Sync Positive Threshold		**2.5**	3.2	**4**	V
	Sync Pulse Minimum Width		**100**			ns
Current Limit						
$V_{CS(TH)}$	Cycle-by-cycle Sense Voltage Threshold (CS - CSG)	RAMP = 0	**106**	120	**134**	mV
	CS Bias Current	CS = 0V		-70	**-95**	µA
	Hiccup Mode Fault Timer			256		Cycles
RES						
I_{RES}	RES current Source			9.7		µA
V_{RES}	RES threshold	C_{RES} Charging	**1.20**	1.25	**1.30**	V
Diode Emulation						
V_{IL}	DEMB Input Low Threshold			2.0	**1.65**	V
V_{IH}	DEMB Input High Threshold		**2.9**	2.6		V
	DEMB Input Pull-Down Resistance			50		kΩ
	SW Zero Cross Threshold			-5		mV
LO Gate Driver						
V_{OLL}	LO Low-state Output Voltage	I_{LO} = 100mA		0.1	**0.18**	V
V_{OHL}	LO High-state Output Voltage	I_{LO} = -100mA, V_{OHL} = VCC - V_{LO}		0.17	**0.26**	V
	LO Rise Time	C-load = 1000pF		6		ns
	LO Fall Time	C-load = 1000pF		5		ns
I_{OHL}	Peak LO Source Current	V_{LO} = 0V		2.5		A
I_{OLL}	Peak LO Sink Current	V_{LO} = VCC		3.3		A
HO Gate Driver						
V_{OLH}	HO Low-state Output Voltage	I_{HO} = 100mA		0.11	**0.19**	V
V_{OHH}	HO High-state Output Voltage	I_{HO} = -100mA, V_{OHH} = V_{HB} - V_{HO}		0.18	**0.27**	V
	HO Rise Time	C-load = 1000pF		6		ns
	HO Fall Time	C-load = 1000pF		5		ns
I_{OHH}	Peak HO Source Current	V_{HO} = 0V, SW = 0, HB = 8V		2.2		A
I_{OLH}	Peak HO Sink Current	V_{HO} = V_{HB} = 8V		3.3		A
	HB to SW Under-voltage			3		V
	HB DC Bias Current	HB - SW = 8V		70	**100**	µA
SWITCHING CHARACTERISTICS						
	LO Fall to HO Rise Delay	No load		70		ns
	HO Fall to LO Rise Delay	No load		60		ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
THERMAL						
T_{SD}	Thermal Shutdown	Rising		165		°C
	Thermal Shutdown Hysteresis			25		°C
θ_{JA}	Junction to Ambient			40		°C/W
θ_{JC}	Junction to Case			4		°C/W

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics Table.

Note 2: These pins must not exceed VIN.

Note 3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

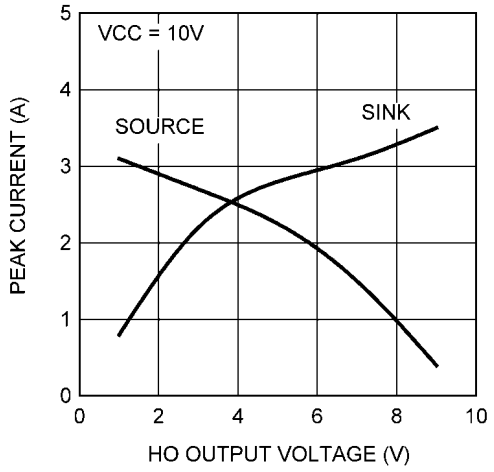
Note 4: All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production at T_A = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 5: Typical specifications represent the most likely parametric normal at 25°C operation.

Note 6: Per VCC Regulator

Typical Performance Characteristics

HO Peak Driver Current vs Output Voltage



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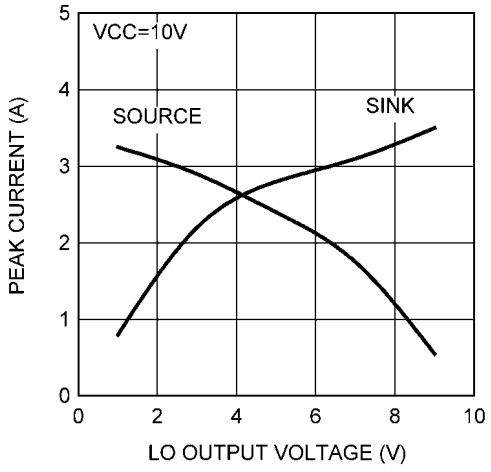
LO Peak Driver Current vs Output Voltage



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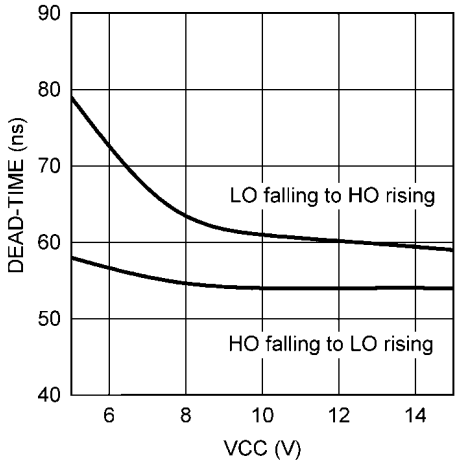
Driver Dead Time vs VCC



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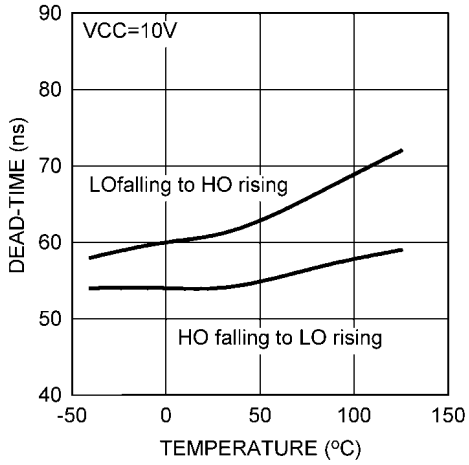
Driver Dead Time vs Temperature



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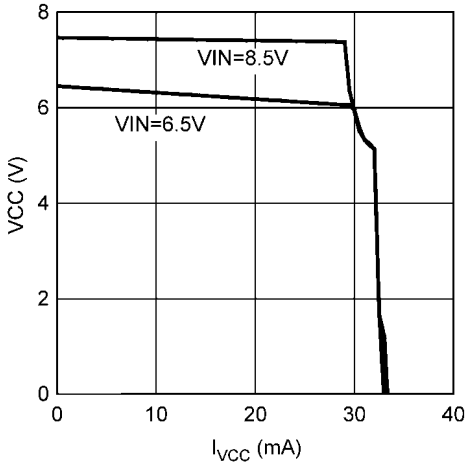
VCC vs I_{VCC}



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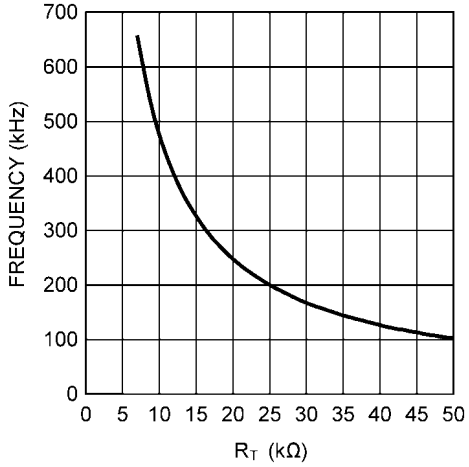
Switching Frequency vs R_T



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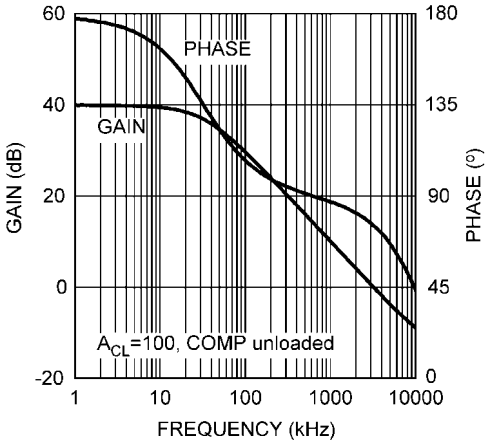
Error Amp Gain and Phase vs Frequency



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Block Diagram

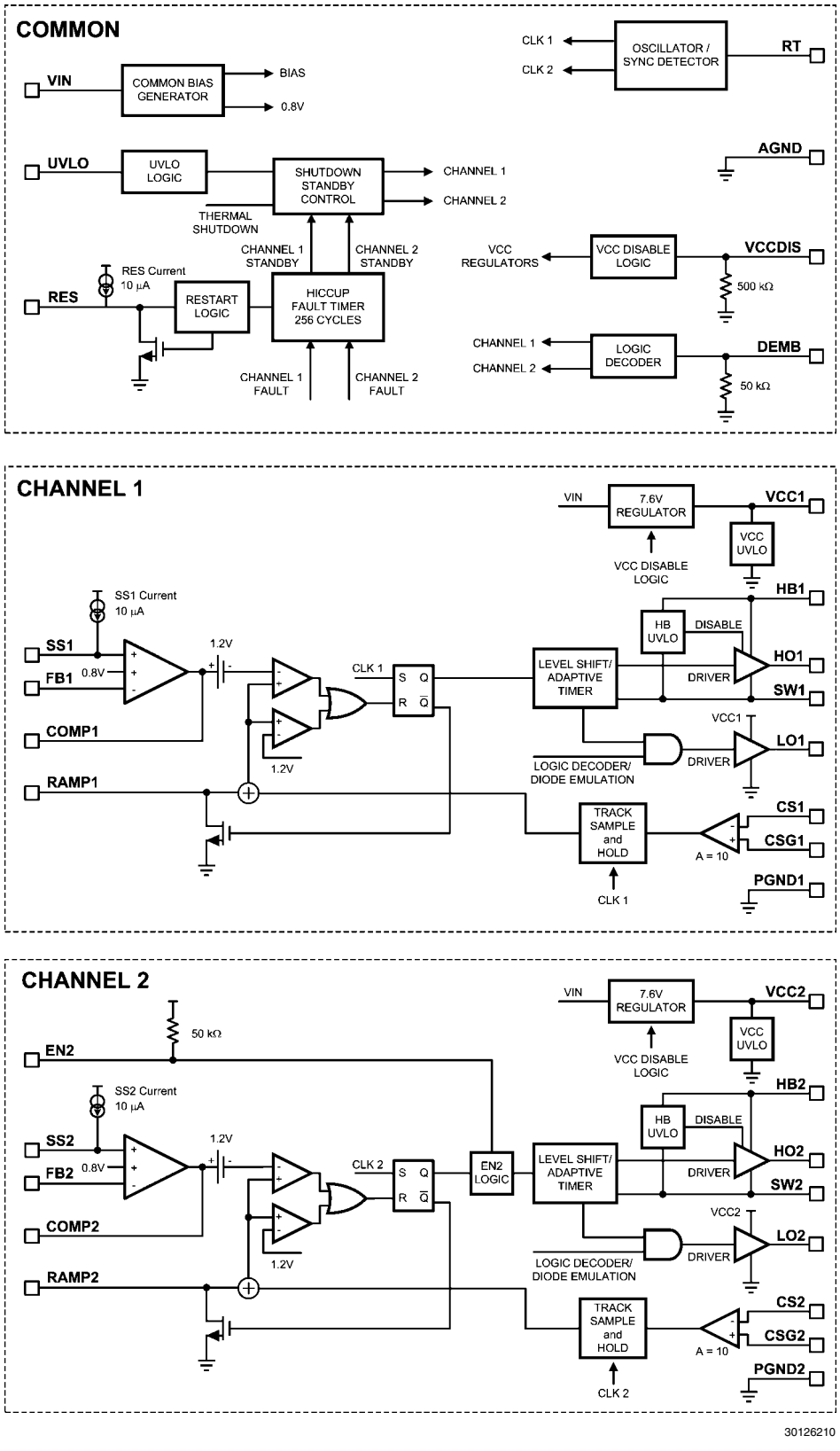


FIGURE 1. Block Diagram

Detailed Operating Description

The LM25119 high voltage switching regulator features all of the functions necessary to implement an efficient dual channel buck regulator that operates over a very wide input voltage range. The LM25119 may be configured as two independent regulators or as a single high current regulator with two interleaved channels. This easy to use regulator integrates high-side and low-side MOSFET drivers capable of supplying peak currents of 2.5 Amps (VCC=8V). The regulator control method is based on current mode control utilizing an emulated current ramp. Emulated peak current mode control provides inherent line feed-forward, cycle-by-cycle current limiting and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of the very small duty cycles necessary in high input voltage applications. The switching frequency is user programmable from 50kHz to 750kHz. An oscillator/synchronization pin allows the operating frequency to be set by a single resistor or synchronized to an external clock. An under-voltage lockout and channel2 enable pin allows either both regulators to be disabled or channel2 to be disabled with full operation of channel1. Fault protection features include current limiting, thermal shutdown and remote shutdown capability. The under-voltage lockout input enables both channels when the input voltage reaches a user selected threshold and provides a very low quiescent shutdown current when pulled low. The LLP32 package features an exposed pad to aid in thermal dissipation.

High Voltage Start-Up Regulator

The LM25119 contains two internal high voltage bias regulators, VCC1 and VCC2, that provide the bias supply for the PWM controllers and gate drive for the MOSFETs of each regulator channel. The input pin (VIN) can be connected directly to an input voltage source as high as 42 volts. The outputs of the VCC regulators are set to 7.6V. When the input voltage is below the VCC set-point level, the VCC output will track the VIN with a small dropout voltage. If VCC1 is in an under voltage condition, channel2 will be disabled. This interdependence is necessary to prevent channel2 from running open loop in the single output interleaved mode when the channel2 error amplifier is disabled (if either VCC is in UV, both channels are disabled).

The outputs of the VCC regulators are current limited at 25mA (minimum) output capability. Upon power-up, the regulators source current into the capacitors connected to the VCC pins. When the voltage at the VCC pins exceed 4.0V and the UVLO pin is greater than 1.25V, both channels are enabled and a soft-start sequence begins. Both channels remain enabled until either VCC pin falls below 3.8V, the UVLO pin falls below 1.25V or the die temperature exceeds the thermal limit threshold.

When operating at higher input voltages the bias power dissipation within the controller can be excessive. An output voltage derived bias supply can be applied to a VCC pins to reduce the IC power dissipation. The VCCDIS input can be used to disable the internal VCC regulators when external biasing is supplied. If VCCDIS >1.25V, the internal VCC regulators are disabled. The externally supplied bias should be coupled to the VCC pins through a diode, preferably a Schottky (low forward voltage). VCCDIS has a 500kΩ internal pull-down resistance to ground for normal operation with no external bias. The internal pull-down resistance can be overridden by pulling VCCDIS above 1.25V through a resistor divider connected to an external bias supply.

The VCC regulator series pass transistor includes a diode between VCC and VIN that should not be forward biased in normal operation.

If the external bias winding can supply VCC greater than VIN, an external blocking diode is required from the input power supply to the VIN pin to prevent the external bias supply from passing current to the input supply through the VCC pins. For VOUT between 5V and 14.5V, VOUT can be connected directly to VCC through a diode. For VOUT < 5V, a bias winding on the output inductor can be added as shown in *Figure 2*.

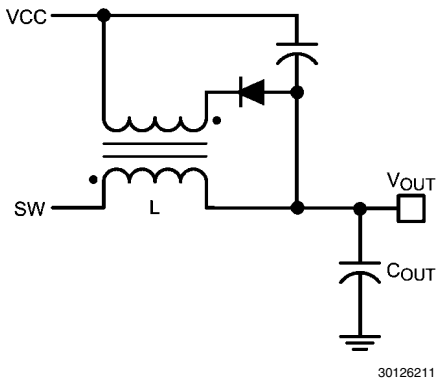


FIGURE 2. VCC Bias Supply with Additional Inductor Winding

In high voltage applications extra care should be taken to ensure the VIN pin does not exceed the absolute maximum voltage rating of 45V. During line or load transients, voltage ringing on the VIN line that exceeds the Absolute Maximum Rating can damage the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the VIN and AGND pins are essential.

UVLO

The LM25119 contains a dual level under-voltage lockout (UVLO) circuit. When the UVLO pin is less than 0.4V, the LM25119 is in shutdown mode. The shutdown comparator provides 100mV of hysteresis to avoid chatter during transitions. When the UVLO pin voltage is greater than 0.4V but less than 1.25V, the controller is in standby mode. In the standby mode the VCC bias regulators are active but the controller outputs are disabled. This feature allows the UVLO pin to be used as a remote enable/disable function. When the VCC outputs exceed their respective under-voltage thresholds (4V) and the UVLO pin voltage is greater than 1.25V, the outputs are enabled and normal operation begins.

An external set-point voltage divider from the VIN to GND is used to set the minimum VIN operating voltage of the regulator. The divider must be designed such that the voltage at the UVLO pin will be greater than 1.25V when the input voltage is in the desired operating range. UVLO hysteresis is accomplished with an internal 20µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO pin voltage exceeds 1.25V threshold, the current source is activated to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25V threshold, the current source is turned off causing the voltage at the UVLO pin to quickly fall. The UVLO pin should not be left floating.

Enable 2

The LM25119 contains an enable function allowing shutdown control of channel2, independent of channel1. If the EN2 pin is pulled below 2.0V, channel2 enters shutdown mode. If the EN2 input is greater than 2.5V, channel2 returns to normal operation. An internal 50kΩ pull-up resistor on the EN2 pin allows this pin to be left floating for normal operation. The EN2 input can be used in conjunction with the UVLO pin to sequence the two regulator channels. If EN2 is held low as the UVLO pin increases to a voltage greater than the 1.25V UVLO threshold, channel1 will begin operation while channel2 remains off. Both channels become operational when the UVLO, EN2, VCC1, and VCC2 pins are above their respective operating thresholds. Either channel of the LM25119 can also be disabled independently by pulling the corresponding SS pin to AGND.

Oscillator and Sync Capability

The LM25119 switching frequency is set by a single external resistor connected between the RT pin and the AGND pin (R_T). The resistor should be located very close to the device and connected directly to the pins of the IC (RT and AGND). To set a desired switching frequency (f_{SW}) of each channel, the resistor can be calculated from the following equation:

$$R_T = \frac{5.2 \times 10^9}{f_{SW}} - 948 \quad (1)$$

Where RT is in ohms and f_{SW} is in Hertz. The frequency f_{SW} is the output switching frequency of each channel. The internal oscillator runs at twice the switching frequency and an internal frequency divider interleaves the two channels with 180° phase shift between PWM pulses at the HO pins.

The RT pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC coupling a positive edge into the RT pin. The voltage at the RT pin is nominally 1.25V and the voltage at the RT pin must exceed 4V to trip the internal synchronization pulse detector. A 5V amplitude signal and 100pF coupling capacitor are recommended. Synchronizing at greater than twice the free-running frequency may result in abnormal behavior of the pulse width modulator. Also, note that the output switching frequency of each channel will be one-half the applied synchronization frequency.

Error Amplifiers and PWM Comparators

Each of the two internal high-gain error amplifiers generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference (0.8V). The output of each error amplifier is connected to the COMP pin allowing the user to provide loop compensation components. Generally a Type II network is recommended. This network creates a pole at 0Hz, a mid-band zero, and a noise reducing high frequency pole. The PWM comparator compares the emulated current sense signal from the RAMP generator to the error amplifier output voltage at the COMP pin. Only one error amplifier is required when configuring the controller as a two channel, single output interleaved regulator. For these applications, the channel1 error amplifier (FB1, COMP1) is configured as the master error amplifier. The channel2 error amplifier must be disabled by connecting the FB2 pin to the VCC2 pin. When configured in this manner the output of the channel2 error amplifier (COMP2) will be disabled and have a high output impedance. To complete the interleaved configuration the COMP1 and the COMP2 pins should be connected together to facilitate PWM control of channel2 and current sharing between channels.

Ramp Generator

The ramp signal used in the pulse width modulator for current mode control is typically derived directly from the buck switch current. This switch current corresponds to the positive slope portion of the inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics that must be filtered or blanked. Also, the current measurement may introduce significant propagation delays. The filtering, blanking time and propagation delay limit the minimum achievable pulse width. In applications where the input voltage may be relatively large in comparison to the output voltage, controlling small pulse widths and duty cycles are necessary for regulation. The LM25119 utilizes a unique ramp generator which does not actually measure the buck switch current but rather reconstructs the signal. Representing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements; a sample-and-hold DC level and the emulated inductor current ramp as shown in *Figure 3*.

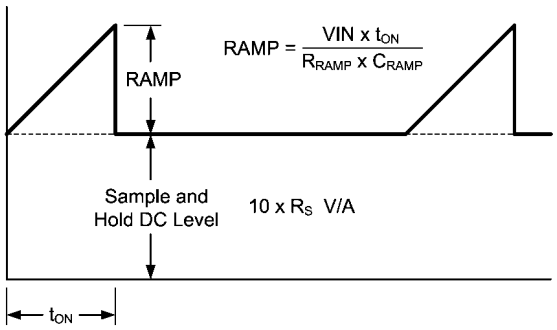


FIGURE 3. Composition of Current Sense Signal

The sample-and-hold DC level is derived from a measurement of the recirculating current flowing through the current sense resistor. The voltage across the sense resistor is sampled and held just prior to the onset of the next conduction interval of the buck switch. The current sensing and sample-and-hold provide the DC level of the reconstructed current signal. The positive slope inductor current ramp is emulated by an external capacitor connected from RAMP pin to AGND and a series resistor connected between SW and RAMP. The ramp resistor should not be connected to VIN directly because the RAMP pin voltage rating could be exceeded under high VIN conditions. The ramp created by the external resistor and capacitor will have a slope proportional to the rising inductor current plus some additional slope required for slope compensation. Connecting the RAMP pin resistor to SW provides optimum slope compensation with a RAMP capacitor slope that is proportional to VIN. This "adaptive slope compensation" eliminates the requirement for additional slope compensation circuitry with high output voltage set points and frees the user from additional concerns in this area. The emulated ramp signal is approximately linear and the ramp slope is given by:

$$\frac{dV_{RAMP}}{dt} = \frac{10 \times K \times V_{IN} \times R_S}{L} \quad (2)$$

The factor of 10 in equation (2) corresponds to the internal current sense amplifier gain of the LM25119. The K factor is a constant which adds additional slope for robust pulse-width modulation control at lower input voltages. In practice this constant can be varied from 1 to 3. R_S is the external sense resistor value.

The voltage on the ramp capacitor is given by:

$$V_{RAMP} = V_{IN} \times \left(1 - e^{\frac{t_{PERIOD}}{R_{RAMP} \times C_{RAMP}}}\right) \quad (3)$$

$$V_{RAMP} \approx \frac{V_{IN} \times t_{PERIOD}}{R_{RAMP} \times C_{RAMP}} \quad (4)$$

The approximation is the first order term in a Taylor Series expansion of the exponential and is valid since t_{PERIOD} is small relative to the RAMP pin R-C time constant.

Multiplying (2) by t_{PERIOD} to convert the slope to a peak voltage, and then equating (2) with (4) allows us to solve for C_{RAMP}:

$$C_{RAMP} = \frac{L}{10 \times R_S \times K \times R_{RAMP}} \quad (5)$$

Choose either C_{RAMP} or R_{RAMP} and use (5) to calculate the other component.

The difference between the average inductor current and the DC value of the sampled inductor current can cause instability for certain operating conditions. This instability is known as sub-harmonic oscillation, which occurs when the inductor ripple current does not return to its initial value by the start of next switching cycle. Sub-harmonic oscillation is normally characterized by alternating wide and narrow pulses at the switch node. The ramp equation above contains the optimum amount of slope compensation, however extra slope compensation is easily added by selecting a lower value for R_{RAMP} or C_{RAMP}.

Current Limit

The LM25119 contains a current limit monitoring scheme to protect the regulator from possible over-current conditions. When set correctly, the emulated current signal is proportional to the buck switch current with a scale factor determined by the current limit sense resistor, R_S, and current sense amplifier gain. The emulated signal is applied to the current limit comparator. If the emulated ramp signal exceeds 1.2V, the present cycle is terminated (cycle-by-cycle current limiting). Shown in *Figure 4* is the current limit comparator and a simplified current measurement schematic. In applications with small output inductance and high input voltage, the switch current may overshoot due to the propagation delay of the current limit comparator. If an overshoot should occur, the sample-and-hold circuit will detect the excess recirculating current before the buck switch is turned on again. If the sample-and-hold DC level exceeds the internal current limit threshold, the buck switch will be disabled and skip pulses until the current has decayed below the current limit threshold. This approach prevents current runaway conditions due to propagation delays or inductor saturation since the inductor current is forced to decay to a controlled level following any current overshoot.

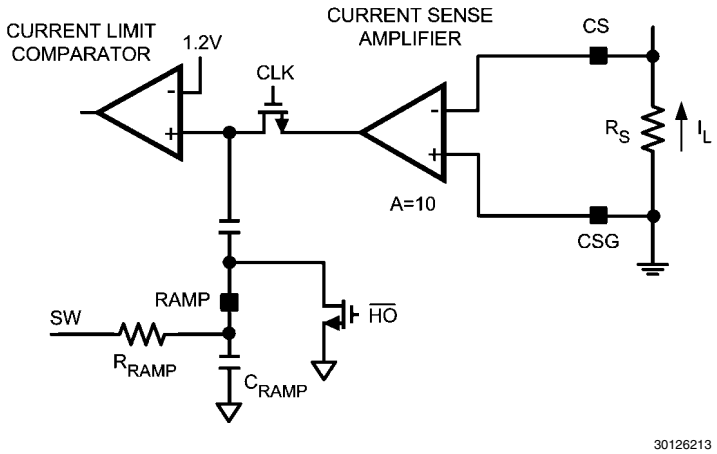


FIGURE 4. Current Limit and Ramp Circuit

Hiccup Mode Current Limiting

To further protect the regulator during prolonged current limit conditions, an internal counter counts the PWM clock cycles during which cycle-by-cycle current limiting occurs. When the counter detects 256 consecutive cycles of current limiting, the regulator enters a low power dissipation hiccup mode with the HO and LO outputs disabled. The restart timer pin, RES, and an external capacitor configure the hiccup mode current limiting. A capacitor on the RES pin (C_{RES}) determines the time the controller will remain in low power standby mode before automatically restarting. A 10µA current source charges the RES pin capacitor to the 1.25V threshold which restarts the overloaded channel. The two regulator channels operate independently. One channel may operate normally while the other is in the hiccup mode overload protection. The hiccup mode commences when either channel experiences 256 consecutive PWM cycles with cycle-by-cycle current limiting. If that occurs, the overloaded channel will turn off and remain off for the duration of the RES pin timer.

The hiccup mode current limiting function can be disabled. The RES configuration is latched during initial power-up when UVLO is above 1.25V and VCC1 and VCC2 are above their UV thresholds, determining hiccup or non-hiccup current limiting. If the RES pin is tied to VCC at initial power-on, hiccup current limit is disabled.

Soft-Start

The soft-start feature allows the regulator to gradually reach the steady state operating point, thus reducing start-up stresses and surges. The LM25119 will regulate the FB pin to the SS pin voltage or the internal 0.8V reference, whichever is lower. At the beginning of the soft-start sequence when SS = 0V, the internal 10µA soft-start current source gradually increases the voltage on an external soft-start capacitor (C_{SS}) connected to the SS pin resulting in a gradual rise of the FB and output voltages.

Either regulator channel of the LM25119 can be disabled by pulling the corresponding SS pin to AGND.

Diode Emulation

A fully synchronous buck regulator implemented with a free-wheel MOSFET rather than a diode has the capability to sink current from the output in certain conditions such as light load, over-voltage or pre-bias startup. The LM25119 provides a diode emulation feature that can be enabled to prevent reverse (drain to source) current flow in the low side free-wheel MOSFET. When configured for diode emulation, the low side MOSFET is disabled when reverse current flow is detected. The benefit of this configuration is lower power loss at no load or light load conditions and the ability to turn on into a pre-biased output without discharging the output. The diode emulation mode allows for start-up into pre-biased loads, since it prevents reverse current flow as the soft-start capacitor charges to the regulation level during startup. The negative effect of diode emulation is degraded light load transient response times. Enabling the diode emulation feature is recommended and allows discontinuous conduction operation. The diode emulation feature is configured with the DEMB pin. To enable diode emulation, connect the DEMB pin to ground or leave the pin floating. If continuous conduction operation is desired, the DEMB pin should be tied to either VCC1 or VCC2.

HO and LO Output Drivers

The LM25119 contains a high current, high-side driver and associated high voltage level shift to drive the buck switch of each regulator channel. This gate driver circuit works in conjunction with an external diode and bootstrap capacitor. A 0.1µF or larger ceramic capacitor, connected with short traces between the HB pin and SW pin, is recommended. During the off-time of the high-side MOSFET, the SW pin voltage is approximately 0V and the bootstrap capacitor charges from VCC through the external bootstrap diode. When operating with a high PWM duty cycle, the buck switch will be forced off each cycle for 320ns to ensure that the bootstrap capacitor is recharged.

The LO and HO outputs are controlled with an adaptive dead-time methodology which insures that both outputs are never enabled at the same time. When the controller commands HO to be enabled, the adaptive dead-time logic first disables LO and waits for the LO voltage to drop. HO is then enabled after a small delay. Similarly, the LO turn-on is disabled until the HO voltage has discharged. This methodology insures adequate dead-time for any size MOSFET.

Care should be exercised in selecting an output MOSFET with the appropriate threshold voltage, especially if VCC is supplied from the regulator output. During startup at low input voltages the MOSFET threshold should be lower than the 4V VCC under-voltage lockout threshold. Otherwise, there may be insufficient VCC voltage to completely turn on the MOSFET as VCC under-voltage lockout is released during startup. If the buck switch MOSFET gate drive is not sufficient, the regulator may not start or it may hang up momentarily in a high power dissipation state. This condition can be avoided by selecting a MOSFET with a lower threshold voltage or if VCC is supplied from an external source higher than the output voltage. If the minimum input voltage programmed by the UVLO pin resistor divider is above the VCC regulation level, this precaution is of no concern.

Maximum Duty Cycle

When operating with a high PWM duty cycle, the buck switch will be forced off each cycle for 320ns to ensure the boot-strap capacitor is recharged and to allow time to sample and hold the current in the low side MOSFET. This forced off-time limits the maximum duty cycle of the controller. When designing a regulator with high switching frequency and high duty cycle requirements, a check should be made of the required maximum duty cycle (including losses) against the graph shown in *Figure 5*.

The actual maximum duty cycle will vary with the operating frequency as follows:

$$D_{MAX} = 1 - f_{SW} \times 320 \times 10^{-9} \quad (6)$$

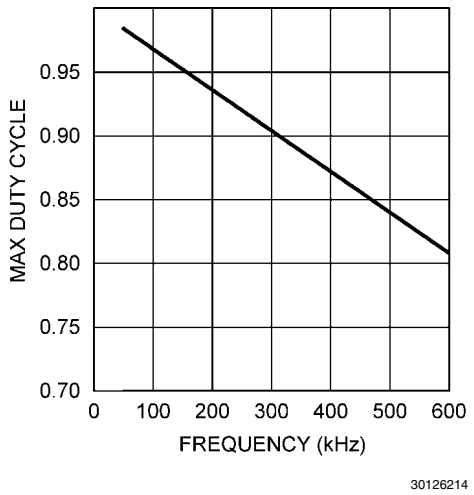


FIGURE 5. Maximum Duty Cycle vs Switching Frequency

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the output driver and the VCC bias regulators. This feature is designed to prevent catastrophic failures from overheating and destroying the device.

Application Information

EXTERNAL COMPONENTS

The procedure for calculating the external components is illustrated with the following design example. Only the values for the 3.3V output are calculated since the procedure is the same for the 1.8V output. The circuit shown in *Figure 14* is configured for the following specifications:

- CH1 output voltage, V_{OUT1} = 3.3V
- CH2 output voltage, V_{OUT2} = 1.8V
- CH1 maximum load current, I_{OUT1} = 8A
- CH2 maximum load current, I_{OUT2} = 8A
- Minimum input voltage, $V_{IN(MIN)}$ = 6V
- Maximum input voltage, $V_{IN(MAX)}$ = 36V
- Switching frequency, f_{SW} = 230kHz

Some component values were chosen as a compromise between the 3.3V and 1.8V outputs to allow identical components to be used on both outputs. This design can be reconfigured in a dual-channel interleaved configuration with a single 3.3V output which requires identical power channels.

TIMING RESISTOR

R_T sets the switching frequency of each regulator channel. Generally, higher frequency applications are smaller but have higher losses. Operation at 230kHz was selected for this example as a reasonable compromise between small size and high efficiency. The value of R_T for 230kHz switching frequency can be calculated as follows:

$$R_T = \frac{5.2 \times 10^9}{f_{SW}} - 948 = 21.66\ k\Omega \quad (7)$$

A standard value or 22.1kΩ was chosen for R_T. The internal oscillator frequency is twice the switching frequency and is about 460kHz.

OUTPUT INDUCTOR

The inductor value is determined based on the operating frequency, load current, ripple current and the input and output voltages.

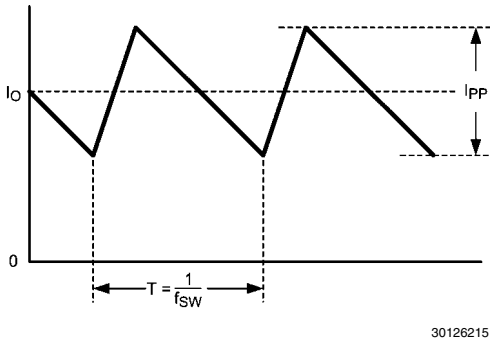


FIGURE 6. Inductor Current

Knowing the switching frequency, maximum ripple current (I_{PP}), maximum input voltage and the nominal output voltage (V_{OUT}), the inductor value can be calculated:

$$L = \frac{V_{OUT}}{I_{PP} \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (8)$$

The maximum ripple current occurs at the maximum input voltage. Typically, I_{PP} is 20% to 40% of the full load current. When operating in the diode emulation mode configuration, the maximum ripple current should be less than twice the minimum load current. For full synchronous operation, higher ripple current is acceptable. Higher ripple current allows for a smaller inductor size, but places more of a burden on the output capacitor to smooth the ripple current. For this example, a ripple current of 25% of 8A was chosen as a compromise for the 1.8V output.

$$L = \frac{3.3V}{0.25 \times 8A \times 230\ kHz} \times \left(1 - \frac{3.3V}{36V}\right) = 6.5\ \mu H \quad (9)$$

The nearest standard value of 6.8µH was chosen for L. Using the value of 6.8µH for L, calculate I_{PP} again. This step is necessary if the chosen value of L differs significantly from the calculated value.

$$I_{PP} = \frac{V_{OUT}}{L \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (10)$$

$$I_{PP} = \frac{3.3V}{6.8\ \mu H \times 230\ kHz} \times \left(1 - \frac{3.3V}{36V}\right) = 1.92A \quad (11)$$

CURRENT SENSE RESISTOR

Before determining the value of current sense resistor (R_S), it is valuable to understand the K factor, which is the ramp slope multiple chosen for slope compensation. The K factor can be varied from 1 to 3 in practice and is defined as:

$$K = \frac{L}{10 \times R_S \times R_{RAMP} \times C_{RAMP}} \quad (12)$$

The performance of the converter will vary depending on the selected K value (See *Table 1*). For this example, 3 was chosen as the K factor to minimize the power loss in sense resistor R_S and the cross-talk between channels. Crosstalk between the two regulators under certain conditions may be observed on the output as switch jitter.

The maximum output current capability ($I_{OUT(MAX)}$) should be 20~50% higher than the required output current, (8A at V_{OUT1}) to account for tolerances and ripple current. For this example, 130% of 8A was chosen (10.4A). The current sense resistor value can be calculated as:

$$R_S = \frac{V_{CS(TH)}}{I_{OUT(MAX)} + \frac{V_{OUT} \times K}{f_{SW} \times L} - \frac{I_{PP}}{2}} \quad (13)$$

$$R_S = \frac{0.12}{10.4A + \frac{3.3V \times 3}{230\ kHz \times 6.8\ \mu H} - \frac{1.92A}{2}} = 0.0076 \quad (14)$$

Where $V_{CS(TH)}$ is the current limit threshold voltage (120mV). A value of 8mΩ was chosen for R_S. The sense resistor must be rated to handle the power dissipation at maximum input voltage when current flows through the free-wheel MOSFET for the majority of the PWM cycle. The maximum power dissipation of R_S can be calculated:

$$P_{RS} = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) I_{OUT}^2 R_S \quad (15)$$

$$P_{RS} = \left(1 - \frac{3.3V}{36V}\right) \times 8^2 \times 0.008 = 0.46W \quad (16)$$

During output short condition, the worst case peak inductor current is limited to:

$$I_{LIM\_PEAK} = \frac{V_{CS(TH)}}{R_S} + \frac{V_{IN(MAX)} t_{ON(MIN)}}{L} \quad (17)$$

$$I_{LIM\_PEAK} = \frac{0.12}{0.008\Omega} + \frac{36V \times 100\ ns}{6.8\ \mu H} = 15.53A \quad (18)$$

Where $t_{ON(MIN)}$ is the minimum HO on-time which is nominally 100ns. The chosen inductor must be evaluated for this condition, especially at elevated temperature where the saturation current rating of the inductor may drop significantly. At the maximum input voltage with a shorted output, the valley current must fall below $V_{CS(TH)} / R_S$ before the high-side MOSFET is allowed to turn on.

RAMP RESISTOR AND RAMP CAPACITOR

The value of ramp capacitor (C_{RAMP}) should be less than 2nF to allow full discharge between cycles by the discharge switch internal to the LM25119. A good quality, thermally stable ceramic capacitor with 5% or less tolerance is recommended. For this design the value of C_{RAMP} was set at the standard capacitor value of 820pF. With the inductor, sense resistor and the K factor selected, the value of the ramp resistor (R_{RAMP}) can be calculated as:

$$R_{RAMP} = \frac{L}{10 \times R_S \times K \times C_{RAMP}} \quad (19)$$

$$R_{RAMP} = \frac{6.8\ \mu H}{10 \times 0.008\Omega \times 3 \times 820\ pF} = 34.5\ k\Omega \quad (20)$$

The standard value of 34kΩ was selected.

OUTPUT CAPACITORS

The output capacitors smooth the inductor ripple current and provide a source of charge during transient loading conditions. For this design example, a 680µF electrolytic capacitor with 10mΩ ESR was selected as the main output capacitor. The fundamental component of the output ripple voltage is approximated as:

$$\Delta V_{OUT} = I_{PP} \times \sqrt{ESR^2 + \left(\frac{1}{8 \times f_{SW} \times C_{OUT}}\right)^2} \quad (21)$$

$$\Delta V_{OUT} = 1.92A \times \sqrt{0.01\Omega^2 + \left(\frac{1}{8 \times 230\ kHz \times 680\ \mu F}\right)^2} \quad (22)$$

$$\Delta V_{OUT} = 19.3\ mV \quad (23)$$

Two 22µF low ERS / ESL ceramic capacitors are placed in parallel with the 680µF electrolytic capacitor, to further reduce the output voltage ripple and spikes.

TABLE 1. Performance Variation by K Factor

	K < 1	1 <— K —> 3		K > 3
Cross Talk	Sub-harmonic oscillation may occur	Higher	Lower	Introduces additional pole near cross-over frequency
Peak Inductor Current with Short Output Condition		Lower	Higher	
Inductor Size		Smaller	Larger	
Power Dissipation of Rs		Higher	Lower	
Efficiency		Lower	Higher	

INPUT CAPACITORS

The regulator input supply voltage typically has high source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. When the buck switch turns on, the current into the buck switch steps to the valley of the inductor current waveform, ramps up to the peak value, and then drops to the zero at turn-off. The input capacitance should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating necessary is $I_{RMS} > I_{OUT} / 2$. Seven 2.2µF ceramic capacitors were used for each channel. With ceramic capacitors, the input ripple voltage will be triangular. The input ripple voltage with one channel operating is approximately:

$$\Delta V_{IN} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}} \quad (24)$$

$$\Delta V_{IN} = \frac{8A}{4 \times 230\ kHz \times 15.4\ \mu F} = 0.565V \quad (25)$$

The ripple voltage of the input capacitors will be reduced significantly with dual channel operation since each channel operates 180 degrees out of phase from the other. Capacitors connected in parallel should be evaluated for RMS current rating. The current will split between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

When the converter is connected to an input power source, a resonant circuit is formed by the line inductance and the input capacitors. To minimize overshoot make $C_{IN} > 10 \times L_{IN}$. The characteristic source impedance (Z_S) and resonant frequency (f_S) are:

$$Z_S = \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (26)$$

$$f_S = \frac{1}{2\pi\sqrt{L_{IN} \times C_{IN}}} \quad (27)$$

Where L_{IN} is the inductance of the input wire. The converter exhibits negative input impedance which is lowest at the minimum input voltage:

$$Z_{IN} = \frac{V_{IN}^2}{P_{OUT}} \quad (28)$$

The damping factor for the input filter is given by:

$$\delta = \frac{1}{2} \times \left(\frac{R_{IN} + ESR}{Z_S} + \frac{Z_S}{Z_{IN}} \right) \quad (29)$$

Where R_{IN} is the input wiring resistance and ESR is the equivalent series resistance of the input capacitors. When $\delta = 1$, the input filter is critically damped. This may be difficult to achieve with practical component values. With $\delta < 0.2$, the input filter will exhibit significant ringing. If δ is zero or negative, there is not enough resistance in the circuit and the input filter will sustain an oscillation. When operating near the minimum input voltage, a bulk aluminum electrolytic capacitor across C_{IN} may be needed to damp the input for a typical bench test setup.

VCC CAPACITOR

The primary purpose of the VCC capacitor (C_{VCC}) is to supply the peak transient currents of the LO driver and bootstrap diode as well as provide stability for the VCC regulator. These peak currents can be several amperes. The recommended value of C_{VCC} should be no smaller than 0.47µF, and should be a good quality, low ESR, ceramic capacitor located at the pins of the IC to minimize potentially damaging voltage transients caused by trace inductance. A value of 1µF was selected for this design.

BOOTSTRAP CAPACITOR

The bootstrap capacitor between the HB and SW pins supplies the gate current to charge the high-side MOSFET gate at each cycle's turn-on and recovery charge for the bootstrap diode. These current peaks can be several amperes. The recommended value of the bootstrap capacitor is at least 0.1µF, and should be a good quality, low ESR, ceramic capacitor located at the pins of the IC to minimize potentially damaging voltage transients caused by trace inductance. The absolute minimum value for the bootstrap capacitor is calculated as:

$$C_{HB} \geq \frac{Q_g}{\Delta V_{HB}} \quad (30)$$

Q_g is the high-side MOSFET gate charge and ΔV_{HB} is the tolerable voltage droop on C_{HB}, which is typically less than 5% of VCC. A value of 0.47µF was selected for this design.

SOFT START CAPACITOR

The capacitor at the SS pin (C_{SS}) determines the soft-start time (t_{SS}), which is the time for the output voltage to reach the final regulated value. The value of C_{SS} for a given time is determined from:

$$C_{SS} = \frac{t_{SS} \times 10\ \mu A}{0.8V} \quad (31)$$

For this application, a value of 0.047µF was chosen for a soft-start time of 3.8ms.

RESTART CAPACITOR

The restart pin sources 10µA into the external restart capacitor (C_{RES}). The value of the restart capacitor is given by:

$$C_{RES} = \frac{10\ \mu A \times t_{RES}}{1.25V} \quad (32)$$

Where t_{RES} is the time the LM25119 remains off before a restart attempt in hiccup mode current limiting. For this application, a value of 0.47µF was chosen for a restart time of 59ms.

OUTPUT VOLTAGE DIVIDER

R_{FB1} and R_{FB2} set the output voltage level, the ratio of these resistors is calculated from:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{0.8V} - 1 \quad (33)$$

2.21kΩ was chosen for R_{FB1} in this design which results in a R_{FB2} value of 6.98kΩ for V_{OUT1} of 3.3V. A reasonable guide is to select the value of R_{FB1} in the range between 500Ω and 10kΩ. The value of R_{FB1} should be large enough to keep the total divider power dissipation small.

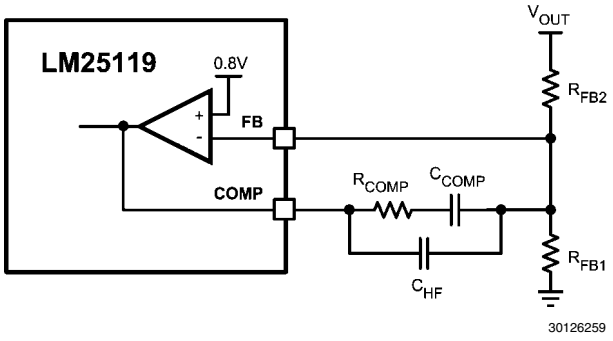


FIGURE 7. Feedback Configuration

UVLO DIVIDER

The UVLO threshold is internally set to 1.25V at the UVLO pin. The LM25119 is enabled when the system input voltage VIN causes the UVLO pin to exceed the threshold voltage of 1.25V. When the UVLO pin voltage is below the threshold, the internal 20µA current source is disabled. When the UVLO pin voltage exceeds the 1.25V threshold, the 20µA current source is enabled causing the UVLO pin voltage to increase, providing hysteresis. The values of R_{UV1} and R_{UV2} can be determined from the following equation:

$$R_{UV2} = \frac{V_{HYS}}{20\ \mu A} \quad (34)$$

$$R_{UV1} = \frac{1.25V \times R_{UV2}}{VIN - 1.25} \quad (35)$$

V_{HYS} is the desired UVLO hysteresis at VIN, and VIN in the second equation is the desired UVLO release (turn-on) voltage. For example, if it is desired for the LM25119 to be enabled when VIN reaches 5.6V, and the desired hysteresis is 1.05V, then R_{UV2} should be set to 52.5kΩ and R_{UV1} should be set to 15.1kΩ. For this application R_{UV2} was selected to be 52.3kΩ, $R_{UV1}$was selected to be 15kΩ. The LM25119 can be remotely shutdown by taking the UVLO pin below 0.4V with an external open collector or open drain device. The outputs and the VCC regulator are disabled in shutdown mode. Capacitor C_{FT} provides filtering for the divider. A value of 100pF was chosen for C_{FT}. The voltage at the UVLO pin should never exceed 15V when using the external set-point divider. It may be necessary to clamp the UVLO pin at high input voltages.

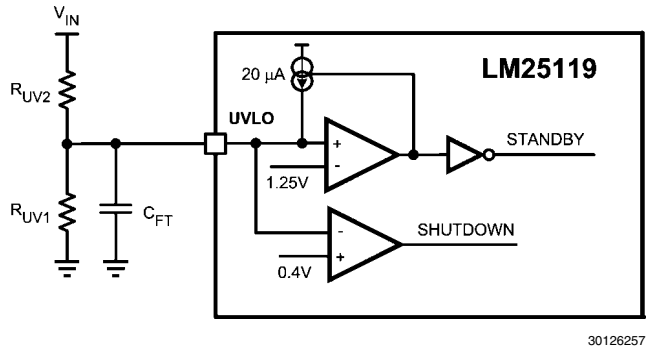


FIGURE 8. UVLO Configuration

MOSFET SELECTION

Selection of the power MOSFETs is governed by the same tradeoffs as switching frequency. Breaking down the losses in the high-side and low-side MOSFETs is one way to compare the relative efficiencies of different devices. When using discrete SO-8 MOSFETs, generally the output current capability range is 2A to 10A. Losses in the power MOSFETs can be broken down into conduction loss, gate charging loss, and switching loss. Conduction loss P_{DC} is approximately:

$$P_{DC\ (HO\text{-}MOSFET)} = D \times (I_O^2 \times R_{DS(ON)} \times 1.3) \quad (36)$$

$$P_{DC\ (LO\text{-}MOSFET)} = (1 - D) \times (I_O^2 \times R_{DS(ON)} \times 1.3) \quad (37)$$

Where, D is the duty cycle and the factor of 1.3 accounts for the increase in MOSFET on-resistance due to heating. Alternatively, the factor of 1.3 can be eliminated and the high temperature on-resistance of the MOSFET can be estimated using the $R_{DS(ON)}$ vs Temperature curves in the MOSFET datasheet. Gate charging loss, P_{GC}, results from the current driving the gate capacitance of the power MOSFETs and is approximated as:

$$P_{GC} = n \times VCC \times Qg \times f_{SW} \quad (38)$$

Where Q_g refers to the total gate charge of an individual MOSFET, and 'n' is the number of MOSFETs. Gate charge loss differs from conduction and switching losses in that the actual dissipation occurs in the LM25119 and not in the MOSFET itself. Further loss in the LM25119 is incurred if the gate driving current is supplied by the internal linear regulator.

Switching loss occurs during the brief transition period as the MOSFET turns on and off. During the transition period both current and voltage are present in the channel of the MOSFET. The switching loss can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_O \times (t_R + t_F) \times f_{SW} \quad (39)$$

Where t_R and t_F are the rise and fall times of the MOSFET. The rise and fall times are usually mentioned in the MOSFET datasheet or can be empirically observed with an oscilloscope. Switching loss is calculated for the high-side MOSFET only. Switching loss in the low-side MOSFET is negligible because the body diode of the low-side MOSFET turns on before the MOSFET itself, minimizing the voltage from drain to source before turn-on. For this example, the maximum drain-to-source voltage applied to either MOSFET is 36V.The selected MOSFETs must be able to withstand 36V plus any ringing from drain to source, and be able to handle at least the VCC voltage plus any ringing from gate to source. A good choice of MOSFET for the 36V input design example is the SI7884. It has an $R_{DS(ON)}$ of 7.5mΩ and total gate charge of 21nC. In applications where a high step-down ratio is maintained in normal operation, efficiency may be optimized by choosing a high-side MOSFET with lower Q_g, and low-side MOSFET with lower $R_{DS(ON)}$.

MOSFET SNUBBER

A resistor-capacitor snubber network across the low-side MOSFET reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and couple noise to the output. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. Start with a resistor value between 5 and 50Ω. Increasing the value of the snubber capacitor results in more damping, but higher snubber losses. Select a minimum value for the snubber capacitor that provides adequate damping of

the spikes on the switch waveform at high load. A snubber may not be necessary with an optimized layout.

ERROR AMPLIFIER COMPENSATION

R_{COMP}, C_{COMP} and C_{HF} configure the error amplifier gain characteristics to accomplish a stable voltage loop gain. One advantage of current mode control is the ability to close the loop with only two feedback components, R_{COMP} and C_{COMP}. The voltage loop gain is the product of the modulator gain and the error amplifier gain. For the 3.3V output design example, the modulator is treated as an ideal voltage-to-current converter. The DC modulator gain of the LM25119 can be modeled as:

$$DC\_GAIN_{(MOD)} = \frac{R_{LOAD}}{(A \times R_S)} \quad (40)$$

Note that A is the gain of the current sense amplifier which is 10 in the LM25119. The dominant low frequency pole of the modulator is determined by the load resistance (R_{LOAD}) and output capacitance (C_{OUT}). The corner frequency of this pole is:

$$f_{P(MOD)} = \frac{1}{(2\pi \times R_{LOAD} \times C_{OUT})} \quad (41)$$

For R_{LOAD} = 3.3V / 8A = 0.413Ω and C_{OUT} = 724µF (effective) then $f_{P(MOD)}$ = 532Hz

DC $Gain_{(MOD)}$ = 0.413Ω / (10 x 8mΩ) = 5.16 = 14.2dB

For the 3.3V design example, the modulator gain vs. frequency characteristic is shown in *Figure 9*.

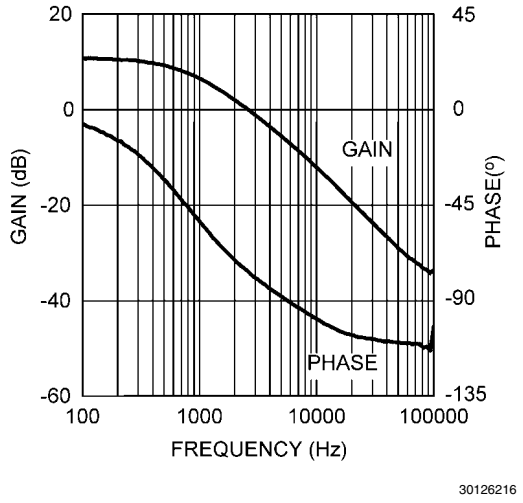


FIGURE 9. Modulator Gain and Phase

Components R_{COMP} and C_{COMP} configure the error amplifier as a Type II configuration. The DC gain of the amplifier is 80dB with a pole at 0Hz and a zero at f_{ZEA} = 1 / (2π x R_{COMP} x C_{COMP}). The error amplifier zero cancels the modulator pole leaving a single pole response at the crossover frequency of the voltage loop. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin. For the design example, a conservative target loop bandwidth (crossover frequency) of 11kHz was selected. The compensation network zero (f_{ZEA}) should be selected at least an order of magnitude less than the target crossover frequency. This constrains the product of R_{COMP} and C_{COMP} for a desired compensation network zero 1 / (2π x R_{COMP} x C_{COMP}) to be about 1.1kHz. Increasing R_{COMP}, while proportionally decreasing C_{COMP}, increases the error amp gain. Conversely, decreasing R_{COMP} while proportionally increasing C_{COMP}, decreases the error amp gain. For the design example C_{COMP} was selected as 6800pF and R_{COMP} was selected as 36.5kΩ. These values configure the compensation network zero at 640Hz. The error amp gain at frequencies greater than f_{ZEA} is: R_{COMP} / R_{FB2}, which is approximately 5.22 (14.3dB).

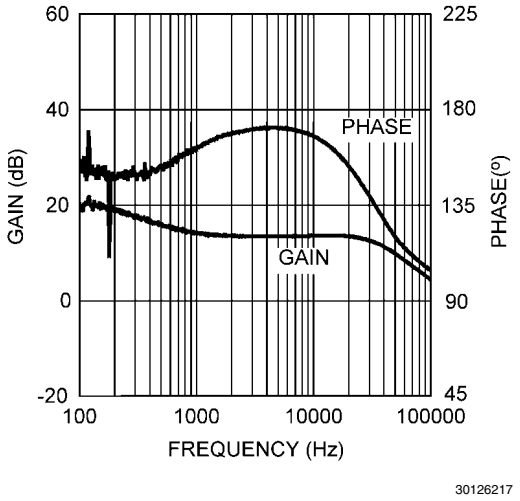


FIGURE 10. Error Amplifier Gain and Phase

The overall voltage loop gain can be predicted as the sum (in dB) of the modulator gain and the error amp gain.

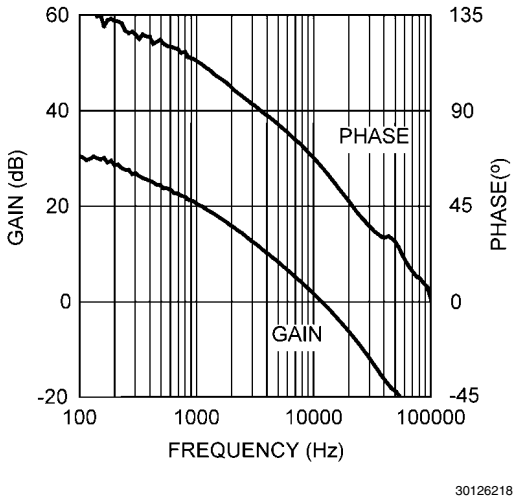


FIGURE 11. Overall Voltage Loop Gain and Phase

If a network analyzer is available, the modulator gain can be measured and the error amplifier gain can be configured for the desired loop transfer function. If the K factor is between 2 and 3, the stability should be checked with the network analyzer. If a network analyzer is not available, the error amplifier compensation components can be designed with the guidelines given. Step load transient tests can be performed to verify acceptable performance. The step load goal is minimum overshoot with a damped response. C_{HF} can be added to the compensation network to decrease noise susceptibility of the error amplifier. The value of C_{HF} must be sufficiently small since the addition of this capacitor adds a pole in the

error amplifier transfer function. This pole must be well beyond the loop crossover frequency. A good approximation of the location of the pole added by C_{HF} is: $f_{P2} = f_{ZEA} \times C_{COMP} / C_{HF}$. The value of C_{HF} was selected as 100pF for the design example.

Miscellaneous Functions

EN2 is left floating which allows channel2 to always remain enabled. If EN2 is pulled below 2V, channel2 is disabled.

The DEMB pin is left floating since this design uses diode emulation. For fully synchronous (continuous conduction) operation, connect the DEMB to a voltage greater than 2.6V.

VCCDIS is left floating to enable the internal VCC regulators. To disable the internal VCC regulators, connect this pin to a voltage greater than 1.25V.

Interleaved Operation

Interleaved operation can offer many advantages in single output, high current applications. The output power path is split between two identical channels reducing the current in each channel by one-half. Ripple current reduction in the output capacitors is reduced significantly since each channel operates 180 degrees out of phase from the other. Ripple reduction is greatest at 50% duty cycle and decreases as the duty cycle varies away from 50%.

Refer to *Figure 12* to estimate the ripple current reduction. Also, the effective ripple in the input and output capacitors occurs at twice the frequency of a single channel design due to the combining of the two channels. All of these factors are advantageous in managing the higher currents and their effects in a high power design.

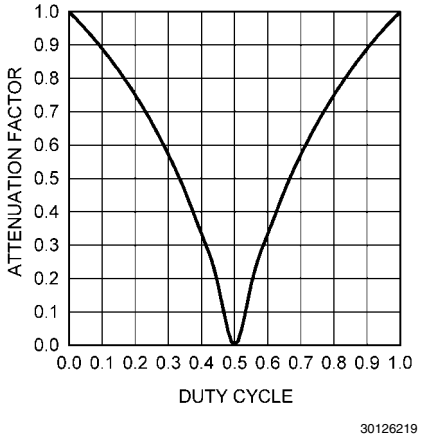


FIGURE 12. Cancellation Factor vs. Duty Cycle for Output Capacitor

To begin an interleaved design, use the previous equations in this datasheet to first calculate the required value of components using one-half the current in the output power path. The Attenuation Factor in *Figure 12* is the ratio of the output capacitor ripple to the inductor ripple vs. duty cycle. The inductor ripple used in this calculation is the ripple in either inductor in a two phase design, not the ripple calculated for a single phase design of the same output power. It can be observed that operation around 50% duty cycle results in almost complete ripple attenuation in the output capacitor. *Figure 12* can be used to calculate the amount of ripple attenuation in the output capacitors.

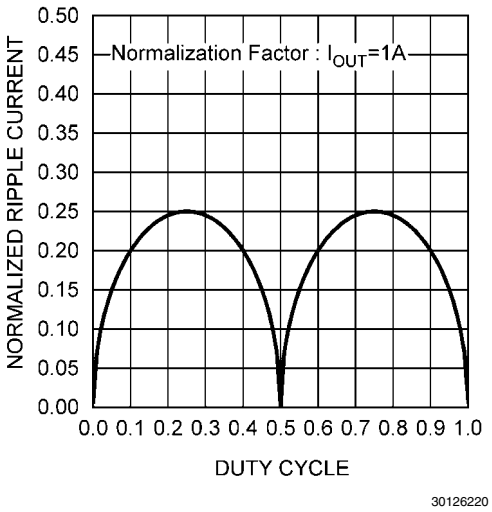


FIGURE 13. Normalized Input Capacitor RMS Ripple Current vs. Duty Cycle

Figure 13 illustrates the ripple current reduction in the input capacitors due to interleaving. As with the output capacitors, there is near perfect ripple reduction near 50% duty cycle. This plot can be used to calculate the ripple in the input capacitors at any duty cycle. In designs with large duty cycle swings, use the worst case ripple reduction for the design.

To configure the LM25119 for interleaved operation, connect COMP1 and COMP2 pins together at the IC. Connecting the FB2 pin to VCC2 pin will disable the channel2 error amplifier with a high output impedance at COMP2. Connect the compensation network between FB1 and the common COMP pins. Connect the two power stages together at the output capacitors. Finally use the plots in *Figure 12* and *Figure 13* along with the duty cycle range to determine the amount of output and input capacitor ripple reduction. Frequently more capacitance than necessary is used in a design just to meet ESR requirements. Reducing the capacitance based solely on ripple reduction graphs alone may violate this requirement.

In the LM25119 evaluation board (schematic shown in *Figure 14*) interleaved operation can be enabled by shorting both outputs together (with identical components in the power train), and using zero ohm resistors for R22 and R21. This shorts VCC2 to FB2 and COMP2 to COMP1 respectively. Also the channel2 feedback network C14, R6, and C15 should be removed. The easy re-configuration between two channel and single channel operation will allow insight into the benefits of interleaved operation.

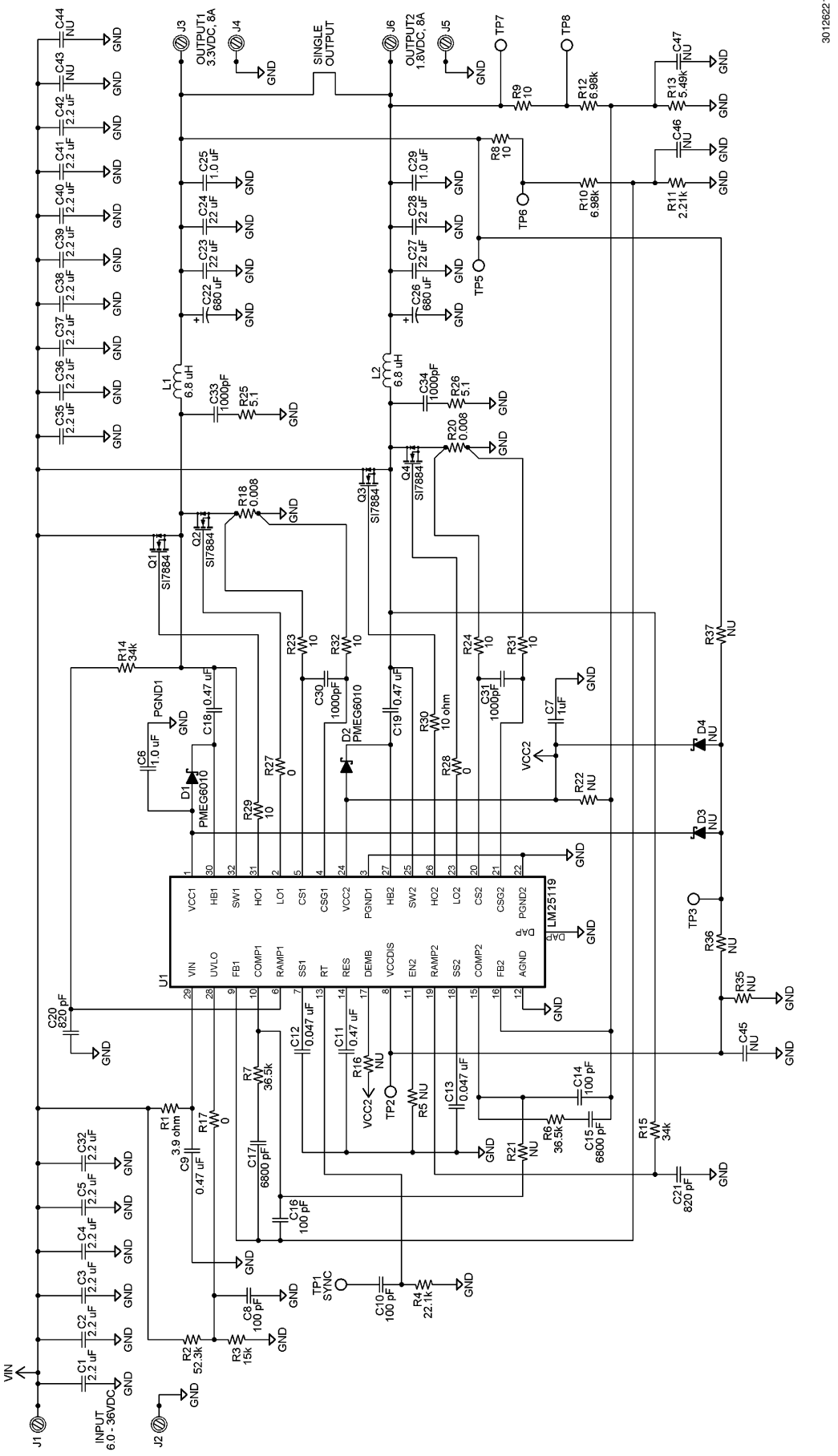


FIGURE 14. 3.3V 8A, 1.8V 8A Typical Application Schematic

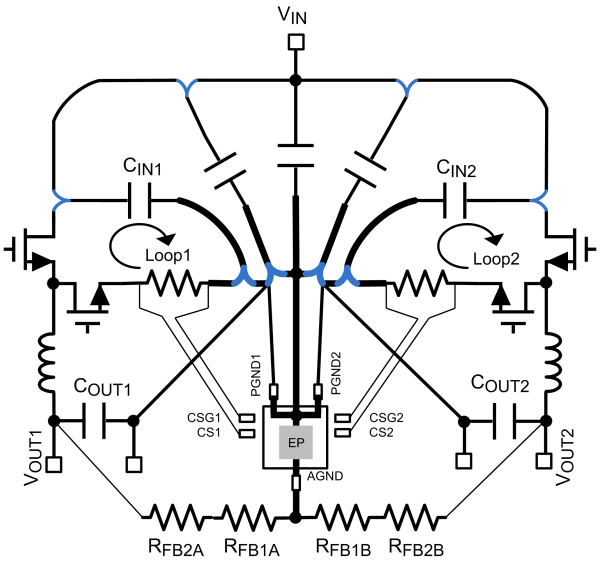
PCB Board Layout Recommendations

The LM25119 consists of two integrated regulators operating almost independently. Crosstalk between the two regulators under certain conditions may be observed as switch jitter. This effect is common for any dual channel regulator. Crosstalk effects are usually most severe when one channel is operating around 50% duty cycle. Careful layout practices help to minimize this effect. The following board layout guidelines apply specifically to the LM25119 and should be followed for best performance.

1. Keep the Loop1 and Loop2, shown in *Figure 15*, as small as possible
2. Keep the signal and power grounds separate
3. Place VCC capacitors (C6, C7) and VIN capacitor (C9) as closes as possible to the LM25119
4. Route CS and CSG traces together with Kelvin connection to the sense resistor
5. Connect AGND and PGND directly to the underside exposed pad
6. Ensure there are no high current paths beneath the underside exposed pad

Switching Jitter Root Causes and Solutions

1. Noise coupling of the high frequency switching between two channels through the input power rail
   - A. Keep the high current path as short as possible
   - B. Choose a FET with minimum lead inductance
   - C. Place local bypass capacitors (C_{IN1}, C_{IN2}) as close as possible to the high-side FETs to isolate one channel from the high frequency noise of the other channel
   - D. Slow down the SW switching speed by increasing gate resistors R29 and R30
   - E. Minimize the effective ESR/ESL of the input capacitor by paralleling input capacitors
2. High frequency AC noise on FB, CS, CSG and COMP
   - A. Use the star ground PCB layout technique and minimize the length of the high current path
   - B. Keep the signal traces away from the SW, HO, HB traces and the inductor
   - C. Add an R-C filter between the CS and CSG pins
   - D. Place CS filter capacitor (C30, C31) next to the LM25119 and on the same PCB layer as the LM25119
3. Ground offset at the switching frequency
   - A. Use the star ground PCB layout technique and minimize the length between the grounds of $C_{IN1}$and C_{IN2}



The bold lines indicate a solid ground plane. Make the traces to the widest and the shortest and use the star ground technique.

These lines indicate the high current paths. Make the traces as wide and short as possible

These lines indicate the small signal paths. The traces can be narrow but keep them away from any radiated noise and away from traces that may couple noise capacitively

These points require the maximum bypassing of the high frequency switching noise. Isolate each channel from the high frequency switching noise of the other channel.

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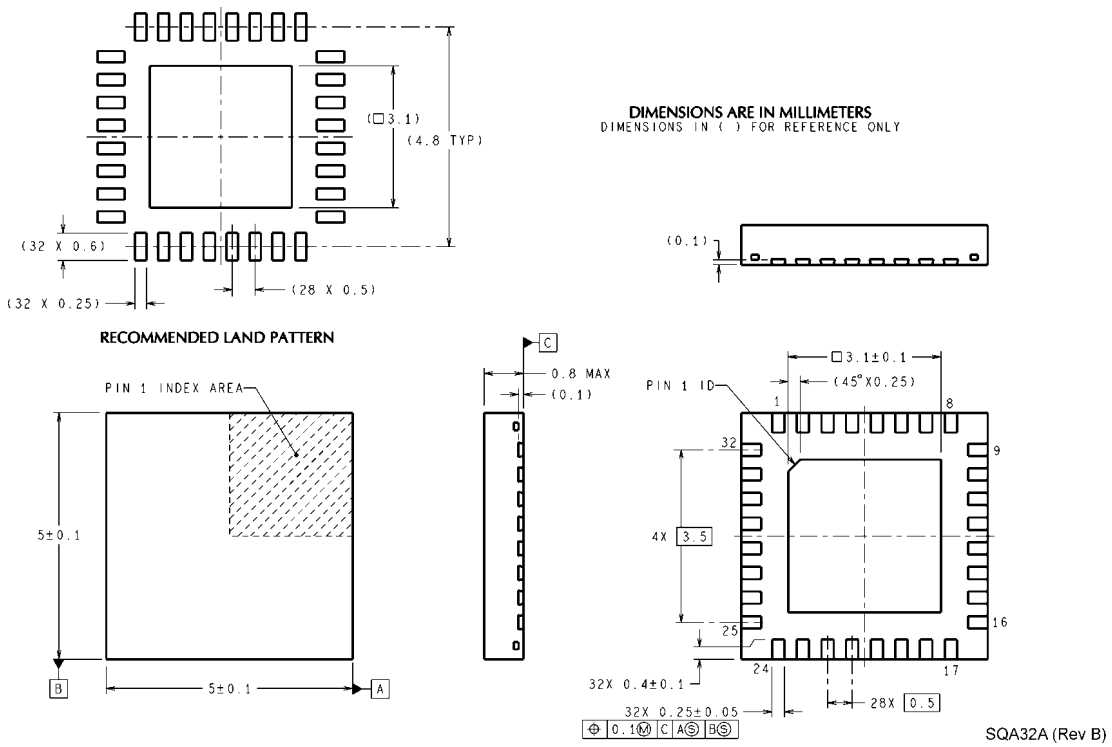
FIGURE 15. Recommended PCB Layout

Physical Dimensions inches (millimeters) unless otherwise noted



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Notes

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