*National Semiconductor*

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# LM25037
# Dual-Mode PWM Controller With Alternating Outputs

## General Description

The LM25037 PWM controller contains all the features necessary to implement balanced double-ended power converter topologies, such as push-pull, half-bridge and full-bridge. These double-ended topologies allow for higher efficiencies and greater power densities compared to common single-ended topologies such as the flyback and forward. The LM25037 can be configured for either voltage mode or current mode control with minimum external components. Two alternating gate drive outputs are provided, each capable of 1.2A peak output current. The LM25037 can be configured to operate directly from the input voltage rail over an ultra-wide range of 5.5V to 75V. Additional features include programmable maximum duty cycle limit, line under-voltage lockout, cycle-by-cycle current limit and a hiccup mode fault protection with adjustable timeout delay, soft-start and a 2 MHz capable oscillator with synchronization capability, precision reference and thermal shutdown.
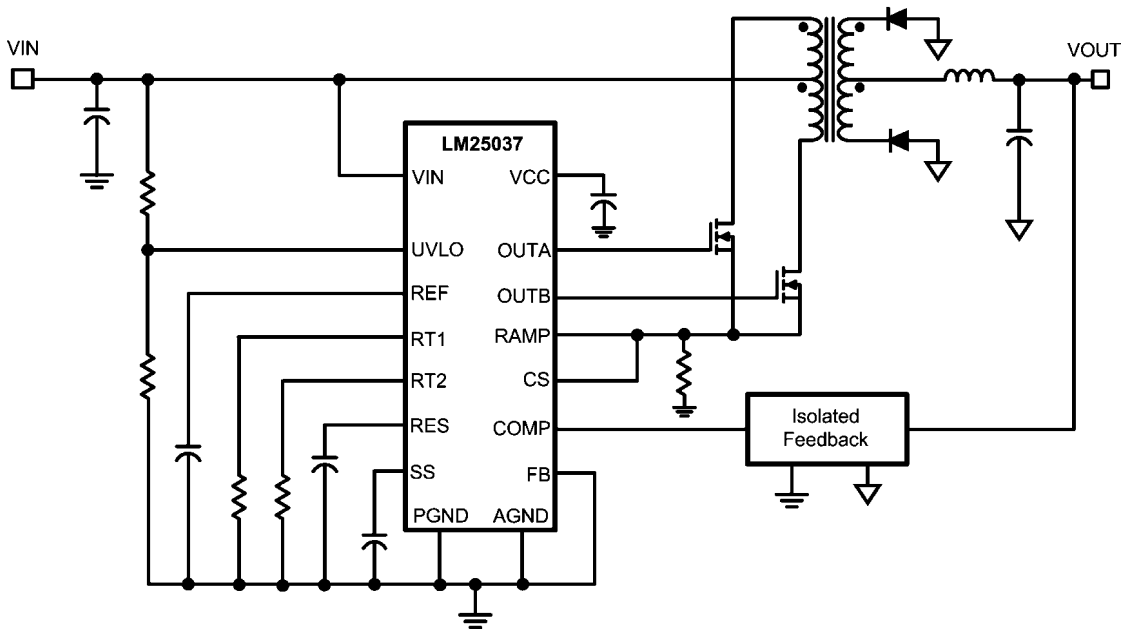
## Features

- Ultra wide input operating range from 5.5V to 75V
- Alternating outputs for double-ended topologies
- Current-mode or feed-forward voltage-mode control
- Programmable maximum duty cycle limit
- 2.0% feedback reference accuracy
- High gain-bandwidth error amplifier
- Programmable line under-voltage lockout (UVLO) with adjustable hysteresis
- Versatile dual mode over-current protection with hiccup delay timer
- Programmable soft-start
- Precision 5V reference output
- Current sense leading edge blanking
- Resistor programmed 2 MHz capable oscillator
- Oscillator synchronization capability with low frequency lockout protection
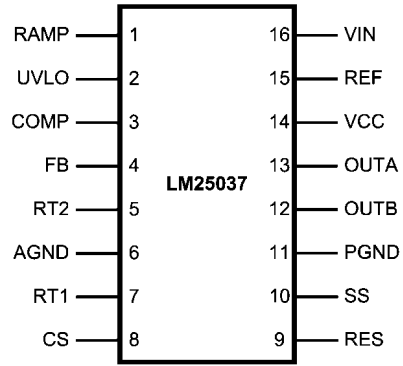
## Package

- TSSOP-16

## Simplified Push-Pull Power Converter



30065101

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# Connection Diagram

```
        RAMP ──── 1          16 ──── VIN
        UVLO ──── 2          15 ──── REF
        COMP ──── 3          14 ──── VCC
          FB ──── 4  LM25037 13 ──── OUTA
         RT2 ──── 5          12 ──── OUTB
        AGND ──── 6          11 ──── PGND
         RT1 ──── 7          10 ──── SS
          CS ──── 8           9 ──── RES
```

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**Top View**
**16-Lead TSSOP Package**

# Ordering Information

| Order Number | Package Type | NSC Package Drawing | Supplied As |
|---|---|---|---|
| LM25037MT | TSSOP-16 | MTC16 | 92 Units per Rail |
| LM25037MTX | | | 2500 Units on Tape and Reel |

# Pin Descriptions

| Pin | Name | Description | Application Information |
|-----|------|-------------|-------------------------|
| 1 | RAMP | Pulse width modulator ramp | Modulation ramp for the PWM comparator. This ramp can be a representative of the primary current (current mode) or proportional to input voltage (feed-forward voltage mode). This pin is reset to ground at the conclusion of every cycle by an internal FET. |
| 2 | UVLO | Line under-voltage lockout | An external voltage divider from the power source sets the shutdown and standby comparator threshold levels. When UVLO exceeds the 0.45V shutdown threshold, the VCC and REF regulators are enabled. When UVLO exceeds the 1.25V standby threshold, the SS pin is released and the device enters the active mode. |
| 3 | COMP | Input to the pulse width modulator | Output of the error amplifier and input to the PWM comparator. |
| 4 | FB | Feedback | Connected to inverting input of the error amplifier. An internal 1.25V reference is connected to the non-inverting input of the error amplifier. In isolated applications using an external error amplifier, this pin should be connected to the AGND pin. |
| 5 | RT2 | Oscillator dead-time control | The resistance connected between RT2 and AGND sets the forced dead-time between switching periods of the alternating outputs. |
| 6 | AGND | Analog ground | Connect directly to Power Ground. |
| 7 | RT1 | Oscillator maximum on-time control | The resistance connected between RT1 and AGND sets the oscillator maximum on-time. The sum of this maximum on-time and the forced dead-time (set by RT2) sets the oscillator period. |
| 8 | CS | Current sense input | If CS exceeds 250 mV the output pulse will be terminated, entering cycle-by-cycle current limit. An internal switch holds CS low for 65 nS after either output switches high to blank leading edge transients. |
| 9 | RES | Restart timer | If cycle-by-cycle current limit is reached during any cycle, a 18 µA current is sourced to the external RES pin capacitor. If the RES capacitor voltage reaches 2.0V, the soft-start capacitor will be fully discharged and then released with a pull-up current of 1 uA. After the first output pulse (when SS = 1V), the SS pin charging current will increase to the normal level of 100 µA. |
| 10 | SS | Soft-start | An external capacitor and an internal 100uA current source set the soft-start ramp. The SS current source is reduced to 1 µA following a restart event (RES pin high). |
| 11 | PGND | Power ground | Connect directly to Analog Ground |
| 12 | OUTB | Output driver | Alternating gate drive output of the pulse width modulator. Capable of 1.2A peak source and sink current. |
| 13 | OUTA | Output driver | Alternating gate drive output of the pulse width modulator. Capable of 1.2A peak source and sink current. |
| 14 | VCC | Output of the high voltage start-up regulator. The VCC voltage is regulated to 7.7V. | If an auxiliary winding raises the voltage on this pin above the regulation set point, the internal start-up regulator will shutdown thus reducing the IC power dissipation. Locally decouple VCC with a 0.47 µF or greater capacitor. |
| 15 | REF | Output of a 5V reference | Locally decouple with a 0.1 µF or greater capacitor. Maximum output current is 10 mA (typ). |
| 16 | VIN | Input voltage source | Input to the VCC Start-up regulator. Operating input range is 5.5V to 75V. For power sources outside of this range, the LM25037 can be biased directly at VCC by an external regulator. |

# Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| VIN to GND | -0.3V to 76V |
| VCC, RAMP , OUTA, OUTB to GND | -0.3V to 16V |
| CS to GND | -0.3V to 1.0V |
| UVLO, FB, RT2, RT1, SS, REF to GND | -0.3V to 7V |
| COMP, RES(Note 2) | |

| | |
|---|---|
| ESD Rating | |
| Human Body Model | 2kV |
| Storage Temperature Range | −65°C to + 150°C |
| Junction Temperature | 150°C |

# Operating Ratings

| | |
|---|---|
| VIN Voltage | 5.5V to 75V |
| External Voltage Applied to VCC | 8V to 14V |
| Operation Junction Temperature | −40°C to + 125°C |

# Electrical Characteristics

Specifications with standard typeface are for $T_J$ = 25°C, and those with **boldface** type apply over full **operating junction temperature range** of −40°C to + 125°C. $V_{VIN}$ = 12V, $V_{VCC}$ = 10V, $R_{RT1}$ = 30.1 kΩ, $R_{RT2}$ = 30.1 kΩ, $V_{UVLO}$ = 3V unless otherwise stated.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Startup Regulator (VCC Pin)** | | | | | | |
| $V_{VCC}$ | VCC voltage | $I_{VCC}$ = 10 mA | **7.2** | 7.7 | **8.1** | V |
| $I_{VCC(Lim)}$ | VCC current limit | $V_{VCC}$ = 7V | **20** | | | mA |
| $V_{VCC(UV)}$ | VCC Under-voltage threshold | | **4.6** | 5 | **5.4** | V |
| | Hysteresis | | | 0.5 | | V |
| $I_{VIN}$ | Startup regulator current | $V_{VIN}$ = 20V, $V_{UVLO}$ = 0V | | 35 | **58** | µA |
| | | $V_{VIN}$ = 75V, $V_{UVLO}$ = 0V | | 45 | **80** | µA |
| | Supply current into VCC from external source | Outputs & COMP open, $V_{VCC}$ = 10V, Outputs switching | | 4 | | mA |
| **Voltage Reference Regulator (REF Pin)** | | | | | | |
| $V_{REF}$ | REF Voltage | $I_{REF}$ = 0 mA | **4.75** | 5 | **5.15** | V |
| | REF Voltage Regulation | $I_{REF}$ = 0 to 2.5 mA | | 7 | **25** | mV |
| $I_{REF(Lim)}$ | REF Current Limit | $V_{REF}$ = 4.5V | **5** | 10 | | mA |
| | VREF Under-Voltage Threshold | | **3.7** | 4 | **4.3** | V |
| $V_{REF(UV)}$ | Hysteresis | | | 0.4 | | V |
| **Under-Voltage Lock Out and Shutdown (UVLO Pin)** | | | | | | |
| $V_{UVLO}$ | Under-voltage threshold | | **1.20** | 1.25 | **1.295** | V |
| $I_{UVLO}$ | Hysteresis current | UVLO pin sinking | **17** | 22 | **26** | µA |
| | Under-voltage Shutdown Threshold | UVLO voltage rising | **0.35** | 0.45 | **0.6** | V |
| | Hysteresis | | | 0.1 | | V |
| **Current Sense Input (CS Pin)** | | | | | | |
| $V_{CS}$ | Current Limit Threshold | | **0.22** | 0.255 | **0.29** | V |
| | CS delay to output | CS from zero to 1V. Time for OUTA and OUTB to fall to 90% of VCC. Output load = 0 pF. | | 27 | | ns |
| | Leading edge blanking time at CS | | | 65 | | ns |
| | CS sink impedance (clocked) | Internal FET sink impedance | | 21 | **45** | Ω |
| **Current Limit Restart (RES Pin)** | | | | | | |
| $V_{RES}$ | RES Threshold | | **1.9** | 2 | **2.2** | V |
| | Charge source current | $V_{RES}$ = 1.5V | **14** | 18 | **21** | µA |
| | Discharge sink current | $V_{RES}$ = 1V | **5** | 8 | **11** | µA |
| **Soft-Start (SS Pin)** | | | | | | |
| $I_{SS}$ | Charging current in normal operation | $V_{SS}$ = 0 | **70** | 100 | **130** | µA |
| | Charging current during a hiccup mode restart | $V_{SS}$ = 0 | **0.6** | 1 | **1.4** | µA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Soft-Stop Current Sink | $V_{SS}$ = 2.0V | **70** | 100 | **130** | µA |
| **Oscillator (RT1 and RT2 Pins)** | | | | | | |
| $DT_1$ | Dead-Time 1 | $R_{RT2}$ = 15 kΩ | **40** | 75 | **105** | ns |
| $DT_2$ | Dead-Time 2 | $R_{RT2}$ = 50 kΩ | | 250 | | ns |
| $F_{SW1}$ | Frequency 1 (at OUTA, half oscillator frequency) | $R_{RT1}$ = 30.1 kΩ, $R_{RT2}$ = 30.1 kΩ, | **178** | 200 | **222** | kHz |
| $F_{SW2}$ | Frequency 2 (at OUTA, half oscillator frequency) | $R_{RT1}$ = 11 kΩ, $R_{RT2}$ = 30.1 kΩ, | **448** | 515 | **578** | kHz |
| | DC level | | | 2 | | V |
| | Input Sync threshold | | **2.5** | 3 | **3.4** | V |
| **PWM Controller (Comp Pin)** | | | | | | |
| | Delay to output | | | 65 | | ns |
| $V_{PWM-OS}$ | SS to RAMP offset | | **0.7** | 1 | **1.2** | V |
| | Minimum duty cycle | $V_{SS}$ = 0V | | | 0 | % |
| | COMP Open Circuit Voltage | $V_{FB}$ = 0V | **4.5** | 4.75 | **5.0** | V |
| | COMP short circuit current | $V_{FB}$ = 0V, COMP = 0V | **0.5** | 1 | **1.5** | mA |
| **Voltage Feed-Forward (RAMP Pin)** | | | | | | |
| | RAMP sink impedance(Clocked) | | | 5 | **20** | Ω |
| **Error Amplifier** | | | | | | |
| GBW | Gain Bandwidth | | | 4 | | MHz |
| | DC Gain | | | 75 | | dB |
| | Input Voltage | $V_{FB}$ = COMP | **1.22** | 1.245 | **1.27** | V |
| | COMP sink capability | $V_{FB}$ = 1.5V COMP=1V | 5 | 13 | | mA |
| | FB Bias Current | | | 10 | | nA |
| **Main Output Drivers (OUTA and OUTB Pins)** | | | | | | |
| | Output high voltage | $I_{OUT}$ = 50 mA, (Source) | **Vcc-0.5** | Vcc-0.25 | | V |
| | Output low voltage | $I_{OUT}$ = 100 mA (Sink) | | 0.2 | **0.5** | V |
| | Rise time | $C_{LOAD}$ = 1 nF | | 17 | | ns |
| | Fall time | $C_{LOAD}$ = 1 nF | | 18 | | ns |
| | Peak source current | $V_{VCC}$ = 10V | | 1.2 | | A |
| | Peak sink current | $V_{VCC}$ = 10V | | 1.2 | | A |
| **Thermal Shutdown** | | | | | | |
| $T_{SD}$ | Thermal Shutdown Threshold | | | 165 | | °C |
| | Thermal Shutdown Hysteresis | | | 25 | | °C |
| **Thermal Resistance** | | | | | | |
| $\theta_{JC}$ | Junction to Case | TSSOP-16 | | 29 | | °C/W |
| $\theta_{JA}$ | Junction to Ambient | TSSOP-16 | | 125 | | °C/W |

**Note 1:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

**Note 2:** COMP, RES are output pins. As such, it is not recommended that external power sources be connected to these pins.

**Note 3:** All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production at $T_A$ = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

**Note 4:** Typical specifications represent the most likely parametric norm at 25°C operation.

**Note 5:** The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. 2kV for all pins.
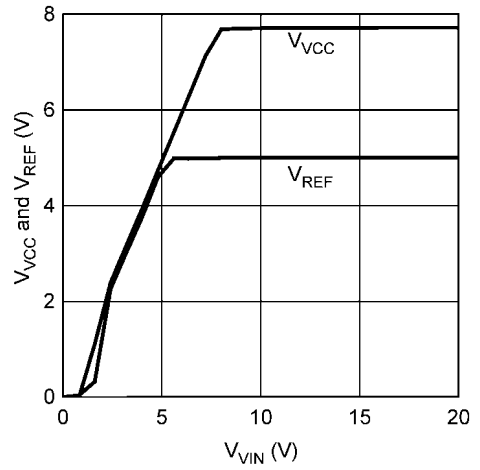
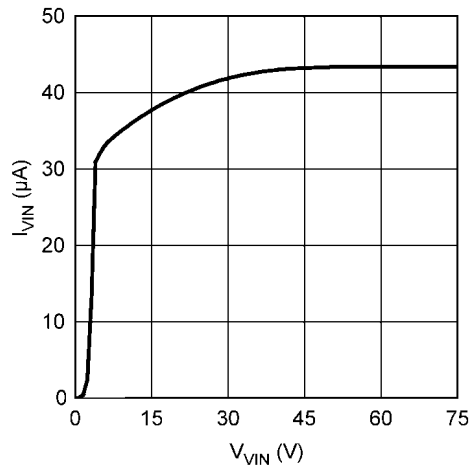# Typical Performance Characteristics

**Typical Application Circuit Efficiency**
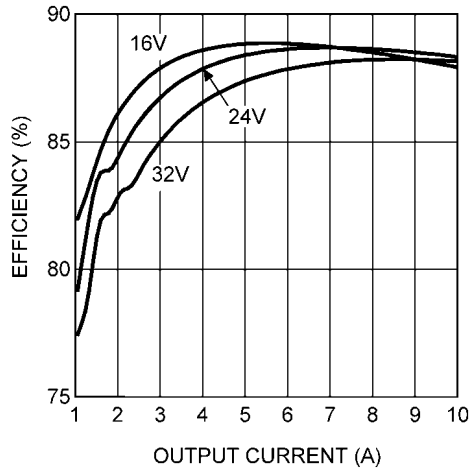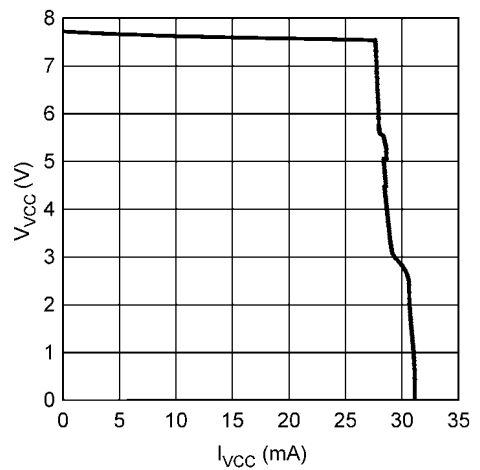


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**V_VCC and V_REF vs V_VIN**



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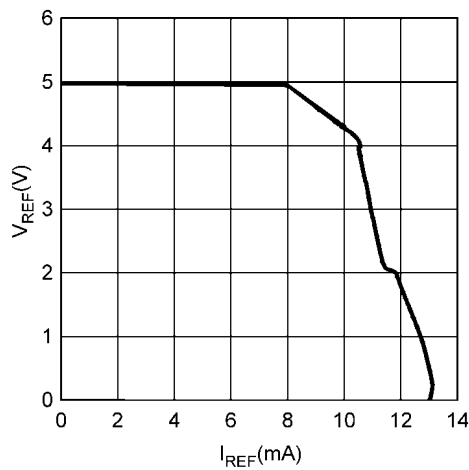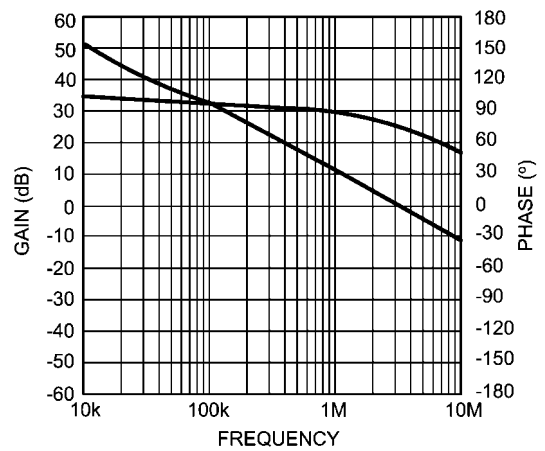**Start-Up Regulator Current (UVLO = 0)**



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**V_VCC vs I_VCC**



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**V_REF vs I_REF**



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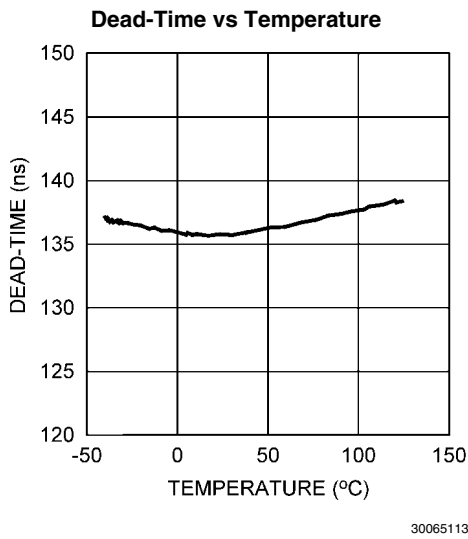**Feedback Amplifier Gain/Phase**



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**Oscillator Frequency vs RT1**



30065108

**Dead-Time vs RT2**



30065110

**V$_{FB}$ vs Temperature**



30065111

**Oscillator Frequency vs Temperature**



30065112

**Dead-Time vs Temperature**



30065113

**Soft-Start and Restart Current vs Temperature**



SOFT-START CURRENT

RESTART CURRENT

30065114

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## Block Diagram
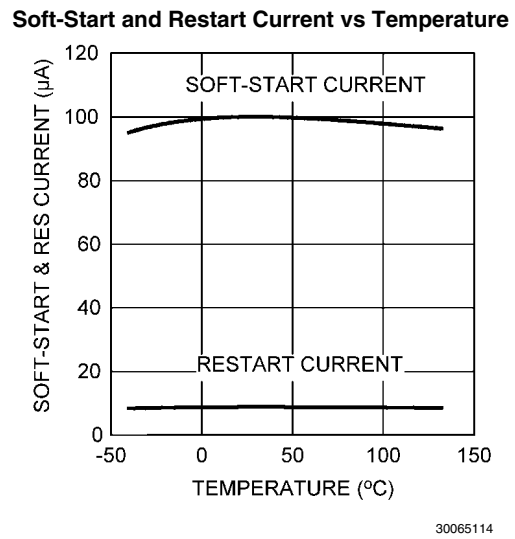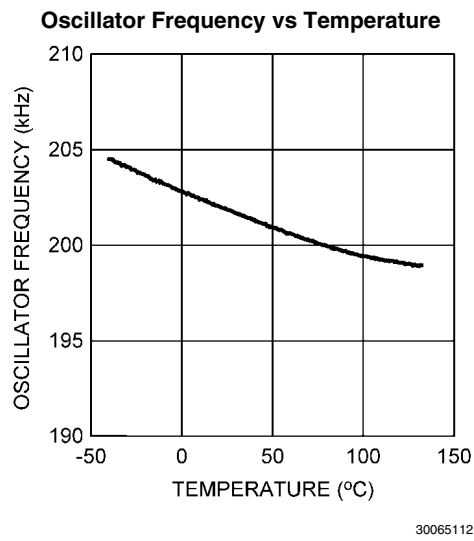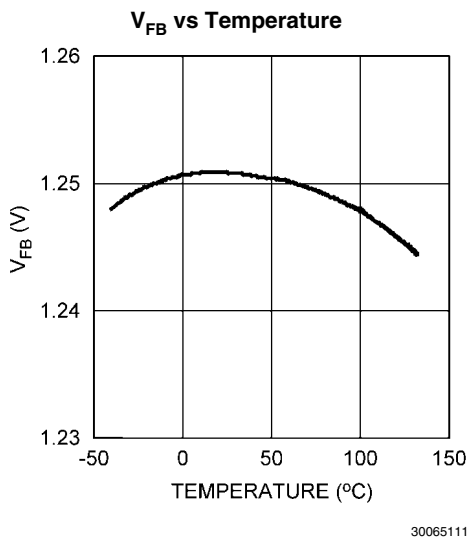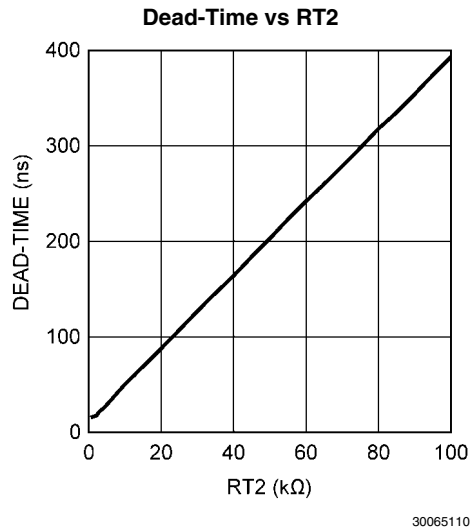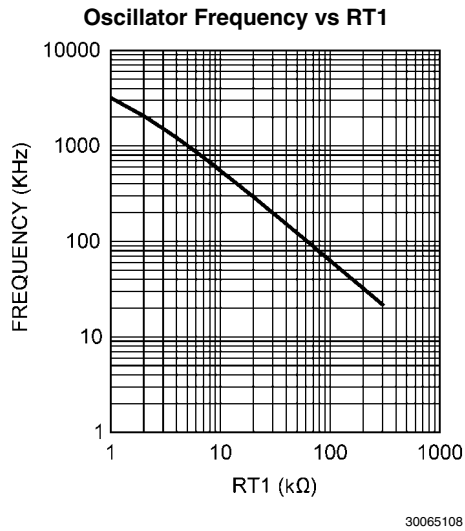


**FIGURE 1. Simplified Block Diagram**

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# Functional Description

The LM25037 PWM controller contains all the features necessary to implement double-ended power converter topologies such as push-pull, half-bridge and full-bridge. The unique architecture allows the modulator to be configured for either voltage-mode or current-mode control. The LM25037 provides two alternative gate driver outputs to drive the primary side power MOSFETs with programmable forced dead-time. The LM25037 can be configured to operate with bias voltages ranging from 5.5V to 75V. Additional features include line under-voltage lockout, cycle-by-cycle current limit, voltage feed-forward compensation, and hiccup mode fault protection with adjustable delays, soft-start, and a 2MHz capable oscillator with synchronization capability, precision reference and thermal shutdown. These rich set of features simplify the design of double ended topologies. The functional block diagram is shown in *Figure 1*.

### HIGH-VOLTAGE START-UP REGULATOR

The LM25037 contains an internal high voltage, low drop-out start-up regulator that allows the input pin (VIN) to be connected directly to the supply voltage over a range of 5.5V to a maximum of 75V. The regulator output at VCC (7.7V) is internally current limited with a guaranteed minimum of 20 mA. When the UVLO pin potential is greater than 0.45V, the VCC regulator is enabled to charge an external capacitor connected to the VCC pin. The VCC regulator provides power to the voltage reference (REF) and the gate drivers (OUTA and OUTB). When the voltage on the VCC pin exceeds its Under Voltage (VCC UV) threshold of 5.0V nominal, the internal voltage reference (REF) reaches its regulation set point of 5V and the UVLO voltage is greater than 1.25V, the controller outputs are enabled. The value selected for the VCC capacitor depends on the total system design, and its start-up characteristics. The recommended range of values for the VCC capacitor is 0.47 µF to 10 µF.The internal power dissipation of the LM25037 can be reduced by powering VCC from an external supply. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.2V to shut off the internal start-up regulator. Powering VCC from an auxiliary winding improves efficiency while reducing the controller's power dissipation. The VCC UV circuit will still function in this mode, requiring that VCC never falls below 5.0V nominal during the start-up sequence. The VCC regulator series pass transistor includes a diode between VCC and VIN that should not be forward biased in normal operation. Therefore the auxiliary VCC voltage should never exceed the VIN voltage.

An external DC bias voltage can be used instead of the internal regulator by connecting the external bias voltage to both the VCC and the VIN pins. In this particular case, the external bias must be greater than max VCC UV of 5.4V and less than the VCC maximum operating voltage rating (14V).

### LINE UNDER-VOLTAGE DETECTOR

The LM25037 contains a dual level line Under-Voltage Lock Out (UVLO) circuit. When the UVLO pin voltage is below 0.45V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.45V but less than 1.25V, the controller is in standby mode. In standby mode the VCC and REF bias regulators are active while the controller outputs are disabled. When the VCC and REF outputs exceed their respective under-voltage thresholds and the UVLO pin voltage is greater than 1.25V, the outputs are enabled and normal operation begins. An external set-point voltage divider

from VIN to GND can be used to set the minimum operating voltage of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 1.25V when VIN enters the desired operating range. UVLO hysteresis is accomplished with an internal 22 µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO pin voltage exceeds 1.25V threshold, the current source is activated to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25V threshold, the current source is disabled causing the voltage at the UVLO pin to quickly fall. The hysteresis of the 0.45V shutdown comparator is internally fixed at 100 mV.

The UVLO pin can also be used to implement various remote enable/disable functions. Turning off the converter by forcing the UVLO pin to standby condition provides a controlled soft-stop. See the Soft-Start section for more details.

### REFERENCE

The REF pin is the output of a 5V linear regulator that can be used to bias an opto-coupler transistor and external housekeeping circuits. The regulator output is internally current limited to 10 mA (typical).

### ERROR AMPLIFIER

An internal high gain error amplifier is provided within the LM25037. The amplifier's non-inverting reference is tied to a 1.25V reference. In non-isolated applications the power converter output is connected to the FB pin via the voltage setting resistors and loop compensation is connected between the COMP and FB pins. A typical gain/phase plot is shown in performance curves section.

For most isolated applications the error amplifier function is implemented on the secondary side. Since the internal error amplifier is configured as an open drain output, it can be disabled by connecting FB to ground. The internal 5K pull-up resistor connected between the COMP pin and the 5V reference can be used as the pull-up for an opto-coupler or other isolation device .

### CYCLE-BY-CYCLE CURRENT LIMIT

The CS pin is to be driven by a signal representative of the transformer primary current. The current sense signal can be generated by using a sense resistor or a current sense transformer. If the voltage sensed at the CS pin exceeds 0.255V, the current sense comparator terminates the output driver pulse. If the high current condition persists, the controller operates in a cycle-by-cycle current limit mode with duty cycle determined by the current sense comparator instead of the PWM comparator. Cycle-by-cycle current limiting may eventually trigger the hiccup mode restart cycle; depending on the configuration of the RES pin (see Overload Protection Timer below). To suppress noise, a small R-C filter connected to the CS pin and located near the controller is recommended. An internal 21Ω MOSFET discharges the external current sense filter capacitor at the conclusion of every cycle. The discharge MOSFET remains on for an additional 65 ns after either OUTA or OUTB driver switches high to blank leading edge transients in the current sensing circuit. Discharging the CS pin filter each cycle and blanking leading edge spikes reduces the filtering requirements and improves the current sense response time. The current sense comparator is very fast and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the CS and AGND pins. If a sense resistor located in the source of the main MOSFET switch is used for current sensing, a low inductance

type of resistor is required. When designing with a current sense resistor, all the noise sensitive, low power ground connections should be connected together near the AGND pin, and a single connection should be made to the power ground (sense resistor ground point).

## OVERLOAD PROTECTION TIMER

The LM25037provides a current limit restart timer to disable the outputs and force a delayed restart (hiccup mode) if a current limit condition is repeatedly sensed. The number of cycle-by-cycle current limit events required to trigger the restart is programmed by the external capacitor at the RES pin. During each PWM cycle, the LM25037 either sources to or sinks current from the RES pin capacitor. If no current limit is detected during a cycle, a 8 µA discharge current sink is enabled to pull the RES pin towards ground. If a current limit is detected, the 8 µA sink current is disabled and an 18 µA current source causes the voltage at the RES pin to gradually increase. The LM25037 protects the converter with cycle-by-cycle current limiting while the voltage at RES pin increases. If the RES voltage reaches the 2.0V threshold, the following restart sequence occurs (also see *Figure 2*):

- The RES capacitor and SS capacitors are fully discharged.
- The soft-start current source is reduced from 100 µA to 1 µA.
- The SS capacitor voltage slowly increases. When the SS voltage reaches ≅1V, the PWM comparator will produce the first narrow output pulse. After the first pulse occurs, the SS source current reverts to the normal 100 µA level. The SS voltage increases at its normal rate, gradually increasing the duty cycle of the output drivers.
- If the overload condition persists after restart, cycle-by-cycle current limiting will begin to increase the voltage on the RES capacitor again, repeating the hiccup mode sequence.

- If the overload condition no longer exists after restart, the RES pin will be held at ground by the 8 µA current sink and normal operation resumes.

The overload timer function is very versatile and can be configured for the following modes of protection:

1. **Cycle-by-cycle only:** The hiccup mode can be completely disabled by connecting a zero to 50 kΩ resistor from the RES pin to AGND. In this configuration, the cycle-by-cycle protection will limit the output current indefinitely and no hiccup sequences will occur.

2. **Hiccup only:** The timer can be configured for immediate activation of a hiccup sequence upon detection of an overload by leaving the RES pin open circuit. In this configuration, the first detection of current limit condition by the CS pin comparator will initiate a hiccup cycle with SS capacitor fully discharged and a delayed restart.

3. **Delayed Hiccup:** Connecting a capacitor to the RES pin provides a programmed interval of cycle-by-cycle limiting before initiating a hiccup mode restart, as previously described. The dual advantages of this configuration are that a short term overload will not cause a hiccup mode restart but during extended overload conditions, the average dissipation of the power converter will be very low.

4. **Externally Controlled Hiccup:** The RES pin can also be used as an input. By externally driving the pin to a level greater than the 2.0V hiccup threshold, the controller will be forced into the delayed restart sequence. For example, the external trigger for a delayed restart sequence could come from an over-temperature protection circuit or an output over-voltage sensor
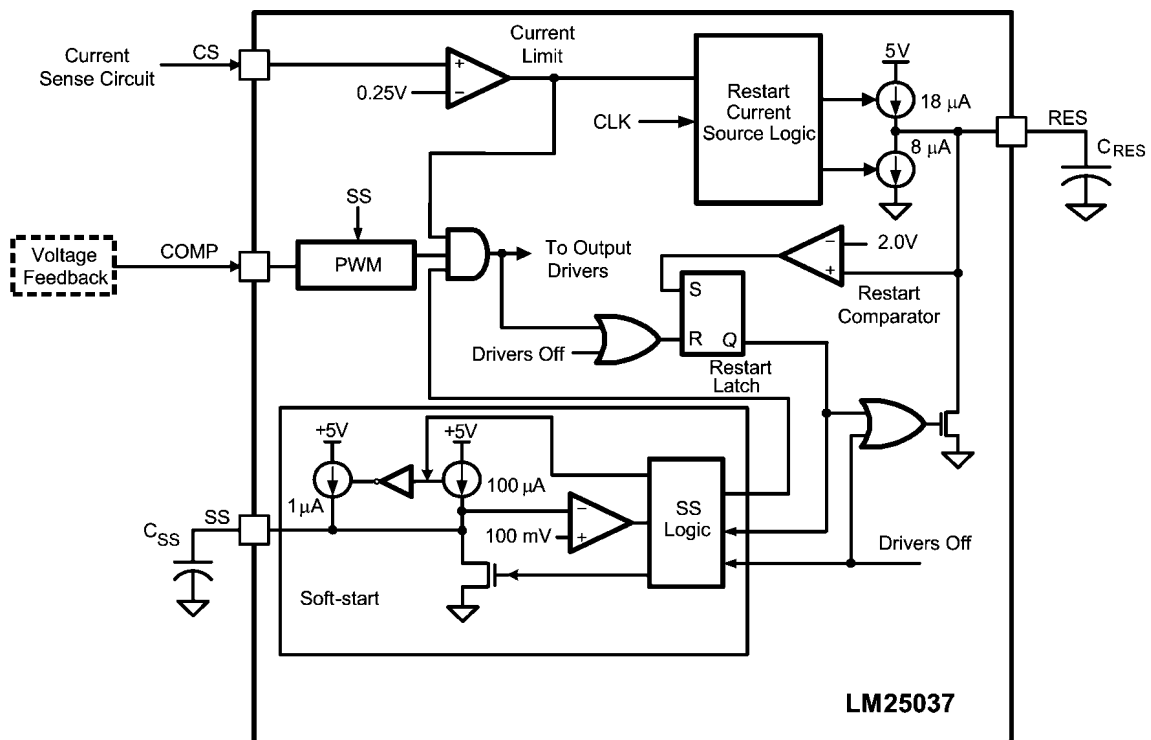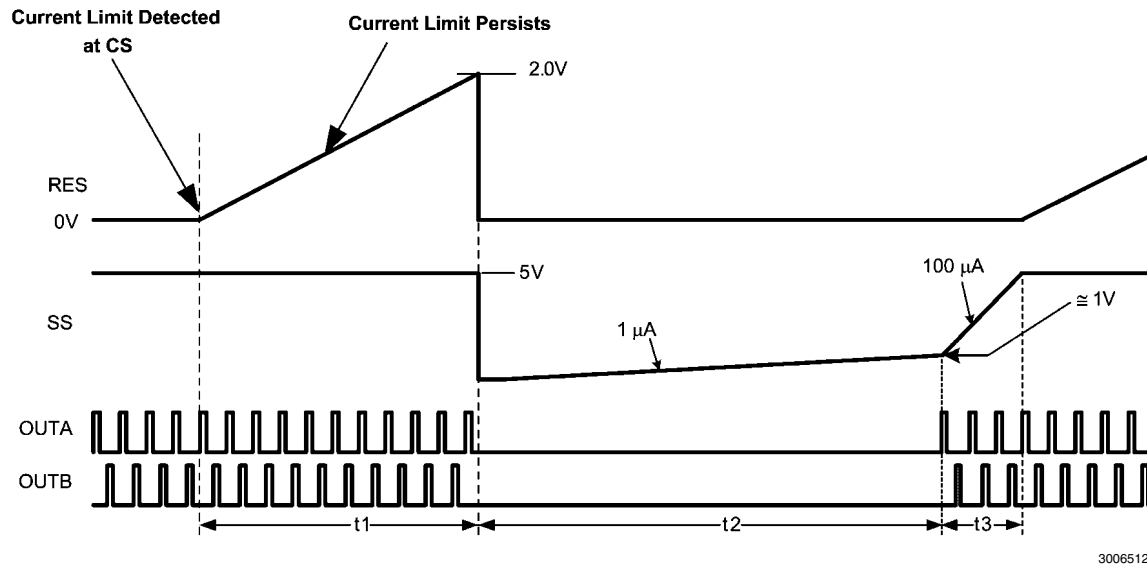


FIGURE 2. Current Limit Restart Circuit

**FIGURE 3. Current Limit Restart Timing**

**SOFT-START**

The soft-start circuit allows the regulator to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. When bias is supplied to the LM25037, the SS pin capacitor is discharged by an internal MOSFET. When the UVLO, VCC and REF pins reach their operating thresholds, the SS capacitor is released and charged with a 100 µA current source. The PWM comparator control voltage at the COMP pin is clamped to the SS pin voltage by an internal amplifier. When the PWM comparator input reaches 1V, output pulses commence with slowly increasing duty cycle. The voltage at the SS pin eventually increases to 5V, while the voltage at the PWM comparator increases to the value required for regulation as determined by the voltage feedback loop.

One method to disable the regulator is to ground the SS pin. This forces the internal PWM control signal to ground, reducing the output duty cycle quickly to zero. Releasing the SS pin initiates a soft-start sequence and normal operation resumes. A second shutdown method is discussed in the UVLO section.

**PWM COMPARATOR**

The pulse width modulation (PWM) comparator compares the voltage ramp signal at the RAMP pin to the loop error signal. The loop error signal is derived from the internal error amplifier (COMP pin). The resulting control voltage passes through a 1V level shift before being applied to the PWM comparator. This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The common mode input voltage range of the PWM comparator is from 0 to 4.3V.

**RAMP PIN**

The voltage at the RAMP pin provides the modulation ramp for the PWM comparator. The PWM comparator compares the modulation ramp signal at the RAMP pin to the loop error signal to control the output duty cycle. The modulation ramp can be implemented either as a ramp proportional to input voltage, known as feed-forward voltage mode control, or as a ramp proportional to the primary current, known as current mode control. The RAMP pin is reset by an internal FET with an $R_{DS(ON)}$ of 5Ω (typical) at the end of every cycle. The ability to configure the RAMP pin for either voltage mode or current mode allows the controller to be implemented for the optimum control method for the selected power stage topology. Configuring RAMP pin is explained below and the differences between voltage mode control and current mode control in various double-ended topologies is explained in Applications Information section.

**FEED-FORWARD VOLTAGE MODE**

An external resistor ($R_{FF}$) and capacitor ($C_{FF}$) connected to VIN, AGND, and the RAMP pins is required to create the PWM ramp signal as shown in *Figure 4* below. It can be seen that the slope of the signal at RAMP will vary in proportion to the input line voltage. This varying slope provides line feed-forward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal by the pulse width modulator comparator to control the duty cycle of the outputs. With a constant error signal, the on-time ($t_{ON}$) varies inversely with the input voltage (VIN) to stabilize the Volt • Second product of the transformer primary. At the end of clock period, an internal FET will be enabled to reset the $C_{FF}$ capacitor. The formulae for $R_{FF}$ and $C_{FF}$ and component selection criteria are explained in Applications Information section. The amplitude of the signal driving RAMP pin must not exceed the common mode input voltage range of the PWM comparator (3.3V) while in normal operation.
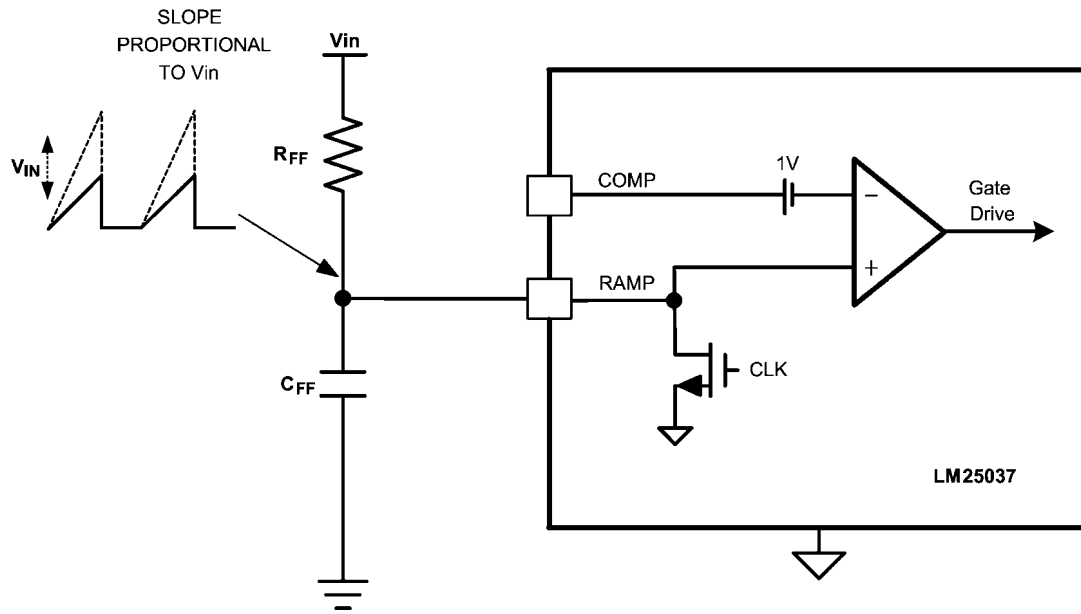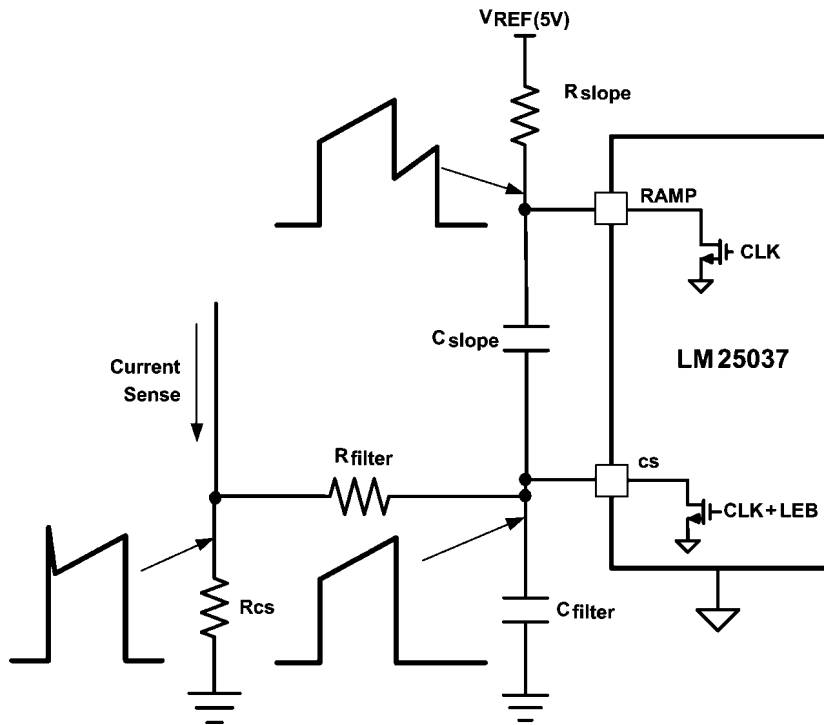
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**FIGURE 4. Feed-Forward Voltage Mode Configuration**

## CURRENT MODE

The LM25037 can be configured for current mode control by injecting a signal representative of primary current into the RAMP pin. One way to achieve this is shown in *Figure 5*. Filter components $R_{filter}$ and $C_{filter}$ are used to filter leading edge noise spikes. The signal at the CS pin is thus a ramp on a pedestal. The pedestal corresponds to the continuous conduction current in the transformer at the beginning of an OUTA or OUTB conduction cycle. The R-C circuit ($R_{Slope}$ and $C_{Slope}$), shown in *Figure 5*, tied to $V_{REF}$ adds an additional ramp to the current sense signal. This additional ramp signal, known as slope compensation, is required to avoid instabilities at duty cycles above 50% (25% per phase). The compensated RAMP signal consists of two parts, the primary current signal and the slope compensation. The compensated RAMP signal is compared to the error signal by the PWM comparator to control the duty cycle of the outputs. The RAMP capacitor and CS capacitor are reset through internal discharge FETs. The $R_{DS(ON)}$ of RAMP discharge FET is 5Ω (typical); this ensures fast discharge of the RAMP reset capacitor. Any dc voltage source can be used in place of $V_{REF}$ to generate the slope compensation ramp.

The timing diagram shown in *Figure 6* depicts the current mode waveforms and relative timing. When OUTA or OUTB is enabled, the signal at the RAMP pin consists of the CS pin signal (current ramp on a pedestal) plus the slope compensation ramp (dotted lines). When OUTA or OUTB is turned off, the primary current component is absent but the voltage at the RAMP pin continues to rise due to slope compensation component until the end of the clock period, after which it is reset by the RAMP discharge FET. A component selection example is explained in detail in the Applications Information section.

**FIGURE 5. Current Mode Configuration with Slope Compensation**
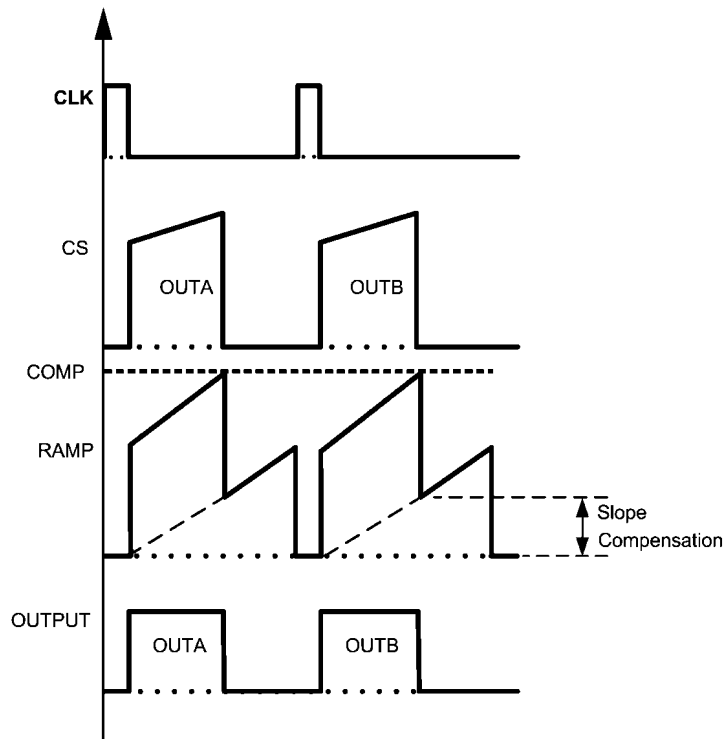


**FIGURE 6. Timing Diagram for Current Mode Configuration**

**LM25037**

## OSCILLATOR

The LM25037 oscillator frequency and the maximum duty cycle are set by two external resistors connected between the RT1 and RT2 pins to AGND. The minimum dead-time between OUTA and OUTB pulses is proportional to the RT2 resistor value and the overall oscillator frequency is inversely proportional to RT1 and RT2 resistor values. Each output switches at half the oscillator frequency. Initially, RT2 should be selected for the desired dead-time or for the desired maximum duty cycle ($D_{max}$).

$$RT2 = \frac{Dead\text{-}Time}{5.0 \times 10^{-12}} \quad 50\ ns < DT < 250\ ns$$

or

$$RT2 = \frac{(1 - D_{max})\,/\,F_{OSC}}{5.0 \times 10^{-12}}$$

It is recommended to set the dead-time range between 50 ns and 250 ns. Beyond 250 ns, RT2 becomes excessively large, and is prone to noise pickup. Fixed internal delays limit the dead-time to greater than 50 ns. After the dead-time has been programmed by RT2, the overall oscillator frequency can be set by selecting resistor RT1 from :

$$RT1 = \frac{\dfrac{1}{F_{OSC}} - (Dead\text{-}Time)}{0.162 \times 10^{-9}}$$

For example, if the desired oscillator frequency is 400 kHz (OUTA and OUTB each switching at 200 kHz) and desired dead-time is 100 ns, the maximum duty cycle for each output will be 96% and the values of RT1 and RT2 will be 15 kΩ and 20 kΩ respectively.



$$T_{onmax}\ \alpha\ RT1$$
$$T_{Dead\text{-}Time}\ \alpha\ RT2$$
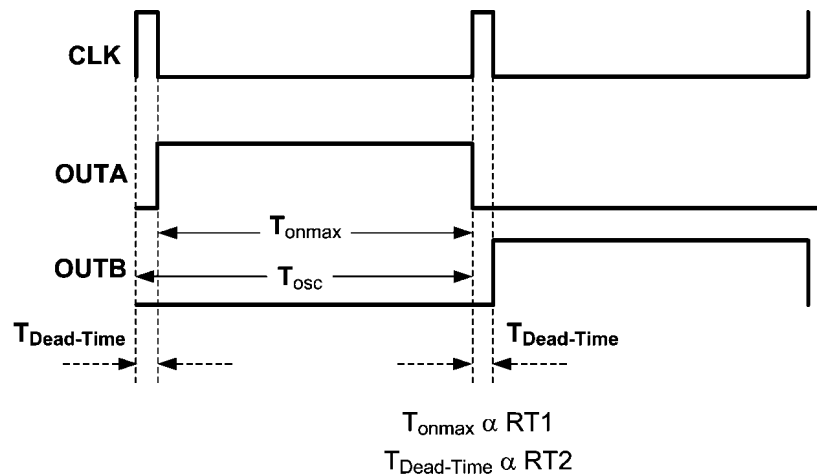
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**FIGURE 7. Timing Diagram of OUTA, OUTB and Dead-Time Set by RT2**

As shown in *Figure 7*, the internal clock pulse width is the same as the dead-time set by RT2. This dead-time pulse is used to limit the maximum duty cycle for each of the outputs. Also, the discharge FET connected to the RAMP pin is enabled during the dead-time every clock period. The voltages at both the RT1 and RT2 pins are internally regulated to a nominal 2V. Both the resistors RT1 and RT2 should be located as close as possible to the IC, and connected directly to the pins. The tolerance of the external resistors and the frequency tolerance indicated in the Electrical Characteristics table must be taken into account when determining the worst case frequency range.

### SYNC CAPABILITY

The LM25037 can be synchronized to an external clock by applying a narrow ac pulse to the RT1 pin. The external clock must be at least 10% higher than the free-running oscillator frequency set by the RT1 and RT2 resistors. If the external clock frequency is less than the programmed frequency, the LM25037 will ignore the synchronizing pulses. The synchronization pulse width at the RT1 pin must be a minimum of 15 ns wide. The synchronization signal should be coupled into the RT1 pin through a 100 pF capacitor or another value small enough to ensure the sync pulse width at RT1 is less than

60% of the clock period under all conditions. When the synchronizing pulse transitions from low-to-high (rising edge), the voltage at the RT1 pin must be driven to exceed 3.0V from its nominal 2.0V volt dc level. During the synchronization clock signal's low time, the voltage at the RT1 pin will be clamped at 2V volts by an internal regulator. The RT1 and RT2 resistors are always required, whether the oscillator is free running or externally synchronized.

### GATE DRIVER OUTPUTS (OUTA & OUTB)

The LM25037 provides two alternating gate driver outputs, OUTA and OUTB. The internal gate drivers can each source and sink 1.2A peak each. The maximum duty cycle is inherently limited to less than 50% and is based on the value of RT2 resistor. As an example, if the COMP pin is in a high state, RT1 = 15K and RT2 = 20K then the outputs will operate at maximum duty cycle of 96%.

### THERMAL PROTECTION

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum rated junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state with the output drivers (OUTA and OUTB) and the bias regulators

(VCC and REF) disabled. This helps to prevent catastrophic failures from accidental device overheating. During thermal shutdown, the soft-start capacitor is fully discharged and the controller follows a normal start-up sequence after the junction temperature falls to the operating level (140°C).

# Application Information

The following information is intended to provide guidelines for the design process when applying the LM25037.

### TOPOLOGY and CONTROL ALGORITHM CHOICE

The LM25037 has all the features required to implement double-ended power converter topologies such as push-pull, half-bridge and full-bridge with minimum external components. One key feature is the flexibility in control algorithm selection, i.e., the LM25037 can be used to implement either voltage mode control or current mode control. Designers familiar with these topologies recognize that conventionally, current mode control is used for push-pull and full-bridge topologies while voltage mode control is required for the half-bridge topology. In limited applications, voltage mode control can be used for push-pull and full-bridge topologies as well, with special care to maintain flux balance, such as using a dc-blocking capacitor in the primary (full-bridge). The goal of this section is to illustrate implementation of both current mode control and voltage mode control using the LM25037 and aid the designer in the design process.

### VOLTAGE MODE CONTROL USING THE LM25037

An external resistor ($R_{FF}$) and capacitor ($C_{FF}$) connected to VIN, AGND, and the RAMP pins is required to create a sawtooth modulation ramp signal shown in *Figure 8*. The slope of the signal at RAMP will vary in proportion to the input line voltage. The varying slope provides line feed-forward information necessary to improve line transient response with voltage mode control. With a constant error signal, the on-time ($t_{ON}$) varies inversely with the input voltage (VIN) to stabilize the Volt • Second product of the transformer primary.

Using a line feed-forward ramp for PWM control requires very little change in the voltage regulation loop to compensate for changes in input voltage, as compared to a fixed slope oscillator ramp. Furthermore, voltage mode control is less susceptible to noise and does not require leading edge filtering, and is therefore a good choice for wide input range power converters. Voltage mode control requires a more complicated compensation network, due to the complex-conjugate poles of the L-C output filter.

In push-pull and full-bridge topologies, any asymmetry in the volt-second product applied to primary in one phase may not be cancelled by subsequent phase, possibly resulting in a dc current build-up in the transformer, which pushes the transformer core towards saturation. Special care in the transformer design, such as gapping the core, or adding ballasting resistance in the primary is required to rectify this imbalance when using voltage mode control with these topologies. Current mode control naturally corrects for any volt-second asymmetry in the primary.

The recommended capacitor value range for $C_{FF}$ is 100 pF to 1500 pF. Referring to *Figure 8*, it can be seen that value $C_{FF}$ must be small enough such that the capacitor can be discharged within the clock (CLK) pulse width each cycle. The CLK pulse width is same as the dead-time set by RT2. The minimum possible dead-time for LM25037 is 50 ns and the internal discharge FET $R_{DS(ON)}$ is 5Ω (typical),

The value of $R_{FF}$ required can be calculated from

$$R_{FF} = \frac{-1}{F_{OSC} \times C_{FF} \times \ln\left(1 - \frac{V_{RAMP}}{VIN_{min}}\right)}$$

For example, assuming a $V_{Ramp}$ of 1 volt at $VIN_{min}$ (a good compromise of signal range and noise immunity), oscillator frequency, $F_{OSC}$ of 250 kHz, $VIN_{min}$ of 24 Volts, and $C_{FF}$ = 270 pF results in a value for $R_{FF}$ of 348 kΩ.
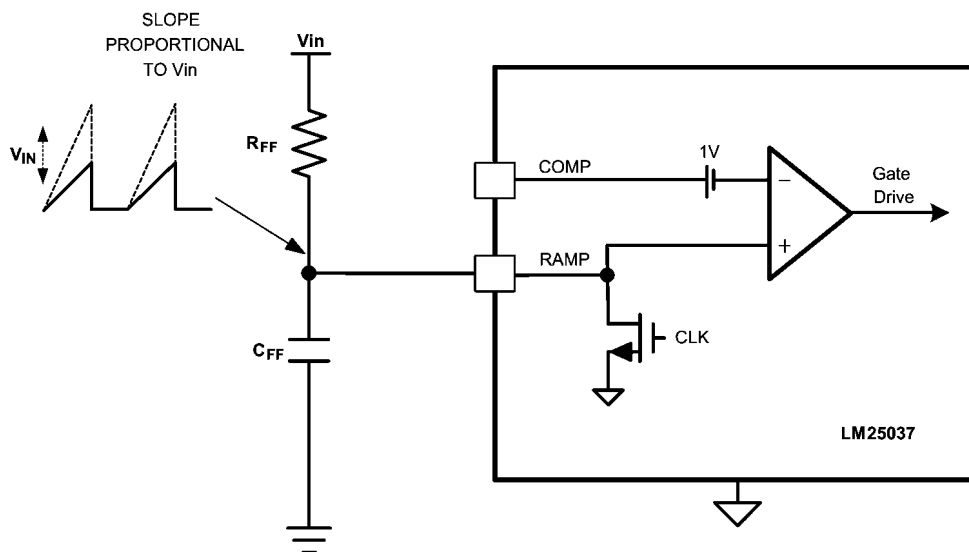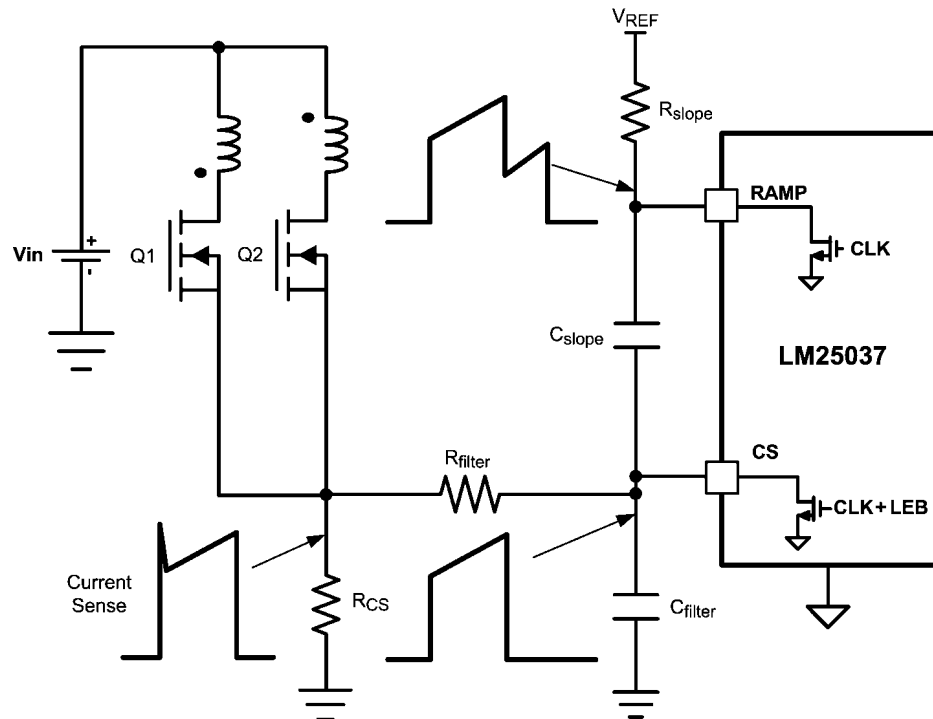


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**FIGURE 8. Feed-Forward Voltage Mode Configuration**

## CURRENT MODE CONTROL USING THE LM25037

The LM25037 can be configured in current mode control by applying the primary current signal into the RAMP pin. One way to achieve this is shown in *Figure 9*, which depicts a simplified push-pull converter. The primary current is sensed using a sense resistor and the current information is then fil-

tered and applied to the RAMP pin through capacitor $C_{slope}$, for use as the modulation ramp. It can be seen that the signal applied to the RAMP pin consists of the primary current information from the CS pin plus an additional ramp for slope compensation, added by $R_{slope}$ and $C_{slope}$.



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**FIGURE 9. Current Mode Configuration**

Current mode control inherently provides line voltage feed-forward, cycle-by-cycle current limiting and ease of loop compensation as it removes the additional pole due to output inductor. Also, in push-pull and full-bridge converters, current mode control inherently balances volt-second product in both the phases by varying the duty cycle as needed to terminate the cycle at the same peak current for each output phase. For duty cycles greater than 50% (25% for each phase), peak current mode controlled circuits are subject to sub-harmonic oscillation. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow duty cycles at the controller output. Adding an artificial ramp (slope compensation) to the current sense signal will eliminate this potential oscillation. Current mode control is also susceptible to noise and layout considerations. It is recommended that $C_{Filter}$ and $C_{slope}$ be placed as close to the IC as possible to avoid any noise pickup and trace inductance. When the converter is operating at low duty cycles and light load, the primary current amplitude is small and is susceptible to noise. The artificial ramp, added to avoid sub-harmonic oscillations, provides additional benefits by improving the noise immunity of the converter.

Configuration and component selection for current mode control is recommended as follows: The current sense resistor is selected such that during over current condition, the voltage across the current sense resistor is above the minimum CS threshold of 220 mV. It is recommended to set the impedances of $R_{Filter}$ and $C_{Filter}$ as seen from $C_{slope}$ at rela-

tively low values, so that the slope compensation is primarily dictated by $R_{slope}$ and $C_{slope}$ components. For example, if the filtering time ($R_{Filter}$ and $C_{Filter}$) for leading edge noise is selected for 50 ns and if the value selected for $R_{Filter} = 25\Omega$, then

$$C_{Filter} = \frac{50 \times 10^{-9}}{3 \times 25\Omega}$$

Resulting in a value of $C_{Filter}$ = 680 pF (approximated to a standard value). In general, the amount of slope compensation required to avoid sub-harmonic oscillation is equal to at least one-half the down-slope of the output inductor current, transformed to the primary. To mitigate sub-harmonic oscillation after one switching period, the slope compensation has to be equal to one times the down slope of the filter inductor current transformed to primary. This is known as deadbeat control. For circuits where primary current is sensed, the amount of slope compensation for dead-beat control can be calculated from:

$$\text{Slope-Comp} = \frac{\text{Turns-Ratio} \times \text{Vout} \times R_{CS}}{F_{OSC} \times L_{filter}}$$

Where, Turns-Ratio is referred with respect to the primary. For example, for a 5V output converter with a turns ratio between secondary and primary of 1:2, an oscillator frequency

($F_{OSC}$) of 250 kHz, a filter inductance of 4 µH ($L_{Filter}$) and a current sense resistor ($R_{CS}$) of 32 mΩ, slope compensation of 80 mV will suffice. The slope compensation "volts" that results from the above expression is the maximum voltage of the artificial ramp added linearly to the RAMP pin till the end of maximum switching period. For circuits where a current sense tramsformer is used for primary current sensing, the turns-ratio of the current sense transformer has to be taken into account.

$C_{slope}$ should be selected such that it can be fully discharged by the internal RAMP discharge FET. Capacitor values ranging from 100 pF to 1500 pF are recommended. The value must be small enough such that the capacitor can be discharged within the clock (CLK) pulse width each cycle.

$R_{slope}$ can be selected from the following formula:

$$R_{slope} = \frac{-1}{F_{OSC} \times C_{slope} \times \ln\left(1 - \dfrac{\text{Slope-Comp}}{V_{REF}}\right)} - R_{filter}$$

For example, with a $C_{slope}$ of 1500 pF, $F_{OSC}$ of 250 kHz, reference voltage of 5V ($V_{REF}$), slope compensation of 80 mV and $R_{filter}$ = 25Ω results in $R_{slope}$ value of 165 kΩ.

### VIN and VCC

The voltage applied to the VIN pin, which may be the same as the system voltage applied to the power transformer's primary ($V_{PWR}$), can vary in the range from 5.5V to 75V. The current into the VIN pin depends primarily on the gate charge provided by the output drivers, the switching frequency, and any external loads on the VCC and REF pins. It is recommended that the filter shown in *Figure 10* be used to suppress transients that may occur at the input supply. This is particularly important when VIN is operated close to the maximum operating rating of the LM25037.

When power is applied to VIN and the UVLO pin voltage is greater than 0.45V, the VCC regulator is enabled and supplies current into an external capacitor connected to the VCC pin. When the voltage on the VCC pin reaches the regulation point of 7.7V, the voltage reference (REF) is enabled. The reference regulation set point is 5V. The outputs (OUTA and OUTB) are enabled when the two bias regulators reach their set point and the UVLO pin potential is greater than 1.25V. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.1V to shut off the internal start-up regulator.

After the outputs are enabled and the external VCC supply voltage has begun supplying power to the IC, the current into the VIN pin drops below 1 mA. VIN should remain at a voltage equal to or above the VCC voltage to avoid reverse current through protection diodes.
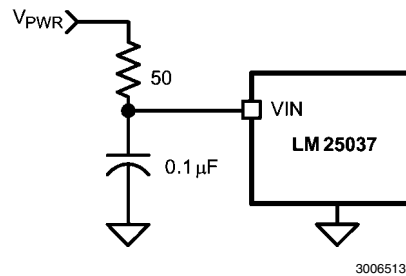


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**FIGURE 10. Input Transient Protection**

### FOR APPLICATIONS WITH >75V INPUT

For applications where the system input voltage exceeds 75V or the IC power dissipation is of concern, the LM25037 can be powered from an external start-up regulator as shown in *Figure 11*. In this configuration, the VIN and the VCC pins should be connected together. The voltage at the VCC and VIN pins must be at least 5.5V (> Max VCC UV voltage) yet not exceed 14V. An auxiliary winding can be used to reduce the power dissipation in the external regulator once the power converter is active. The NPN base-emitter reverses breakdown voltage, which can be as low as 5V for some transistors, should be considered when selecting the transistor.
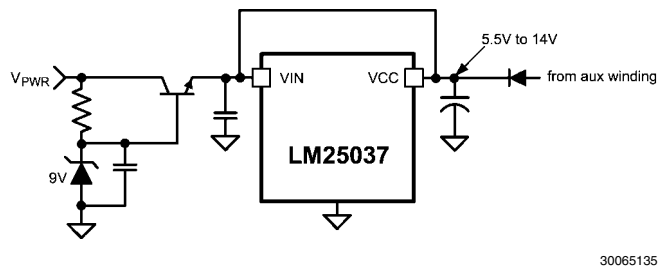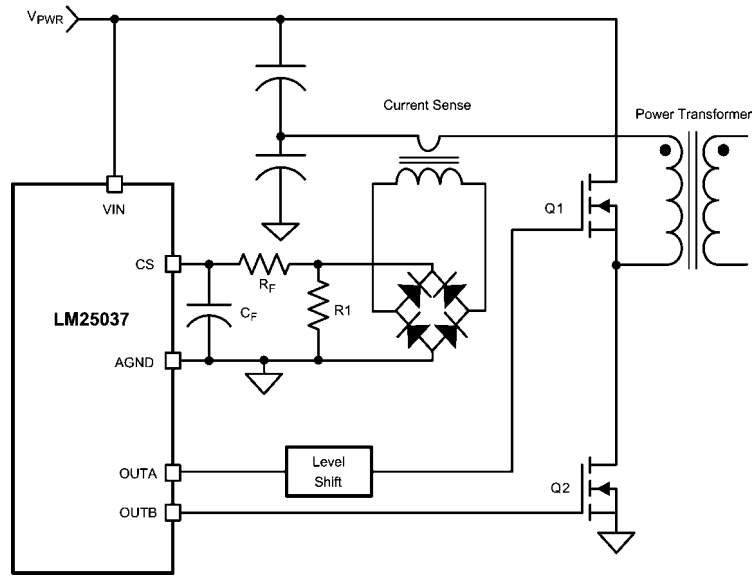


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**FIGURE 11. Start-up Regulator for VPWR >75V**

### CURRENT SENSE

The CS pin should receive an input signal representative of the transformer's primary current, either from a current sense transformer or from a resistor in series with the source of the OUTA and OUTB MOSFET switches. In both cases, the sensed current creates a voltage ramp across R1, and the $R_F$/$C_F$ filter suppresses noise and transients as shown in *Figure 12* and *Figure 13*. R1, $R_F$ and $C_F$ should be located as close to the LM25037 as possible, and the ground connection from the current sense transformer, or R1, should be a dedicated track to the AGND pin. The current sense components must provide greater than 220 mV at the CS pin when an overcurrent condition exists.

**FIGURE 12. Current Sense Using Transformer**
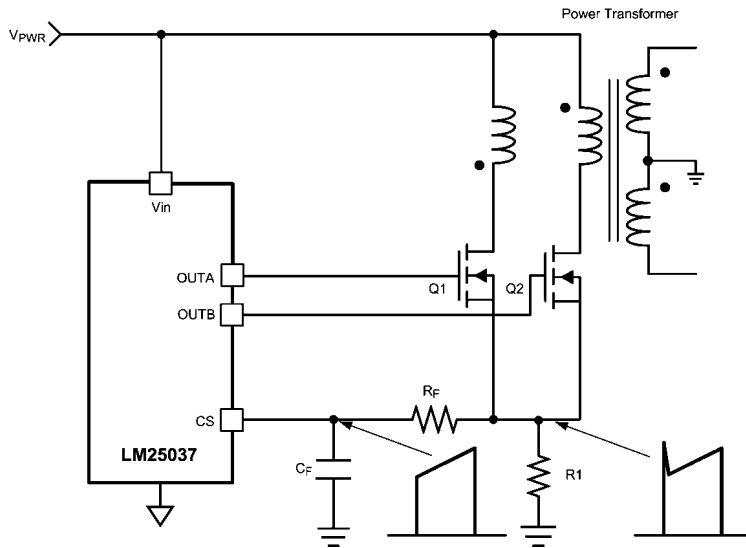


**FIGURE 13. Current Sense Using Current Sense Resistor (R1)**

## UVLO DIVIDER SELECTION

A dedicated comparator connected to the UVLO pin detects an input under-voltage condition. When the UVLO pin voltage is below 0.45V, the LM25037 controller is in a low current shutdown mode. For a UVLO pin voltage greater than 0.45V but less than 1.25V, the controller is in standby mode with VCC and REF regulators active but no switching. Once the UVLO pin voltage is greater than 1.25V, the controller is fully enabled. When the UVLO pin voltage rises above the 1.25V threshold, an internal 22 µA current source as shown in *Figure 14*, is activated thus providing threshold hysteresis. The 22 µA current source is deactivated when the voltage at the UV-LO pin falls below 1.25V. Resistance values for R1 and R2 can be determined from the following equations:

$$R_1 = \frac{\left(V_{HYS} - \frac{20 \times 10^{-3} \times V_{PWR}}{1.25}\right)}{22\ \mu A}$$

$$R_2 = \frac{1.25 \times R_1}{V_{PWR} - 1.25}$$

Where $V_{PWR}$ is the desired turn-on voltage and $V_{HYS}$ is the desired UVLO hysteresis at $V_{PWR}$.
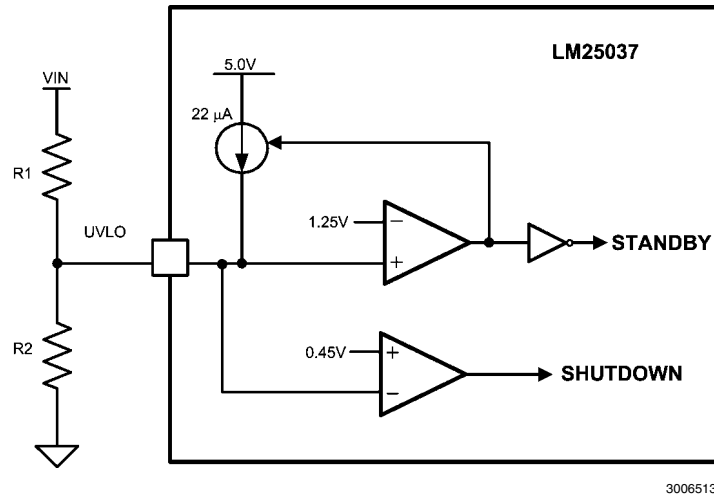
**FIGURE 14. Basic UVLO Configuration**

For example, if the LM25037 is to be enabled when $V_{PWR}$ reaches 33V, and disabled when $V_{PWR}$ decreases to 30V, R1 should be 113 kΩ, and R2 should be 4.42 kΩ. The voltage at the UVLO pin should not exceed 7V at any time. Be sure to check both the power and voltage rating (0603 resistors can be rated as low as 50V) for the selected R1 resistor. To main-

tain the UVLO threshold accuracy, a resistor tolerance of 1% or better is recommended.

Remote control of the LM25037 operational modes can be accomplished with open drain device(s) connected to the UV-LO pin as shown in *Figure 15*.
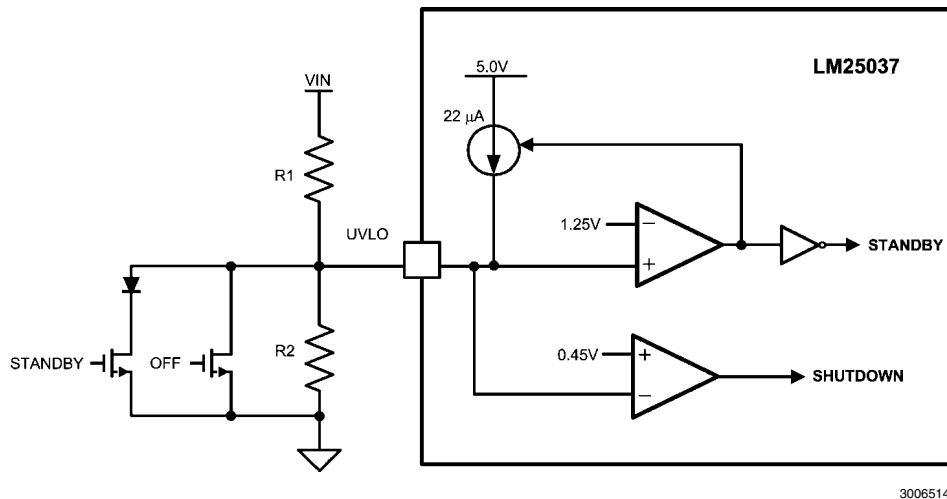


**FIGURE 15. Remote Standby and Disable Control**

## HICCUP MODE CURRENT LIMIT RESTART (RES)

The basic operation of the hiccup mode current limit is described in the functional description. The delay time to the initiation of a hiccup cycle is programmed by the selection of the RES pin capacitor $C_{RES}$ as illustrated in *Figure 16*.
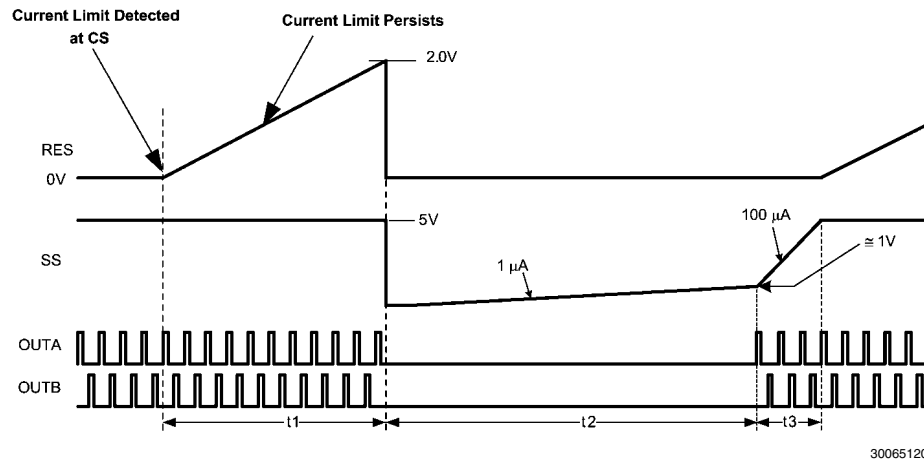


**FIGURE 16. Hiccup Over-Load Restart Timing**

In the case of continuous cycle-by-cycle current limit detection at the CS pin, the time required for $C_{RES}$ to reach the 2.0V hiccup mode threshold is:

$$t1 = \frac{C_{RES} \times 2.0V}{18\ \mu A} = 111k \times C_{RES}$$

For example, if $C_{RES}$ = 0.01 μF the time t1 is approximately 2.0 ms. The cool down time, t2 is set by the soft-start capacitor ($C_{SS}$) and the internal 1 μA SS current source, and is equal to:

$$t2 = \frac{C_{SS} \times 1V}{1\ \mu A} = 1M \times C_{SS}$$

If $C_{SS}$ = 0.01 μF, t2 is ≅10 ms.

The soft-start time t3 is set by the internal 100 μA current source, and is equal to:

$$t3 = \frac{C_{SS} \times 4V}{100\ \mu A} = 40k \times C_{SS}$$

If $C_{SS}$ = 0.01 μF, t3 is ≅ 400 μs.

The time t2 provides a periodic cool-down time for the power converter in the event of a sustained overload or short circuit. This off time results in lower average input current and lower power dissipation within the power components. It is recommended that the ratio of t2 / (t1 + t3) be in the range of 5 to 10 to take advantage of this feature.

If the application requires no delay from the first detection of a current limit condition to the onset of the hiccup mode (t1 = 0), the RES pin can be left open (no external capacitor). If it is desired to disable the hiccup mode entirely, the RES pin should be connected to ground (AGND).

## PRINTED CIRCUIT BOARD LAYOUT

The LM25037 Current Sense and PWM comparators are very fast, and respond to short duration noise pulses. The components at the CS, COMP, SS, UVLO, RT2 and the RT1 pins should be as physically close as possible to the IC, thereby minimizing noise pickup on the PC board trace inductances.

Layout considerations are critical for the current sense filter. If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense filter components and to the IC pins. The ground side of the transformer should be connected via a dedicated PC board trace to the AGND pin, rather than through the ground plane.

If the current sense circuit employs a sense resistor in the drive transistor source, low inductance resistors should be used. In this case, all the noise sensitive, low-current ground trace should be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point).

While employing current mode control, RAMP pin capacitor and CS pin capacitor must be placed close to the IC. Also, a short direct trace should be employed to connect RAMP capacitor to the CS pin.

The gate drive outputs of the LM25037 should have short, direct paths to the power MOSFETs in order to minimize inductance in the PC board The two ground pins (AGND, PGND) must be connected together with a short, direct connection, to avoid jitter due to relative ground bounce.

If the internal dissipation of the LM25037 produces high junction temperatures during normal operation, the use of multiple vias under the IC to a ground plane can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) will help reduce the junction temperatures. If using forced air cooling, avoid placing the LM25037 in the airflow shadow of tall components, such as input capacitors.
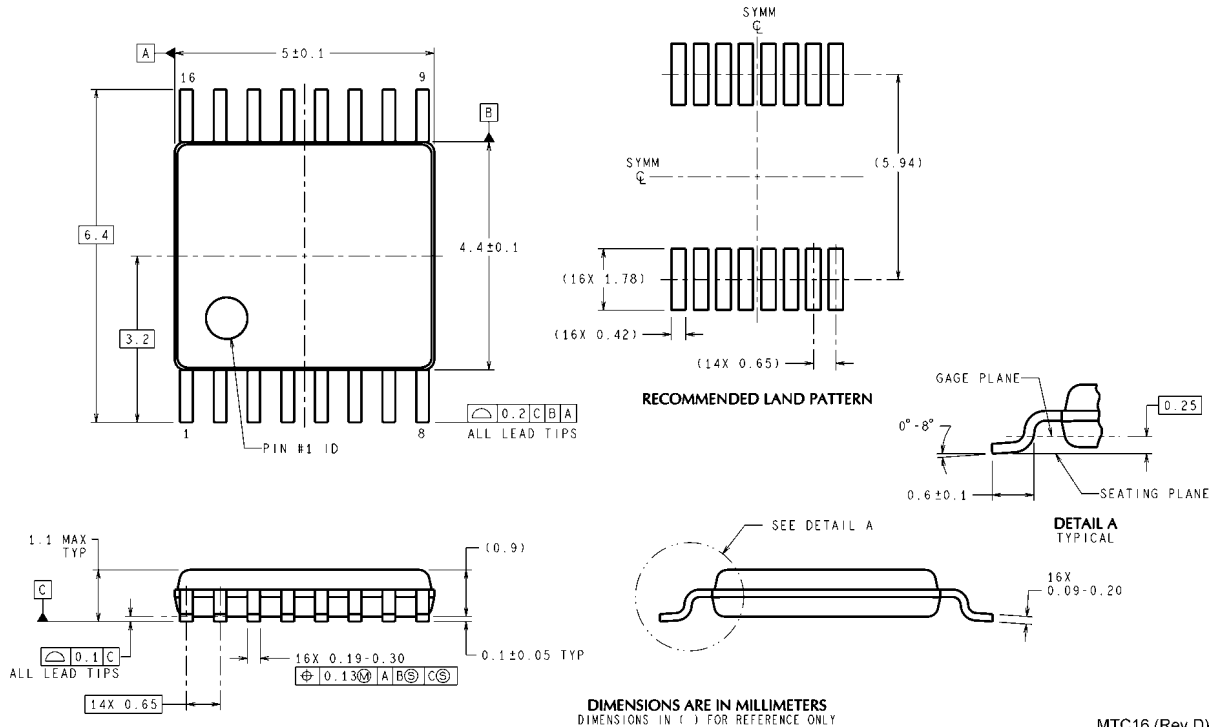
## APPLICATION EXAMPLE

The following schematic shows an example of a 50W push-pull converter controlled by LM25037. The operating input voltage range is 16V to 32V, and the output voltage is 5V. The output current capability is 10 Amps. The converter is configured for current mode control with external slope compensation. An auxiliary winding of the output filter inductor L3 is used to raise the VCC voltage to reduce the power dissipation.
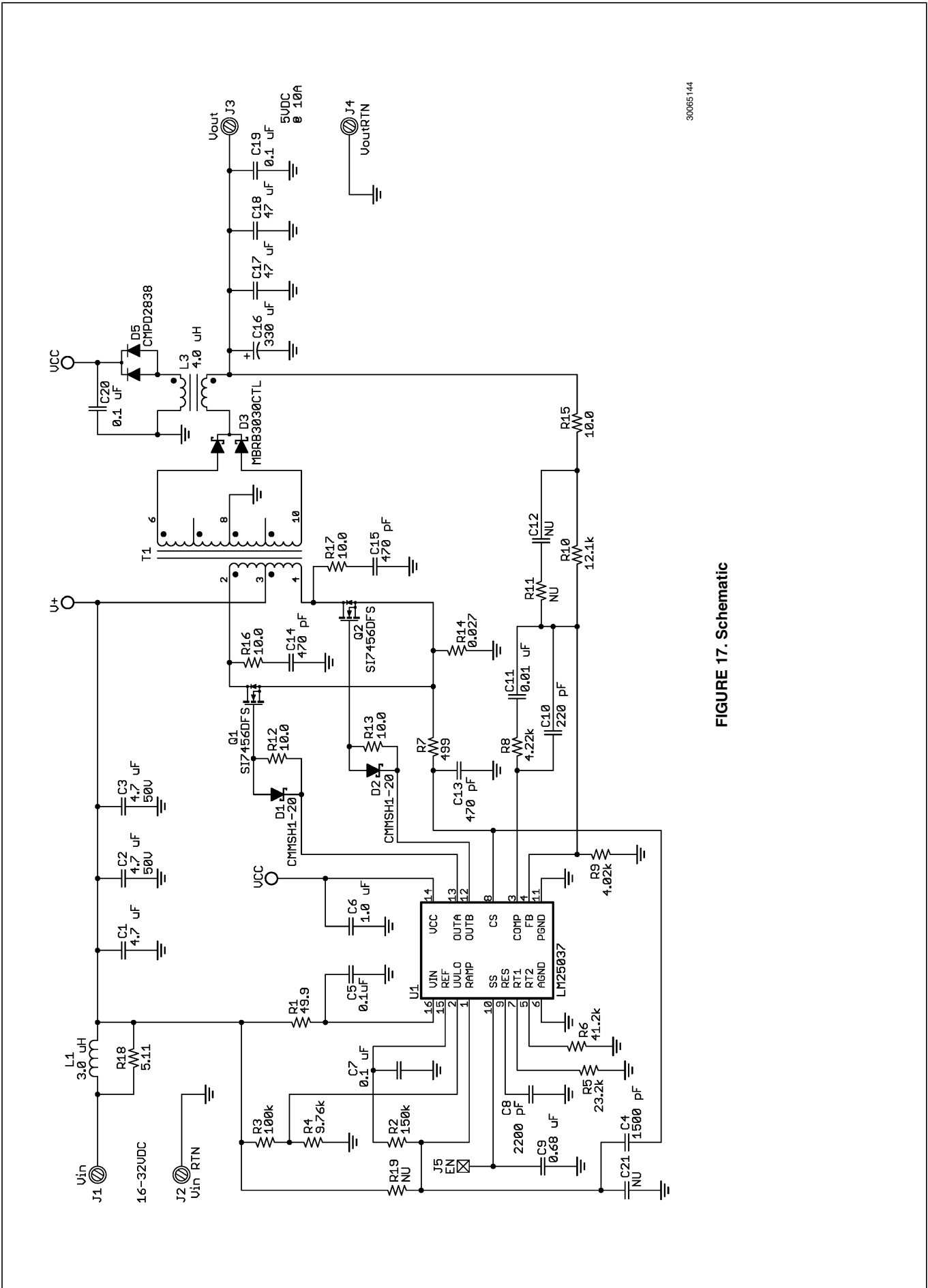
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**FIGURE 17. Schematic**

# Physical Dimensions inches (millimeters) unless otherwise noted



**RECOMMENDED LAND PATTERN**

**DETAIL A**
TYPICAL

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MTC16 (Rev D)

**16-Lead TSSOP Package**
**NS Package Number MTC16**

# Notes

# Notes

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