National Semiconductor

ADVANCE INFORMATION
June 2004

LM2501
Mobile Pixel Link (MPL) Camera Interface Serializer and Deserializer

General Description

The LM2501 device is a Serializer/Deserializer that adapts existing video busses to Mobile Pixel Link (MPL). MPL is intended to replace wide LVCMOS video interfaces inside portable electronics equipment benefiting their cost, size, EMI and power consumption.

By using the LM2501 SERDES chipset, the interconnect is reduced from 12 active signals to only 3 active signals providing a 75% reduction. This eases interconect and flex design, size and cost.

Contained in a 24 lead Ultra Thin CSP Package, the Serializer resides beside the video source (camera) and translates the parallel bus from LVCMOS levels to serial MPL levels for transmission over a flex cable to the Deserializer located by the respective destination Video Input Port.

An extra clock transport is provided to deliver a clock signal to the target. For example, from the main board to the flip board where the camera module is located. Transmission of the clock also benefits from MPL's low power transmission and low EMI.

The Power_Down (PD*) input controls the power state of the MPL interface. When PD* is asserted, the MD, MC and WC signals are powered down to save current and reduce power dissipation.

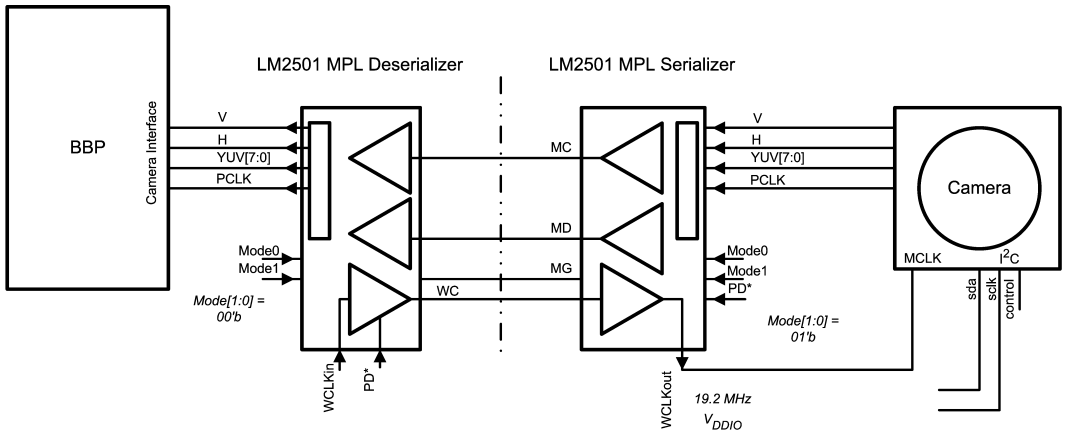
Features

- 160 Mbps Raw Throughput
- MPL-0 Meets MPL Physical Layer Specification
- Configurable as a Serializer or Deserializer
- Complete LVCMOS to MPL Translation
- Serializes 8-bit Camera Interface
  — 8-bit color data
  — plus VSYNC and HSYNC bits
- Link power down mode reduces quiescent power under ~ 10 µA (actual TBD)
- 1.7V–3.1V and 2.9-3.1V Supply Voltage
- Interfaces to 1.8V–3.0V Logic
- Offered in a small 24L UCSP Package
  — 3.5 mm X 4.5 mm
  — 0.6 mm Max Height

System Benefits

- Reduced Wire Interface
- Low Power
- Low EMI
- Extra Clock Transport
- Intrinsic Level Translation

Typical Application Diagram



Ordering Information

NSID	Package Type	Package ID
LM2501SL	24-Lead Ultra Thin CSP 3.5 X 4.5 X 0.6 mm	SLE24A

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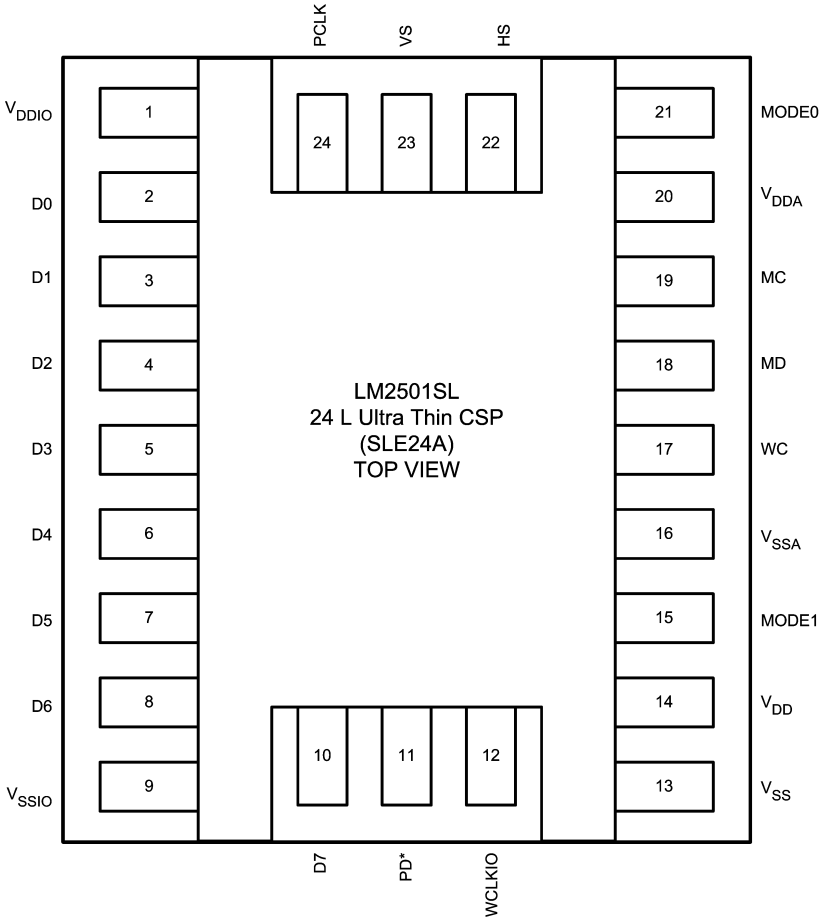
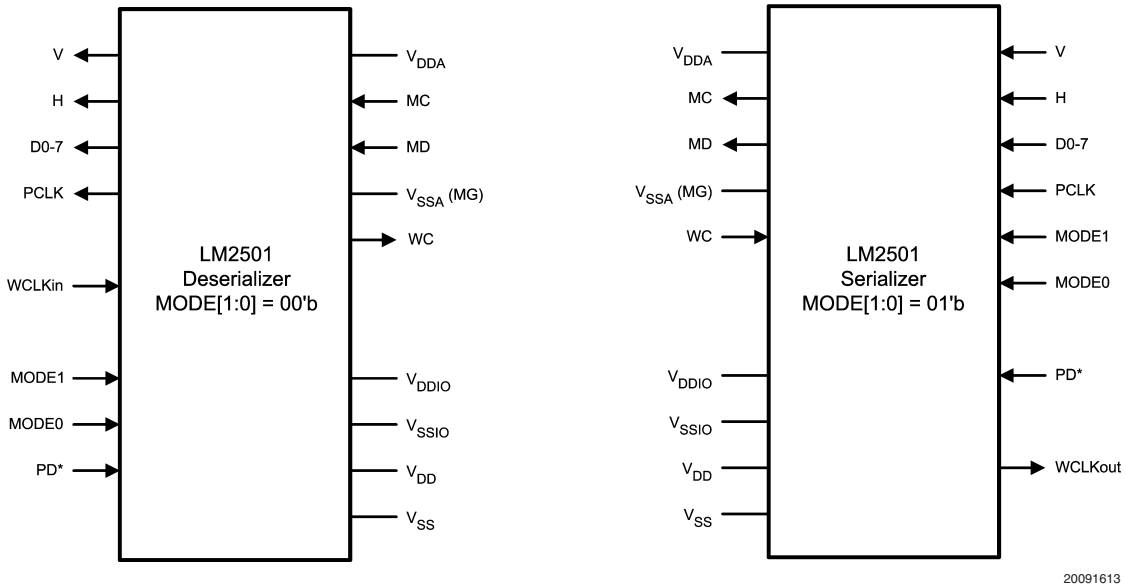
Connection Diagram



TOP VIEW

General Block Diagrams: Serializer and Deserializer



Pin Description

Pin Name	No. of Pins	I/O, Type	Description
MPL SERIAL BUS PINS			
MD	1	IO, MPL	MPL Data line. Serializer is a Line Driver. Deserializer is a Receiver. Configured by the Mode[1:0] pins.
MC	1	IO, MPL	MPL Clock line. Serializer is a Line Driver. Deserializer is a Receiver. Configured by the Mode[1:0] pins.
MG	1	Ground	See VSSA below.
CONFIGURATION/PARALLEL BUS PINS			
Mode[1:0]	2	I, LVCMOS	Mode Configuration Input pins: Mode[1:0], **NOTE** - Applies to REV F/G Samples only. 00 : Deserializer 01 : Serializer with PD* input 10 : Reserved 11 : Reserved
PD*	1	I, LVCMOS	Power_Down. Input pin. Active Low. When PD* is Low the device is in the sleep state.
D0–D7	8	IO, LVCMOS	8-bit Bi-directional Data Bus – Serializer Input, Deserializer Output
VS	1	IO, LVCMOS	VSYNC – Serializer Input, Deserializer Output
HS	1	IO, LVCMOS	HSYNC – Serializer Input, Deserializer Output
PCLK	1	IO, LVCMOS	Pixel Clock. Serializer Input, Deserializer Output
WHISPER CLOCK			
WCLKIO	1	IO, LVCMOS	Extra Clock Input for WhisperClock Link – Deserializer Input. Serializer Output.
WC	1	IO, MPL	Extra WhisperClock MPL signal – Serializer is an MPL input signal, Deserializer is an MPL output signal.
POWER/GROUND PINS			
V_{DDA}	1	Power	Power Supply Pin for the MPL Interface. 3.0V ± 3%
V_{SSA}	1	Ground	Ground Pin for the MPL Interface, also known as MG (MPL Ground)
V_{DD}	1	Power	Power Supply Pin for the digital core and Serializer PLL. 3.0V ± 3%
V_{SS}	1	Ground	Ground Pin for the digital core and Serializer PLL.
V_{DDIO}	1	Power	Power Supply Pin for the parallel interface. 1.7V to 3.1V
V_{SSIO}	1	Ground	Ground Pin for the parallel interface.

Notes:
I = Input, O = Output, IO = Input/Output
Do NOT float unused inputs.

ES Revision notes

Rev D/E	Sampled on MPL200EVK	Use prior datasheet edition
Rev F	S/D* and TM pins changed to Mode[1:0]	Use this datasheet edition
Rev G	MPL RX enhancements	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DDA})	−0.3V to +TBDV
Supply Voltage (V_{DD})	−0.3V to +TBDV
Supply Voltage (V_{DDIO})	−0.3V to +TBDV
LVCMOS Input/Output Voltage	−0.3V to (V_{DDIO} +0.3V)
MPL Input/Output Voltage	TBD
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature Soldering, 4 Seconds	+260˚C
ESD Ratings:	
HBM, 1.5 kΩ, 100pF	≥±2 kV
EIAJ, 0Ω, 200 pF	≥±200V
Maximum Package Power Dissipation Capacity at 25˚C	
24L UCSP Package	TBD W
Derate TBD Package above 25˚C	TBD mW/˚C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
V_{DDA} to V_{SSA} and				
V_{DD} to V_{SS}	2.9	3.0	3.1	V
V_{DDIO} to V_{SSIO}	1.7		3.1	V
PLK Clock Frequency	4		16	MHz
WC Clock Frequency	4		28	MHz
Ambient Temperature	0	25	70	˚C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
MPL							
I_{OLL}	Logic Low Current			4.8 I_B	5.0 I_B	5.3 I_B	µA
I_{OMS}	Mid Scale Current				3.0 I_B		µA
I_{OHL}	Logic High Current			0.8 I_B	1.0 I_B	1.2 I_B	µA
I_B	Current Bias				150		µA
LVCMOS (1.7V to 3.1V)							
V_{IH}	Input Voltage High Level			0.7 V_{DDIO}		V_{DDIO} +0.3	V
V_{IL}	Input Voltage Low Level			−0.3		0.3 V_{DDIO}	V
I_{IN}	Input Current (includes I_{OZ})			−5	0	+5	µA
I_{IH}	Input Current High Level			−1	0	+1	µA
I_{IL}	Input Current Low Level			−1	0	+1	µA
V_{OH}	Output Voltage High Level	I_{OH} = −2 mA		0.8 V_{DDIO}			V
V_{OL}	Output Voltage Low Level	I_{OL} = 2 mA				0.2 V_{DDIO}	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			TBD		mA
SUPPLY CURRENT							
I_{CC}	Total Supply Current — Enabled	PCLK = 16MHz WC = 28MHz MD = 0101-1010 pattern C_L = 15 pF	Serializer		TBD	TBD	µA
			Deserializer		TBD	TBD	µA
I_{CCZ}	Supply Current — Disable	Power_Down Mode	PD* = L		1	10	µA
			PD* = L		1	10	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
PARALLEL BUS TIMING							
t_{SET}	Set Time - Data to Clock	Inputs	*Figure 2*	TBD			ns
t_{HOLD}	Hold Time - Clock to Data			TBD			ns
t_{RISE}	Rise Time	Outputs, C_L = 15 pF					ns
t_{FALL}	Fall Time						ns
PC_{LOW}	PCLK Low				50		%
PC_{HIGH}	PCLK High				50		%
t_{DVBC}	Data Valid before Clock		*Figure 2*	TBD			ns
t_{DVAC}	Data Valid after Clock			TBD			ns
SERIAL BUS TIMING							
t_{DVBC}		*Figure 1*					
t_{DVAC}							
POWER UP TIMING (see *Figures 5, 6*)							
t_1	WC Start Up Delay	*Figure 5* Planned Rev G ES test Chip will double WC cyc counts on T_1 to T_4 (SER) parameters to support higher WC rates.			100		WC_{CYC}
t_2	WC Low Initialization Low State			11	12	13	WC_{CYC}
t_3	WC Pulse Width High			11	12	13	WC_{CYC}
t_4	WC Low State			11	12	13	WC_{CYC}
t_5	WC_{IN} to WC_{OUT} Latency (SER)			6	7	8	WC_{CYC}
t_6	TBD				9		WC_{CYC}
t_7	SER PLL Lock Time	*Figure 6*			4,096		MC_{CYC}
t_8	MC Low Initialization Low State			11	12	13	MC_{CYC}
t_9	MC Pulse Width High			11	12	13	MC_{CYC}
t_{10}	MC Low State			11	12	13	MC_{CYC}
t_{11}	SER Latency				TBD		MC_{CYC}
t_{12}	DES Latency				TBD		MC_{CYC}
POWER OFF TIMING							
t_{PAZ}	Disable Time to Power Off						µs
t_{PZA}	Enable Time from Power Off						µs

Input Timing Requirements

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
REFERENCE CLOCK ($WCLK_{IN}$)						
f_{WC}	Clock Frequency		4		28	MHz
WC_{DC}	Clock Duty Cycle		45	50	55	%
t_T	Clock Transition Times (Rise or Fall, 10%–90%)		1		6	ns
PIXEL CLOCK (PCLK)						
f_{PCLK}	Clock Frequency		4		16	MHz
t_{CP}	Clock Period		62.5		250	ns
CLK_{DC}	Clock Duty Cycle		45	50	55	%
t_T	Clock transition Time		1		6	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for $V_{DD} = V_{DDA} = 3.0V$ and $V_{DDIO} = 2.7V$ and $T_A = 25^{\circ}C$.

Note 3: Current into a device pin is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to Ground unless otherwise specified.

Timing Diagrams

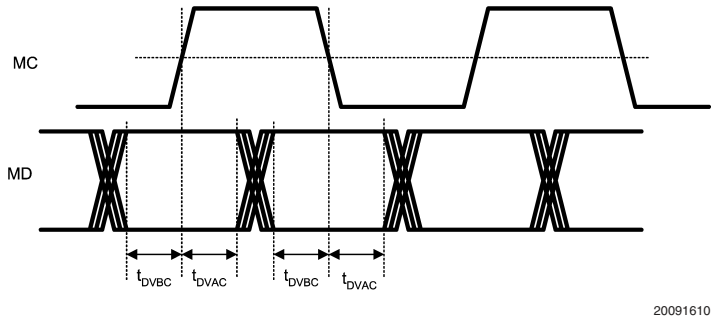


FIGURE 1. Serial Data Valid

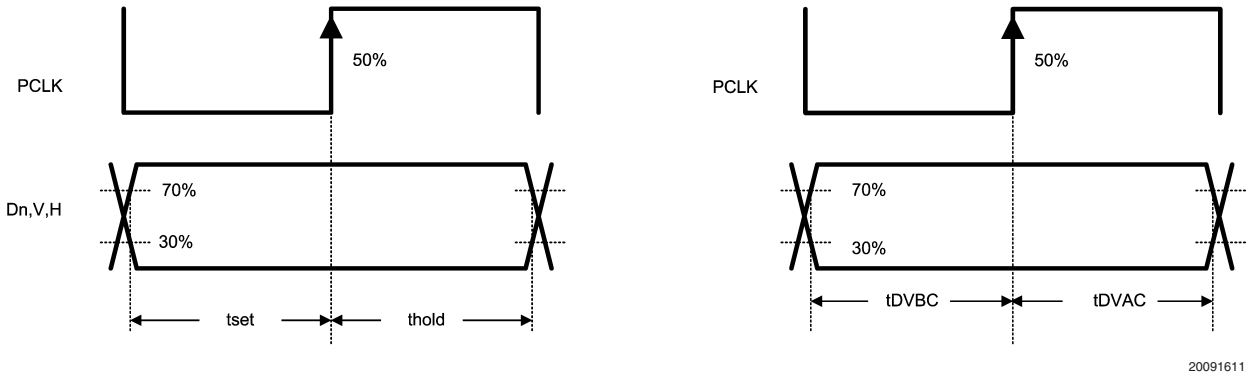


FIGURE 2. Parallel Set, Hold and Data Valid

Application Information

Typical application connections for the LM2501 are shown below.

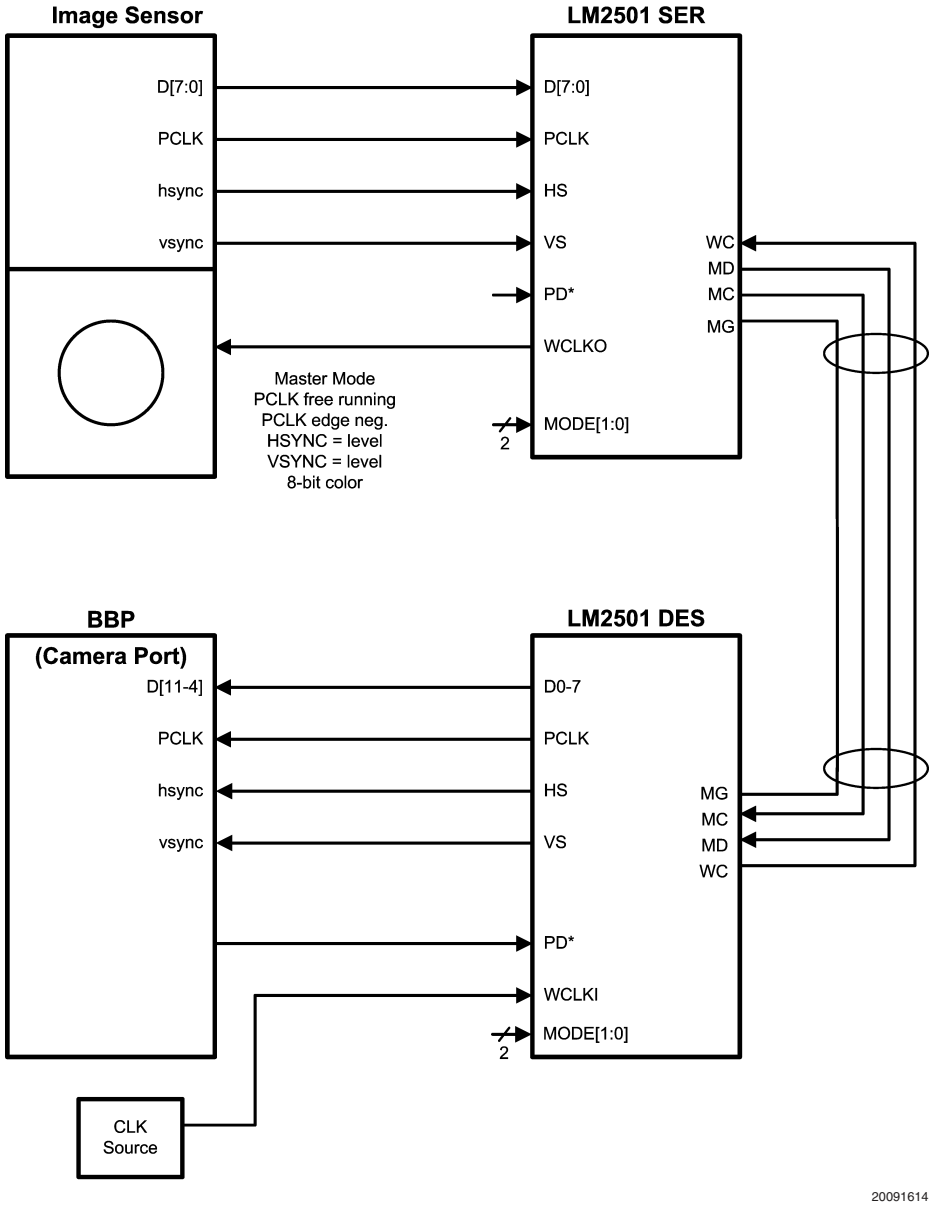


FIGURE 3. Camera Application

The application shown in *Figure 3* illustrates a connection between an Image sensor and a host utilizing an MPL-0 link. .

Functional Description

SERIAL BUS OPERATION

Bus Overview

The MPL bus is a simple 2-signal line interface that is intended to replace wide low voltage CMOS video busses inside handheld portable devices. The MPL physical layer is purpose-built for an extremely low power and low EMI data transmission while requiring the fewest number of signal lines. No external line components are required, as termination is provided internal to the MPL receiver. The MPL interface is designed to be used with common 50 Ω lines using standard materials and connectors. Lines may be microstrip or stripline construction. Total length of the interconnect is expected to be less than 0.3 meters. This device is meets the requirements of the MPL-0 Standard (PHY Layer only).

SERIAL BUS TIMING

Data valid is relative to both edges as shown in *Figure 4*. Data valid is specified as: Data Valid before Clock, Data Valid after Clock, (Note relative to both edges).

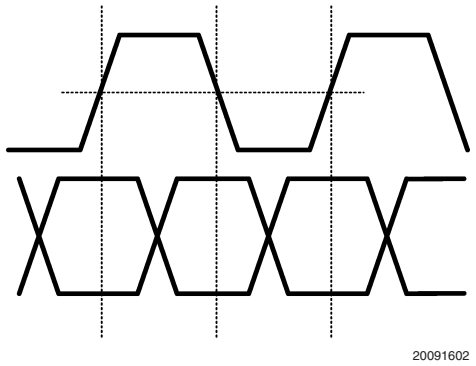


FIGURE 4. Master-to-Slave Timing (MC, MDm)

SERIAL BUS PHASES

There are three bus phases on the MPL serial bus. These are determined by the state of the MC and MD lines. Two of the bus phases have options. The MPL bus phases are shown in *Table 1*.

TABLE 1. MPL Bus Phases

Name		WC State	MC State	MD State	Phase Description	Pre-Phase	Post-Phase
OFF (O)		0	0	0	Bus is Powered-Off	na	I (WC)
Initialization (I)	WC	A	0	0	WC Start Up	O	I (MC)
	MC/MD	A	A	0	MPL Start Up	I (WC)	A
Active (A)		A	A	X	Data Out (Write)	I (MC)	A or O

Notes on Line State: 0 = no current (off), L = Logic Low, H = Logic High, X = Low or High, A — Active Clock

Functional Description (Continued)

SERIAL BUS POWER-UP

In the sleep state, WC, MC and MD are turned off with zero current flowing. Both devices need to be enabled by asserting their PD* inputs. The DES will then initialize the SER via the WC signal as shown in *Figure 5*. The DES waits 7 WC cycles before its $WCLK_{out}$ is active. Note, there is no phase or frequency relationship between WC and MC.

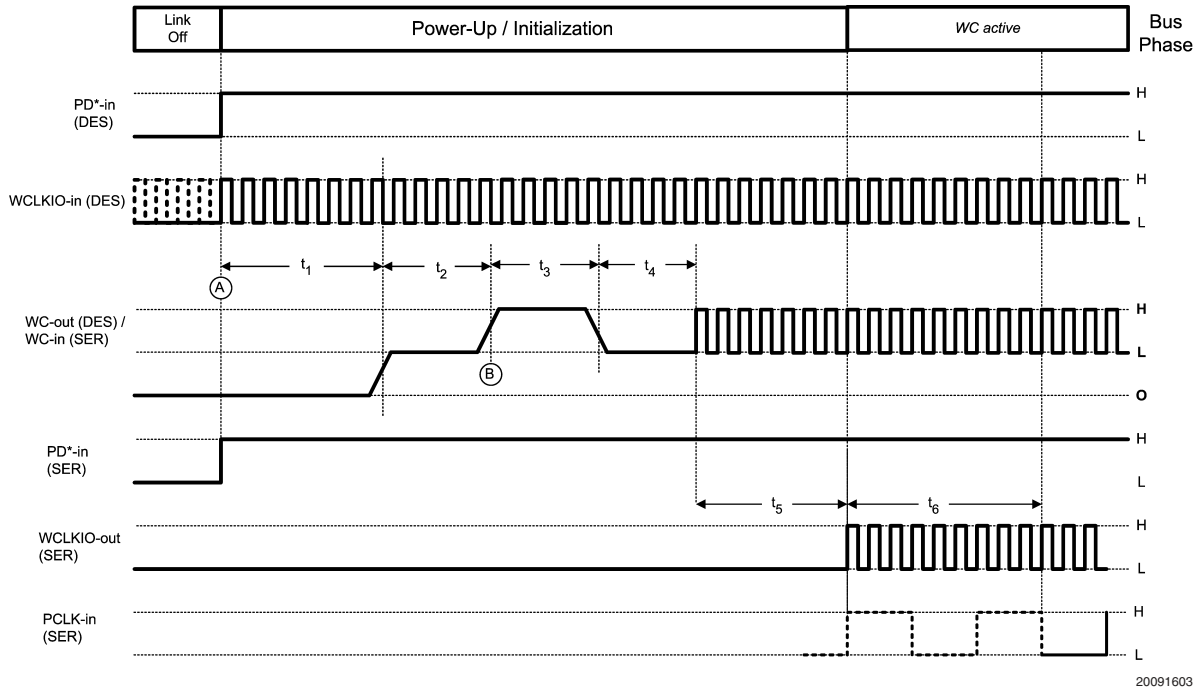


FIGURE 5. Bus Power Up Timing — WC

Functional Description (Continued)

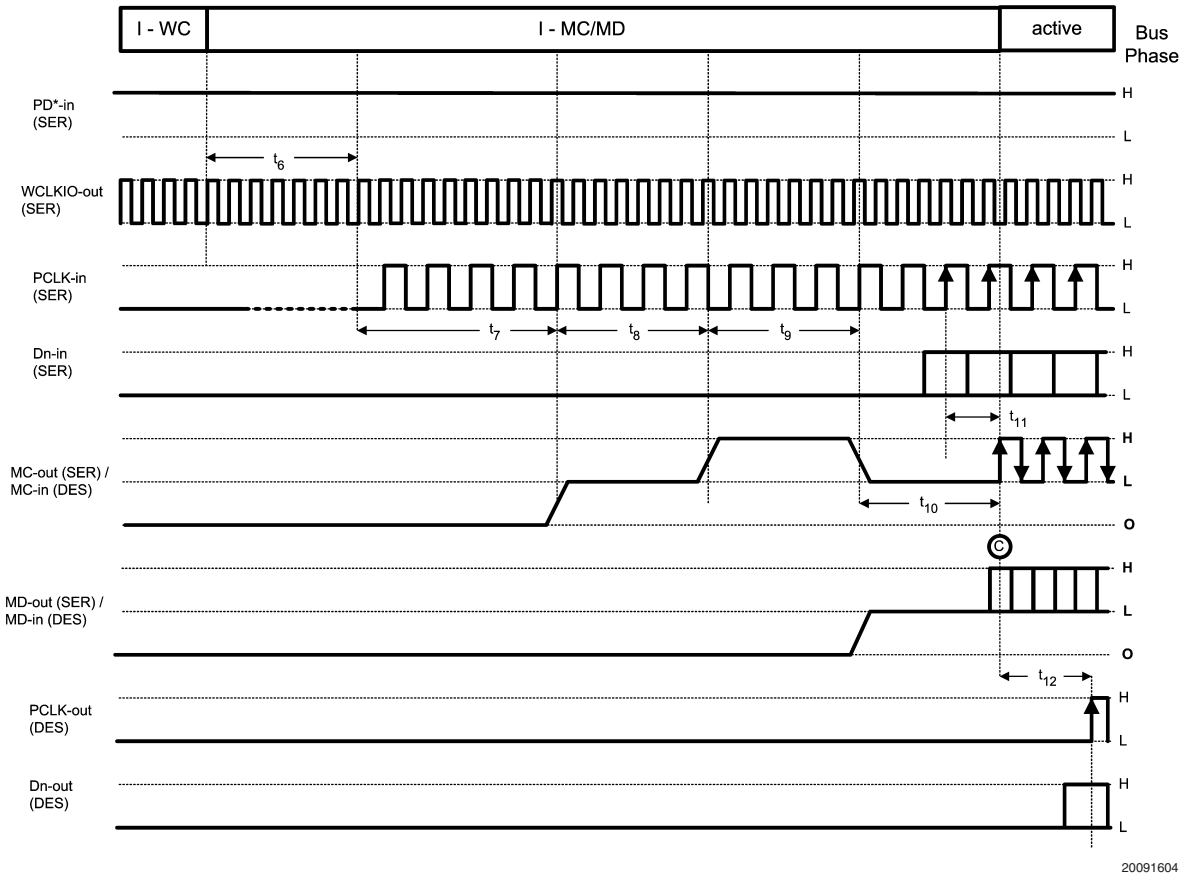


FIGURE 6. Bus Power Up Timing — MC/MD

In *Figure 6*, the Serializer timing is shown. For the part to establish lock, WCLKIO(out) must be active, and a valid PCLK applied. After lock is obtained, the MC and MD lines are initialized and then active transmission occurs. *Table Switching Characteristics* lists the timing parameters of *Figures 5, 6*.

SERIAL BUS POWER-OFF

In the power-off state, WC, MD and MC are turned off with zero current flowing. This is considered the Sleep state (Power-off) and the transition off may occur after the last data bit time or at any time afterwards from an Idle phase as shown in *Figure 7*.

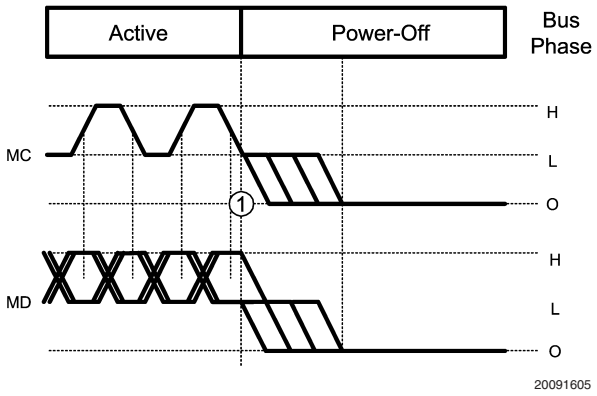


FIGURE 7. Bus Power Down Timing

Functional Description (Continued)

CAMERA INTERFACE

The Camera Interface provides serialization of color and control bits. The interface provides data transport in a single direction. Byte alignment is provided by the intrinsic first rising edge of the MC line. PCLK is required and must be **free-running**. Data may be raw Bayer or BT656 color information. Data is strobed on the **rising-edge** on the input to the Serializer. Data is sent LSB first (D0).

MPL provides the data transport path, control of the Camera device is provided by an I^2C control bus.

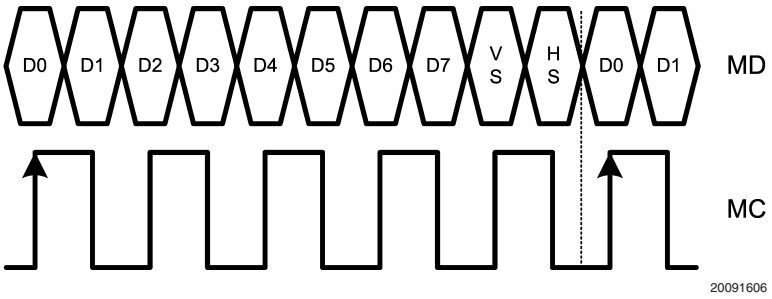


FIGURE 8. Camera Mode Serial Interface

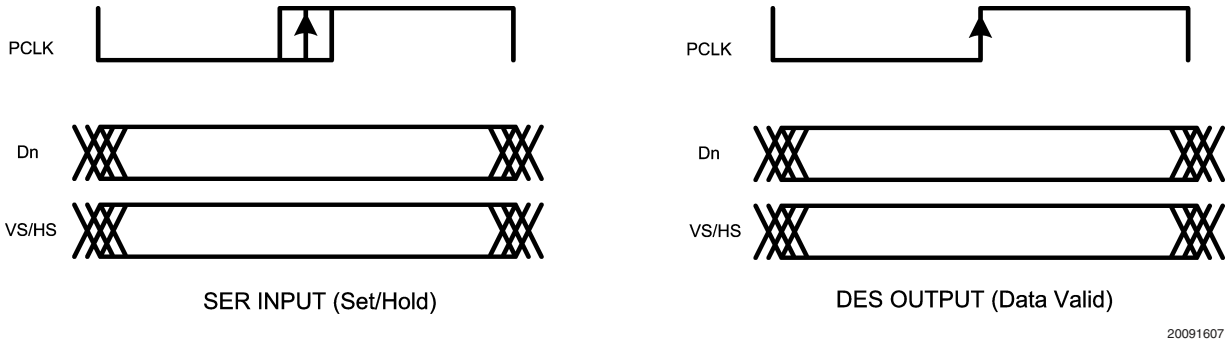


FIGURE 9. Parallel Bus Timing

Features and Operation

POWER DOWN/OFF

The device may be powered by its PD* pin. A Low on this pin will power down the entire device.

TABLE 2. Power Down Output States

Mode	Pin	Type	Output State in Power Down
SER	WCLKIO	LVCMOS	LOW
SER	MC	MPL	OFF
SER	MD	MPL	OFF
DES	D[0:7]	LVCMOS	LOW
DES	V, H	LVCMOS	LOW
DES	PCLK	LVCMOS	LOW
DES	WC	MPL	OFF

UN-USED/OPEN INPUTS

Un-used control/inputs pins must be driven to their appropriate logic states to set up the desired operating modes.

UN-USED OUTPUTS

Unused outputs should be left open to minimize power dissipation.

POWERING UP

The LM2501 should be powered up with all power supplies at the same time, alternately VDDIO may lag VDD and VDDA. Do not power up with VDDIO before VDD and VDDA.

PHASE-LOCKED LOOP

When the device is configured as a Serializer, a PLL is provided to generate the serial link clock. The Phase-locked loop system generates the serial data clock at five times the input clock. The PLL operates with an input clock between 4 MHz and 16 MHz. The Deserializer does not utilize the PLL and its PLL is powered down.

RESET

PD* should be held Low until the power supply has powered up and is stable. The PD* should then be de-asserted to generate a RESET and start up. Stopping the WCLKIO or the PCLK will not RESET the part. A power cycle or PD* cycle is requested to generate a RESET event.

SERIALIZER/DESERIALIZER SELECTION

The Mode[1:0] pins are used to configure the device as either a Serializer or Deserializer and other configuration options.

WHISPERCLOCK

An additional clock signal is sent from the Deserializer to the Serializer. This can be used to pass a clock reference (4 MHz to 28 MHz) up to the Camera device from the host. This link is independent of the Serial data path (opposite direction). See also *Figure 5*. The SER can only start up, if the WCLKIO(ser-out) has been active.

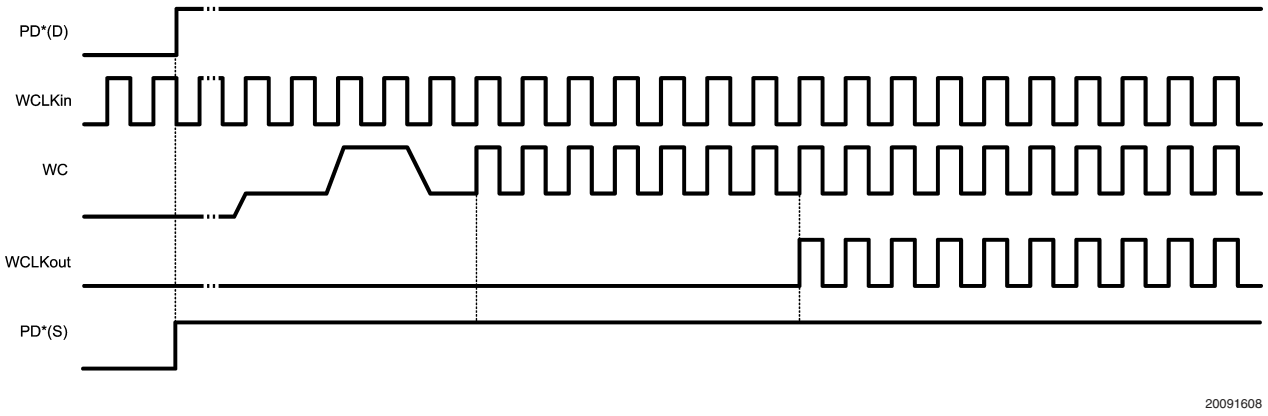


FIGURE 10. Sleep to Active

Features and Operation (Continued)

When the Deserializer's PD* signal is de-asserted, the WC output will power up and initialize the serializer and start transmitting the clock reference. Once the Serializer received the clock, it waits seven cycles, and then outputs the clock signal. Seven cycles later, the Serializer's PLL will begin to lock if PCLK is present.

When the Deserializer's PD* signal is asserted, the WC signal is turned off.

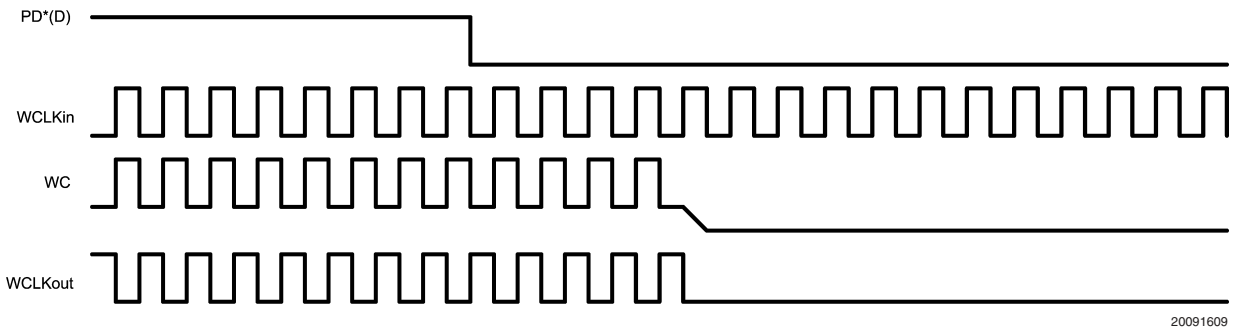


FIGURE 11. Active to Sleep

MISC. Definitions:

Bus States:

Logic Low — 5Idata flowing from the Receiver to the Driver

Logic High — Idata flowing from the Receiver to the Driver

Power Off — No Current flowing in the interconnect

Signals & Nomenclature:

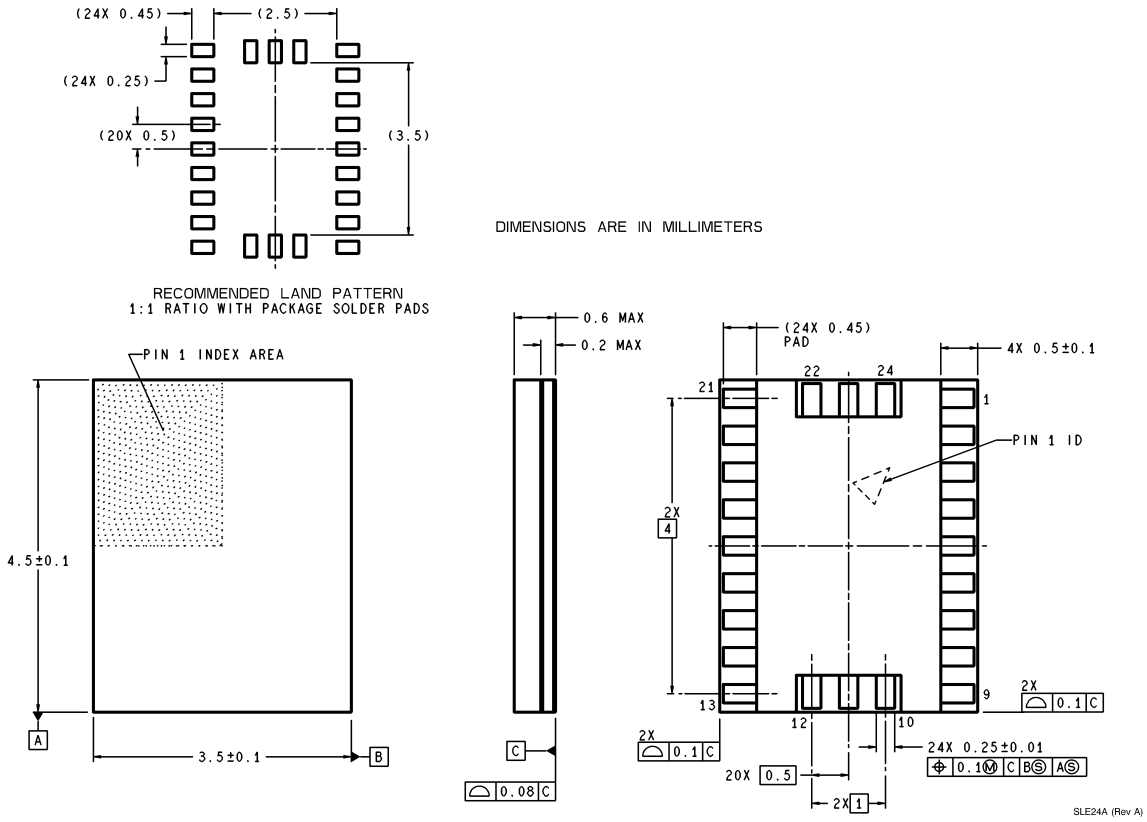
MD = MPL Data Signal, subscript denotes source, m = master, s = slave

MC = MPL Clock Signal

WC = MPL WhisperClock Signal

* = Active Low Signal

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number LM2501SL
NS Package Number SLE24A

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