Description

The main function of the SX8722 is to acquire signal from Wheatstone bridges or single ended sensors.

The input can be a pressure sensor, a GMR or AMR magnetic sensor, a chemical sensor, a thermistor or a mix of several of these sensors.

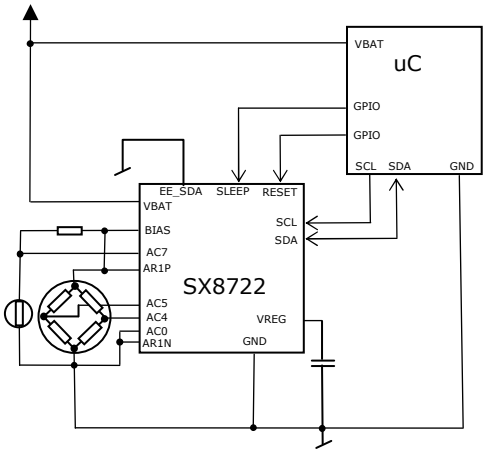
The SX8722 Sensor interface is totally configurable through an I^2C compatible interface.

Several parameters are configurable through this interface such as alarms or signal post processing.

Applications

- Pressure sensing (industrial, altimeter, diving computer)
- Chemical sensing (monitoring, security)
- Magnetic sensing (compass)

Typical Application Circuit

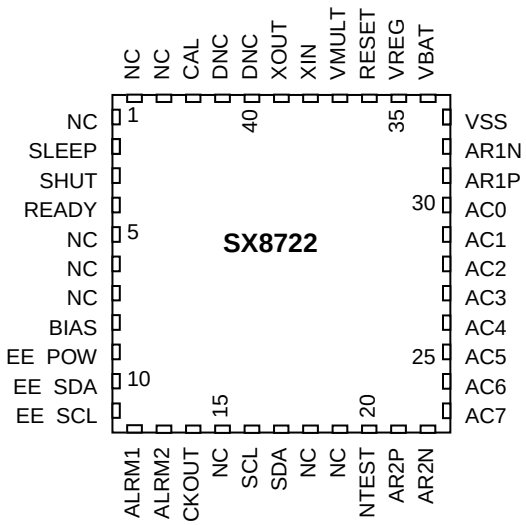


Typical pressure & temperature sensing application with sleep control

Features

- 16 + 10 bits differential acquisition
- Preamplifier programmable gain up to 1000
- Sensor offset compensation up to 15 times full scale of input signal
- 4 differential or 7 single ended signal inputs
- 2 differential reference inputs
- I2C compatible connection to application
- Internal RC and 32kHz Oscillators
- Low power modes
  - o Sleep
  - o Shutdown
- 4 Full configuration pre selections including:
  - o ZoomingADC™ configuration
  - o 2 alarms with on & off thresholds
  - o Digital filtering
- I2C EEPROM interface
- Clock out pin
- Calibration pin
- Reset pin
- Ready / Busy pin

Pin configuration



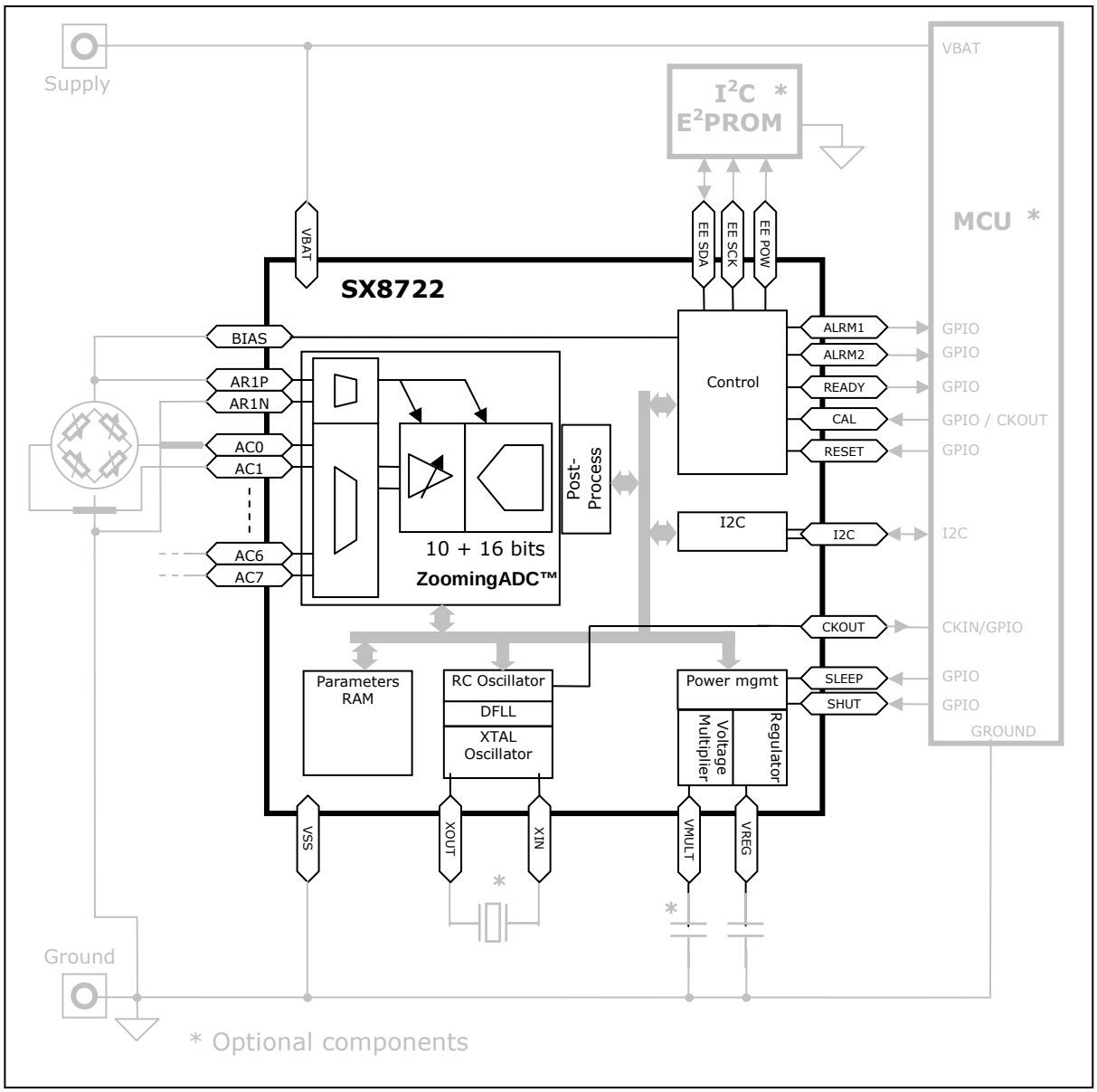
7x7mm MLPQ 44

Table of contents

Ordering information

SX8722I070LF	IC	MLPQ 7x7mm 44pin, -40 to 85°C, tape & reel
XE8000EV120	SX8722 evaluation kit	

SX8722 Block diagram



Pin description

Pin	Name	Type	Description	Status at POR
1	NC		Not connected	
2	SLEEP	I	Sleep pin, sets the circuit in sleep mode	Internal pull-up
3	SHUT	I	Shutdown pin, sets the circuit in shutdown mode	Internal pull-up
4	READY	O	Is high when a measurement data is available	Low
5	NC		Not connected	
6	NC		Not connected	
7	NC		Not connected	
8	BIAS	O	Bias pin, is high when a measurement is performed	Low
9	EE_POW	O	Supply pin for the management of the optional EEPROM	Low
10	EE_SDA	IO	Data pin of the optional EEPROM	Low
11	EE_SCL	IO	Clock out pin of the optional EEPROM	Low
12	ALRM1	O	Alarm 1 pin, is high when alarm 1 "on" threshold is reach	Low
13	ALRM2	O	Alarm 2 pin, is high when alarm 2 "on" threshold is reach	Low
14	CKOUT	O	System clock output	Low
15	NC		Not connected	
16	SCL	IO	Serial clock in of the I2C Compatible interface	Input
17	SDA	IO	Serial data of the I2C Compatible interface	Input
18	NC		Not connected	
19	NC		Not connected	
20	NTEST	I	Must be connected to Vbat	
21	AR2P	A	Second Analog reference input (positive pin)	
22	AR2N	A	Second Analog reference input (negative pin)	
23	AC7	A	ZoomingADC™ input 7	
24	AC6	A	ZoomingADC™ input 6	
25	AC5	A	ZoomingADC™ input 5	
26	AC4	A	ZoomingADC™ input 4	
27	AC3	A	ZoomingADC™ input 3	
28	AC2	A	ZoomingADC™ input 2	
29	AC1	A	ZoomingADC™ input 1	
30	AC0	A	ZoomingADC™ input 0	
31	AR1P	A	First Analog reference input (positive pin)	
32	AR1N	A	First Analog reference input (negative pin)	
33	VSS	Power	Negative power supply	
34	VBAT	Power	Positive power supply	
35	VREG	A	External capacitor for the internal regulator	
36	RESET	I	Reset the SX8722 when high	
37	VMULT	A	External capacitor for the internal voltage multiplier	
38	XIN	I	XTAL connection, left unconnected when not used	
39	XOUT	O	XTAL connection, left unconnected when not used	
40	DNC		Do not connect	Internal pull-up
41	DNC		Do not connect	Internal pull-up
42	CAL	I	Calibration pin, set low to use XTAL.	Internal pull-up
43	NC		Not connected	
44	NC		Not connected	

Type: I: digital input, O: digital output, IO: digital I/O, A: analog

Absolute maximum ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Parameter	Symbol	Conditions	Min	Max	Unit
Power supply	V_{BAT}		V_{SS} – 0.3	5.5	V
Storage temperature	T_{STORE}		-55	150	°C
Temperature under bias	T_{BIAS}		-40	125	°C
Max sensor common mode	V_{VR_P}		V_{SS} - 300	V_{BATT} +300	mV
	V_{VR_N}				
Input voltage			V_{SS} - 300	V_{BATT} +300	mV
Peak soldering temperature	T			260	°C

Notes

1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Electrical characteristics

All values valid within the operating conditions unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating conditions						
Power supply	V_{BATT}		2.4		5.5	V
Operating temperature	T_{OP}		-40		85	°C
Current consumption						
Active current	I_{OP}			TBD		µA
Sleep current[1]	I_{sleep}			1.6	2.0	µA
Sleep current[2]	I_{sleep}			4.5	5.0	µA
Shutdown current	I_{shut}			0.5	0.9	µA
Time base						
Time base error		T=25°C, V_{BATT}=5V			TBD	%
		operating range			TBD	%
Digital I/O						
Input logic high	V_{IH}		0.7			V_{BATT}
Input logic low	V_{IL}				0.3	V_{BATT}
Output logic high	V_{OH}	I_{OH}<4mA	V_{BATT} -0.4			V
Output logic low	V_{OL}	I_{OL}<4mA			0.4	V

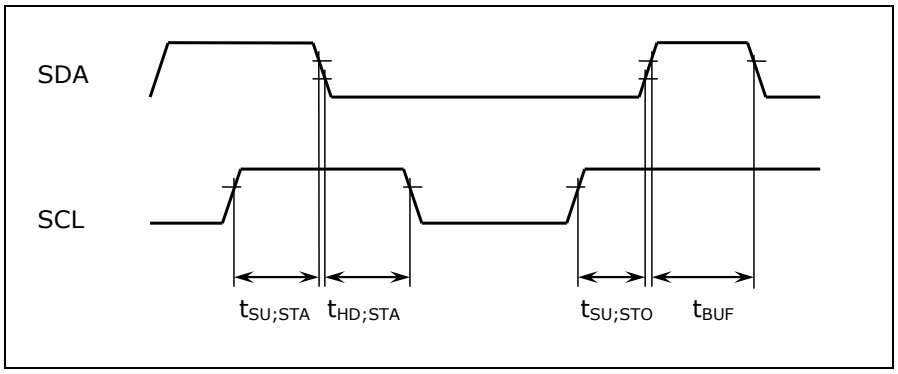
[1] With external 32.768kHz Xtal connected
[2] Without external 32.768kHz Xtal connected

Electrical characteristics (Cont.)

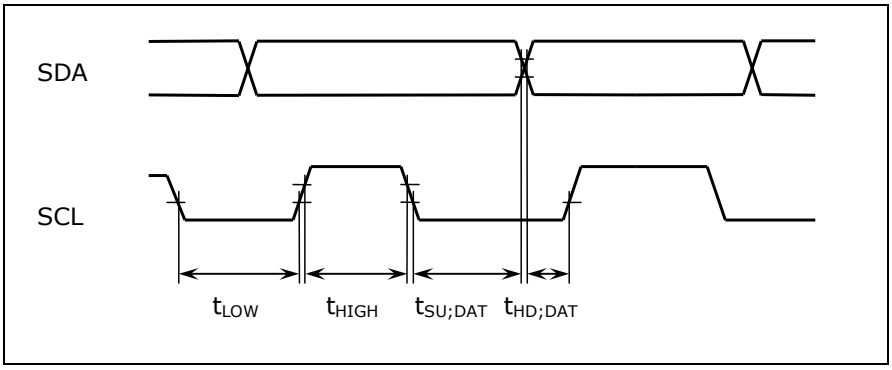
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Two wire bus timing specification(1)						
SCL clock frequency	f_{SCL}		0		100	kHz
SCL low period	t_{LOW}		4.7			µs
SCL high period	t_{HIGH}		4.0			µs
data setup time	$t_{SU;DAT}$		250			ns
data hold time	$t_{HD;DAT}$		4.0			ns
Repeated start setup time	$t_{SU;STA}$		4.7			µs
Start condition hold time	$t_{HD;STA}$		4.0			µs
Stop condition hold time	$t_{HD;STO}$		4.0			µs
Bus free time between start and stop	t_{BUF}		4.7			µs

Notes
1) All timing specifications are referred to V_{ILmin} and V_{IHmax} voltage levels defined for the SCL and SDA pins.

The diagram below shows the START & STOP conditions timing



The diagram below shows the data timings.



Functional description

The SX8722 is a ZoomingADC™ with I2C compatible interface allowing multiple setups.

The major modules of the SX8722 are the ZoomingADC™, the signal post processing, the control unit and the power management

The SX8722 offers several configuration possibilities allowing the developer to use it as a peripheral of its system or to use it as a stand alone system generating alarms.

The ZoomingADC™ is made of 1 input multiplexer, 3 programmable gain amplifiers and a 16 bits ∑Δ ADC.
The input multiplexer allows measuring 4 differential sensors or 7 single ended sensors or a combination of differential and single-ended.
The total gain of the PGA enables an amplification of 1000 and the offset correction can reach up to 15 times the full scale input signal.

The SX8722 is not only giving access to the very efficient ZoomingADC™ technology, it also gives access to a very low power acquisition system entirely configurable to reach as low as 0.5uA in shutdown mode.
The low power modes can be reached through pins or specific serial commands.

The whole chip is controlled by a set of registers; these registers have factory default settings and can be modified in 2 ways: the serial interface commands or an optional external EEPROM.
At Startup the SX8722 checks for EEPROM presence and updates its registers with EEPROM contents.

The whole chip is working at 1.2MHz using its internal RC oscillator, this frequency can be calibrated.

The clock calibration can be done using several methods: External 32.768 kHz XTAL, External 32.768 kHz reference signal, or EEPROM parameter configuration.

Several corrections can be applied on the measured signal such as different digital filters.

The SX8722 offers two alarm pins. "on" and "off" thresholds can be set independently.

A Clock out pin can be enabled to have the exact frequency of the core available.

External EEPROM and sensors can be biased by the dedicated SX8722 pins EE_POW and BIAS allowing the most efficient power management.

The pin READY is a single signal that can be used to interrupt the host microcontroller.

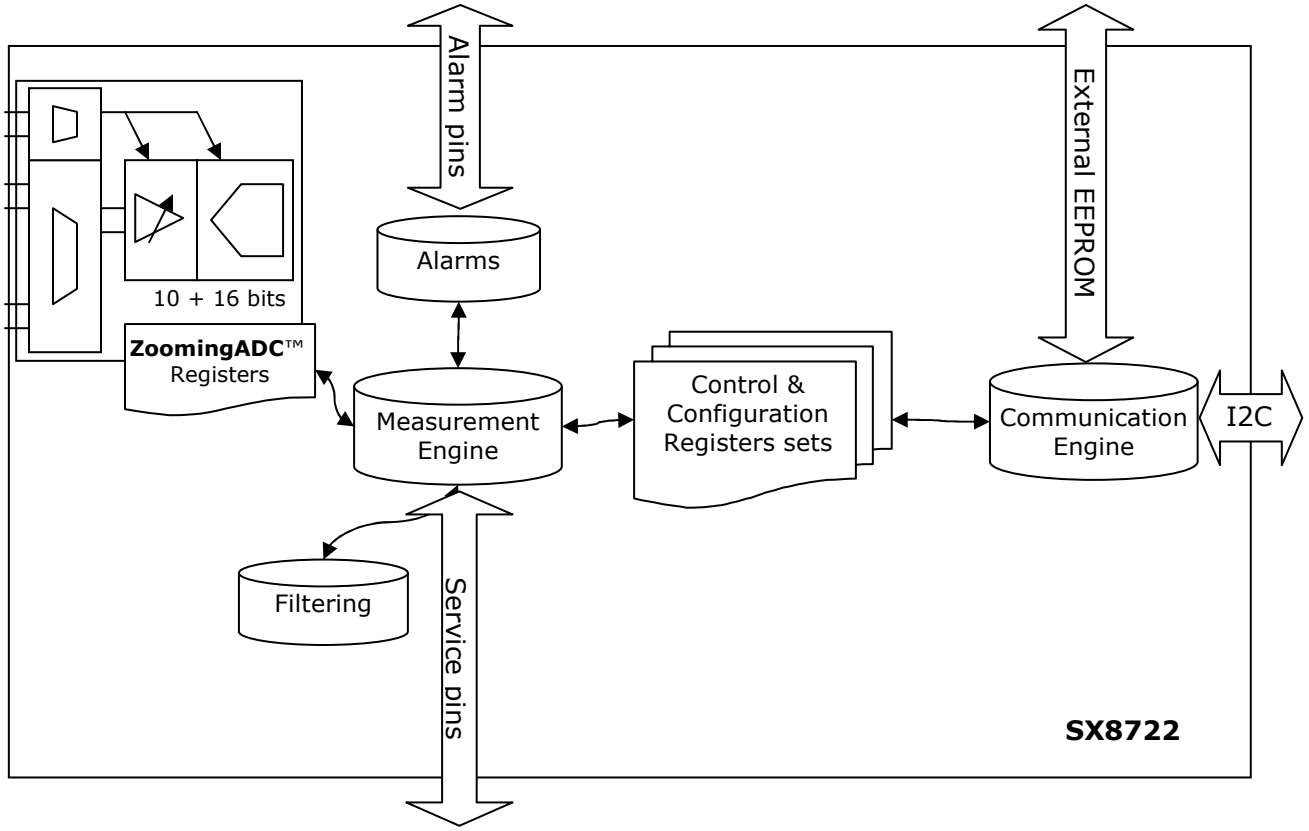
The RESET pin enables the host system to reset the SX8722 to its startup settings at any time.

The internal voltage multipliers is automatically enabled when working below 3 Volts

Functional description (Cont.)

The SX8722 implements 4 configuration register sets. Each of these sets completely defines the behavior of the ZoomingADC™. This allows the user to preset 4 different measurement configurations that can be activated by setting a single bit.

The diagram below explains the registers sets system more in details:

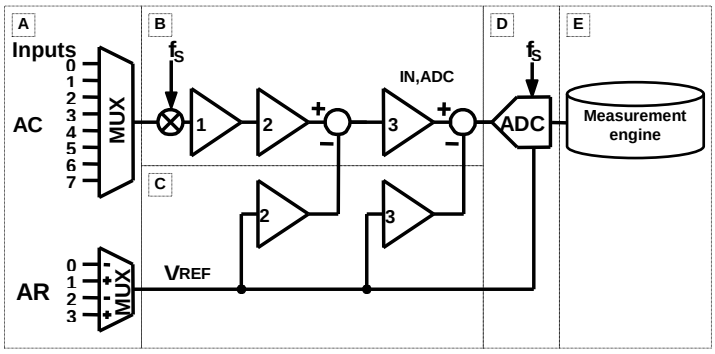


The measurement engine copies the configuration register sets in the ZoomingADC™ physical registers and writes back the conversion results.

The communication engine controls read/write access from the I2C or the external EEPROM.

Functional description (Cont.)

The SX8722 core is the ZoomingADC™, the diagram below shows more in detail the architecture of this acquisition chain.



The block schematic above is separated in function boxes:

A. Input multiplexers
   - Routing of the input signal.
   - Routing of the reference.

B. Programmable gain amplifiers
   - Can be enabled/disabled separately.
   - Each PGA has programmable gain from 1 to 10.
   - Total PGA gain available = PGA1 x PGA2 x PGA3 = 1000.

C. Offset cancellation
   - Subtract or add a reference multiple to the input signal.
   - Can compensate up to 15 times the full scale signal.

D. ADC
   - Sigma-Delta ADC.
   - Offers several sampling frequencies.
   - Over sampling rates and elementary conversion combinations allow setting the ideal resolution for the ideal conversion time.

E. Measurement engine
   - Manages up to 4 ZoomingADC™ configurations.
   - Updates the measured values.

SX8722 registers map

This chapter summarizes the SX8722 registers and their addresses.
Detailed description can be found in "Advanced configuration" section.

SX8722 General control registers (addresses 0x00 to 0x03)

Hex	Register	Description
0x00	SXCtrl1	Control register of the SX8722
0x01	SXCtrl2	Control register of the SX8722
0x02	SXCfgEn	Configuration enable register, enables configurations from 1 to 4
0x03	SXUpdated	Updated value on configuration registers

Table 1 SX8722 General control registers (addresses 0x00 to 0x03)

SX8722 Configuration1 registers (addresses 0x0A to 0x1B)

Hex	Register	Description
0x0A	C1ZAdcReg1	ZoomingADC™ Register 01
0x0B	C1ZAdcReg2	ZoomingADC™ Register 02
0x0C	C1ZAdcReg3	ZoomingADC™ Register 03
0x0D	C1ZAdcReg4	ZoomingADC™ Register 04
0x0E	C1ZAdcReg5	ZoomingADC™ Register 05
0x0F	C1ZAdcReg6	ZoomingADC™ Register 06
0x10	C1SXCfg1	SX configurations related to this set
0x11	C1FParam	Filter size
0x12	C1Alrm1OnMsb	Alarm 1 "ON" threshold msb
0x13	C1Alrm1OnLsb	Alarm 1 "ON" threshold lsb
0x14	C1Alrm1OffMsb	Alarm 1 "OFF" threshold msb
0x15	C1Alrm1OffLsb	Alarm 1 "OFF" threshold lsb
0x16	C1Alrm2OnMsb	Alarm 2 "ON" threshold msb
0x17	C1Alrm2OnLsb	Alarm 2 "ON" threshold lsb
0x18	C1Alrm2OffMsb	Alarm 2 "OFF" threshold msb
0x19	C1Alrm2OffLsb	Alarm 2 "OFF" threshold lsb
0x1A	C1DataOutMsb	Configuration 1 data out MSB
0x1B	C1DataOutLsb	Configuration 1 data out LSB

Table 2 Configuration 1 (addresses 0x0A to 0x1B)

The configuration registers 2 to 4 have the same organization and their addresses are as follow:
configuration2 0x2A – 0x3B
configuration3 0x4A – 0x5B
configuration4 0x6A – 0x7B

Access the SX8722

Description

The SX8722 is configured trough register sets and general control registers.

All the accesses to the SX8722 registers are done through the I2C interface using read and write commands.

The next paragraph describes two approaches to configure the SX8722

SX8722 configuration

As it will be shown in the next chapter there are two ways to write data in the SX8722 registers:

- Direct write: This command writes 8 bits to a defined address. This implies knowledge of the value to be written to this address.
- Masked write: This command can write a single bit in a byte using a mask.

SX8722 Commands

This chapter describes the commands that are coded in the SX8722.

The SX8722 commands are summarized below, detailed timing diagrams can be found at the end of this document under "Electrical characteristics" section.

Type	Command	Description	Byte
Data access	write_direct	Writes 8bit data to a given address	0x10
	write_masked	Writes bits to given address using a given mask	0x20
	read	Reads 8bit data from a given address	0x30
SX8722 MODES	sleep	Sets the SX8722 to sleep mode	0x40
	shutdown	Sets the SX8722 to shutdown mode	0x50
	reset	Resets the SX8722	0x60
EEPROM	save_eeprom	Saves the SX8722 registers in the external EEPROM (if present)	0x70
	load_eeprom	Loads the SX8722 registers with the content of the external EEPROM (if present)	0x80

Table 3 SX8722 commands

Serial communication

The serial interface is a read-write 2 wire slave device. The SCL wire carries the clock information and SDA carries the data. The output drivers on the bus are open drain current sinks.

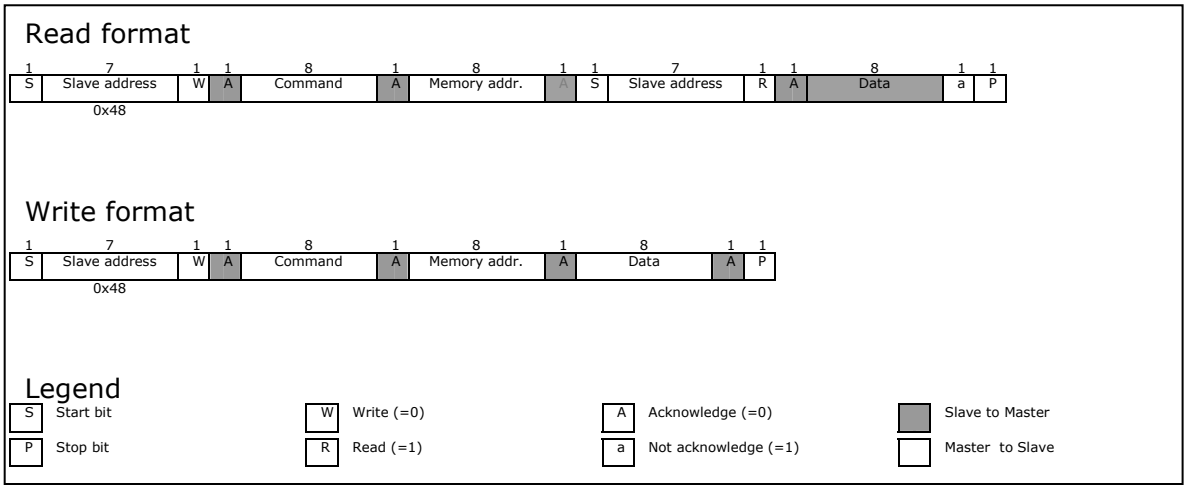
The SCL wire is controlled by the master on the bus. Since the SX8722 is fairly slow, it may stretch the low clock phase when required. The SDA wire is controlled by the master or the slave depending on the operation.

SDA only changes while the clock signal is low except for the (repeated) start or stop conditions.

The (repeated) start condition for the transmission is a high to low transition on SDA while SCL is high. The stop condition is a low to high transition while SCL is high.

To read data from the SX8722, the master has to send successively a start bit, the slave address, a write bit. If the slave address corresponds to the address of the SX8722 and the preceding operation is completed, the SX8722 sends an acknowledge bit. The master then sends the read command which is acknowledged by the salve, the memory address that it would like to read which is also acknowledged by the slave. The master issues a repeated start, repeats the slave address and read bit. The slave acknowledges and returns the data to the master. The master terminates the communication by a "not acknowledge" and a stop bit.

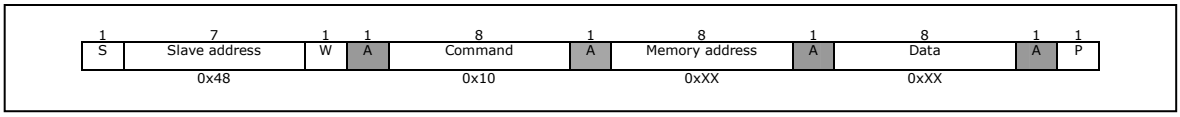
To write data to the SX8722, the format is very similar. Only the data direction is different and the acknowledgement of the slave after the data reception.



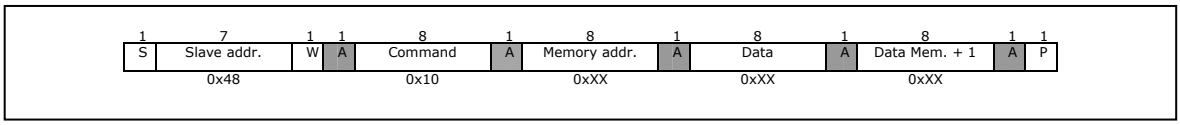
Serial communication (Cont.)

Write data direct

The diagram below shows the write operation.

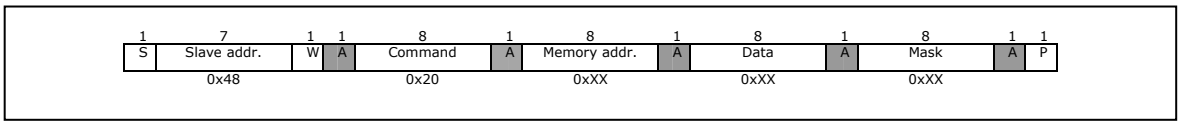


The diagram below shows the write operation at successive addresses (burst mode)



Write data masked

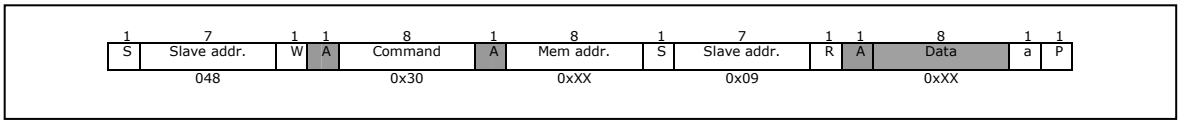
The diagram below show the write masked operation.



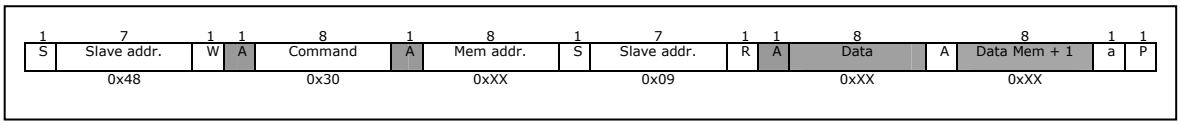
Serial communication (Cont.)

Read data

Read data diagram.



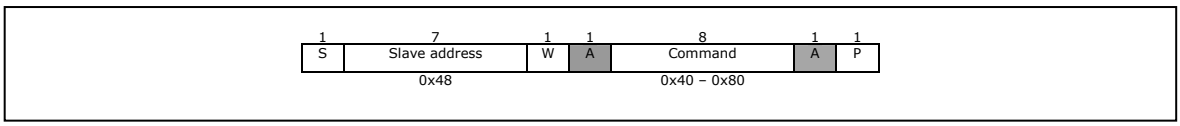
Read data diagram successive addresses (burst mode)



Note: If a read sequence is initiated without sending previously an address, the data shifted out will be the latest conversion result and its corresponding configuration ID (24 bits). See next page for more information.

Other commands

The diagram below shows the other commands syntax.



Unknown commands

The SX8722 does not answer to unknown commands.

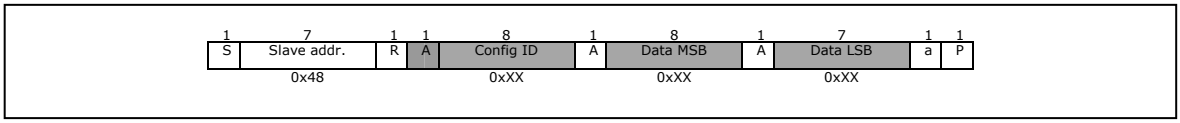
Serial communication (Cont.)

Reading data after a measurement.

The SX8722 performs measurements successively and stores the latest results in the enabled configurations data out registers.

Every time a measurement is performed the pin READY makes a positive pulse allowing the host microcontroller to retrieve data from the SX8722.

When the SX8722 is addressed and read the output is as shown below. Config ID indicates which channel is shifted out.



Predefined settings

Introduction

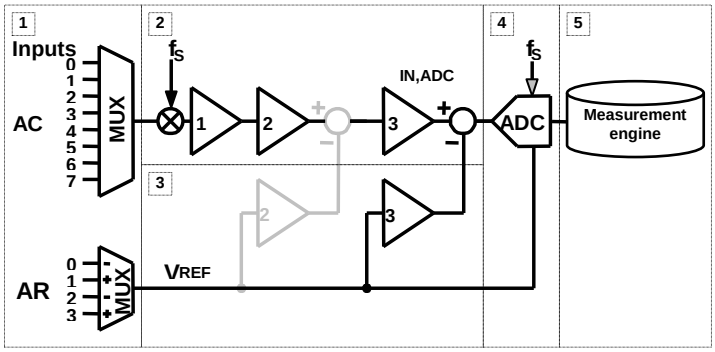
This chapter intends to ease the handling of the SX8722 using a set of predefined settings.
These settings are covering a large range of the SX8722 possibilities.

However to avoid too much complexity some features are not handled by these settings.

A more detailed use of the SX8722 can be found under the "advanced configuration" of this document.
This chapter contains predefined command using the masked write mode.

All the settings described in this chapter use the addresses of the 1st configuration register set, use the registers definition table to translate them to other register sets.

Features covered by predefined settings



The block schematic above shows the functions covered and controlled by the predefined settings set.
It includes:

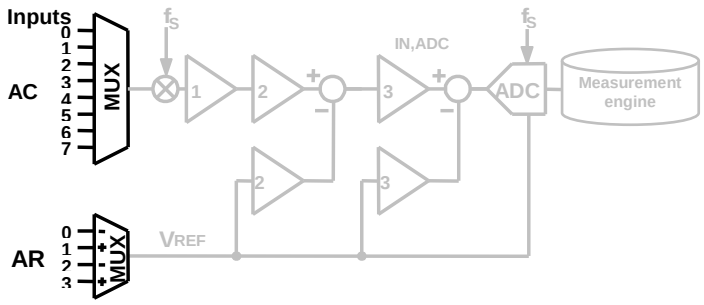
1. The input multiplexers
2. The programmable gain amplifiers
3. The offset cancellation
4. The ADC
5. The Measurement engine

Note: Grayed out blocks in the schematic means that they are not used in the current function.

Predefined settings (Cont.)

Input multiplexers

Overview



The diagram above shows the input multiplexer organization; these are enabling the selection of both the input and the reference sources.

Input channel selection.

The following settings allow configuring the input multiplexers of the ZoomingADC™

Differential mode

Function	Address	Data	Mask
AC0 – AC1	0x0F	0x00	0x06
AC2 – AC3		0x02	
AC4 – AC5		0x04	
AC6 –AC7		0x06	

Single-ended mode

Function	Address	Data	Mask
AC0 – AC1	0x0F	0x22	0x2E
AC0 – AC2		0x24	
AC0 – AC3		0x26	
AC0 – AC4		0x28	
AC0 – AC5		0x2A	
AC0 – AC6		0x2C	
AC0 – AC7		0x2E	

Invert input polarity

Function	Address	Data	Mask
Sign inversion	0x0F	0x10	0x10

Predefined settings (Cont.)

Input multiplexers cont'd

Reference channel selection

Function	Address	Data	Mask
AR1P – AR1N	0x0F	0x00	0x01
AR2P – AR2N		0x01	

Application example

In this example we want to measure a signal between AC0 and AC1 in single ended having a reference voltage between AR1P and AR1N.

The following settings must be sent to SX8722:

Function	Address	Data	Mask
Set input to AC1 – AC0	0x0F	0x00	0x06
Set reference to AR1P – AR1N	0x0F	0x00	0x01

Note: This command can be optimized, since the reference and input setting are sharing the same address the mask and the settings can be added.

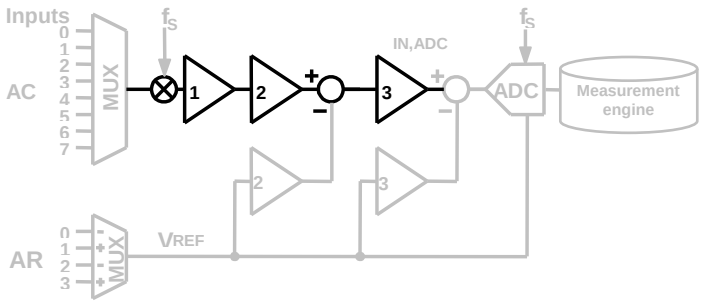
The following command shows the optimized way

Function	Address	Data	Mask
Set input to AC1 – AC0, set reference to AR1P – AR1N	0x0F	0x00	0x07

Predefined settings (Cont.)

Programmable gain amplifier settings

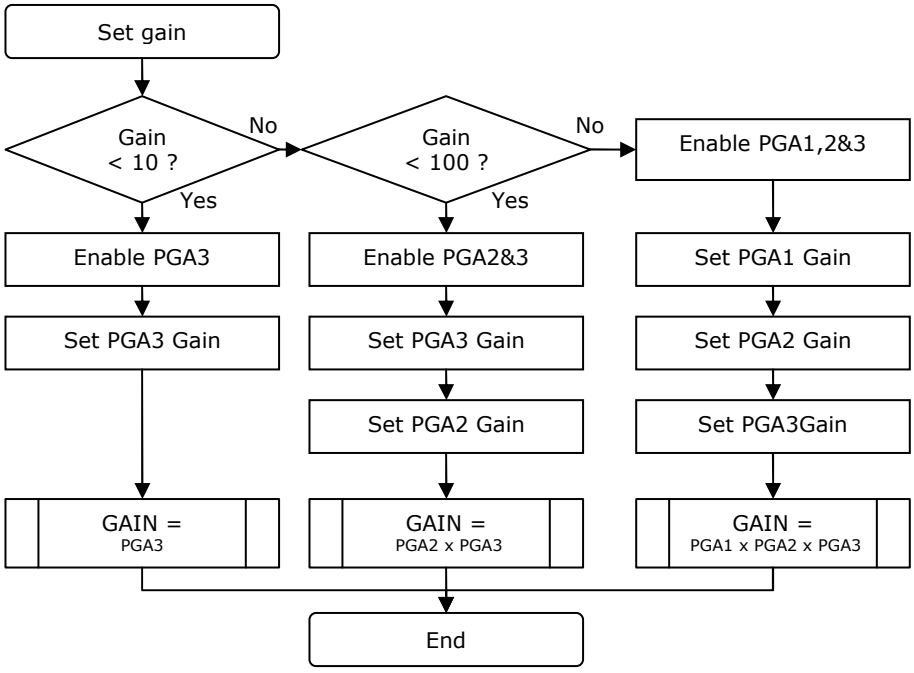
Overview



The diagram above shows the programmable gain amplifier organization, these are 3 PGA that are cascaded, the gain is made by multiplying them (disabled PGAs have the equivalent gain of 1).

Configuration flow

The diagram below shows the flow to set the gain of your configuration:



Predefined settings (Cont.)

Programmable gain amplifiers settings cont'd

Enable/disable PGAs

Function	Address	Data	Mask
Enable PGA3	0x0B	0x08	0x08
Disable PGA3		0x00	
Enable PGA2&3		0x0A	0x0A
Disable PGA2&3		0x00	
Enable PGA1,2&3		0x0E	0x0E
Disable PGA1,2&3		0x00	

PGA 3 Gain configuration

Function	Address	Data	Mask
Gain = 1	0x0D	0x0C	0x7F
Gain = 2		0x18	
Gain = 3		0x24	
Gain = 4		0x30	
Gain = 5		0x3C	
Gain = 6		0x48	
Gain = 7		0x54	
Gain = 8		0x60	
Gain = 9		0x6C	
Gain = 10		0x78	

PGA 2 Gain configuration

Function	Address	Data	Mask
Gain = 1	0x0C	0x00	0x30
Gain = 2		0x10	
Gain = 5		0x20	
Gain = 10		0x30	

PGA 1 Gain configuration

Function	Address	Data	Mask
Gain = 1	0x0D	0x00	0x80
Gain = 10		0x80	

Predefined settings (Cont.)

Programmable gain amplifier settings cont'd

Application example

The total gain to set in this example is 300.

The following settings must be sent to SX8722:

Function	Address	Data	Mask
Enable PGA1, 2 & 3	0x0B	0x0E	0x0E
PGA3 Gain = 3	0x0D	0x24	0x7F
PGA2 Gain = 10	0x0C	0x30	0x30
PGA1 Gain = 10	0x0D	0x80	0x80

Note: This command can be optimized, since PGA1 and PGA3 gains are sharing the same address the mask and the settings can be added.

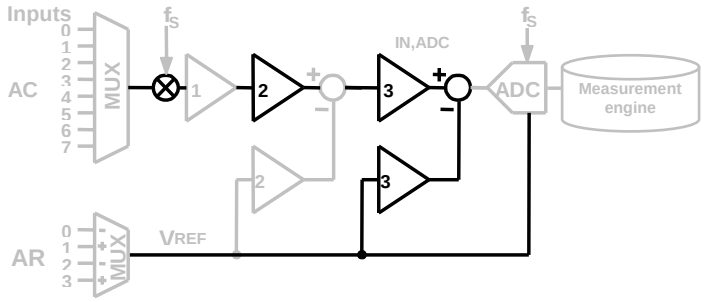
The following list of settings shows the optimized command

Function	Address	Data	Mask
Enable PGA1, 2 & 3	0x0B	0x0E	0x0E
PGA3 Gain = 3, PGA1 Gain = 10	0x0D	0xA4	0xFF
PGA2 Gain = 10	0x0C	0x30	0x30

Predefined settings (Cont.)

Offset cancellation

Overview

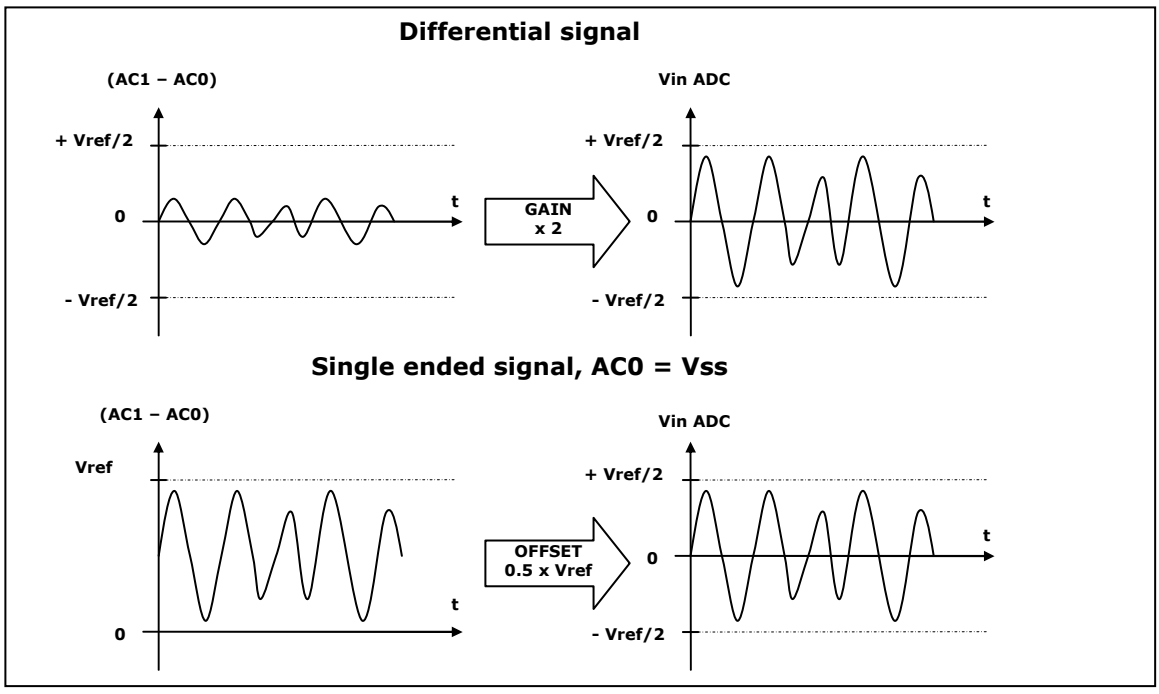


The offset cancellation consists in adding or subtracting a fraction or a multiple of the reference to the signal before the ADC input.

In the predefined settings only the addition or the subtraction of VREF/2 is implemented.

More offsets configuration can be defined using the "advanced configuration" at the end of this document.

The drawings below explain the offset concept.



Predefined settings (Cont.)

Offset cancellation (Cont.)

The following settings add 0.5 x Vref or subtract 0.5 x Vref from the signal.

Function	Address	Data	Mask
Offset3 = 0.5 x Vref	0x0E	0x06	0x7F
Offset3 = -0.5 x Vref		0x46	

Application examples

Case 1
Input signal = Vref
Input selection = AC0 – AC1. (see "input multiplexers" chapter)
Offset to remove is Vref/2.

The following command must be sent to SX8722:

Function	Address	Data	Mask
Offset3 = 0.5 x Vref	0x0E	0x06	0x7F

Case 2

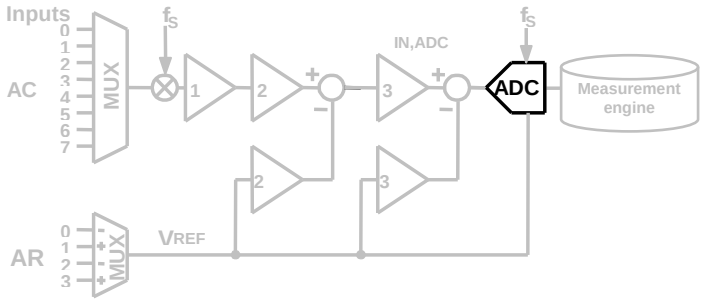
Input signal = Vref
Input selection = AC1 – AC0. (see "input multiplexers" chapter)
Offset to remove is -Vref/2.

Function	Address	Data	Mask
Offset3 = -0.5 x Vref	0x0E	0x46	0x7F

Predefined settings (Cont.)

ADC parameters

Overview



The ADC parameters are mainly the resolution and acquisition speed.
Detailed ADC parameters and configuration can be found in the "advanced configuration" chapter

The table below gives the main configurations available using the predefined settings and their main characteristics:

Name	Reso-lution [bits]	Conversion time [ms](typ)	Sampling Frequency [kHz] (typ)	Over - sampling ratio	Number of elementary conversions	Comments
S16	16	27.3	300	1024	8	Maximum resolution, thermal noise reduced to its minimum
N16	16	6.8		1024	2	Standard 16 bits resolution
F16	16	3.4		1024	1	Fastest 16 bits resolution
N12	12	0.22		64	1	Standard 12 bits resolution
N8	8	0.06		16	1	Standard 8 bits resolution

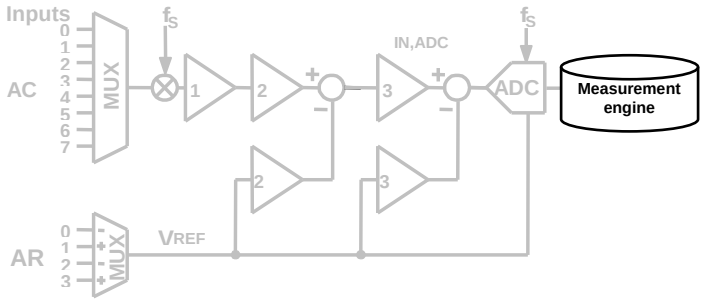
ADC settings

Function	Address	Data	Mask
S16	0x0C	0x7C	0x7C
N16		0x3C	
F16		0x1C	
N12		0x0C	
N8		0x04	

Predefined settings (Cont.)

Measurement engine

Overview



The measurement engine manages the configuration register sets and controls registers contents.

Based on these parameters it configures the ZoomingADC™, supervises post processing of the measurements, stores the results and flags the READY signal.

Once enabled the configuration 1 will be applied to the ZoomingADC™ and measurement will be done until the configuration is disabled using the disable command.

Note: All the predefined settings refer to configuration 1, to change other configurations simply adapt the address value.

More detailed functionalities are described at page 29.

Measurement engine settings

Application	Address	Data	Mask
Configuration 1 enabled	0x02	0x01	0x01
Configuration 1 disabled		0x00	

Default configuration

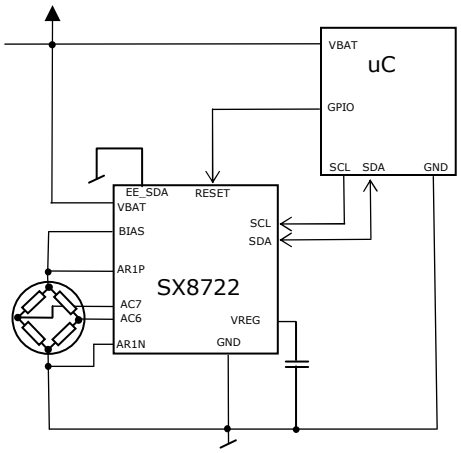
The SX8722 default configuration is described in this chapter.

Hardware considerations

The SX8722 default hardware configuration is as follow:

- 1uF Vreg capacitor connected to Vreg pin
- EE_SDA connected to ground
- 3.0 – 5.0 power supply on Vbat, 0V on GND
- Wheatstone bridge type sensor connected to AC0-AC1 biased through bias pin
- VRef = VBias = VBat
- Host micro controller I2C connected to SDA and SCL of the SX8722
- Host micro controller GPIO connected to RESET input of the SX8722

Schematic of the default configuration:



Startup conditions:
RESET = "0"

SX8722 ZoomingADC™ default settings

The SX8722 starts upon a power on reset and then goes into measurement mode.

By default the measurement mode parameters are as follows:

Differential measurement on channel AC0 – AC1, gain 1, 16 bits resolution, reference on AR1P – AR1N, no filtering, continuous measurements.

The READY pin will pulse from "0" to "1" at every sample available. The host microcontroller can then read the data.

Advanced configuration

The advanced configuration section is entering more in depth in the SX8722 usage.
In this section you will find:

Overview

- Measurement engine
- I2C EEPROM
- Using the SX8722 Stand alone
- Calibration process
- Working below 3 Volts
- Control registers
- ZoomingADC™
- ZoomingADC ™ Performances

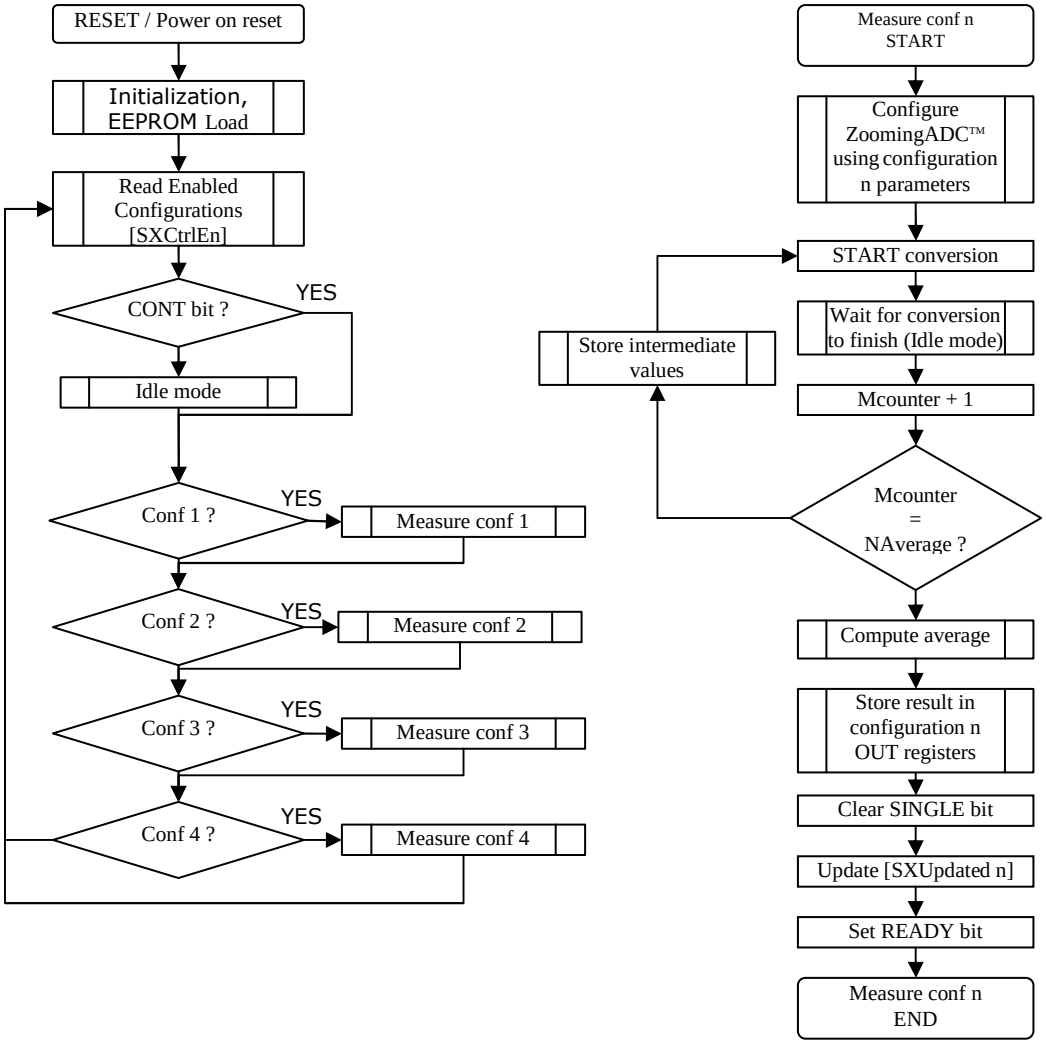
Advanced configuration (Cont.)

Measurement engine

Overview

The measurement engine is the interface between the configuration register sets and the ZoomingADC™.

Functional flowchart



The flowchart above shows the measurement engine function. It performs successively the measurements for each enabled configuration.
If in one or more configurations the bit CONT is set to 1, the measurements are performed again until the CONT bit is set to 0 through the I2C interface.
The engine goes out from the Idle mode every time an event occurs on the I2C interface.

Advanced configuration (Cont.)

Measurement engine (Cont.)

SXCfgEn – Configuration enabling register

Writing this register allows enabling or disabling the different configuration register sets.

Note: When the configuration is set to SINGLE, the bit CONFx is cleared automatically after the measurement is done.

Bits	7	6	5	4	3	2	1	0
SXCfgEn	reserved	reserved	reserved	reserved	CONF4	CONF3	CONF2	CONF1

SXUpdated – Updated configuration register

The configuration update registers contain which configuration has been updated by a measurement result.

Bits	7	6	5	4	3	2	1	0
SXUpdated	OVF4	OVF3	OVF2	OVF1	UCONF4	UCONF3	UCONF2	UCONF1

These bits are set to 1 every time a measurement is done on one of the 4 configurations. When the registers are read, these bits are set back to 0 by the communication engine, the bits 4 to 7 indicates an overflow.

Configuration register – measurement mode

This register is present in each configuration; the bits 0 & 1 are controlling the measurement mode.
Addresses 0x10, 0x30, 0x50, 0x70

Bits	7	6	5	4	3	2	1	0
C1SXCfg	Reserved	FILTER TYPE [2:0]			ALRM1	ALRM2	SINGLE	CONT

The bit SINGLE is set by the user, once the measurement is done; the measurement engine clears the CONF bit of the configuration.

The bit CONT is set by the user, the measurement is done continuously until this bit is cleared by the user.

Advanced configuration (Cont.)

Measurement engine (Cont.)

Filtering

Filter types

The available filters are described in the following chapter there are 2 different filtering types:

1. Average filtering.
2. Moving average filtering.

The average filtering is an addition of n values divided by n, this kind of filter is useful when having a very noisy signal; the maximum average value is 256.

Advantage: Reduces noise due to the high quantity of samples.
Disadvantage: Takes the acquisition time of n samples to have a result.

The sliding window averaging is a filter that takes the n last measurements and gives the mean value of them.
Advantage: result on each acquisition.
Disadvantage: limited at ten samples.

Important note: The hardware filtering is faster, these additional filters should be used only if the number of conversion and the over sampling rate are set to their maximum.

Configuration register – filtering

This register is present in each configuration; the bits 4 to 6 are controlling the filtering mode.
Addresses 0x10, 0x30, 0x50, 0x70

Bits	7	6	5	4	3	2	1	0
C1SXCfg	Reserved	FILTER TYPE [2:0]			ALRM1	ALRM2	SINGLE	CONT

The table below shows the filter selection.

Filter type [6:4]	
Code	**mode**
000	none
001	Average filtering
010	moving average filtering
011	reserved

Advanced configuration (Cont.)

Measurement engine (Cont.)

Filtering (Cont.)

Filter parameter register

This register is present in each configuration; the bits 0 to 7 are controlling the filter size.

Addresses 0x11, 0x31, 0x51, 0x71

Bits	7	6	5	4	3	2	1	0
C1FParam	Filter size [7:0]							

This register contains the number of samples used for the filtering.

Note that for a moving average filtering, this number is limited to 10.
(Putting a higher value will be interpreted as 10.)

Advanced configuration (Cont.)

Measurement engine (Cont.)

Alarms

The SX8722 offers two alarms pins that have configurable on & off thresholds; these thresholds are on 16 bits.

Each configuration register set has 2 alarms, which can be enabled, when more than one configuration is using the same alarm pin, logical function is interacting between the two alarms sources. This condition can be a logical OR (default) or a logical AND.

Configuration register – alarms

Addresses 0x10, 0x30, 0x50, 0x70

Bits	7	6	5	4	3	2	1	0
C1SXCfg	Reserved	FILTER TYPE [2:0]			ALRM1	ALRM2	SINGLE	CONT

The bits 2 & 3 enable the alarm 1 & 2 when set to 1.

Alarm threshold registers

Addresses 0x12 to 0x19, 0x32 to 0x39, 0x52 to 0x59 and 0x72 to 0x79

Bits	7	6	5	4	3	2	1	0
C1Alrm1OnMsb	S1ALRM1ON [15:8]							
C1Alrm1OnLsb	S1ALRM1ON [7:0]							
C1Alrm1OffMsb	S1ALRM1OFF [15:8]							
C1Alrm1OffLsb	S1ALRM1OFF [7:0]							
C1Alrm2OnMsb	S1ALRM2ON [15:8]							
C1Alrm2OnLsb	S1ALRM2ON [7:0]							
C1Alrm2OffMsb	S1ALRM2OFF [15:8]							
C1Alrm2OffLsb	S1ALRM2OFF [7:0]							

SXCtrl2 – SX8722 Control register 2

This register is common to all configurations; it sets the relationship between the different alarm sources. See the diagram next page for more information

Address 0x02

Bits	7	6	5	4	3	2	1	0
SXCtrl2	reserved	reserved	reserved	reserved	AL1OnC	AL1OffC	AL2OnC	AL2OffC

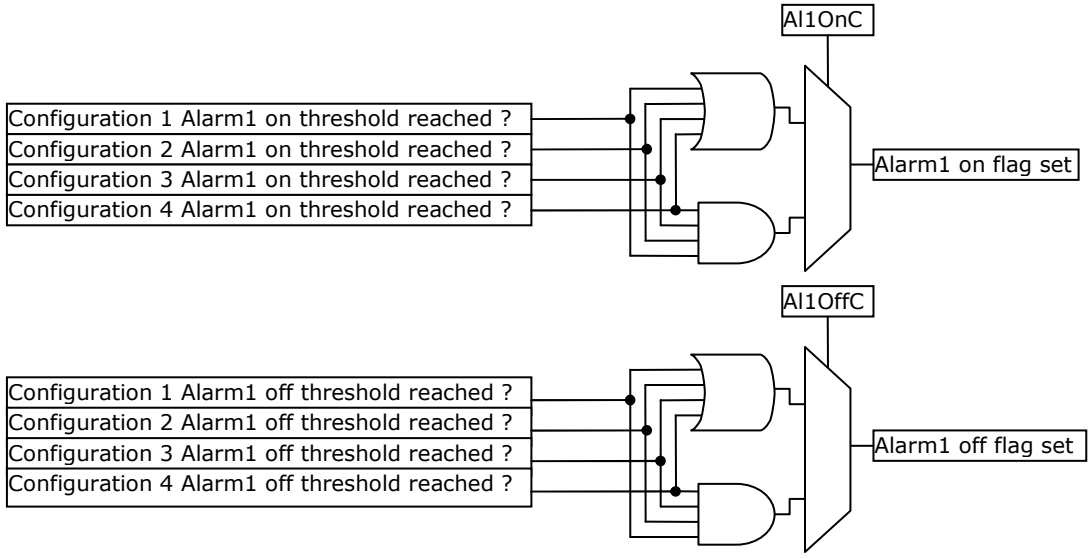
When set to 1 the condition is AND and when set to 0 the condition is OR, see diagram on the following page.

Advanced configuration (Cont.)

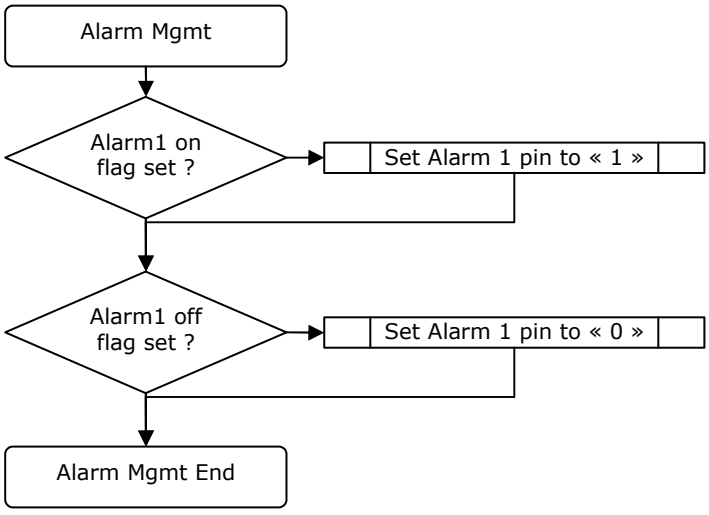
Measurement engine (Cont.)

Alarms(cont.)

The diagram below shows the interaction between alarms sources.



The flowchart below shows the management of the alarms flag (when at least one alarm is on)



Advanced configuration (Cont.)

I2C EEPROM

Overview

The SX8722 can interface a Standard I2C EEPROM. This allows:

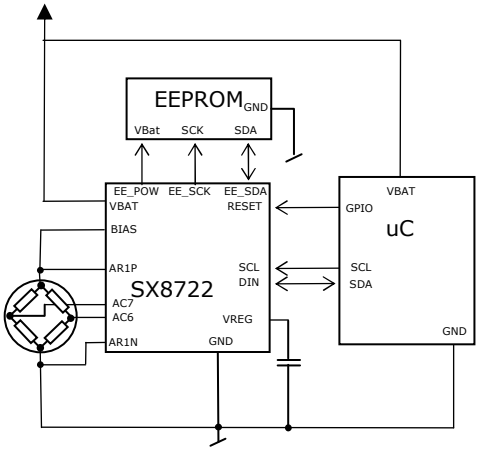
- Stand alone usage.
- Parameters saving by save command.
- Parameters restore by load command.

The EE_POW pin allows the SX8722 to power the EEPROM in order to guarantee the lowest power having the EEPROM unpowered when unused.

When no EEPROM is used, the EE_SDA pin must be tied to ground.

Schematic

The schematic below shows the connections using standard I2C EEPPROM.



Advanced configuration (Cont.)

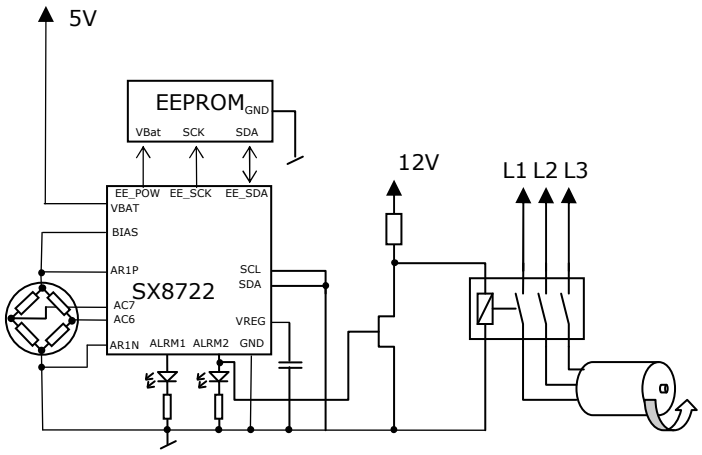
Using the SX8722 Stand alone

The SX8722 can be used stand alone to monitor signals and to generate alarms on configured thresholds.

Using a preprogrammed EEPROM allows the setup of these monitoring tasks.

Schematic

The schematic below shows an example of a stand alone configuration.



Advanced configuration (Cont.)

Frequency calibration process

Overview

The SX8722 has an internal RC Oscillator working at 1.2 MHz +/- 600kHz.
This frequency can be calibrated using 2 methods.

- 32.768kHz Xtal
- Input of a 32.768 kHz signal on the CAL pin.

Using an 32.768 kHz XTAL

When the SX8722 is connected to a 32.768 XTAL between XIN & XOUT, the CAL pin must be grounded. This indicates to SX8722 that an XTAL is present and allows frequency auto-calibration at power on.

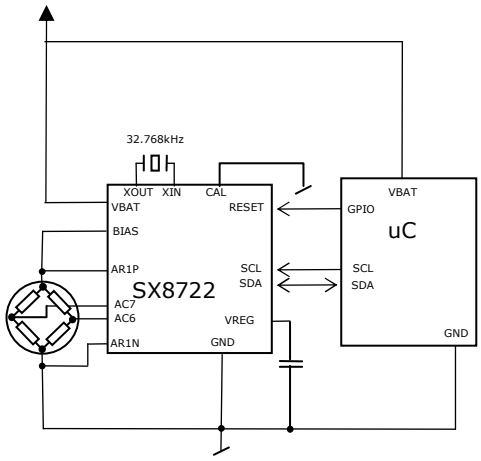
Using a 32.768 kHz External clock source

The host microcontroller can at any time send a 32.768kHz signal on CAL pin, the detection of a rising edge on the this pin initiates a calibration process. When the chip is calibrated, the pin DOUT or READY rises to high level.

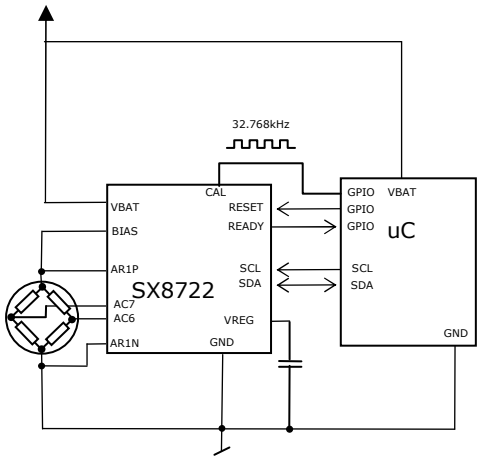
Schematics

The schematics below show both configurations:

Using a 32.768kHz XTAL



Using an external 32.768kHz signal



NOTES:
If an external EEPROM is present, the calibration value is saved in it.
The tolerance of the calibration signal must remain around 32.768 kHz +/- 10%

Advanced configuration (Cont.)

Working below 3 Volts

Operating range

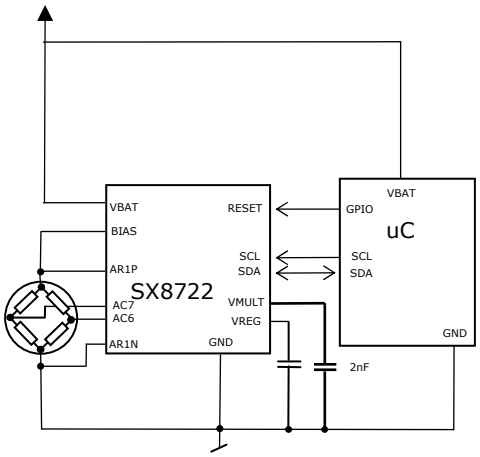
The SX8722 operating range is 5.5Volts downto 2.4Volts. However, below 3 Volts the SX8722 enables an internal voltage multiplier to power the ZoomingADC™.

Internal voltage multiplier

This internal voltage multiplier is automatically enabled when the power supply goes below 3 Volts but the internal voltage multiplier requires an external capacitor between VMULT pin and ground, the value of this capacitor must be between 1 and 3nF.

Schematic

The schematic below shows the capacitor connection:



Advanced configuration (Cont.)

Control registers

The parameters available on these registers affect the whole SX8722 and are common to all configuration register sets.

SXCtrl1 – SX8722 Control register 1

Bits	7	6	5	4	3	2	1	0
SXCtrl1	EE_D	XTAL_D	CKOUT	RESERVED	EE	SLEEP	SHUT	CAL

Pos	SXCtrl1	rw	reset	description
7	EE_D	r	x	Indicates if an EEPROM was detected at startup
6	XTAL_D	r	x	Indicates if an XTAL was detected at startup
5	CKOUT	rw	0	Enables the clock output on CKOUT pin
4	RESERVED	rw	0	
3	EE	r	0	Is set to 1 when SX8722 loaded its configuration from the EEPROM at startup
2	SLEEP	rw	0	When set to 1 this bit activates the Sleep mode of the SX8722S. Setting pin SLEEP to 1 has the same effect
1	SHUT	rw	0	When set to 1 this bit activates the Shutdown mode of the SX8722. Setting pin SHUT to 1 has the same effect
0	CAL	r	0	This flag shows if the SX8722 clock has been successfully. calibrated

SXCtrl2 – SX8722 Control register 2

Bits	7	6	5	4	3	2	1	0
SXCtrl2	reserved	reserved	reserved	reserved	AL1OnC	AL1OffC	AL2OnC	AL2OffC

Pos	SXCtrl1	rw	reset	description
3	AL1OnC	rw	0	Sets the logical condition for alarm 1 on (0 = OR, 1 = AND)
2	AL1OffC	rw	0	Sets the logical condition for alarm 1 off (0 = OR, 1 = AND)
1	AL2OnC	rw	0	Sets the logical condition for alarm 2 on (0 = OR, 1 = AND)
0	AL2OffC	rw	0	Sets the logical condition for alarm 2 off (0 = OR, 1 = AND)

More information about the alarms condition usage on page 33.

Advanced configuration (Cont.)

ZoomingADC™

ZoomingADC™ Features

The ZoomingADC™ is a complete and versatile low-power analog front-end interface typically intended for sensing applications. The key features of the ZoomingADC™ are:

Programmable 6 to 16-bit dynamic range oversampled ADC
- Flexible gain programming between 0.5 and 1000
- Flexible and large range offset compensation
- 4-channel differential or 8-channel single-ended input multiplexer
- 2-channel differential reference inputs
- Power saving modes

Overview

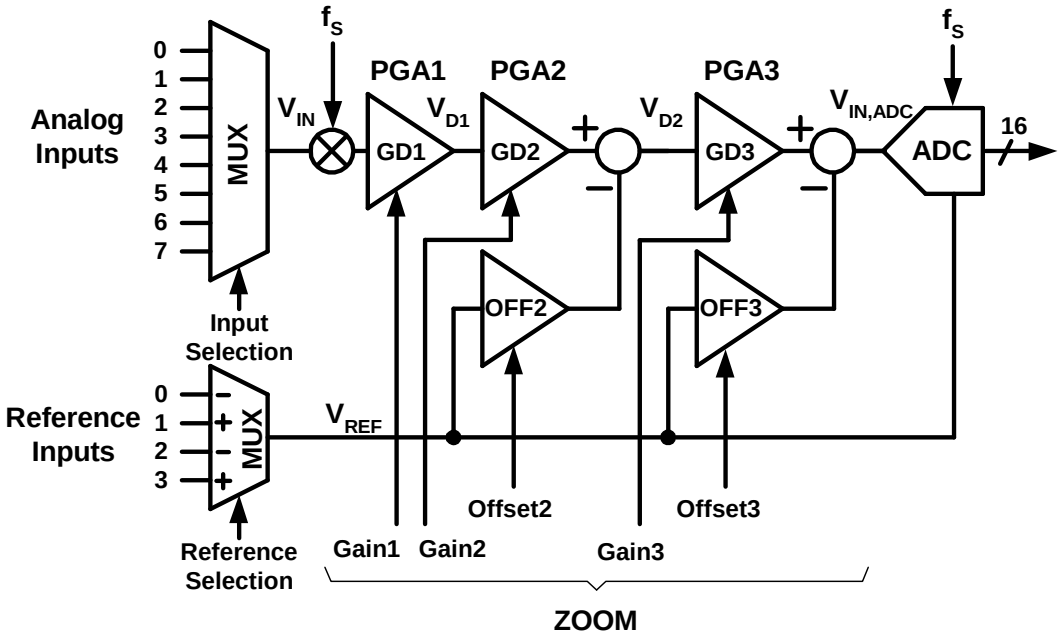


Figure 1. ZoomingADC™ general functional block diagram

The total acquisition chain consists of an input multiplexer, 3 programmable gain amplifier stages and an oversampled A/D converter. The reference voltage can be selected on two different channels. Two offset compensation amplifiers allow for a wide offset compensation range. The programmable gain and offset allow to zoom in on a small portion of the reference voltage defined input range.

Advanced configuration (Cont.)

Register map

There are six registers in the acquisition chain (AC), namely **CxZadcReg1**, **CxZadcReg2**, **CxZadcReg3**, **CxZadcReg4**, **CxZadcReg5** and **CxZadcReg6**. Table 5 to Table 10 show the mapping of control bits and functionality of these registers while Table 4 **:** gives an overview of these six.

The register map only gives a short description of the different configuration bits. More detailed information is found in subsequent sections.

register name
CxZadcReg1
CxZadcReg2
CxZadcReg3
CxZadcReg4
CxZadcReg5
CxZadcReg6

Table 4 : AC registers

pos.	CxZadcReg1	rw	reset	description
7	reserved	w r0	0 l	
6:5	SET_NELCONV[1:0]	r w	01	sets the number of elementary conversions
4:2	SET_OSR[2:0]	r w	010	sets the oversampling rate of an elementary conversion
1	reserved	r w	0	
0	reserved	r w	0	

Table 5: CxZadcReg1

pos.	CxZadcReg2	rw	reset	description
7:6	IB_AMP_ADC[1:0]	r w	11	Bias current selection of the ADC converter
5:4	IB_AMP_PGA[1:0]	r w	11	Bias current selection of the PGA stages
3:0	ENABLE[3:0]	r w	0000	Enables the different PGA stages and the ADC

Table 6: CxZadcReg2

pos.	CxZadcReg3	rw	reset	description
7:6	FIN[1:0]	r w	00	Sampling frequency selection
5:4	PGA2_GAIN[1:0]	r w	00	PGA2 stage gain selection
3:0	PGA2_OFFSET[3:0]	r w	0000	PGA2 stage offset selection

Table 7: CxZadcReg3

pos.	CxZadcReg4	rw	reset	description
7	PGA1_GAIN	r w	0	PGA1 stage gain selection
6:0	PGA3_GAIN[6:0]	r w	0000000	PGA3 stage gain selection

Table 8: CxZadcReg4

Advanced configuration (Cont.)

Register map (Cont.)

pos.	CxZadcReg5	rw	reset	description
7	reserved	r	0	Unused
6:0	PGA3_OFFSET[6:0]	r w	0000000	PGA3 stage offset selection

Table 9: CxZadcReg5

pos.	CxZadcReg6	rw	reset	description
7	reserved	r	0	Activity flag
6	reserved	w r0	0	Selects default configuration
5:1	AMUX[4:0]	r w	00000	Input channel configuration selector
0	VMUX	r w	0	Reference channel selector

Table 10 CxZadcReg6

Advanced configuration (Cont.)

ZoomingADC™ Description

Figure 2 gives a more detailed description of the acquisition chain.

Acquisition Chain

Figure 1 shows the general block diagram of the acquisition chain (AC).

Analog inputs can be selected among eight input channels, while reference input is selected between two differential channels.

The core of the zooming section is made of three differential programmable amplifiers (PGA). After selection of a combination of input and reference signals V_{IN} and V_{REF}, the input voltage is modulated and amplified through stages 1 to 3. Fine gain programming up to 1'000V/V is possible. In addition, the last two stages provide programmable offset. Each amplifier can be bypassed if needed.

The output of the PGA stages is directly fed to the analog-to-digital converter (ADC), which converts the signal $V_{IN,ADC}$ into digital.

Like most ADCs intended for instrumentation or sensing applications, the ZoomingADC™ is an over-sampled converter (See Note1). The ADC is a so-called incremental converter with bipolar operation (the ADC accepts both positive and negative input voltages). In first approximation, the ADC output result relative to full-scale (*FS*) delivers the quantity:

$$\frac{OUT_{ADC}}{FS/2} \cong \frac{V_{IN,ADC}}{V_{REF}/2} \qquad \text{(Eq. 1)}$$

in two's complement (see Sections 0 and 0 for details). The output code OUT_{ADC} is $-FS/2$ to $+FS/2$ for $V_{IN,ADC} \cong -V_{REF}/2$ to $+V_{REF}/2$ respectively. As will be shown in section 0, $V_{IN,ADC}$ is related to input voltage V_{IN} by the relationship:

$$V_{IN,ADC} = GD_{TOT} \cdot V_{IN} - GDoff_{TOT} \cdot V_{REF} \ \text{(V)} \qquad \text{(Eq. 2)}$$

where GD_{TOT} is the total PGA gain, and $GDoff_{TOT}$ is the total PGA offset.

1 Note: Over-sampled converters are operated with a sampling frequency f_S much higher than the input signal's Nyquist rate (typically f_S is 20-1'000 times the input signal bandwidth). The sampling frequency to throughput ratio is large (typically 10-500). These converters include digital decimation filtering. They are mainly used for high resolution, and/or low-to-medium speed applications.

Advanced configuration (Cont.)

ZoomingADC™ Detailed block diagram

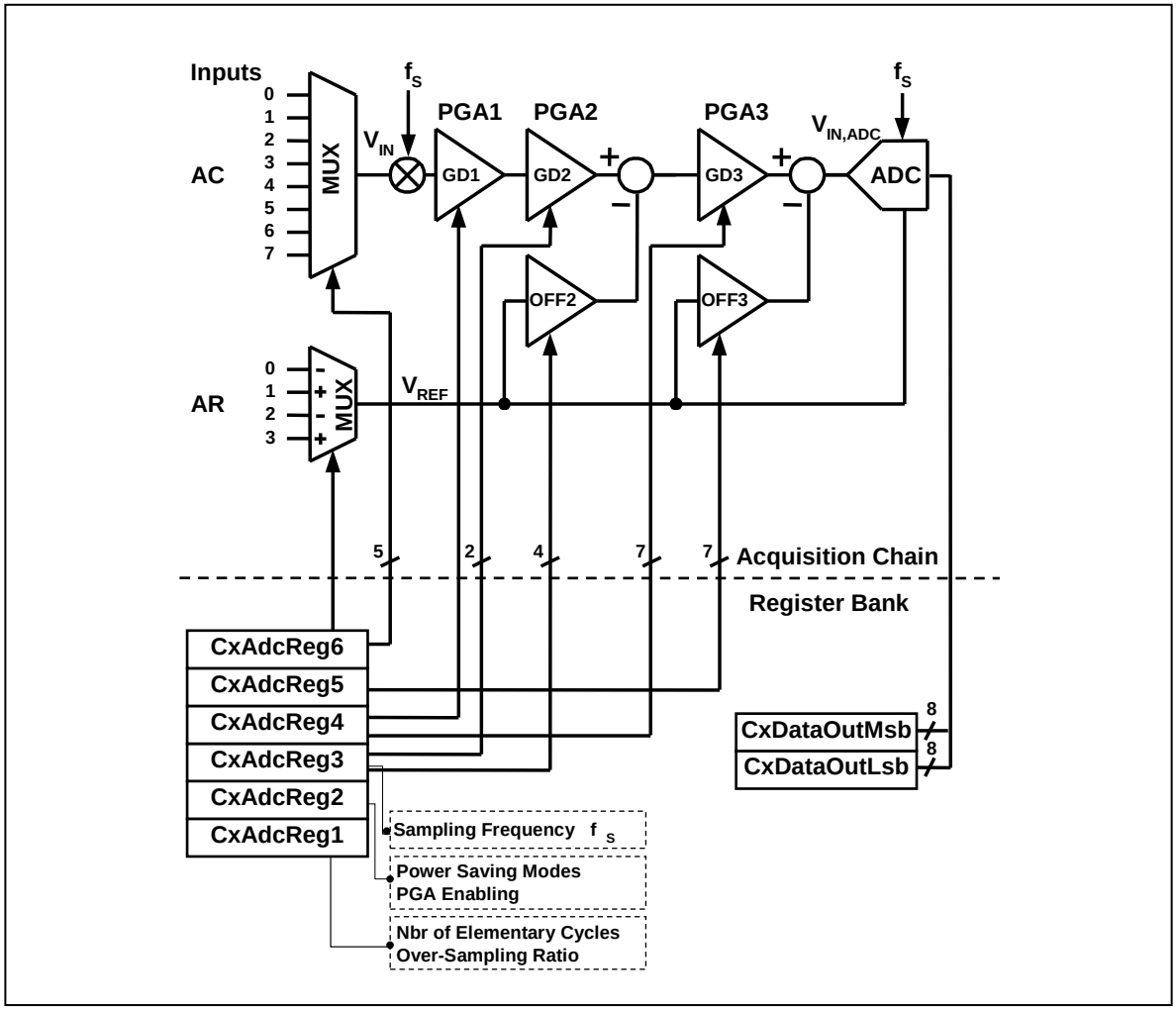


Figure 2. ZoomingADC™ detailed functional block diagram

Advanced configuration (Cont.)

ZoomingADC™ registers

Figure 2 shows a detailed functional diagram of the ZoomingADC™.

In Table 11 the configuration of the peripheral registers is detailed. The system has a bank of eight 8-bit registers: six registers are used to configure the acquisition chain (**CxZAdcReg1 to 6**), and two registers are used to store the output code of the analog-to-digital conversion (**CxDataOutMSB & LSB**).

Table 11. Peripheral registers to configure the acquisition chain (AC)
and to store the analog-to-digital conversion (ADC) result

Register Name	Bit Position							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CxDataOutLSB	OUT[7:0]							
CxDataOutMSB	OUT[15:8]							
CxZadcReg1 Default values:	R 0	SET_NELC[1:0] 01		SET_OSR[2:0] 010			R 0	R 0
CxZadcReg2 Default values:	IB_AMP_ADC[1:0] 11		IB_AMP_PGA[1:0] 11		ENABLE[3:0] 0001			
CxZadcReg3 Default values:	FIN[1:0] 00		PGA2_GAIN[1:0] 00		PGA2_OFFSET[3:0] 0000			
CxZadcReg4 Default values:	PGA1_G 0	PGA3_GAIN[6:0] 0000000						
CxZadcReg5 Default values:	0	PGA3_OFFSET[6:0] 0000000						
CxZadcReg6 Default values:	R 0	R 0	AMUX[4:0] 00000					VMUX 0

Note Bits labelled R are reserved

Advanced configuration (Cont.)

ZoomingADC™ registers (Cont.)

With:

- OUT: (r) digital output code of the analog-to-digital converter. (MSB = OUT[15])
- SET_NELC: (rw) sets the number of elementary conversions to $2^{SET\_NELC[1:0]}$. To compensate for offsets, the input signal is chopped between elementary conversions (1,2,4,8).
- SET_OSR: (rw) sets the over-sampling rate (*OSR*) of an elementary conversion to $2^{(3+SET\_OSR[2:0])}$. *OSR* = 8, 16, 32, ..., 512, 1024.
- CONT: (rw) setting this bit starts a conversion. A new conversion will automatically begin as long as the bit remains at 1.
- IB_AMP_ADC: (rw) sets the bias current in the ADC to 0.25*(1+ IB_AMP_ADC[1:0]) of the normal operation current (25, 50, 75 or 100% of nominal current). To be used for low-power, low-speed operation.
- IB_AMP_PGA: (rw) sets the bias current in the PGAs to 0.25*(1+IB_AMP_PGA[1:0]) of the normal operation current (25, 50, 75 or 100% of nominal current). To be used for low-power, low-speed operation.
- ENABLE: (rw) enables the ADC modulator (bit 0) and the different stages of the PGAs (PGAi by bit i=1,2,3). PGA stages that are disabled are bypassed.
- FIN: (rw) These bits set the sampling frequency of the acquisition chain. Expressed as a fraction of the oscillator frequency, the sampling frequency is given as: 00 → 1/4 f_{RC}, 01 → 1/8 f_{RC}, 10 → 1/32 f_{RC}, 11→ ~8kHz.
- PGA1_GAIN: (rw) sets the gain of the first stage: 0 → 1, 1 → 10.
- PGA2_GAIN: (rw) sets the gain of the second stage: 00 → 1, 01 → 2, 10 → 5, 11 → 10.
- PGA3_GAIN: (rw) sets the gain of the third stage to PGA3_GAIN[6:0]·1/12.
- PGA2_OFFSET: (rw) sets the offset of the second stage between −1 and +1, with increments of 0.2. The MSB gives the sign (0 → positive, 1 → negative); amplitude is coded with the bits PGA2_OFFSET[5:0].
- PGA3_OFFSET: (rw) sets the offset of the third stage between −5.25 and +5.25, with increments of 1/12. The MSB gives the sign (0 → positive, 1 → negative); amplitude is coded with the bits PGA3_OFFSET[5:0].
- AMUX(4:0): (rw) AMUX[4] sets the mode (0 → 4 differential inputs, 1 → 7 inputs with A(0) = common reference) AMUX(3) sets the sign (0 → straight, 1→ cross) AMUX[2:0] sets the channel.
- VMUX: (rw) sets the differential reference channel (0 → R(1) and R(0), 1 → R(3) and R(2)). (r = read; w = write; rw = read & write)

Advanced configuration (Cont.)

Input Multiplexers

The ZoomingADC™ has eight analog inputs AC_A(0) to AC_A(7) and four reference inputs AC_R(0) to AC_R(3). Let us first define the differential input voltage V_{IN} and reference voltage V_{REF} respectively as:

$$V_{IN} = V_{INP} - V_{INN} \quad \text{(V)} \qquad \text{(Eq. 3)}$$

and:

$$V_{REF} = V_{REFP} - V_{REFN} \quad \text{(V)} \qquad \text{(Eq. 4)}$$

As shown in Table 12 the inputs can be configured in two ways: either as 4 differential channels (V_{IN1} = AC_A(1) - AC_A(0),..., V_{IN4} = AC_A(7) - AC_A(6)), or AC_A(0) can be used as a common reference, providing 7 signal paths all referred to AC_A(0). The control word for the analog input selection is **AMUX[4:0]**. Notice that the bit **AMUX[3]** controls the sign of the input voltage.

AMUX[4:0] (RegACCfg5[5:1])	V_{INP}	V_{INN}	AMUX[4:0] (RegACCfg5[5:1])	V_{INP}	V_{INN}
00x00	AC_A(1)	AC_A(0)	01x00	AC_A(0)	AC_A(1)
00x01	AC_A(3)	AC_A(2)	01x01	AC_A(2)	AC_A(3)
00x10	AC_A(5)	AC_A(4)	01x10	AC_A(4)	AC_A(5)
00x11	AC_A(7)	AC_A(6)	01x11	AC_A(6)	AC_A(7)
10000	AC_A(0)		11000		AC_A(0)
10001	AC_A(1)		11001		AC_A(1)
10010	AC_A(2)		11010		AC_A(2)
10011	AC_A(3)	AC_A(0)	11011	AC_A(0)	AC_A(3)
10100	AC_A(4)		11100		AC_A(4)
10101	AC_A(5)		11101		AC_A(5)
10110	AC_A(6)		11110		AC_A(6)
10111	AC_A(7)		11111		AC_A(7)

Table 12.Analog input selection

Similarly, the reference voltage is chosen among two differential channels (V_{REF1} = AC_R(1)-AC_R(0) or V_{REF2} = AC_R(3)-AC_R(2)) as shown in Table 13 The selection bit is **VMUX**. The reference inputs V_{REFP} and V_{REFN} (common-mode) can be up to the power supply range.

VMUX (RegACCfg5[0])	V_{REFP}	V_{REFN}
0	AC_R(1)	AC_R(0)
1	AC_R(3)	AC_R(2)

Table 13. Analog Reference input selection

Advanced configuration (Cont.)

Programmable Gain Amplifiers

As seen in Figure 1, the zooming function is implemented with three programmable gain amplifiers (PGA). These are:

- PGA1: coarse gain tuning
- PGA2: medium gain and offset tuning
- PGA3: fine gain and offset tuning

All gain and offset settings are realized with ratios of capacitors. The user has control over each PGA activation and gain, as well as the offset of stages 2 and 3. These functions are examined hereafter.

ENABLE[3:0]	Block
xxx0 xxx1	ADC disabled ADC enabled
xx0x xx1x	PGA1 disabled PGA1 enabled
x0xx x1xx	PGA2 disabled PGA2 enabled
0xxx 1xxx	PGA3 disabled PGA3 enabled

Table 14. ADC & PGA enabling

PGA1_GAIN	PGA1 Gain GD_1 (V/V)
0	1
1	10

Table 15. PGA1 Gain Settings

PGA2_GAIN[1:0]	PGA2 Gain GD_2 (V/V)
00	1
01	2
10	5
11	10

Table 16. PGA2 gain settings

Advanced configuration (Cont.)

Programmable Gain Amplifiers (Cont.)

PGA2_OFFSET[3:0]	PGA2 Offset $GDoff_2$ (V/V)
0000	0
0001	+0.2
0010	+0.4
0011	+0.6
0100	+0.8
0101	+1
1001	-0.2
1010	-0.4
1011	-0.6
1100	-0.8
1101	-1

Table 17. PGA2 offset settings

PGA3_GAIN[6:0]	PGA3 Gain GD_3 (V/V)
0000000	0
0000001	1/12(=0.083)
...	...
0000110	6/12
...	...
0001100	12/12
0010000	16/12
...	
0100000	32/12
...	
1000000	64/12
...	
1111111	127/12(=10.58)

Table 18. PGA3 gain settings

Advanced configuration (Cont.)

Programmable Gain Amplifiers (Cont.)

PGA3_OFFSET[6:0]	PGA3 Offset $GDoff_3$ (V/V)
0000000	0
0000001	+1/12(=+0.083)
0000010	+2/12
...	...
0010000	+16/12
...	...
0100000	+32/12
...	...
0111111	+63/12(=+5.25)
1000000	0
1000001	-1/12(=-0.083)
1000010	-2/12
...	...
1010000	-16/12
...	...
1100000	-32/12
...	...
1111111	-63/12(=-5.25)

Table 19. PGA3 offset settings

PGA & ADC Enabling

Depending on the application objectives, the user may enable or bypass each PGA stage. This is done according to the word **ENABLE** and the coding given in Table 14. To reduce power dissipation, the ADC can also be inactivated while idle.

PGA1

The first stage can have a buffer function (unity gain) or provide a gain of 10 (see Table 15). The voltage V_{D1} at the output of PGA1 is:

$$V_{D1} = GD_1 \cdot V_{IN} \quad \text{(V)} \qquad \text{(Eq. 5)}$$

where GD_1 is the gain of PGA1 (in V/V) controlled with the bit **PGA1_GAIN**.

PGA2

The second PGA has a finer gain and offset tuning capability, as shown in Table 16 and Table 17. The voltage V_{D2} at the output of PGA2 is given by:

$$V_{D2} = GD_2 \cdot V_{D1} - GDoff_2 \cdot V_{REF} \quad \text{(V)} \qquad \text{(Eq. 6)}$$

where GD_2 and $GDoff_2$ are respectively the gain and offset of PGA2 (in V/V). These are controlled with the words **PGA2_GAIN[1:0]** and **PGA2_OFFSET[3:0]** .

Advanced configuration (Cont.)

PGA3

The finest gain and offset tuning is performed with the third and last PGA stage, according to the coding of Table 18 and Table 19. The output of PGA3 is also the input of the ADC. Thus, similarly to PGA2, we find that the voltage entering the ADC is given by:

$$V_{IN,ADC} = GD_3 \cdot V_{D2} - GDoff_3 \cdot V_{REF} \text{ (V)} \qquad \text{(Eq. 7)}$$

where GD_3 and $GDoff_3$ are respectively the gain and offset of PGA3 (in V/V). The control words are **PGA3_GAIN[6:0]** and **PGA3_OFFSET[6:0]** . To remain within the signal compliance of the PGA stages, the condition:

$$V_{D1}, V_{D2} < V_{DD} \quad \text{(V)} \qquad \text{(Eq. 8)}$$

must be verified.

Finally, combining equations Eq. 5 to Eq. 7 for the three PGA stages, the input voltage $V_{IN,ADC}$ of the ADC is related to V_{IN} by:

$$V_{IN,ADC} = GD_{TOT} \cdot V_{IN} - GDoff_{TOT} \cdot V_{REF} \text{ (V)} \qquad \text{(Eq. 9)}$$

where the total PGA gain is defined as:

$$GD_{TOT} = GD_3 \cdot GD_2 \cdot GD_1 \text{ (V/V)} \qquad \text{(Eq. 10)}$$

and the total PGA offset is:

$$GDoff_{TOT} = GDoff_3 + GD_3 \cdot GDoff_2 \qquad \text{(V/V)} \qquad \text{(Eq. 11)}$$

ADC Characteristics

The main performance characteristics of the ADC (resolution, conversion time, etc.) are determined by three programmable parameters:

- sampling frequency f_S,
- over-sampling ratio *OSR*, and
- number of elementary conversions N_{ELCONV}.

The setting of these parameters and the resulting performances are described hereafter.

Advanced configuration (Cont.)

Conversion Sequence

A conversion is started each time the bit **START** or the bit **DEF** is set. As depicted in Figure 3, a complete analog-to-digital conversion sequence is made of a set of N_{ELCONV} elementary incremental conversions and a final quantization step. Each elementary conversion is made of (OSR+1) sampling periods T_S=1/f_S, i.e.:

$$T_{ELCONV} = (OSR+1)/f_S \quad \text{(s)} \qquad \text{(Eq. 12)}$$

The result is the mean of the elementary conversion results. An important feature is that the elementary conversions are alternatively performed with the offset of the internal amplifiers contributing in one direction and the other to the output code. Thus, converter internal offset is eliminated if at least two elementary sequences are performed (i.e. if $N_{ELCONV} \geq 2$). A few additional clock cycles are also required to initiate and end the conversion properly.

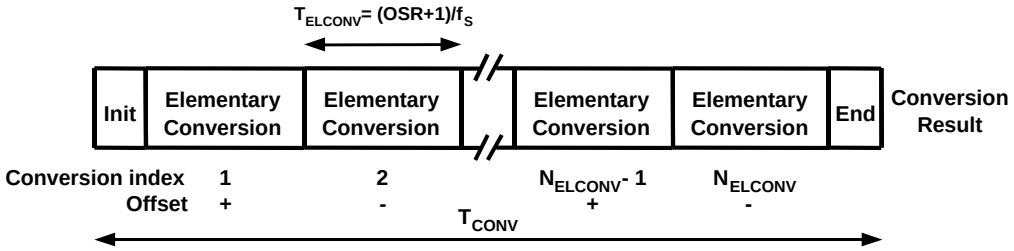


Figure 3. Analog-to-digital conversion sequence

Sampling Frequency

The word **FIN[1:0]** is used to select the sampling frequency f_S (Table 20). Three sub-multiples of the internal RC-based frequency f_{RCEXT} can be chosen. For **FIN** = "11", sampling frequency is about 8kHz. Additional information on oscillators and their control can be found in the clock block documentation.

FIN[1:0]	Sampling Frequency f_S (Hz)	
	LC01/05	LC02
00	$1/4 \cdot f_{RC}$	$1/8 \cdot f_{RCEXT}$
01	$1/8 \cdot f_{RC}$	$1/16 \cdot f_{RCEXT}$
10	$1/32 \cdot f_{RC}$	$1/64 \cdot f_{RCEXT}$
11	~8kHz	~4kHz

Table 20. Sampling frequency settings (f_{RC}= RC-based frequency)

Advanced configuration (Cont.)

Over-Sampling Ratio

The over-sampling ratio (*OSR*) defines the number of integration cycles per elementary conversion. Its value is set with the word **SET_OSR[2:0]** in power of 2 steps (see Table 21) given by:

$$OSR = 2^{3+\text{SET\_OSR}[2:0]} \quad (-) \qquad \text{(Eq. 13)}$$

SET_OSR[2:0] (RegACCfg0[4:2])	Over-Sampling Ratio *OSR* (-)
000	8
001	16
010	32
011	64
100	128
101	256
110	512
111	1024

Table 21. Over-sampling ratio settings

Elementary Conversions

As mentioned previously, the whole conversion sequence is made of a set of N_{ELCONV} elementary incremental conversions. This number is set with the word **SET_NELC[1:0]** in power of 2 steps (see Table 22) given by:

$$N_{ELCONV} = 2^{\text{SET\_NELC}[1:0]} \quad (-) \qquad \text{(Eq. 14)}$$

SET_NELC[1:0] (RegACCfg0[6:5])	# of Elementary Conversions N_{ELCONV} (-)
00	1
01	2
10	4
11	8

Table 22. Number of elementary conversion settings

As already mentioned, N_{ELCONV} must be equal or greater than 2 to reduce internal amplifier offsets.

Advanced configuration (Cont.)

Resolution

The theoretical resolution of the ADC, without considering thermal noise, is given by:

$$n = 2 \cdot \log_2(OSR) + \log_2(N_{ELCONV}) \quad \text{(Bits)} \qquad \text{(Eq. 15)}$$

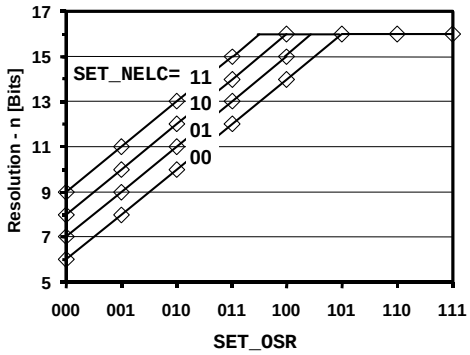


Figure 4. Resolution vs. SET_OSR[2:0] and SET_NELC[2:0]

SET_OSR [2:0]	SET_NELC			
	00	01	10	11
000	6	7	8	9
001	8	9	10	11
010	10	11	12	13
011	12	13	14	15
100	14	15	16	16
101	16	16	16	16
110	16	16	16	16
111	16	16	16	16

(shaded area: resolution truncated to 16 bits due to output register size **RegACOut[15:0]**)

Table 23. Resolution vs. SET_OSR[2:0] and SET_NELC[1:0] settings

Using look-up Table 23 or the graph plotted in Figure 4, resolution can be set between 6 and 16 bits. Notice that, because of 16-bit register use for the ADC output, **practical resolution is limited to 16 bits**, i.e. $n \leq 16$. Even if the resolution is truncated to 16 bit by the output register size, it may make sense to set OSR and N_{ELCONV} to higher values in order to reduce the influence of the thermal noise in the PGA

Advanced configuration (Cont.)

Conversion Time & Throughput

As explained using Figure 3, conversion time is given by:

$$T_{CONV} = (N_{ELCONV} \cdot (OSR+1)+1) / f_S \quad \text{(s)} \qquad \text{(Eq. 16)}$$

and throughput is then simply $1/T_{CONV}$. For example, consider an over-sampling ratio of 256, 2 elementary conversions, and a sampling frequency of 500kHz (**SET_OSR** = "101", **SET_NELC** = "01", f_{RC} = 2MHz, and **FIN** = "00"). In this case, using Table 24, the conversion time is 515 sampling periods, or 1.03ms. This corresponds to a throughput of 971Hz in continuous-time mode. The plot of Figure 5 illustrates the classic trade-off between resolution and conversion time.

SET_OSR [2:0]	SET_NELC[1:0]			
	00	01	10	11
000	10	19	37	73
001	18	35	69	137
010	34	67	133	265
011	66	131	261	521
100	130	259	517	1033
101	258	515	1029	2057
110	514	1027	2053	4105
111	1026	2051	4101	8201

Table 24. Normalized conversion time ($T_{CONV} \cdot f_S$) vs. SET_OSR[2:0] and SET_NELC[1:0] (normalized to sampling period $1/f_S$)

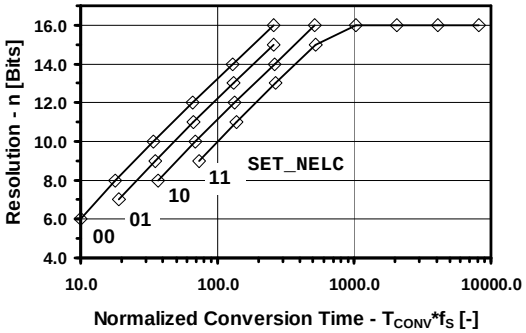


Figure 5. Resolution vs. normalized conversion time for different SET_NELC[1:0]

Advanced configuration (Cont.)

Output Code Format

The ADC output code is a 16-bit word in two's complement format (see Table 25). For input voltages outside the range, the output code is saturated to the closest full-scale value (i.e. 0x7FFF or 0x8000). For resolutions smaller than 16 bits, the non-significant bits are forced to the values shown in Table 26. The output code, expressed in LSBs, corresponds to:

$$OUT_{ADC} = 2^{16} \cdot \frac{V_{IN,ADC}}{V_{REF}} \cdot \frac{OSR+1}{OSR} \quad \text{(LSB)} \qquad \text{(Eq.17)}$$

Recalling equation Eq. 9, this can be rewritten as:

$$OUT_{ADC} = 2^{16} \cdot \frac{V_{IN}}{V_{REF}} \cdot \left(GD_{TOT} - GDoff_{TOT} \cdot \frac{V_{REF}}{V_{IN}} \right) \cdot \frac{OSR+1}{OSR} \qquad \text{(LSB)} \quad \text{(Eq. 18)}$$

where, from Eq. 10 and Eq. 11, the total PGA gain and offset are respectively:

$$GD_{TOT} = GD_3 \cdot GD_2 \cdot GD_1 \text{ (V/V)}$$

and:

$$GDoff_{TOT} = GDoff_3 + GD_3 \cdot GDoff_2 \qquad \text{(V/V)}$$

ADC Input Voltage $V_{IN,ADC}$	% of Full Scale (FS)	Output in LSBs	Output Code in Hex
+2.49505 V	+0.5·FS	$+2^{15}$-1 =+32'767	7FFF
+2.49497 V	…	$+2^{15}$-2 =+32'766	7FFE
…	…	…	…
+76.145µV	…	+1	0001
0V	0	0	0000
-76.145µV	…	-1	8FFF
…	…	…	…
-2.49505V	…	-2^{15}-1 =-32'767	8001
-2.49513V	-0.5·FS	-2^{15} =-32'768	8000

Table 25. Basic ADC Relationships (example for: V_{REF} = 5V, *OSR* = 512, *n* = 16 bits)

Advanced configuration (Cont.)

Output Code Format (Cont.)

SET_OSR [2:0]	SET_NELC = 00	SET_NELC = 01	SET_NELC = 10	SET_NELC = 11
000	1000000000	100000000	10000000	1000000
001	10000000	1000000	100000	10000
010	100000	10000	1000	100
011	1000	100	10	1
100	10	1	-	-
101	-	-	-	-
110	-	-	-	-
111	-	-	-	-

Table 26. Last forced LSBs in conversion output registers for resolution settings smaller than 16 bits (*n* < 16) (RegACOutMSB[7:0] & RegACOutLSB[7:0])

The equivalent LSB size at the input of the PGA chain is:

$$LSB = \frac{1}{2^n} \cdot \frac{V_{REF}}{GD_{TOT}} \cdot \frac{OSR}{OSR+1} \quad \text{(V)} \qquad \text{(Eq. 19)}$$

Notice that the input voltage $V_{IN,ADC}$ of the ADC must satisfy the condition:

$$\left|V_{IN,ADC}\right| \le \frac{1}{2} \cdot (V_{REFP} - V_{REFN}) \cdot \frac{OSR}{OSR+1} \quad \text{(V)} \qquad \text{(Eq. 20)}$$

to remain within the ADC input range.

Advanced configuration (Cont.)

Power Saving Modes

During low-speed operation, the bias current in the PGAs and ADC can be programmed to save power using the control words **IB_AMP_PGA[1:0]** and **IB_AMP_ADC[1:0]** (see Table 27). If the system is idle, the PGAs and ADC can even be disabled, thus, reducing power consumption to its minimum. This can considerably improve battery lifetime.

IB_AMP_ADC [1:0]	IB_AMP_PGA [1:0]	ADC Bias Current	PGA Bias Current	Max. f_S [kHz]
00	x	$1/4 \cdot I_{ADC}$	x	62.5
01		$1/2 \cdot I_{ADC}$		125
10		$3/4 \cdot I_{ADC}$		250
11		I_{ADC}		500
x	00	x	$1/4 \cdot I_{PGA}$	62.5
	01		$1/2 \cdot I_{PGA}$	125
	10		$3/4 \cdot I_{PGA}$	250
	11		I_{PGA}	500

Table 27. ADC & PGA power saving modes and maximum sampling frequency

Specifications and Measured Curves

This section presents measurement results for the acquisition chain. A summary table with circuit specifications and measured curves are given.

Default Settings

Unless otherwise specified, the measurement conditions are the following:

- Temperature T_A = +25°C
- V_{BATT} = +5V, GND = 0V, V_{REF} = +5V, V_{IN} = 0V
- RC frequency f_{RC} = 2MHz, sampling frequency f_S = 500kHz
- Offsets $GDOff_2$ = $GDOff_3$ = 0
- Power operation: normal (**IB_AMP_ADC[1:0]** = **IB_AMP_PGA[1:0]** = '11')
- Resolution: for n = 12 bits: OSR = 32 and N_{ELCONV} = 4
  for n = 16 bits: OSR = 512 and N_{ELCONV} = 2

Advanced configuration (Cont.)

Specifications

Unless otherwise specified: Temperature T_A = +25°C, V_{BATT} = +5V, GND = 0V, V_{REF} = +5V, V_{IN} = 0V, RC frequency f_{RC} = 2MHz, sampling frequency f_S = 500kHz, Overall PGA gain GD_{TOT} = 1, offsets $GDOff_2$ = $GDOff_3$ = 0. Power operation: normal (`IB_AMP_ADC[1:0]` = `IB_AMP_PGA[1:0]` = '11'). For resolution n = 12 bits: OSR = 32 and N_{ELCONV} = 4. For resolution n = 16 bits: OSR = 512 and N_{ELCONV} = 2.

PARAMETER	VALUE			UNITS	COMMENTS/CONDITIONS
	MIN	TYP	MAX		
ANALOG INPUT CHARACTERISTICS					
Differential Input Voltage Ranges	-2.42		+2.42	V	Gain = 1, *OSR* = 32
$V_{IN} = (V_{INP} - V_{INN})$	-24.2		+24.2	mV	(Note 1)
	-2.42		+2.42	mV	Gain = 100, *OSR* = 32
					Gain = 1000, *OSR* = 32
Reference Voltage Range					
$V_{REF} = (V_{REFP} - V_{REFN})$			V_{Batt}	V	
PROGRAMMABLE GAIN AMPLIFIERS (PGA)					
Total PGA Gain, GD_{TOT}	0.5		1000	V/V	
PGA1 Gain, GD_1	1		10	V/V	See Table 15
PGA2 Gain, GD_2	1		10	V/V	See Table 16
PGA3 Gain, GD_3	0		127/12	V/V	Step=1/12 V/V, See Table 18
Gain Setting Precision (each stage)	-3	±0.5	+3	%	
		±5		ppm/°C	
Gain Temperature Dependence					
Offset	-1		+1	V/V	
PGA2 Offset, $GDoff_2$	-127/12		+127/1	V/V	Step=0.2 V/V, See Table 17
PGA3 Offset, $GDoff_3$	-3	±0.5	2	%	Step=1/12 V/V, See Table 19
Offset Setting Precision (PGA2 or 3)		±5	+3	ppm/°C	(Note 2)
Offset Temperature Dependence	1500			kΩ	
Input Impedance	150			kΩ	
PGA1	150			kΩ	PGA1 Gain = 1 (Note 3)
					PGA1 Gain = 10 (Note 3)
PGA2, PGA3		205		µV	Maximal gain (Note 3)
Output RMS Noise		340		µV	
PGA1		365		µV	(Note 4)
PGA2					(Note 5)
PGA3					(Note 6)
ADC STATIC PERFORMANCE					
Resolution, n	6		16	Bits	(Note 7)
No Missing Codes					(Note 8)
Gain Error		±0.15		% of FS	(Note 9)
Offset Error		±1		LSB	n = 16 bits (Note 10)
Integral Non-Linearity, INL					
Resolution n = 16 Bits		±1.0		LSB	(Note 11)
Differential Non-Linearity, DNL					
Resolution n = 16 Bits		±0.5		LSB	(Note 12)
Power Supply Rejection Ratio, PSRR		78		dB	V_{Batt} = 5V ± 0.3V (Note 13)
		72		dB	V_{Batt} = 3V ± 0.3V (Note 13)

Advanced configuration (Cont.)

Specifications (Cont'd)

PARAMETER	VALUE			UNITS	COMMENTS/CONDITIONS
	MIN	TYP	MAX		
DYNAMIC PERFORMANCE					
Sampling Frequency, f_S	3			kHz	
Conversion Time, T_{CONV}		133		cycles/f_S	n = 12 bits (Note 14)
		1027		cycles/f_S	n = 16 bits (Note 14)
Throughput Rate (Continuous Mode), $1/T_{CONV}$		3.76		kSps	n = 12 bits, f_S = 500kHz
		0.49		kSps	n = 16 bits, f_S = 500kHz
Nbr of Initialization Cycles, N_{INIT}	0		2	cycles	
Nbr of End Conversion Cycles, N_{END}	0		5	cycles	
PGA Stabilization Delay		*OSR*		cycles	(Note 15)
DIGITAL OUTPUT					
ADC Output Data Coding					Binary Two's Complement See Table 25 and Table 26
POWER SUPPLY					
Voltage Supply Range, V_{Batt}	+2.4	+5	+5.5	V	
Analog Quiescent Current Consumption, Total (I_Q)		720/620		µA	Only Acquisition Chain V_{Batt} = 5V/3V
ADC Only		250/190		µA	V_{Batt} = 5V/3V
PGA1		165/150		µA	V_{Batt} = 5V/3V
PGA2		130/120		µA	V_{Batt} = 5V/3V
PGA3		175/160		µA	V_{Batt} = 5V/3V
Analog Power Dissipation					All PGAs & ADC Active
Normal Power Mode		3.6/1.9		mW	V_{Batt} = 5V/3V (Note 16)
3/4 Power Reduction Mode		2.7/1.4		mW	V_{Batt} = 5V/3V (Note 17)
		1.8/0.9		mW	V_{Batt} = 5V/3V (Note 18)
1/2 Power Reduction Mode		0.9/0.5		mW	V_{Batt} = 5V/3V (Note 19)
1/4 Power Reduction Mode					
TEMPERATURE					
Specified Range	-40		+85	°C	
Operating Range	-40		+125	°C	

Notes:

(1) Gain defined as overall PGA gain $GD_{TOT} = GD_1 \cdot GD_2 \cdot GD_3$. Maximum input voltage is given by: $V_{IN,MAX} = \pm(V_{REF}/2) \cdot (OSR/OSR+1)$.
(2) Offset due to tolerance on $GDoff_2$ or $GDoff_3$ setting. For small intrinsic offset, use only ADC and PGA1.
(3) Measured with block connected to inputs through AMUX block. Normalized input sampling frequency for input impedance is f_S = 512kHz. This figure must be multiplied by 2 for f_S = 256kHz, 4 for f_S = 128kHz. Input impedance is proportional to $1/f_S$.
(4) Figure independent from PGA1 gain and sampling frequency f_S. See equation Eq. 21 to calculate equivalent input noise.
(5) Figure independent on PGA2 gain and sampling frequency f_S.. See equation Eq. 21 to calculate equivalent input noise.
(6) Figure independent on PGA3 gain and sampling frequency f_S. See equation Eq. 21 to calculate equivalent input noise.
(7) Resolution is given by $n = 2 \cdot \log2(OSR) + \log2(N_{ELCONV})$. *OSR* can be set between 8 and 1024, in powers of 2. N_{ELCONV} can be set to 1, 2, 4 or 8.
(8) If a ramp signal is applied to the input, all digital codes appear in the resulting ADC output data.

Advanced configuration (Cont.)

Specifications (Cont'd)

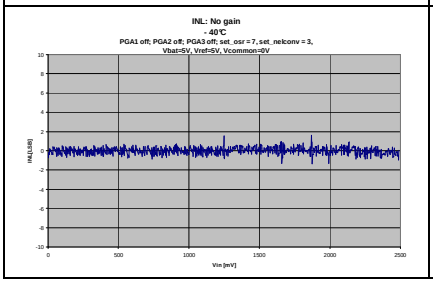
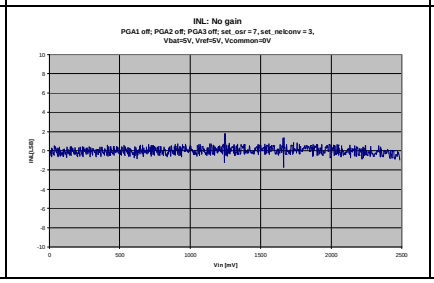
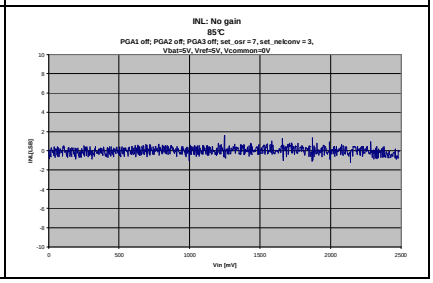
(9) Gain error is defined as the amount of deviation between the ideal (theoretical) transfer function and the measured transfer function (with the offset error removed).
(10) Offset error is defined as the output code error for a zero volt input (ideally, output code = 0). For ± 1 LSB offset, N_{ELCONV} must be ≥2.
(11) INL defined as the deviation of the DC transfer curve of each individual code from the best-fit straight line. This specification holds over the full scale.
(12) DNL is defined as the difference (in LSB) between the ideal (1 LSB) and measured code transitions for successive codes.
(13) Figures for Gains = 1 to 100. PSRR is defined as the amount of change in the ADC output value as the power supply voltage changes.
(14) Conversion time is given by: $T_{CONV} = (N_{ELCONV} \cdot (OSR + 1) + 1) / f_S$. *OSR* can be set between 8 and 1024, in powers of 2. N_{ELCONV} can be set to 1, 2, 4 or 8.
(15) PGAs are reset after each writing operation to registers **RegACCfg1-5**. The ADC must be started after a PGA or inputs common-mode stabilisation delay. This is done by writing bit `Start` several cycles after PGA settings modification or channel switching. Delay between PGA start or input channel switching and ADC start should be equivalent to *OSR* (between 8 and 1024) number of cycles. This delay does not apply to conversions made without the PGAs.
(16) Nominal (maximum) bias currents in PGAs and ADC, i.e. **IB_AMP_PGA[1:0]** = '11' and **IB_AMP_ADC[1:0]** = '11'.
(17) Bias currents in PGAs and ADC set to 3/4 of nominal values, i.e. **IB_AMP_PGA[1:0]** = '10', **IB_AMP_ADC[1:0]** = '10'.
(18) Bias currents in PGAs and ADC set to 1/2 of nominal values, i.e. **IB_AMP_PGA[1:0]** = '01', **IB_AMP_ADC[1:0]** = '01'.
(19) Bias currents in PGAs and ADC set to 1/4 of nominal values, i.e. **IB_AMP_PGA[1:0]** = '00', **IB_AMP_ADC[1:0]** = '00'.

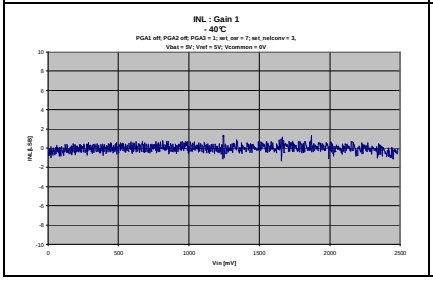
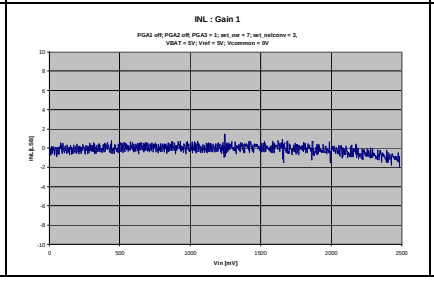
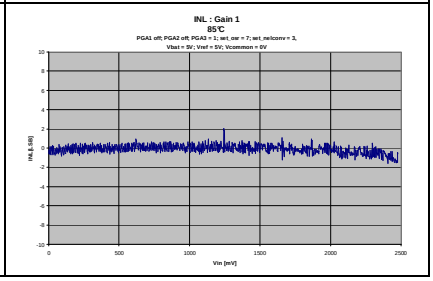
Advanced configuration (Cont.)

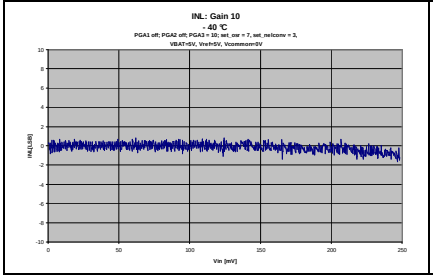
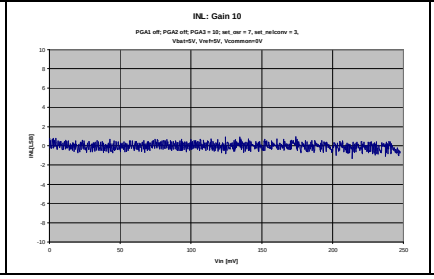
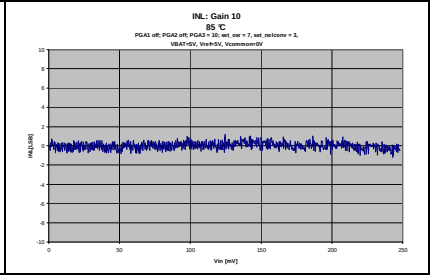
ZoomingADC ™ Performances

Integral non linearity

The following tables show the Integral non linearity over the SX8722 temperature range.

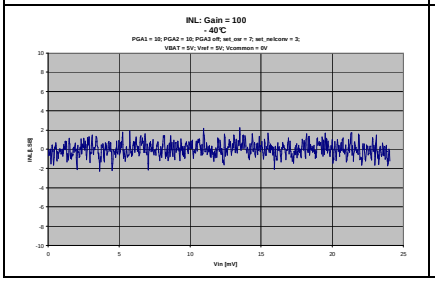
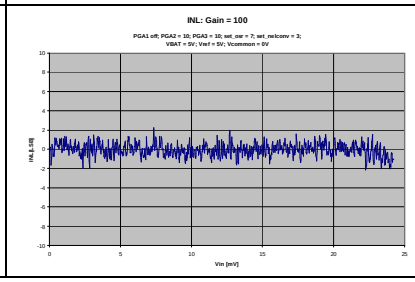
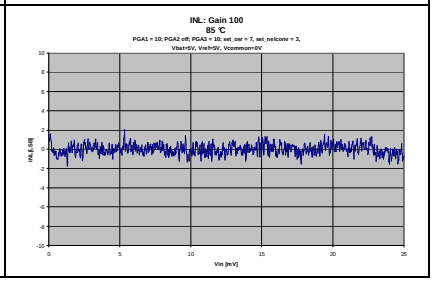
ADC without PGA		
-40°C	25°C	85°C
		

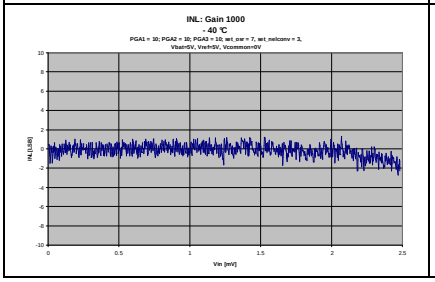
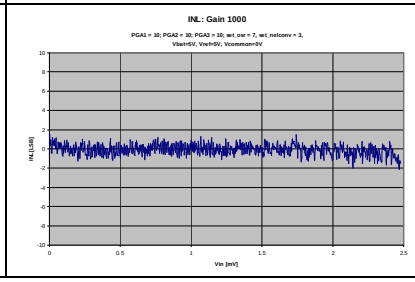
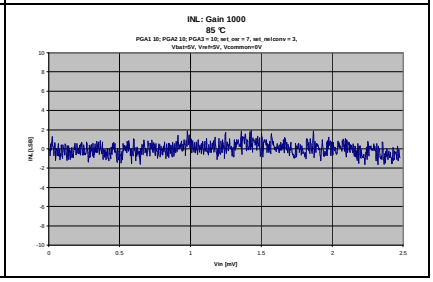
Gain 1		
-40°C	25°C	85°C
		

Gain 10		
-40°C	25°C	85°C
		

Advanced configuration (Cont.)

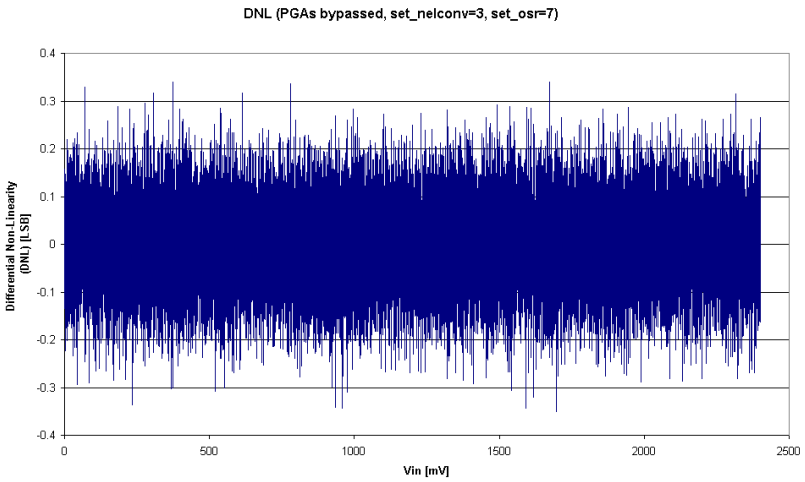
Integral non linearity (Cont.)

Gain 100		
-40°C	25°C	85°C
		

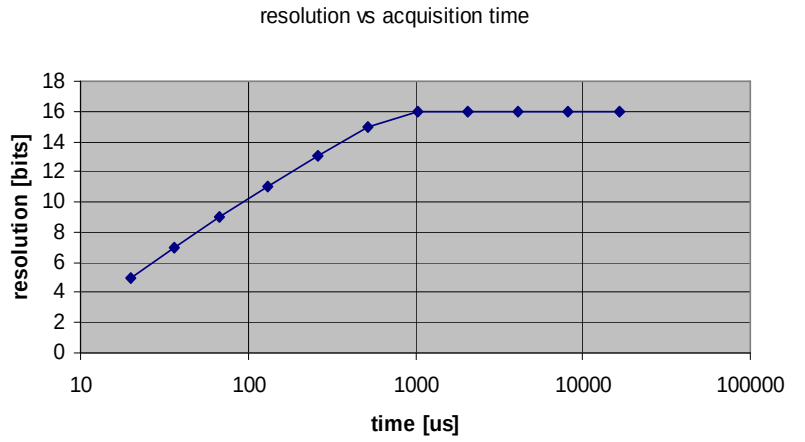
Gain 1000		
-40°C	25°C	85°C
		

Advanced configuration (Cont.)

Differential non linearity

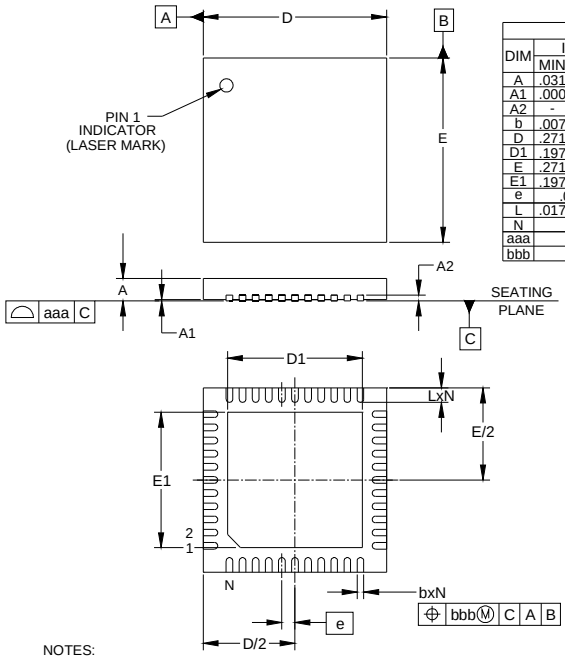
DNL: significantly lower than one LSB	

Resolution vs Acquisition time

resolution vs acquisition time	

Package specifications

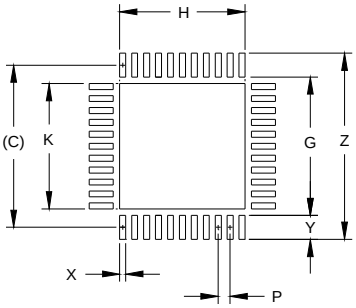
Outline drawings MLPQ 7x7mm 44 pins



DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.040	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.271	.275	.279	6.90	7.00	7.10
D1	.197	.203	.207	5.00	5.15	5.25
E	.271	.275	.279	6.90	7.00	7.10
E1	.197	.203	.207	5.00	5.15	5.25
e	.020 BSC			0.50 BSC		
L	.017	.021	.025	0.45	0.55	0.65
N	44			44		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern MLPQ 7x7mm 44 pins



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.268)	(6.80)
G	.228	5.80
H	.207	5.25
K	.207	5.25
P	.021	0.50
X	.011	0.30
Y	.039	1.00
Z	.307	7.80

NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Contact Information

Semtech Corporation
Advanced Communication and Sensing Business Unit
Monruz 2, 2000 Neuchâtel, Switzerland
www.semtech.com