DESCRIPTION

The SX8723S is a data acquisition system based on Semtech's low power ZoomingADC™ technology. It directly connects most types of miniature sensors with a general purpose microcontroller.

With 2 differential inputs, it can adapt to multiple sensor systems. Its digital outputs are used to bias or reset the sensing elements.

FEATURES

- Up to 16-bit differential data acquisition
- Programmable gain: (1/12 to 1000)
- Sensor offset compensation up to 15 times full scale of input signal
- 2 differential or 4 single-ended signal inputs
- Programmable Resolution versus Speed versus Supply current
- Internal time base
- Low-power (250 uA for 16b @ 250 S/s)
- SPI interface, 2 Mbps serial clock

APPLICATIONS

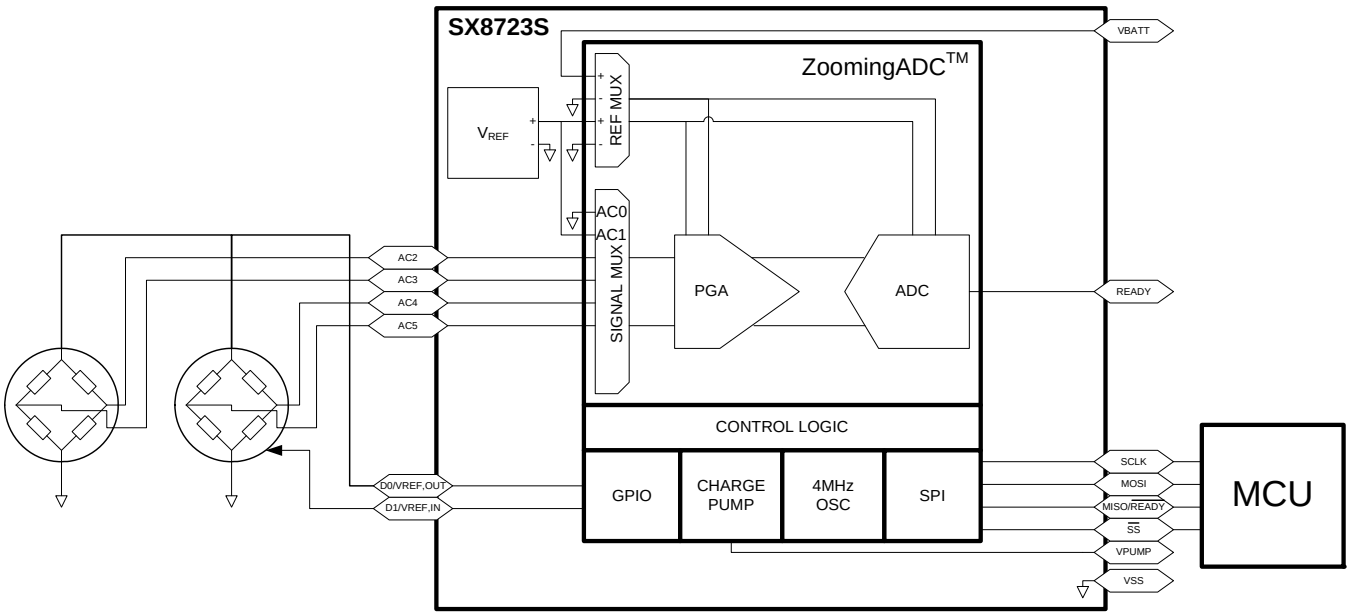
- Industrial pressure sensing
- Industrial temperature sensing
- Industrial chemical sensing
- Barometer
- Compass

ORDERING INFORMATION

DEVICE	PACKAGE	REEL QUANTITY
SX8723SWLTDT	MLPQ-W-16 4x4	1000

- Available in tape and reel only
- WEEE/RoHS compliant, Pb-Free and Halogen Free.

FUNCTIONAL BLOC DIAGRAM



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ELECTRICAL SPECIFICATIONS

1 Absolute Maximum Ratings

Note The Absolute Maximum Ratings, in table below, are stress ratings only. Functional operation of the device at conditions other than those indicated in the Operating Conditions sections of this specification is not implied.
Exposure to the absolute maximum ratings, where different to the operating conditions, for an extended period may reduce the reliability or useful lifetime of the product.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Units
Power supply	V_{BATT}		V_{SS} - 0.3	6.5	V
Storage temperature	T_{STORE}		-55	150	°C
Temperature under bias	T_{BIAS}		-40	140	°C
Input voltage	V_{INABS}	All inputs	V_{SS} - 300	V_{BATT} + 300	mV
Peak reflow temperature	T_{PKG}			260	°C
ESD conditions	ESD_{HBM}	Human Body Model ESD	2000		V
Latchup			100		mA

2 Operating Conditions

Unless otherwise specified: *VREF,ADC* = *VBATT*, *VIN* = 0V, Over-sampling frequency *fs* = 250 kHz, *PGA3 on with Gain = 1*, *PGA1&PGA2 off*, offsets *GDOff2* = *GDOff3* = 0. Power operation: normal (*IbAmpAdc[1:0]* = *IbAmpPga[1:0]* = '01').
For resolution n = 12 bits: *OSR* = 32 and *NELCONV* = 4.
For resolution n = 16 bits: *OSR* = 256 and *NELCONV* = 2.
Bandgap chopped at *NELCONV* rate. If *VBATT* < 3V, Charge Pump is forced on. If *VBATT* > 3V, Charge Pump is forced off.

Table 2. Operating conditions limits

Parameter	Symbol	Comment/Condition	Min	Typ	Max	Unit
Power supply	VBATT		2.4		5.5	V
Operating temperature	TOP		-40		125	°C

.

Table 3. Electrical Characteristics

Parameter	Symbol	Comment/Condition	Min	Typ	Max	Unit
CURRENT CONSUMPTION[1]						
Active current, 5.5V	IOP55	16 b @ 250 Sample/s ADC, fs = 125 kHz		250	300	µA
		16 b @ 1kSample/s PGA3 + ADC, fs = 500 kHz		650	850	
		16 b + gain 1000 @ 1kSample/s PGA3,2,1 + ADC, fs = 500 kHz		1000	1250	
Active current, 3.3V	IOP33	16 b @ 250 Sample/s ADC, fs = 125 kHz		150		µA
		16 b @ 1 kSample/s PGA3 + ADC, fs = 500 kHz		500		
		16 b + gain 1000 @ 1kSample/s PGA3,2,1 + ADC, fs = 500 kHz		830		
Sleep current	ISLEEP	@25°C		150	250	nA
		up to 85°C		200		
		@125°C		250		
TIME BASE						
Max ADC Over-Sampling frequency	fSmax	@25°C	425	500	575	kHz
ADC Over-Sampling frequency drift	fST			0.15		% / °C
DIGITAL I/O						
Input logic high	VIH		0.7			VBATT
Input logic low	VIL				0.3	VBATT
Output logic high	VOH	IOH < 4 mA			VBATT-0.4	V
Output logic low	VOL	IOL < 4 mA	0.4			V
Leakages currents						

Table 3. Electrical Characteristics

Parameter	Symbol	Comment/Condition	Min	Typ	Max	Unit
Input leakage current	I_{LeakIn}	Digital input mode, no pull-up or pull-down	-100		100	nA
VREF: Internal Bandgap Reference						
Absolute output voltage	V_{BG}	V_{BATT} > 3V	1.19	1.22	1.25	V
Variation over Temperature	V_{BGT}	V_{BATT} > 3V, over Temperature	-1.5		+1.5	%
Total Output Noise	V_{BGN}	V_{BATT} > 3V			1	mVrms

1. The device can be operated in either active or sleep states. The Sleep state is complete shutdown, but the active state can have a variety of different current consumptions depending on the settings. Some examples are given here: The Sleep state is the default state after power-on-reset. The chip can then be placed into an active state after a Slave Select command on $\overline{SS}$ pin is received.

Table 4. ZoomingADC Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ANALOG INPUT CHARACTERISTICS						
Differential Input Voltage Range $V_{IN} = V_{INP}-V_{INN}$		Gain=1, OSR=32, V_{REF}=5V. **Note 1**	-2.42		+2.42	V
		Gain=100, OSR=32, V_{REF}=5V	-24.2		+24.2	mV
		Gain=1000, OSR=32, V_{REF}=5V	-2.42		+2.42	mV
PROGRAMMABLE GAIN AMPLIFIER						
Total PGA Gain	GD_{TOT}	**Note 1**	1/12		1000	V/V
PGA1 Gain	GD_1	(see **Table 10, page 22**)	1		10	V/V
PGA2 Gain	GD_2	(see **Table 11, page 22**)	1		10	V/V
PGA3 Gain	GD_3	Step = 1/12 V/V (see **Table 12, page 22**)	1/12		127/12	V/V
Gain Settings Precision (each stage)		Gain ≥ 1	-3	±0.5	+3	%
Gain Temperature Dependence				±5		ppm / °C
PGA2 Offset	GD_{OFF2}	Step = 0.2 V/V (see **Table 11, page 22**)	-1		+1	V/V
PGA3 Offset	GD_{OFF3}	Step = 1/12 V/V (see **Table 12, page 22**)	-63/12		+63/12	V/V
Offset Settings Precision (PGA2 or PGA3)		**Note 2**	-3	±0.5	+3	%
Offset Temperature Dependence				±5		ppm / °C
Input Impedance on ADC	Z_{INADC}		500			kΩ
Input Impedance on PGA1 (see **section 11.1, page 48**)	Z_{INPGA1}	Gain = 1. **Note 3**	900	1150		kΩ
		Gain = 10. **Note 3**	250	350		kΩ
Input Impedance on PGA2	Z_{INPGA2}	Gain = 1. **Note 3**	500	1000		kΩ
		Gain = 10. **Note 3**	125	270		kΩ
Input Impedance on PGA3	Z_{INPGA3}	Gain = 1. **Note 3**	500	780		kΩ
		Gain = 10. **Note 3**	125	190		kΩ

Table 4. ZoomingADC Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output RMS Noise per over-sample		PGA1. **Note 4**		205		µV
		PGA2. **Note 4**		340		µV
		PGA3. **Note 4**		365		µV
ADC STATIC PERFORMANCES						
Resolution (No Missing Codes)	n	**Note 5** **Note 6**	6		16	Bits
Gain Error		**Note 7**		±0.15		%
Offset Error		n = 16 bits. **Note 8**		±1		LSB
Integral Non-Linearity	INL	resolution n = 12 bits. **Note 9**		±0.6		LSB
		resolution n = 16 bits. **Note 9**		±1.5		LSB
Differential Non-Linearity	DNL	resolution n = 12 bits. **Note 10**		±0.5		LSB
		resolution n = 16 bits. **Note 10**		±0.5		LSB
Power Supply Rejection Ratio DC	PSRR	V_{BATT} = 5V +/- 0.3V. **Note 11**		78		dB
		V_{BATT} = 3V +/- 0.3V. **Note 11**		72		dB
ADC DYNAMIC PERFORMANCES						
Conversion Time	T_{CONV}	n = 12 bits. **Note 12**		133		fs cycles
		n = 16 bits. **Note 12**		517		fs cycles
Throughput Rate (Continuous Mode)	$1/T_{CONV}$	n = 12 bits, fs = 250 kHz		1.88		kSps
		n = 16 bits, fs = 250 kHz		0.483		kSps
PGA Stabilization Delay		**Note 13** (see **Table 11, page 22**)		OSR		fs cycles
ZADC ANALOG QUIESCENT CURRENT						
ADC Only Consumption	I_Q	V_{BATT} = 5.5V/3.3V		285/210		µA
PGA1 Consumption		V_{BATT} = 5.5V/3.3V		104/80		µA
PGA2 Consumption		V_{BATT} = 5.5V/3.3V		67/59		µA
PGA3 Consumption		V_{BATT} = 5.5V/3.3V		98/91		µA
ANALOG POWER DISSIPATION: All PGAs & ADC Active						
Normal Power Mode		V_{BATT} = 5.5V/3.3V. **Note 14**		4.0/2.0		mW
3/4 Power Reduction Mode		V_{BATT} = 5.5V/3.3V. **Note 15**		3.2/1.6		mW
1/2 Power Reduction Mode		V_{BATT} = 5.5V/3.3V. **Note 16**		2.4/1.1		mW
1/4 Power Reduction Mode		V_{BATT} = 5.5V/3.3V. **Note 17**		1.5/0.7		mW

(1) Gain defined as overall *PGA* gain *GDTOT* = *GD1* x *GD2* x *GD3*. Maximum input voltage is given by: $V_{IN,MAX} = \pm(V_{REF} / 2) (OSR / OSR+1)$.
(2) Offset due to tolerance on *GDoff2* or *GDoff3* setting. For small intrinsic offset, use only *ADC* and *PGA1*.
(3) Measured with block connected to inputs through *Amux* block. Normalized input sampling frequency for input impedance is f_S = 500 kHz (f_S max, worst case). This figure must be multiplied by 2 for f_S = 250 kHz, 4 for f_S = 125 kHz. Input impedance is proportional to $1/f_S$.
(4) Figure independent from gain and sampling frequency. fs. The effective output noise is reduced by the over-sampling ratio
(5) Resolution is given by n = 2 log2(*OSR*) + log2(N_{ELCONV}). *OSR* can be set between 8 and 1024, in powers of 2. N_{ELCONV} can be set to 1, 2, 4 or 8.
(6) If a ramp signal is applied to the input, all digital codes appear in the resulting *ADC* output data.
(7) Gain error is defined as the amount of deviation between the ideal (theoretical) transfer function and the measured transfer function (with the offset error removed).
(8) Offset error is defined as the output code error for a zero volt input (ideally, output code = 0). For 1 LSB offset, N_{ELCONV} must be at least 2.

(9) INL defined as the deviation of the DC transfer curve of each individual code from the best-fit straight line. This specification holds over the full scale.
(10) DNL is defined as the difference (in LSB) between the ideal (1 LSB) and measured code transitions for successive codes.
(11) Values for Gain = 1. PSRR is defined as the amount of change in the *ADC* output value as the power supply voltage changes.
(12) Conversion time is given by: $T_{CONV} = (N_{ELCONV}(OSR + 1) + 1) / fs$. *OSR* can be set between 8 and 1024, in powers of 2. N_{ELCONV} can be set to 1, 2, 4 or 8.
(13) PGAs are reset after each writing operation to registers **RegACCfg1-5**, corresponding to change of configuration or input switching. The *ADC* should be started only some delay after a change of PGA configuration through these registers. Delay between change of configuration of PGA or input channel switching and ADC start should be equivalent to OSR (between 8 and 1024) number of cycles. This is done by writing bit Start several cycles after *PGA* settings modification or channel switching. This delay does not apply to conversions made without the *PGAs*.
(14) Nominal (maximum) bias currents in *PGAs* and *ADC*, i.e. *IbAmpPga[1:0]* = '11' and *IbAmpAdc[1:0]* = '11'.
(15) Bias currents in *PGAs* and *ADC* set to 3/4 of nominal values, i.e. *IbAmpPga[1:0]* = '10', *IbAmpAdc[1:0]* = '10'.
(16) Bias currents in *PGAs* and *ADC* set to 1/2 of nominal values, i.e. *IbAmpPga[1:0]* = '01', *IbAmpAdc[1:0]* = '01'.
(17) Bias currents in *PGAs* and *ADC* set to 1/4 of nominal values, i.e. *IbAmpPga[1:0]* = '00', *IbAmpAdc[1:0]* = '00'.

2.1 Timing Characteristics

Table 5. General timings

Parameter	Symbol	Comment/Condition	Min	Typ	Max	Unit
ADC INTERRUPT (READY) TIMING SPECIFICATIONS						
READY pulse width	t_{IRQ}	**Note 18**		1		1/fs
STARTUP TIMES						
Startup sequence time at POR	$t_{STARTUP}$				800	µs
Time to enable RC from Sleep after a SPI command	t_{RCEN}			100	450	µs
Effective Start	t_{START_SPI}			250		µs

(18) The READY pulse indicates End of Conversion. This is a Positive pulse of duration equal to one cycle of the ADC sampling rate in "continuous mode". See also **Figure 15, page 30** for data conversion waveforms.

2.1.1 POR Timings

The Slave Select pin ($\overline{SS}$) can be used to detect the effective start of the device. See **section 9.4, page 42** for functional descriptions. The SPI interface can be accessed as soon as the $\overline{SS}$ pin (slave) is set to 'input' as illustrated on **Figure 2**.

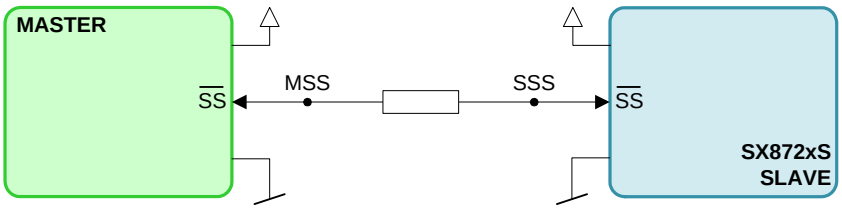


Figure 1. SPI Master detecting start sequence through Slave Select pin

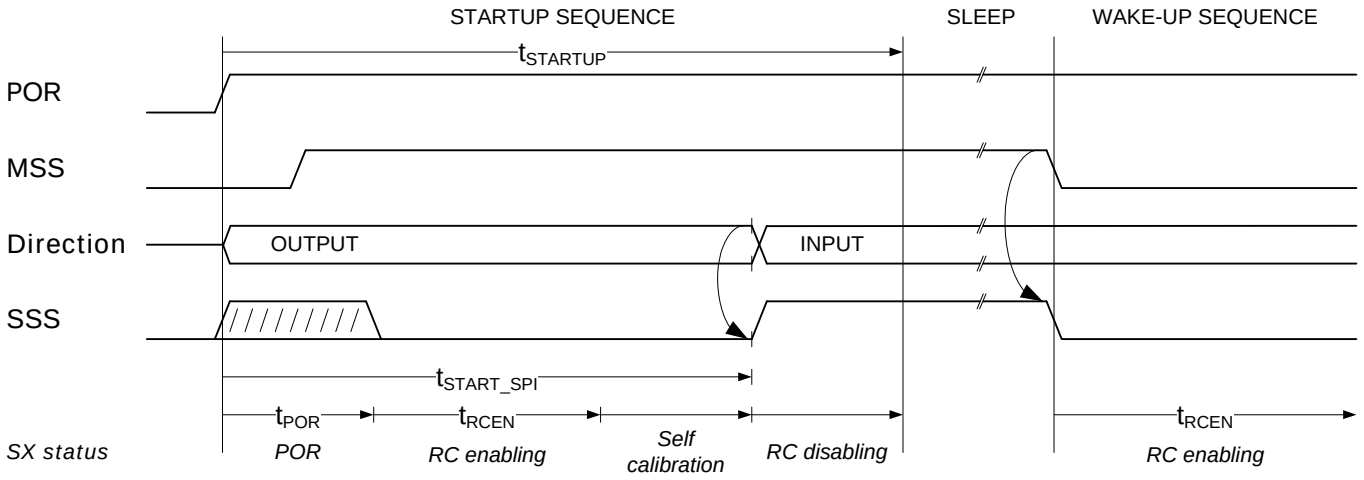


Figure 2. Slave Select pin and Power-On-Reset Timings

2.1.2 SPI interface timings

Parameter	Symbol	Min	Typ	Max	Units
$\overline{SS}$ to SCLK Edge	t_{SSSC}	30			ns
SCLK Period	t_{SC}	500			ns
SCLK Low Pulse width	t_{SCL}	200			ns
SCLK High Pulse width	t_{SCH}	200			ns
Data Output Valid after SCLK Edge	t_{DV}		125	200	ns
Data Input Setup Time before SCLK Edge	t_{DS}	0			ns
Data Input Hold Time after SCLK Edge	t_{DH}	100	250		ns
$\overline{SS}$ High after SCLK Edge	t_{SCSS}	0			ns
$\overline{SS}$ High to MISO High Impedance	t_{SSD}			30	ns

2.1.3 SPI timing diagram

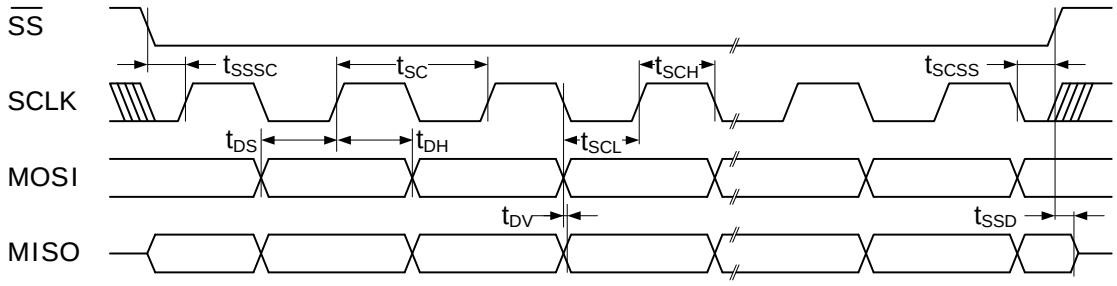
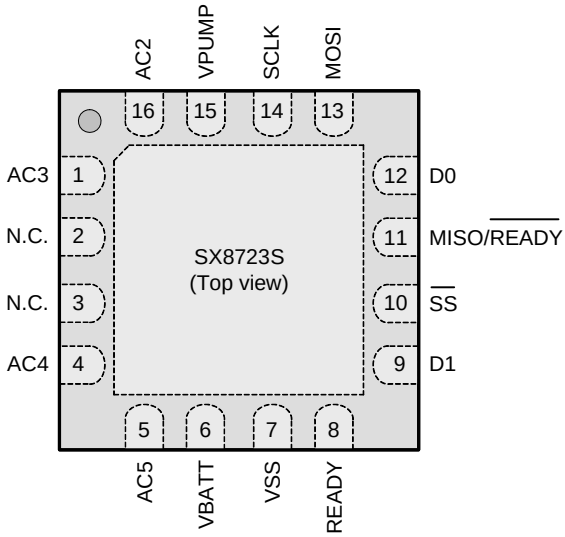


Figure 3. SPI timing diagram

3 Pin Configuration



4 Marking Information

nnnnn = Part Number
yyww = Date Code[1]
xxxxx = Semtech Lot Number
xxxxx

1.Date codes and Lot numbers starting with the 'E' character are used for Engineering samples

5 Pin Description

Note The bottom pad is internally connected to *VSS*. It should also be connected to *VSS* on PCB to reduce noise and improve thermal behavior.

Pin	Name	Type	Function
1	AC3	Analog Input	Differential sensor input in conjunction with AC2
2	N.C.	-	Not used
3	N.C.	-	Not used
4	AC4	Analog Input	Differential sensor input in conjunction with AC5
5	AC5	Analog Input	Differential sensor input in conjunction with AC4
6	VBATT	Power Input	2.4V to 5.5V power supply
7	VSS	Power Input	Chip Ground
8	READY	Digital Output	Data Ready (active high). Conversion complete flag.
9	D1	Digital IO	Digital output sensor drive (V_{BATT} or V_{SS})
		Analog	V_{REF} Input in optional operating mode
10	SS	Digital Input	Chip select (active low).
11	MISO/$\overline{\text{READY}}$	Digital Output	Serial data output (Master Input, Slave Output), or data out combined with READY (active low when ADC Data Ready function enabled).
12	D0	Digital IO	Digital output sensor drive (V_{BATT} or V_{SS})
		Analog	V_{REF} Output in optional operating mode
13	MOSI	Digital Input	Serial data input (Master Output, Slave Input).
14	SCLK	Digital Input	Serial clock input.
15	VPUMP	Power IO	Charge pump output. Raises ADC supply above V_{BATT} if V_{BATT} supply is too low. Recommended range for capacitor is 1nF to 10 nF. Connect the capacitor to ground.
16	AC2	Analog Input	Differential sensor input in conjunction with AC3

6 General Description

The SX8723S is a complete low-power acquisition path with programmable gain, acquisition speed and resolution.

6.1 Bloc diagram

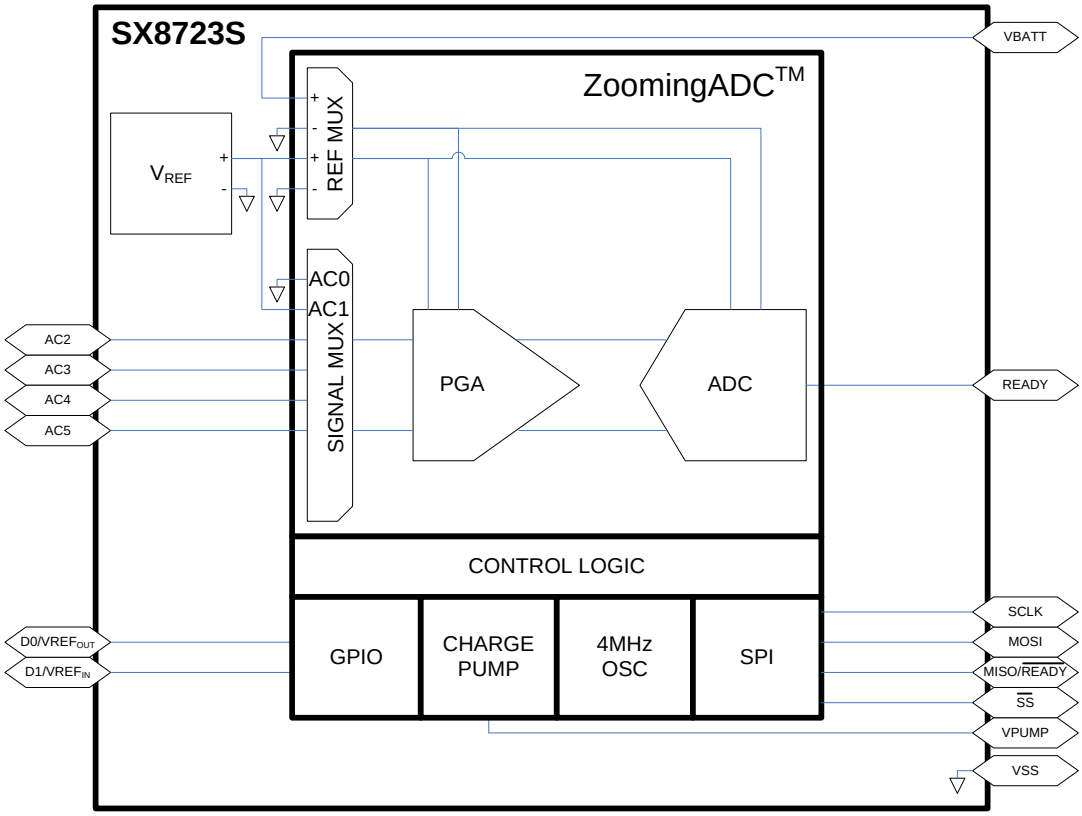


Figure 4. SX8723S bloc diagram

6.2 VREF

The internally generated *VREF* is a trimmed bandgap reference with a nominal value of 1.22V that provides a stable voltage reference for the *ZoomingADC*.

This reference voltage is directly connected to one of the ZoomingADC reference multiplexer inputs.

The bandgap voltage stability is only guaranteed for *VBATT* voltages of 3V and above. As *VBATT* drops down to 2.4V, the bandgap voltage could reduce by up to 50mV.

The bandgap has relatively weak output drive so it is recommended that if the bandgap is required as a signal input then *PGA1* must be enabled with gain = 1.

6.3 GPIO

The *GPIO* block is a multipurpose 2 bit input/output port. In addition to digital behavior, *D0* and *D1* pins can be programmed as analog pins in order to be used as output (reference voltage monitoring) and input for an external

reference voltage (For further details see **Figure 7**, **Figure 8**, **Figure 9** and **Figure 10**). Each port terminal can be individually selected as digital input or output.

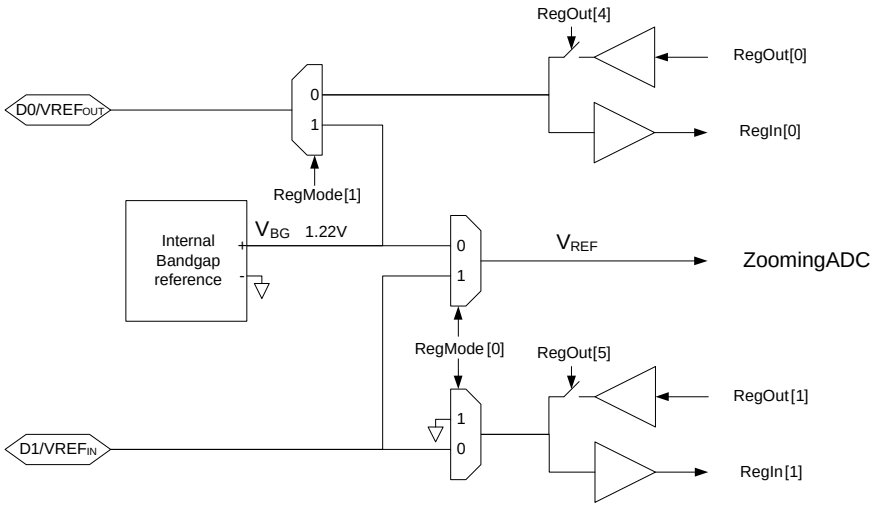


Figure 5. GPIO bloc diagram

The direction of each bit within the *GPIO* block (input only or input/output) can be individually set using the bits of the **RegOut** (address 0x40) register. If *D[x]Dir* = 1, both the input and output buffer are active on the corresponding *GPIO* block pin. If *D[x]Dir*= 0, the corresponding *GPIO* block pin is an input only and the output buffer is in high impedance. After power on reset the GPIO block pins are in input/output mode (*D[x]Dir* are reset to 1).

The input values of *GPIO* block are available in **RegIn** (address 0x41) register (read only). Reading is always direct - there is no debounce function in the *GPIO* block. In case of possible noise on input signals, an external hardware filter has to be realized. The input buffer is also active when the *GPIO* block is defined as output and the effective value on the pin can be read back.

Data stored in the LSB bits of **RegOut** register are outputted at *GPIO* block if *D[x]Dir= 1*. The default values after power on reset is low (0).
The digital pins are able to deliver a driving current up to 8 mA.

When the bits *VrefD0Out* and *VrefD1In* in the **RegMode** (address 0x70) register are set to 1 the *D0* and *D1* pins digital behavior are automatically bypassed in order to either input or output the voltage reference signals.

6.3.1 Optional Operating Mode: External Vref

D0 and *D1* are multi-functional pins with the following functions in different operating modes (see **RegMode** register for control settings):

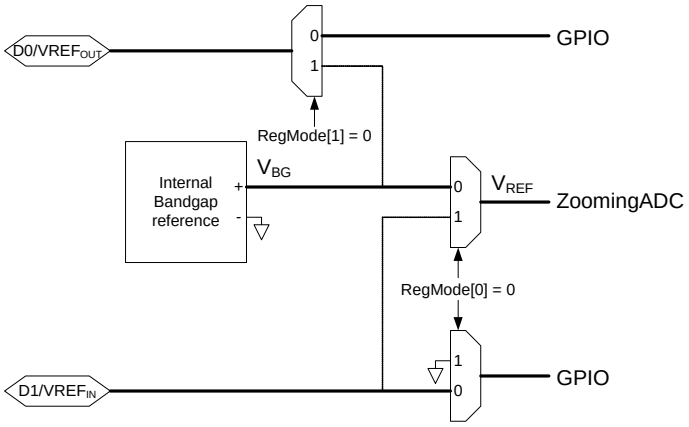


Figure 7. D0 and D1 are Digital Inputs / Outputs

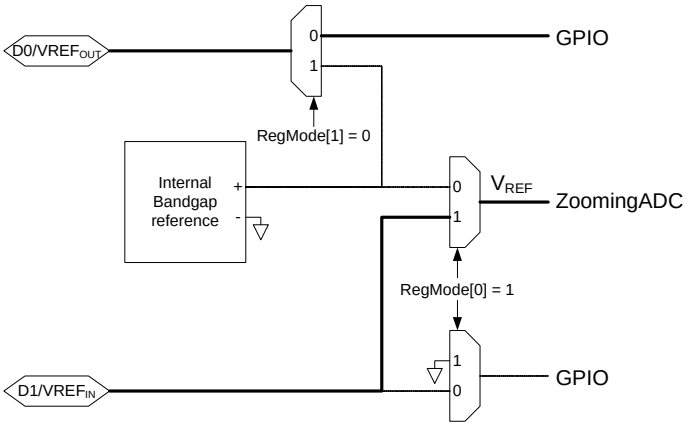


Figure 8. D1 is Reference Voltage Input and D0 is Digital Input / Output

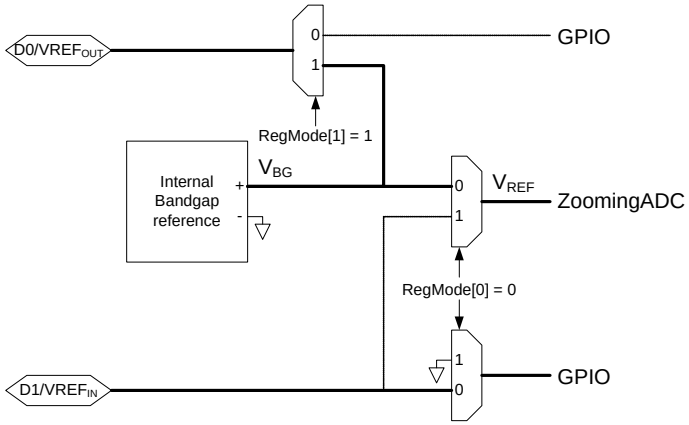


Figure 9. D1 is Digital Input / Output and D0 Reference Voltage Output

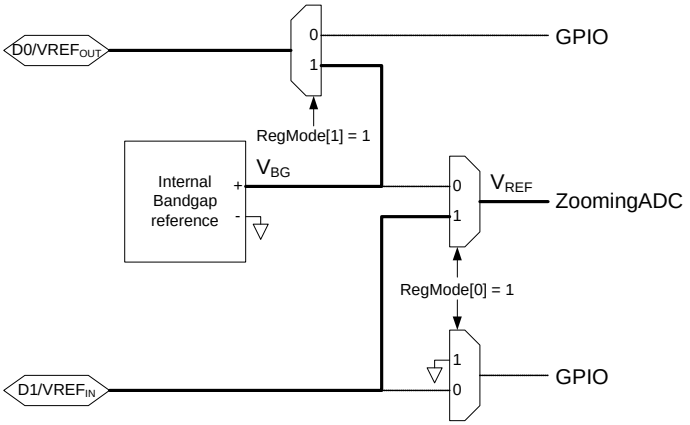


Figure 10. D0 is Reference Voltage Output and D1 is Reference Voltage Input

This allows external monitoring of the internal bandgap reference or the ability to use an external reference input for the *ADC*, or the option to filter the internal V_{REF} output before feeding back as $V_{REF,ADC}$ input. The internally generated V_{REF} is a trimmed as ADC reference with a nominal value of 1.22V. When using an external $V_{REF,ADC}$ input, it may have any value between 0V and V_{BATT}. Simply substitute the external value for 1.22 V in the *ADC* conversion calculations.

6.4 Charge Pump

This block generates a supply voltage able to power the analog switch drive levels on the chip higher than VBATT if necessary.

If *VBATT* voltage drops below 3V then the block should be activated. If *VBATT* voltage is greater than 3V then *VBATT* may be switched straight through to the *VPUMP* output. If the charge pump is not activated then *VPUMP* = *VBATT*.

If control input bit *MultForceOff* = 1 in **RegMode** (address 0x70)register then the charge pump is disabled and *VBATT* is permanently connected to *VPUMP* output.

If control input bit *MultForceOn* = 1 in **RegMode** register then the charge pump is permanently enabled. This overrides *MultForceOff* bit in **RegMode** register.

An external capacitor is required on *VPUMP* pin. This capacitor should be large enough to ensure that generated voltage is smooth enough to avoid affecting conversion accuracy but not so large that it gives an unacceptable settling time. A recommended value is around 2.2nF.

6.5 RC Oscillator

This block provides the master clock reference for the chip. It produces a clock at 4 MHz which is divided internally in order to generate the clock sources needed by the other blocks.

The oscillator technique is a low power relaxation design and it is designed to vary as little as possible over temperature and supply voltage.

This oscillator is trimmed at manufacture chip test.

The *RC* oscillator will start up after a chip reset to allow the trimming values to be read and calibration registers. Once this has been done, the oscillator will be shut down and the chip will enter a sleep state while waiting for a SPI communication.

The worst case duration from reset (or POR) to the sleep state is 800us.

6.5.1 Wake-up from sleep

When the device is in sleep state, the *RC* oscillator will start up after a communication. The start up sequence for the *RC* oscillator is 450us in worst case.
During this time, the internal blocs using the RC can not be used: no ADC conversion can be started.

7 ZoomingADC

7.1 Overview

The *ZoomingADC* is a complete and versatile low-power analog front-end interface typically intended for sensing applications. In the following text the *ZoomingADC* will be referred as *ZADC*.

The key features of the *ZADC* are:

- Programmable 6 to 16-bit dynamic range over-sampled *ADC*
- Flexible gain programming between 1/12 and 1000
- Flexible and large range offset compensation
- Differential or single-ended input
- 2-channel differential reference inputs
- Power saving modes

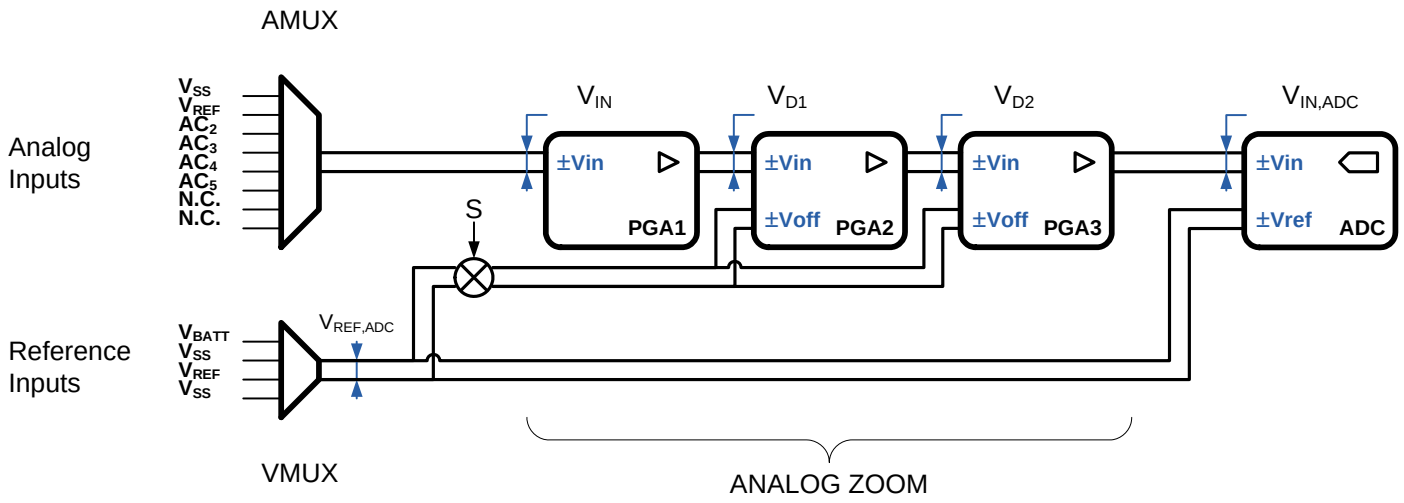


Figure 11. ZADC General Functional Block Diagram

The total acquisition chain consists of an input multiplexer, 3 programmable gain amplifier stages and an over sampled A/D converter. The reference voltage can be selected on two different channels. Two offset compensation amplifiers allow for a wide offset compensation range. The programmable gain and offset allow the application to zoom in on a small portion of the reference voltage defined input range.

7.1.1 Acquisition Chain

Figure 11, page 17 shows the general block diagram of the acquisition chain (*AC*). A control block (not shown in **Figure 11**) manages all communications with the SPI peripheral. The clocking is derived from the internal 4 MHz Oscillator.

Analog inputs can be selected through an 8 input multiplexer, while reference input is selected between two differential channels. It should however be noted that only 7 acquisition channels (including the VREF) are available when configured as single ended since the input amplifier is always operating in differential mode with both positive and negative input selected through the multiplexer.

The core of the zooming section is made of three differential programmable amplifiers (*PGA*). After selection of an input and reference signals VIN and VREF,ADC combination, the input voltage is modulated and amplified through stages 1 to 3. Fine gain programming up to 1'000 V/V is possible. In addition, the last two stages provide programmable offset. Each amplifier can be bypassed if needed.

The output of the cascade of *PGA* is directly fed to the analog-to-digital converter (*ADC*), which converts the signal VIN,ADC into digital.

Like most *ADCs* intended for instrumentation or sensing applications, the ZoomingADC™ is an over-sampled converter [1]. The *ADC* is a so-called incremental converter; with bipolar operation (the *ADC* accepts both positive and negative differential input voltages). In first approximation, the *ADC* output result relative to full-scale (*FS*) delivers the quantity:

$$\frac{OUT_{ADC}}{FS/2} \cong \frac{V_{IN,ADC}}{V_{REF}/2}$$

Equation 1

in two's complement (see **Equation 18** and **Equation 19, page 30** for details). The output code OUTADC is -*FS* / 2 to + *FS* / 2 for VIN,ADC = -VREF,ADC / 2 to + VREF,ADC / 2 respectively. As will be shown, VIN,ADC is related to input voltage VIN by the relationship:

$$V_{IN,ADC} = GD_{TOT} \cdot V_{IN} - GDoff_{TOT} \cdot S \cdot V_{REF} \quad [V]$$

Equation 2

where *GDTOT* is the total *PGA* gain, *GDOFFTOT* is the total magnitude of *PGA* offset and S is the sign of the offset (see **Table 8, page 21**).

7.1.2 Programmable Gain Amplifiers

As seen in **Figure 11, page 17**, the zooming function is implemented with three programmable gain amplifiers (*PGA*). These are:

- *PGA1*: coarse gain tuning
- *PGA2*: medium gain and offset tuning
- *PGA3*: fine gain and offset tuning. Should be set ON for high linearity data acquisition

All gain and offset settings are realized with ratios of capacitors. The user has control over each *PGA* activation and gain, as well as the offset of stages 2 and 3. These functions are examined hereafter.

1. Over-sampled converters are operated with a sampling frequency *fs* much higher than the input signal's Nyquist rate (typically *fs* is 20-1'000 times the input signal bandwidth). The sampling frequency to throughput ratio is large (typically 10-500). These converters include digital decimation filtering. They are mainly used for high resolution, and/or low-to-medium speed applications.

7.1.3 PGA & ADC Enabling

Depending on the application objectives, the user may enable or bypass each *PGA* stage. This is done according to the word *Enable* and the coding given in **Table 6**. To reduce power dissipation, the *ADC* can also be inactivated while idle.

Table 6. ADC and PGA Enabling

Enable (RegACCfg1[3:0])	Block
XXX0 XXX1	ADC disabled ADC enabled
XX0X XX1X	PGA1 disabled PGA1 enabled
X0XX X1XX	PGA2 disabled PGA2 enabled
0XXX 1XXX	PGA3 disabled PGA3 enabled

7.2 ZoomingADC Registers

The system has a bank of eight 8-bit registers: six registers are used to configure the acquisition chain (**RegAcCfg0** to **RegAcCfg5**), and two registers are used to store the output code of the analog-to-digital conversion (**RegAcOutMsb** & **Lsb**).

Table 7. Registers to Configure the Acquisition Chain (AC) and to Store the Analog-to-Digital Conversion (ADC) Result

Register Name	Bit position							
	7	6	5	4	3	2	1	0
RegACOutLsb	*Out*[7:0] **Note 1**							
RegACOutMsb	*Out*[15:8]							
RegACCfg0 Default values:	*Start* 0, **Note 2**	*SetNelconv* 01, **Note 3**		*SetOsr* 010, **Note 4**			*Continuous* 0, **Note 5**	*SampleShiftEn* 0, **Note 6**
RegACCfg1 Default value:	*IbAmpAdc* 11, **Note 7**		*IbAmpPga* 11, **Note 8**		*Enable* 0000, **Note 9**			
RegACCfg2 Default value:	*SetFs* 00, **Note 10**		*Pga2Gain* 00, **Note 12**		Pga2Offset 0000, **Note 14**			
RegACCfg3 Default value:	*Pga1Gain* 0, **Note 11**	*Pga3Gain* 0001100, **Note 13**						
RegACCfg4 Default value:	*DataReadyEn* 0, **Note 15**	*Pga3Offset* 0000000, **Note 16**						
RegACCfg5 Default value:	*Busy* 0, **Note 17**	*Def* 0, **Note 18**	*Amux* 00000, **Note 19**					*Vmux* 0, **Note 20**

(r = read; w = write; rw = read & write)

(1) **Out**: (r) digital output code of the analog-to-digital converter. (*MSB = Out[15]*)
(2) **Start**: (w) setting this bit triggers a single conversion (after the current one is finished). This bit always reads back 0.

(3) **SetNelconv**: (rw) sets the number of elementary conversions to $2^{(SetNelconv[1:0])}$. To compensate for offsets, the input signal is chopped between elementary conversions (1,2,4,8).
(4) **SetOsr**: (rw) sets the over-sampling rate (*OSR*) of an elementary conversion to $2^{(3+SetOsr[2:0])}$. *OSR* = 8, 16, 32, ..., 512, 1024.
(5) **Continuous**: (rw) setting this bit starts a conversion. When this bis is 1, A new conversion will automatically begin directly when the previous one is finished.
(6) **SampleShiftEn**: (rw) the 16-bit samples can be directly shifted out though the SPI interface by the master when a conversion is done.
(7) **IbAmpAdc**: (rw) sets the bias current in the *ADC* to 0.25 x (1+ *IbAmpAdc[1:0]*) of the normal operation current (25, 50, 75 or 100% of nominal current). To be used for low-power, low-speed operation.
(8) **IbAmpPga**: (rw) sets the bias current in the PGAs to 0.25 x (1+*IbAmpPga[1:0]*) of the normal operation current (25, 50, 75 or 100% of nominal current). To be used for low-power, low-speed operation.
(9) **Enable**: (rw) enables the *ADC* modulator (bit 0) and the different stages of the *PGAs* (*PGAi* by bit i=1,2,3). *PGA* stages that are disabled are bypassed.
(10) **SetFs**: (rw) These bits set the over sampling frequency of the acquisition chain. Expressed as a fraction of the oscillator frequency, the sampling frequency is given as: 11 ' 500 kHz, 10 ' 250 kHz, 01 ' 125 kHz, 00 ' 62.5 kHz.
(11) **Pga1Gain**: (rw) sets the gain of the first stage: 0 ' 1, 1 ' 10.
(12) **Pga2Gain**: (rw) sets the gain of the second stage: 00 ' 1, 01 ' 2, 10 ' 5, 11 ' 10.
(13) **Pga3Gain**: (rw) sets the gain of the third stage to *Pga3Gain[6:0]* 1/12.
(14) **Pga2Offset**: (rw) sets the offset of the second stage between -1 and +1, with increments of 0.2. The *MSB* gives the sign (0 positive, 1 negative); amplitude is coded with the bits *Pga2Offset[5:0]*.
(15) **DataReadyEn**: (rw) enables the combined data ready mode with the MISO of the SPI interface.
(16) **Pga3Offset**: (rw) sets the offset of the third stage between -5.25 and +5.25, with increments of 1/12. The *MSB* gives the sign (0 positive, 1 negative); amplitude is coded with the bits *Pga3Offset[5:0]*.
(17) **Busy**: (r) set to 1 if a conversion is running.
(18) **Def**: (w) sets all values to their defaults (PGA disabled, *AMux* not changed, *VMux* not changed, *ADC* enabled, nominal modulator bias current (100%), 2 elementary conversions, *OSR* = 32, N_{ELCONV} = 2, *fs* = 62.5kHz) and starts a new conversion without waiting the end of the preceding one.
(19) **Amux**(4:0): (rw) *Amux[4]* sets the mode (0 ' differential inputs, 1 ' single ended inputs with A0= common reference) *Amux[3]* sets the sign (0 ' straight, 1' cross) *Amux[2:0]* sets the channel.
(20) **Vmux**: (rw) sets the differential reference channel (0 ' V_{BATT}, 1 ' V_{REF}).

7.3 Input Multiplexers (AMUX and VMUX)

The ZoomingADC has analog inputs *AC0* to *AC5* and reference inputs. Let us first define the differential input voltage V_{IN} and reference voltage $V_{REF,ADC}$ respectively as:

$$V_{IN} = V_{INP} - V_{INN} \quad [V]$$

Equation 3

$$V_{REF} = V_{REFP} - V_{REFN} \quad [V]$$

Equation 4

As shown in **Table 8**, the inputs can be configured in two ways: either as 4 differential channels (*VIN1= AC1 - AC0,... , VIN3 = AC5 - AC4*), or *AC0* can be used as a common reference, providing 7 signal paths all referred to *AC0*. The control word for the analog input selection is *Amux*. Notice that the *Amux* bit 4 controls the sign of the input voltage.

Table 8. Analog Input Selection

Amux (RegACCfg5[5:1])	VINP	VINN	Amux (RegACCfg5[5:1])	VINP	VINN
Sign S = 1			**Sign S = -1**		
00x00	AC1(VREF)	AC0(VSS)	01x00	AC1(VSS)	AC0(VREF)
00x01	AC3	AC2	01x01	AC2	AC3
00x10	AC5	AC4	01x10	AC4	AC5
00x11	N.C.	N.C.	01x11	N.C.	N.C.
10000	AC0(VSS)	AC0(VSS)	11000	AC0(VSS)	AC0(VSS)
10001	AC1(VREF)		11001		AC1(VREF)
10010	AC2		11010		AC2
10011	AC3		11011		AC3
10100	AC4		11100		AC4
10101	AC5		11101		AC5
10110	N.C.		11110		N.C.
10111	N.C.		11111		N.C.

Similarly, the reference voltage is chosen among two differential channels (*VREF = VBATT-VSS*, *VREF = VBG-VSS* or *VREF = VREF,IN-VSS*) as shown in **Table 9**. The selection bit is *Vmux*. The reference inputs *VREFP* and *VREFN* (common-mode) can be up to the power supply range.

Table 9. Analog reference Input Selection

Vmux (RegACCfg5[0])	VREFP	VREFN
0	VREF = VBATT	VSS
1	VREF = VBG or VREF,IN[1]	VSS

1. External voltage reference on D1 GPIO pin. See **section 6.3 on page 13** about GPIO and "RegMode[0x70]" on page 47.

7.4 First Stage Programmable Gain Amplifier (PGA1)

The first stage can have a buffer function (unity gain) or provide a gain of 10 (see **Table 10**). The voltage *VD1* at the output of *PGA1* is:

$$V_{D1} = GD_1 \cdot V_{IN} \quad [V]$$

Equation 5

where *GD1* is the gain of *PGA1* (in V/V) controlled with the *Pga1Gain* bit.

Table 10. PGA1 gain settings

Pga1Gain bit (RegACCfg3[7])	PGA1 gain [V/V] *GD1* [V/V]
0	1
1	10

7.5 Second Stage Programmable Gain Amplifier (PGA2)

The second *PGA* has a finer gain and offset tuning capability, as shown in **Table 11**. The *VD2* voltage at the output of *PGA2* is given by:

$$V_{D2} = GD_2 \cdot V_{D1} - GDoff_2 \cdot S \cdot V_{REF} \quad [V]$$

Equation 6

where *GD2* and *GDOFF2* are respectively the gain and offset of *PGA2* (in V/V). These are controlled with the words *Pga2Gain[1:0]* and *Pga2Offset[3:0]*.

Table 11. PGA2 gain and offset settings

Pga2Gain bit field (RegACCfg2[5:4])	PGA2 gain [V/V] *GD2* [V/V]
00	1
01	2
10	5
11	10

Pga2Offset bit field (RegACCfg2[3:0])	PGA2 offset *GDOFF2* [V/V]
0000	0
0001	+0.2
0010	+0.4
0011	+0.6
0100	+0.8
0101	+1
1000	0
1001	-0.2
1010	-0.4
1011	-0.6
1100	-0.8
1101	-1.0

7.6 Third Stage Programmable Gain Amplifier (PGA3)

The finest gain and offset tuning is performed with the third and last *PGA* stage, according to the coding of **Table 12**.

Table 12. PGA3 Gain and Offset Settings

Pga3Gain bit field (RegACCfg3[6:0])	PGA3 Gain *GD3* [V/V]
0000000	0
0000001	1/12 (=0.083)

Pga3Offset bit field (RegACCfg4[6:0])	PGA3 Offset *GDOFF3* [V/V]
0000000	0
0000001	+1/12 (=0.083)

Table 12. PGA3 Gain and Offset Settings

Pga3Gain bit field (RegACCfg3[6:0])	PGA3 Gain *GD3* [V/V]
...	...
0000110	6/12
...	...
0001100	12/12
0010000	16/12
...	...
0100000	32/12
...	...
1000000	64/12
...	...
1111111	127/12 (=10.58)

Pga3Offset bit field (RegACCfg4[6:0])	PGA3 Offset *GDOFF3* [V/V]
...	
0010000	+16/12
...	...
0100000	32/12
...	...
0111111	+63/12 (=+5.25)
1000000	0
1000001	-1/12 (=-0.083)
1000010	-2/12
...	...
1010000	-16/12
...	...
1100000	-32/12
...	...
1111111	-63/12 (=-5.25)

The output of *PGA3* is also the input of the *ADC*. Thus, similarly to *PGA2*, we find that the voltage entering the *ADC* is given by:

$$V_{IN,ADC} = GD_3 \cdot V_{D2} - GDoff_3 \cdot S \cdot V_{REF} \quad [V]$$

Equation 7

where *GD3* and *GDOFF3* are respectively the gain and offset of *PGA3* (in V/V). The control words are *Pga3Gain[6:0]* and *Pga3Offset[6:0]*.

To remain within the signal compliance of the *PGA* stages (no saturation), the condition:

$$|V_{IN}|, |V_{D1}|, |V_{D2}| < \frac{V_{BATT}}{2}$$

Equation 8

must be verified.

To remain within the signal compliance of the *ADC* (no saturation), the condition:

$$\left|V_{IN,ADC}\right| < \left(\frac{V_{REF}}{2}\right)\left(\frac{OSR-1}{OSR}\right)$$

Equation 9

must be verified.
Finally, combining **Equation 5** to **Equation 7** for the three *PGA* stages, the input voltage $V_{IN,ADC}$ of the *ADC* is related to V_{IN} by:

$$V_{IN,ADC} = GD_{TOT} \cdot V_{IN} - GDoff_{TOT} \cdot S \cdot V_{REF} \quad [V]$$

Equation 10

where the total *PGA* gain is defined as:

$$GD_{TOT} = GD_3 \cdot GD_2 \cdot GD_1$$

Equation 11

and the total *PGA* offset is:

$$GDoff_{TOT} = GDoff_3 + GD_3 \cdot GDoff_2$$

Equation 12

7.7 Analog-to-Digital Converter (ADC)

The main performance characteristics of the *ADC* (resolution, conversion time, etc.) are determined by three programmable parameters. The setting of these parameters and the resulting performances are described later.

- *fs*: Over-sampling frequency
- *OSR*: Over-Sampling Ratio
- *NELCONV*: Number of Elementary Conversions

7.7.1 Conversion Sequence

A conversion is started each time the bit *Start* or the *Def* bit is set. As depicted in **Figure 12**, a complete analog-to-digital conversion sequence is made of a set of *NELCONV* elementary incremental conversions and a final quantization step. Each elementary conversion is made of (*OSR*+1) over-sampling periods *Ts*=1/*fs*, i.e.:

$$T_{ELCONV} = (OSR+1)/\ f_S \quad [s]$$

Equation 13

The result is the mean of the elementary conversion results. An important feature is that the elementary conversions are alternatively performed with the offset of the internal amplifiers contributing in one direction and the other to the output code. Thus, converter internal offset is eliminated if at least two elementary sequences are performed (i.e. if *NELCONV* >= 2). A few additional clock cycles are also required to initiate and end the conversion properly.

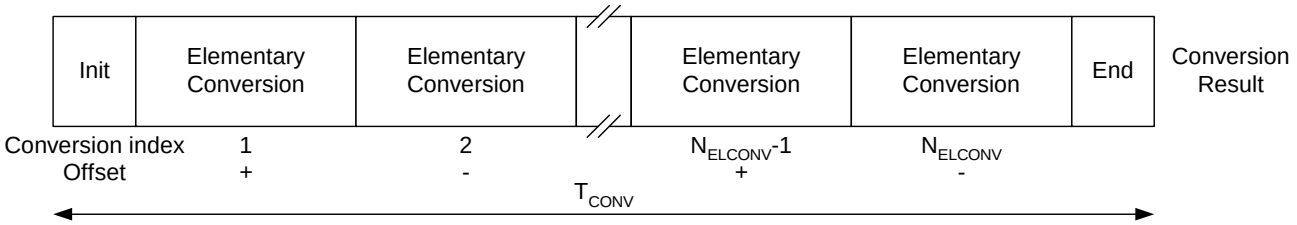


Figure 12. Analog-to-Digital Conversion Sequence

Note	The internal bandgap reference state may be forced High or Low, or may be set to toggle during conversion at either the same rate or half the rate of the Elementary Conversion. This may be useful to help eliminate bandgap related internal offset voltage and 1/*fs* noise.

7.7.2 Over-Sampling Frequency (fs)

The word *SetFs[1:0]* (see **Table 13**) is used to select the over-sampling frequency *fs*. The over-sampling frequency is derived from the 4MHz oscillator clock.

Table 13. Sampling frequency settings

SetFs bit field (RegACCfg2[7:6])	Over-Sampling Frequency fs [Hz]
00	62.5 kHz
01	125 kHz
10	250 kHz
11	500 kHz

7.7.3 Over-Sampling Ratio (OSR)

The over-sampling ratio (*OSR*) defines the number of integration cycles per elementary conversion. Its value is set with the word *SetOsr[2:0]* in power of 2 steps (see **Table 14**) given by:

$$OSR = 2^{3+\text{SetOsr}[2:0]} \quad [-]$$

Equation 14

Table 14. Over-sampling ratio settings

SetOsr[2:0] (RegACCfg[4:2])	Over-Sampling Ratio OSR [-]
000	8
001	16
010	32
011	64
100	128
101	256
110	512
111	1024

7.7.4 Number of Elementary Conversions (Nelconv)

As mentioned previously, the whole conversion sequence is made of a set of *NELCONV* elementary incremental conversions. This number is set with the word *SetNelconv[1:0]* in power of 2 steps (see **Table 15**) given by:

$$N_{ELCONV} = 2^{\text{SetNelconv}[1:0]} \quad [-]$$

Equation 15

Table 15. Number of elementary conversion

SetOsr[2:0] (RegACCfg[4:2])	# of Elementary Conversion NELCONV [-]
00	1
01	2
10	4
11	8

As already mentioned, *NELCONV* must be equal or greater than 2 to reduce internal amplifier offsets.

7.7.5 Resolution

The theoretical resolution of the *ADC*, without considering thermal noise, is given by:

$$n = 2 \cdot \log_2(OSR) + \log_2(N_{ELCONV}) \quad [bit]$$

Equation 16

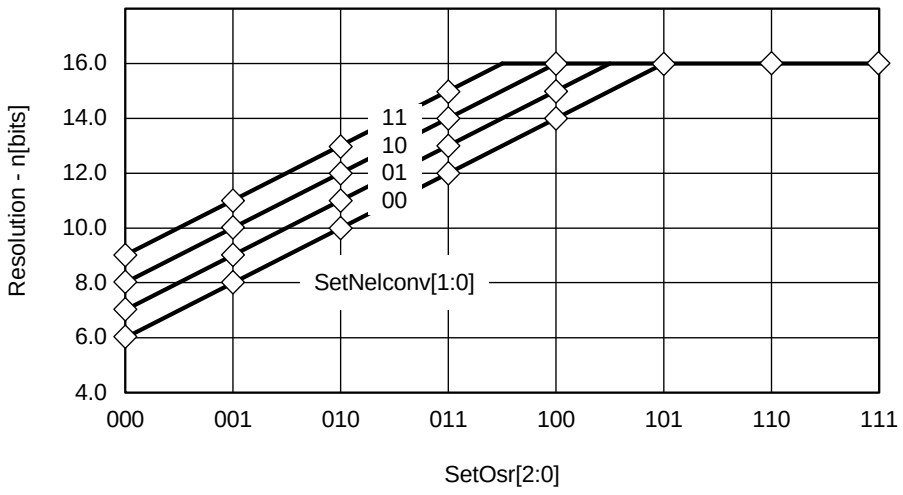


Figure 13. Resolution vs. SetOsr[2:0] and SetNelconv[2:0]

Using look-up **Table 16** or the graph plotted in **Figure 13**, resolution can be set between 6 and 16 bits. Notice that, because of 16-bit register use for the *ADC* output, **practical resolution is limited to 16 bits**, i.e. n = 16. Even if the

resolution is truncated to 16 bit by the output register size, it may make sense to set *OSR* and N_{ELCONV} to higher values in order to reduce the influence of the thermal noise in the PGA.

Table 16. Resolution[1] vs. SetOsr and SetNelconv settings

SetOsr control bits	SetNelconv control bits			
	'00'	**'01'**	**'10'**	**'11'**
'000'	6	7	8	9
'001'	8	9	10	11
'010'	10	11	12	13
'011'	12	13	14	15
'100'	14	15	16	16
'101'	16	16	16	16
'110'	16	16	16	16
'111'	16	16	16	16

1. In shaded area, the resolution is truncated to 16 bits due to output register size **RegACOut[15:0]**

7.7.6 Conversion Time & Throughput

As explained in **Figure 13**, conversion time is given by:

$$T_{CONV} = (N_{ELCONV} \cdot (OSR+1)+1) / f_S \quad [s]$$

Equation 17

and throughput is then simply $1/T_{CONV}$. For example, consider an over-sampling ratio of 256, 2 elementary conversions, and a sampling frequency of 500 kHz (*SetOsr* = "101", *SetNelconv* = "01" and *SetFs* = "00"). In this case, using **Table 17**, the conversion time is 515 sampling periods, or 1.03ms. This corresponds to a throughput of 971Hz in continuous-time mode. The plot of **Figure 14** illustrates the classic trade-off between resolution and conversion time.

Table 17. Normalized conversion time (Tconv x fs) vs. SetOsr and SetNelconv settings[1]

SetOsr bits OSR	SetNelconv control bits NELCONV			
	'00' 1	**'01' 2**	**'10' 4**	**'11' 8**
'000'	10	19	37	73
'001'	18	35	69	137
'010'	34	67	133	265
'011'	66	131	261	521

Table 17. Normalized conversion time (Tconv x fs) vs. SetOsr and SetNelconv settings[1]

SetOsr bits OSR	SetNelconv control bits NELCONV			
	'00' 1	'01' 2	'10' 4	'11' 8
'100'	130	259	517	1033
'101'	258	515	1029	2057
'110'	514	1027	2053	4105
'111'	1026	2051	4101	8201

1. *Normalized to sampling period 1/fs*

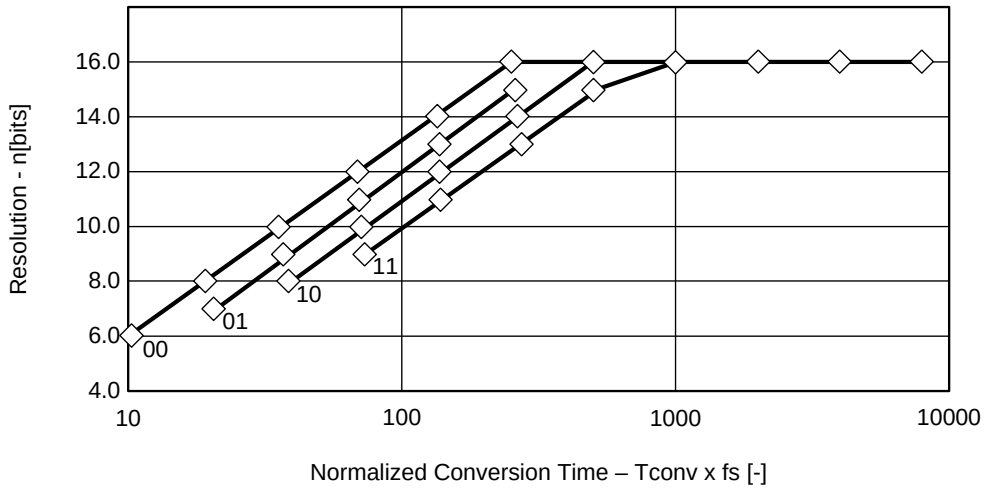


Figure 14. Resolution vs. normalized[1] conversion time for different SetNelconv[1:0]

1. Normalized Conversion Time - TCONV x fs

7.7.7 Continuous-Time vs. On-Request Conversion

The *ADC* can be operated in two distinct modes: "continuous-time" and "on-request" modes (selected using the bit *Continuous*).

In "continuous-time" mode, the input signal is repeatedly converted into digital. After a conversion is finished, a new one is automatically initiated. The new value is then written in the result register, and the corresponding internal trigger pulse is generated. This operation is sketched in **Figure 15**. The conversion time in this case is defined as *TCONV*.

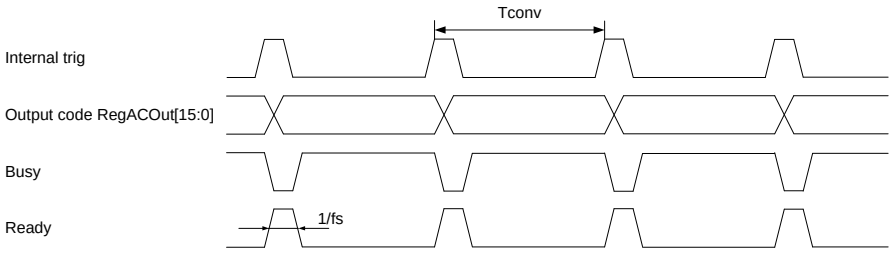


Figure 15. ADC "Continuous-Time" Operation

In the "on-request" mode, the internal behavior of the converter is the same as in the "continuous-time" mode, but the conversion is initiated on user request (with the *Start* bit). As shown in **Figure 16**, the conversion time is also *TCONV*.

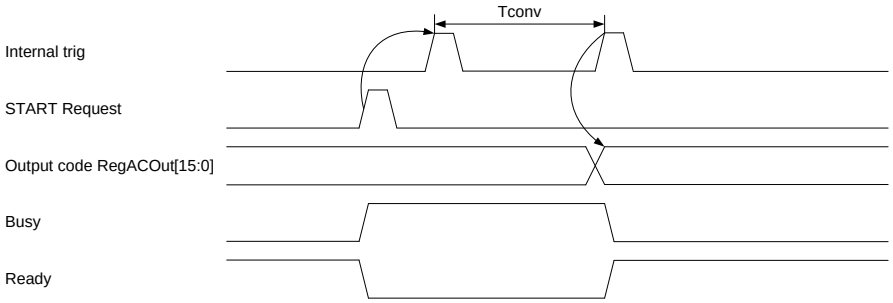


Figure 16. ADC "On-Request" Operation

7.7.8 Output Code Format

The *ADC* output code is a 16-bit word in two's complement format (see **Table 18**). For input voltages outside the range, the output code is saturated to the closest full-scale value (i.e. 0x7FFF or 0x8000). For resolutions smaller than 16 bits, the non-significant bits are forced to the values shown in **Table 19**. The output code, expressed in *LSBs*, corresponds to:

$$OUT_{ADC} = 2^{16} \cdot \frac{V_{IN,ADC}}{V_{REF}} \cdot \frac{OSR+1}{OSR}$$

Equation 18

Recalling **Equation 10, page 24**, this can be rewritten as:

$$OUT_{ADC} = 2^{16} \cdot \frac{V_{IN}}{V_{REF}} \cdot \left(GD_{TOT} - GDoff_{TOT} \cdot S \cdot \frac{V_{REF}}{V_{IN}} \right) \cdot \frac{OSR+1}{OSR} \quad [LSB]$$

Equation 19

where, from **Equation 11** and **Equation 12**, the total *PGA* gain and offset are respectively:

$$GD_{TOT} = GD_3 \cdot GD_2 \cdot GD_1$$

Equation 20

and:

$$GDoff_{TOT} = GDoff_3 + GD_3 \cdot GDoff_2$$

Equation 21

Table 18. Basic ADC Relationships (example for: VREF = 5V, OSR = 512, n = 16bits)

ADC Input Voltage $V_{IN,ADC}$	% of Full Scale (FS)	Output in LSBs	Hexadecimal Output Code
+2.49505 V	+0.5 x FS	$+2^{15}-1 = 32'767$	7FFF
+2.49497 V	...	$+2^{15}-2 = 32'766$	7FFE
...	...	...	...
+76.145 µV	...	+1	0001
0	0	0	0000
-76.145 µV	...	-1	FFFF
...	...	...	...
-2.49505 V	...	$-2^{15}-1 = -32'767$	8001
-2.49513 V	-0.5 x FS	$-2^{15} = -32'768$	8000

Table 19. Last forced LSBs in conversion output register for resolution settings smaller than 16bits[1]

SetOsr[2:0]	SetNelconv = '00'	SetNelconv = '01'	SetNelconv = '10'	SetNelconv = '11'
'000'	1000000000	100000000	10000000	1000000
'001'	10000000	1000000	100000	10000
'010'	100000	10000	1000	100
'011'	1000	100	10	1
'100'	10	1	-	-
'101'	-	-	-	-
'110'	-	-	-	-
'111'	-	-	-	-

1. (n<16) (RegACOutMsb[7:0] & RegACOutLsb[7:0])

The equivalent *LSB* size at the input of the *PGA* chain is:

$$LSB = \frac{1}{2^n} \cdot \frac{V_{REF}}{GD_{TOT}} \cdot \frac{OSR}{OSR+1} \quad [V/V]$$

Equation 22

Notice that the input voltage $V_{IN,ADC}$ of the *ADC* must satisfy the condition:

$$\left|V_{IN,ADC}\right| \le \frac{1}{2} \cdot (V_{REFP} - V_{REFN}) \cdot \frac{OSR}{OSR+1}$$

Equation 23

to remain within the *ADC* input range.

7.7.9 Power Saving Modes

During low-speed operation, the bias current in the *PGAs* and *ADC* can be programmed to save power using the control words *IbAmpPga[1:0]* and *IbAmpAdc[1:0]* (see **Table 20**). If the system is idle, the *PGAs* and *ADC* can even be disabled, thus, reducing power consumption to its minimum. This can considerably improve battery lifetime.

Table 20. ADC & PGA power saving modes and maximum sampling frequency

IbAmpAdc [1:0]	IbAmpPga [1:0]	ADC Bias Current	PGA Bias Current	Max. fs [kHz]
00		1/4 x I_{ADC}		125
01		1/2 x I_{ADC}		250
11		I_{ADC}		500
	00		1/4 x I_{PGA}	125
	01		1/2 x I_{PGA}	250
	11		I_{PGA}	500

8 Application hints

8.1 Power Reduction

The ZoomingADC is particularly well suited for low-power applications. When very low power consumption is of primary concern, such as in battery operated systems, several parameters can be used to reduce power consumption as follows:

- Operate the acquisition chain with a reduced supply voltage V_{BATT}.
- Disable the *PGAs* which are not used during analog-to-digital conversion with *Enable[3:0]*.
- Disable all *PGAs* and the *ADC* when the system is idle and no conversion is performed.
- Use lower bias currents in the *PGAs* and the *ADC* using the control words *IbAmpPga[1:0]* and *IbAmpAdc[1:0]*.
- Reduce sampling frequency.

Finally, remember that power reduction is typically traded off with reduced linearity, larger noise and slower maximum sampling speed.

8.2 Gain Configuration Flow

The diagram below shows the flow to set the gain of your configuration:

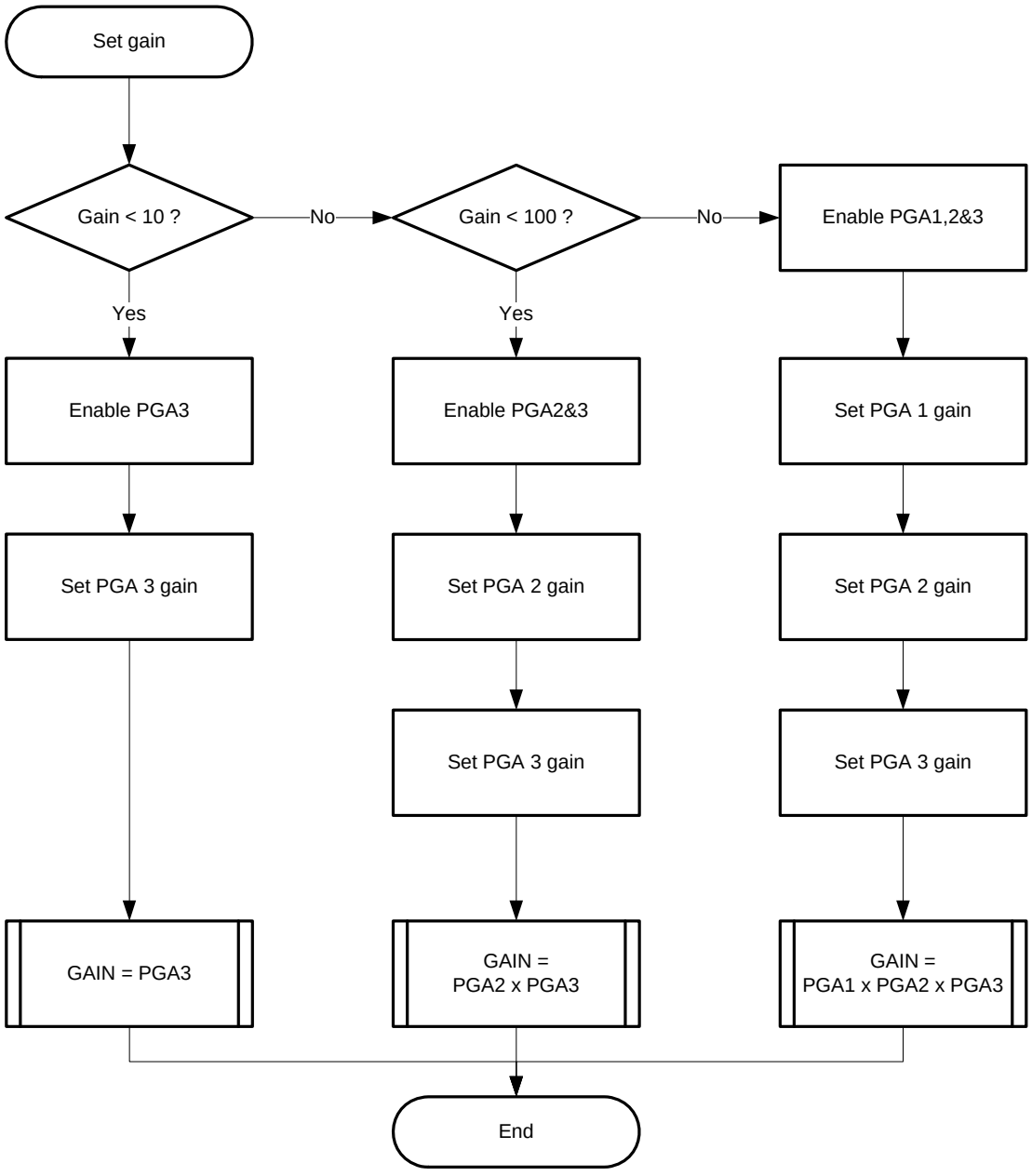


Figure 17. Gain configuration flowchart

9 SPI interface

9.1 Overview

The SX8723S serial port interface implements the following:

- 4-pin Interface + options for synchronization to ADC sample ready
- 7-bit Target Address (max 128 registers)
- 2 Mbps serial clock
- MSB first

The serial interface is a slave port for communication with a serial microprocessor bus, allowing the SX8723S to be controlled by an external processor. The serial interface header must be connected to the host processor, which acts as the master.

The serial interface signals are:

- *SCLK*: **S**erial **Cl**oc**k**
- $\overline{SS}$: Active low **S**lave **S**elect
- *MISO*/$\overline{READY}$: **M**aster **I**nput, **S**lave **O**utput (data out) and optional active low ADC data **Ready** signal.
- *MOSI*: **M**aster **O**utput, **S**lave **I**nput.

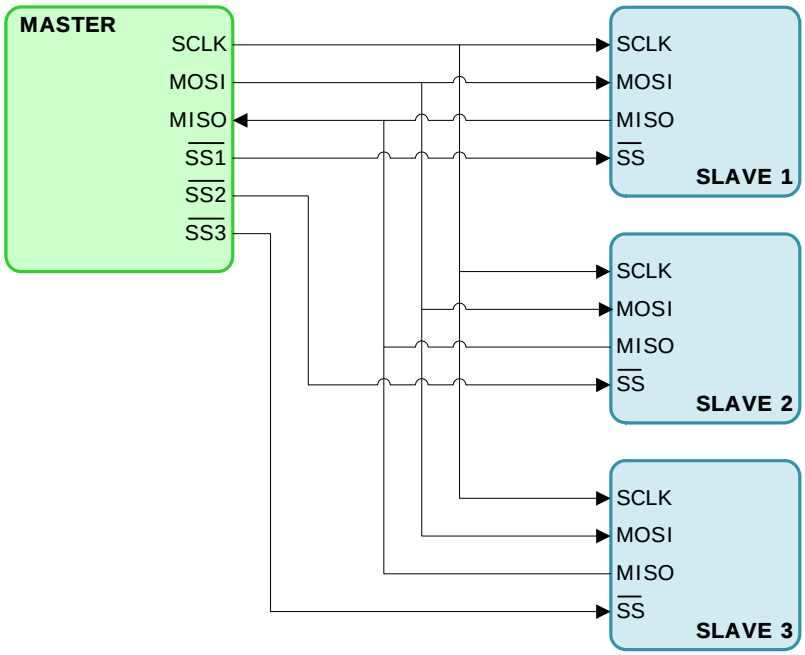


Figure 18. Example of SPI bus with 1 master and 3 slaves

The address and data are transmitted and received MSB first. Valid read/write accesses are possible only when $\overline{SS}$ is active. *MISO* and *MOSI* lines are push-pull pads. As the waveforms illustrate (see below), the slave interface implements a 16-bit shift register. The SPI implemented on the SX8723S is set to the common setting CPOL=0 and CPHA=0 which means data are sampled on the rising edge of the clock, and shifted on the falling one.
The first bit in the serial data is the Direction Bit. This must be set to '1' for reading, and '0' for writing. The following 7 bits represent the target register address, shifted in MSB first. The next byte represents register data, shifted in/out MSB first.

9.2 Data transmission

9.2.1 Write a single register

To write to a register, the Host must provide the following:

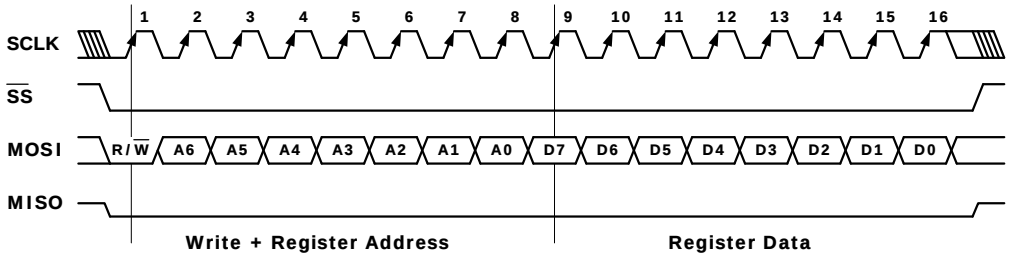


Figure 19. SPI waveform - Write a single register

9.2.2 Read a single register

To read a register from the memory map, the Host must provide the following:

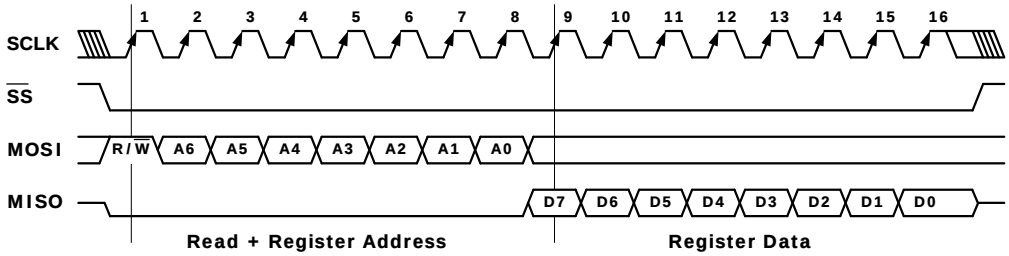


Figure 20. SPI waveform - Read a single register

9.2.3 Multiple Bytes Write/Read Protocol

The SPI protocol is designed to be able to do multiple read/write during a transaction. During one single operation, as long as Slave Select ($\overline{SS}$) stay asserted, the register address is automatically increased to allow sequential read/write (or sequential retrieval of data). The register address will be auto-incremented in multiple read/write commands. Between each different operation though the communication should be restarted.

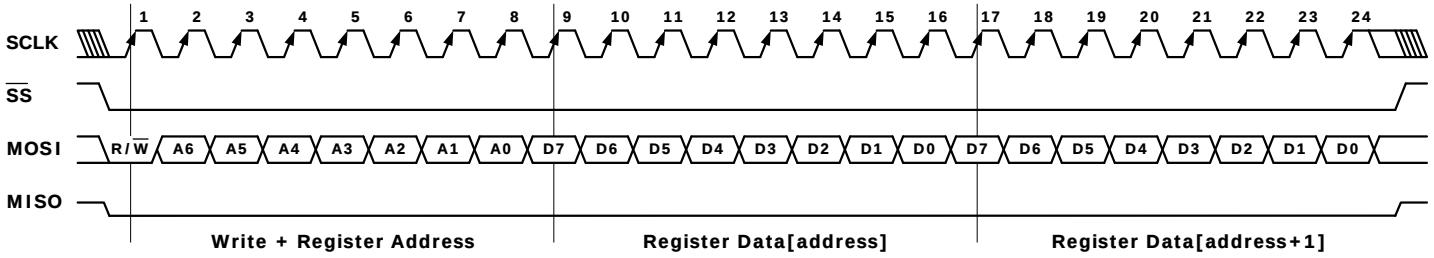


Figure 21. SPI waveform - Multiple bytes SPI Write protocol (2 bytes example)

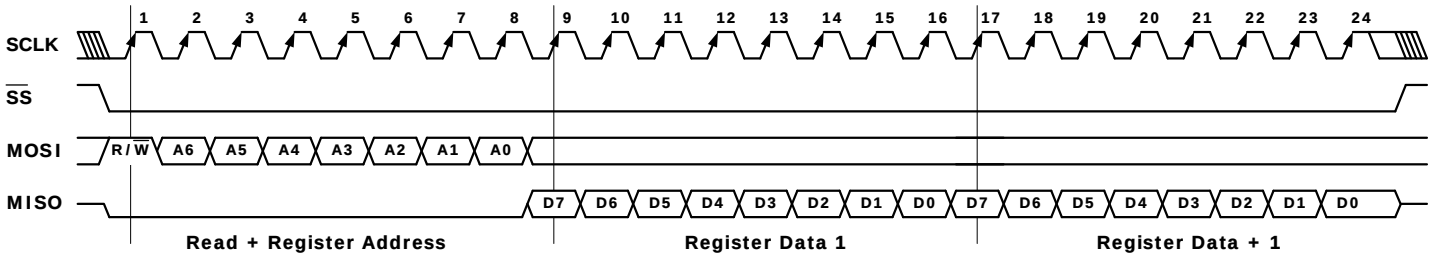


Figure 22. SPI waveform - Multiple bytes SPI Read protocol (2 bytes example)

9.3 ADC Samples Reading

- The default SPI mode the ADC samples must be read with the default SPI read sequences described in **9.2. Data transmission**.
- The SAMPLE SHIFT mode allow to read directly the 16-bit conversion result of **RegACOutLsb[0x50]** and **RegACOutMsb[0x51]** without a register read sequence. This mode is described in **9.3.1. SAMPLE SHIFT Mode**.
- The COMBINED DATA READY mode is a SAMPLE SHIFT mode which combines the ADC Ready function with the SPI MISO signal to reduce the number of wires to 4 between the master and the slave. This mode is described in **9.3.2. COMBINED DATA READY Mode** section.

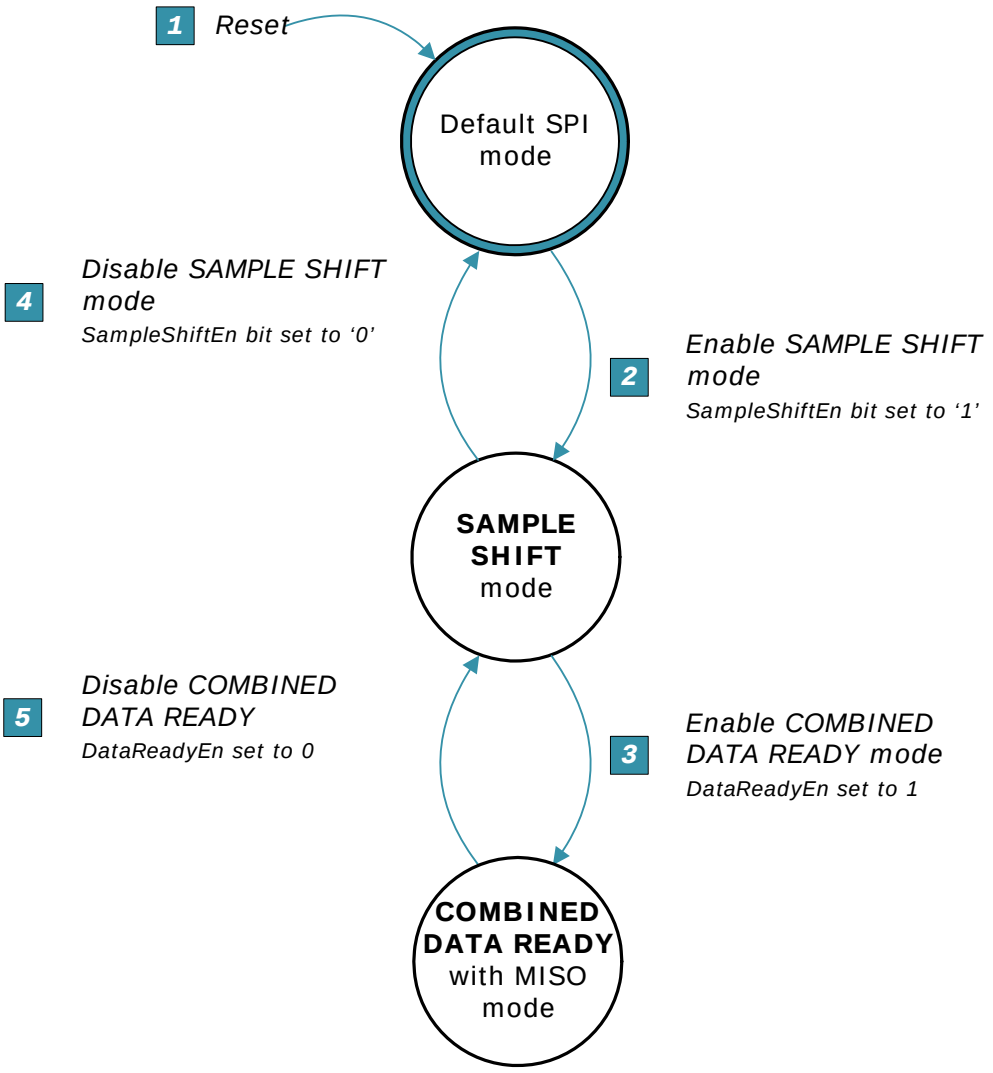


Figure 23. ADC samples reading modes with the SPI interface

When the device is in Sample Shift Mode or Combined Data Ready mode, the register reading will give erroneous data. Always disable the Sample Shift Mode and Combined Data Ready mode to read the registers.

9.3.1 SAMPLE SHIFT Mode

If the *SampleShiftEn* bit of **RegACCfg0[0x52]** is active, the MISO/$\overline{\text{READY}}$ pin is used to shift out ADC samples data. The other registers can not be read in this mode. The ADC samples are clocked out at falling edge of *SCLK*, MSB first (see **Figure 24** below).

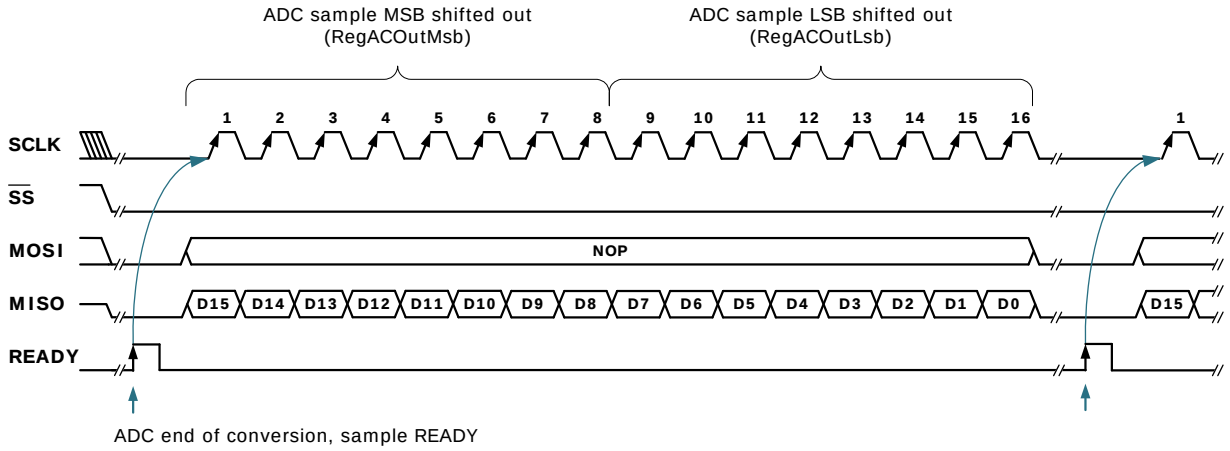


Figure 24. Data Retrieval with the SAMPLE SHIFT Mode (COMBINED DATA READY Mode Disabled)

As illustrated in **Figure 25**, five wires are necessary to connect the master in this mode if to be synchronized to the ADC end of conversion.

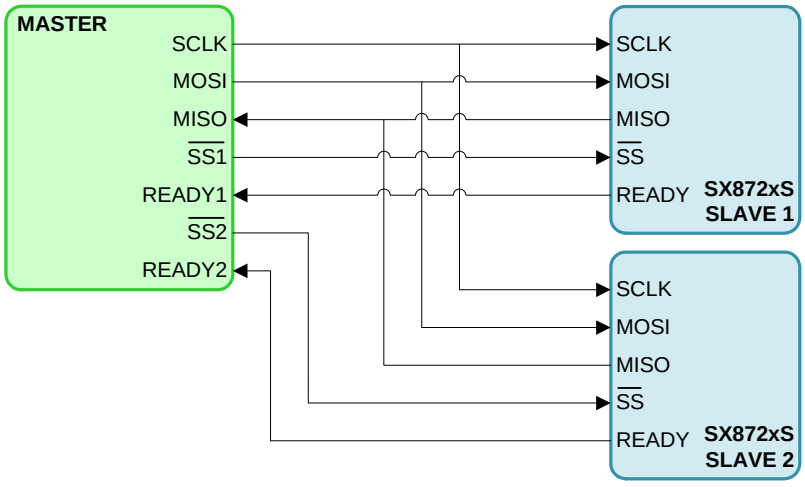


Figure 25. Example with two SX872xS slaves

When the *DataReady* bit is set to '0', this pin functions as *MISO* only. The COMBINED DATA READY mode is disabled.

9.3.2 COMBINED DATA READY Mode

This combined functionality allows for the same control as the SAMPLE SHIFT mode but with fewer pins. Samples shifted out (MISO) are combined with ADC data ready signal ($\overline{\text{READY}}$). The *DataReadyEn* bit in register

RegACCfg4[0x56] determines the function of this pin. As illustrated in **Figure 26**, four wires are necessary to connect the master in this mode if to be synchronized to the ADC end of conversion. The *DataReadyEn* bit modifies only the *MISO/READY* pin functionality. The *READY* pin functionality remains unaffected. In either mode, the *MISO*/READY pin goes to a high-impedance state when *SS* is taken high.

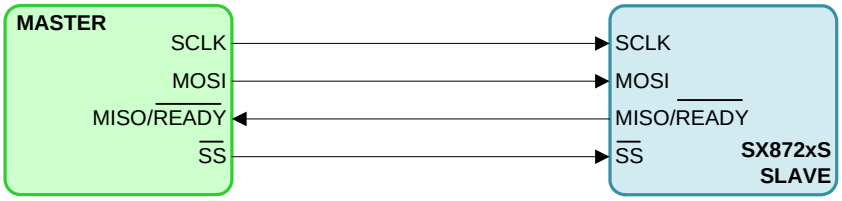


Figure 26. Example of 4-wire Slave

When the *DataReadyEn* bit in **RegACCfg4[0x56]** register is set to '1', this pin functions as both *MISO* and *READY*. Data are shifted out from this pin, MSB first, at the falling edge of *SCLK*. When the *DataReadyModeEn* bit is enabled and a new conversion is complete, *MISO/READY* goes low if it is high. If it is already low, then *MISO/READY* goes high and then goes low (see **Figure 27** below).

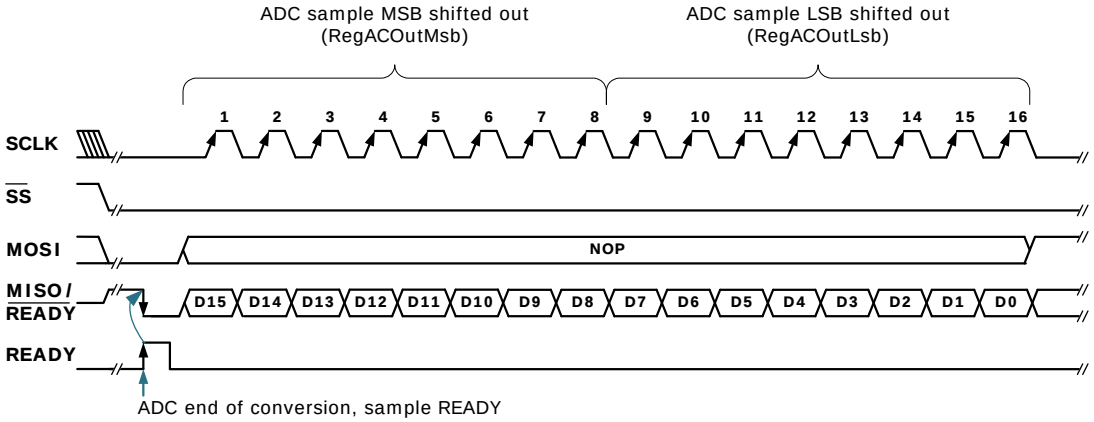


Figure 27. Data Retrieval with the COMBINED DATA READY mode enabled

Similar to the *READY* pin (but with opposite polarity), a falling edge on the *MISO/READY* pin signals that a new conversion result is ready. After *MISO/READY* goes low, the data can be clocked out by providing 16 clocks pulses on *SCLK*.
In order to force *MISO/READY* high (so that *MISO/READY* can be polled for a '0' instead of waiting for a falling edge), a no operation command (NOP) or any other command that does not load the data output register can be sent after

reading out the data. The *MISO/READY* pin goes high after the first rising edge of *SCLK* after reading the conversion result completely (see **Figure 28** below).

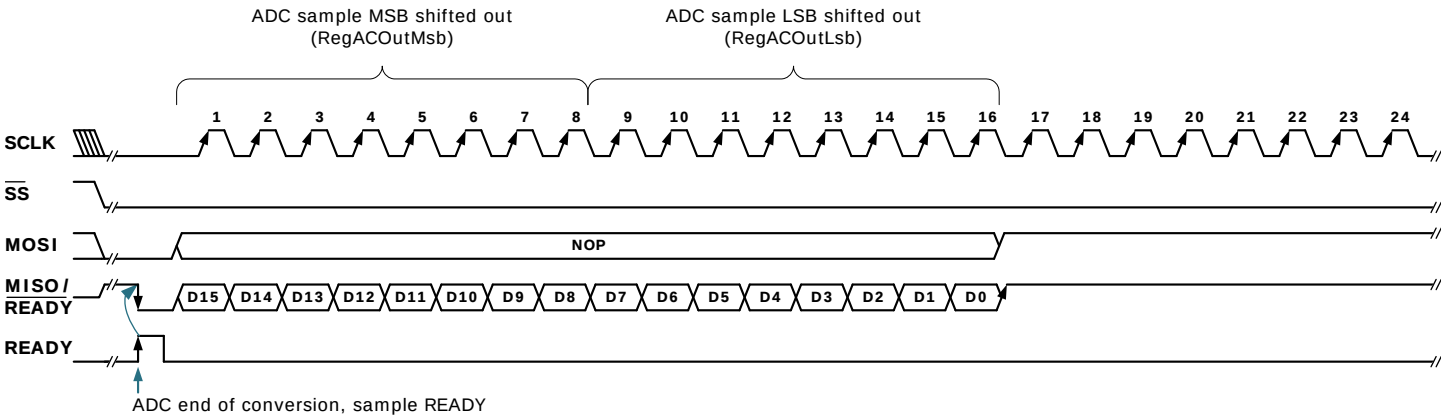


Figure 28. MISO/READY Forced High After Retrieving the Conversion Result

The same condition also applies after a Read Register command. After all the register bits have been read out, the rising edge of *SCLK* forces *MISO/READY* high.

The Combined Data Ready mode must not be used with more than one slave.
To get the interruption on MISO pin, SS should be set to low during all the duration of the Combined Data Ready mode.
In Combined Data Ready mode, MISO is set to high after the data reception.

9.4 Chip Start Detection with Slave Select Pin

At power-up or after a soft reset, $\overline{SS}$ pin is set to output low during the chip initialization (~250us). If the host $\overline{SS}$ pin is configured at an input pulled high during the power-up sequence, it can detect the SX8723S effective start.

Note that if the host pin has a default output high logical level during the power-up or reset sequences this output it will create a short circuit. Therefore, a resistor should be put on the line to ensure that no current spikes are generated.

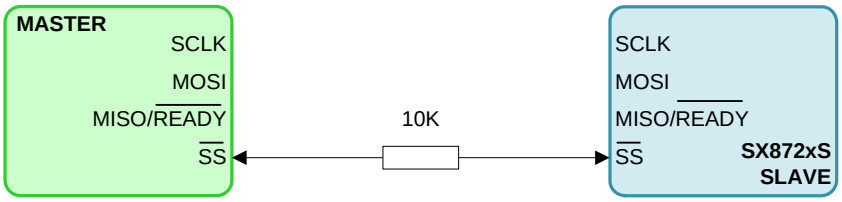


Figure 29. Set a resistor if the host is a high logical level during the startup or the reset

The best value for $\overline{SS}$ resistor should be between 1 kΩ and 10 kΩ. In that range, the current spike is completely avoided and the falling/rising time is ensured.

On **Figure 30** the SPI master uses a separate input for startup status reading. The master $\overline{SS}$ pin is always configured as output for SPI Slave Select. As in the precedent figure, the resistor on the line to ensure that no current spikes are generated when Master and Slave $\overline{SS}$ pins are both configured as outputs during a startup sequence.

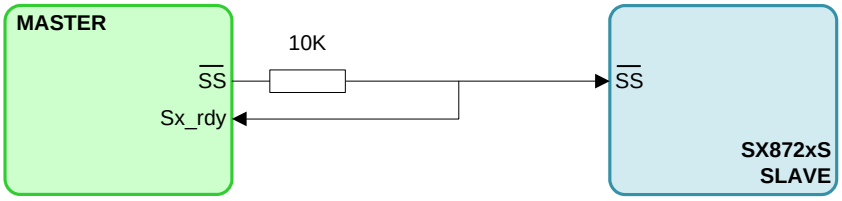


Figure 30. SPI Master using a separate input for startup status reading

9.5 Improving Noise Immunity

Noise may cause incorrect device operation and incorrect data reception. Careful circuit design and PCB layout prevents much of the problems. Noise immunity can be improved using the following methods:

- Keep SPI lines on the PCB away from noisy lines and devices such as switchers.
- Terminate SPI lines at the device using termination resistors as shown in **Figure 31**.

The recommended value for theses resistors is around 100 Ω.

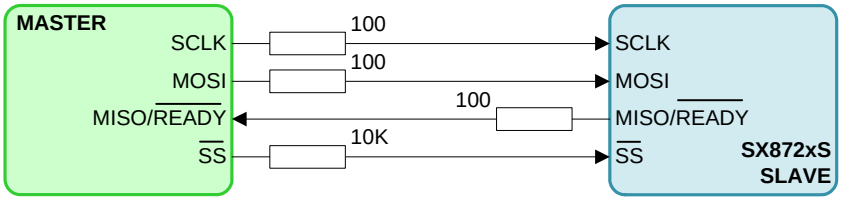


Figure 31. Resistors to improve noise immunity between master and slave

The SCLK, MISO, MOSI and $\overline{SS}$ lines can also be decoupled with capacitors to increase noise performance. The values of R and C then depend on the transmission speed of the SPI bus. For a transmission speed of around 100 kHz, an R of 100 Ω and C of 1nF is suggested. For higher transmission speeds, the values of R and C should be reduced accordingly. But if the operating environment is very noisy, larger values of R and C must be selected, and the transmission speed should be reduced.

10 Register Memory Map and Description

10.1 Register Map

Table 21 below describes the register/memory map that can be accessed through the SPI interface. It indicates the register name, register address and the register contents.

Table 21. Register Map

Address	Register	Bit	Description
RC Register			
0x30	*RegRCen*	1	RC oscillator control
GPIO Registers			
0x40	*RegOut*	8	D0 pads data output and direction control
0x41	*RegIn*	4	D0 pads input data
0x44	*RegSoftReset*		SPI software reset
ADC Registers			
0x50	*RegACOutLsb*	8	LSB of ADC result
0x51	*RegACOutMsb*	8	MSB of ADC result
0x52	*RegACCfg0*	8	ADC conversion control
0x53	*RegACCfg1*	8	ADC conversion control
0x54	*RegACCfg2*	8	ADC conversion control
0x55	*RegACCfg3*	8	ADC conversion control
0x56	*RegACCfg4*	8	ADC conversion control
0x57	*RegACCfg5*	8	ADC conversion control
Mode Register			
0x70	*RegMode*	8	Chip operating mode register

10.2 Registers Descriptions

The register descriptions are presented here in ascending order of Register Address. Some registers carry several individual data fields of various sizes; from single-bit values (e.g. flags), upwards. Some data fields are spread across multiple registers. After power on reset the registers will have the values indicated in the tables "Reset" column. Please write the “Reserved” bits with their reset values.

10.2.1 RC Register

Table 22. RegRCen[0x30]

Bit	Bit Name	Mode	Reset	Description
7:1	-	r	0000000	Reserved
0	*RCEn*	rw	1	Enables RC oscillator. Set 0 for low power mode.

Table 23. RegIn[0x41]

Bit	Bit Name	Mode	Reset	Description
7:2	-	r	0000	Reserved
1	*D1In*	r	-	D1 pad value
0	*D0In*	r	-	D0 pad value

10.2.2 Software reset register

Table 24. RegSoftReset[0x44]

Bit	Name	Mode	Reset	Description
7:0	*SoftReset*	rw	00000000	Write the 0xDE (b11011110) value into this register to reset the device.

10.2.3 ZADC Registers

Table 25. RegACOutLsb[0x50]

Bit	Name	Mode	Reset	Description
7:0	*Out[7:0]*	r	00000000	LSB of the ADC result

Table 26. RegACOutMsb[0x51]

Bit	Name	Mode	Reset	Description
7:0	*Out[15:8]*	r	00000000	MSB of the ADC result

Table 27. RegACCfg0[0x52]

Bit	Name	Mode	Reset	Description
7	*Start*	rw	0	Starts an ADC conversion
6:5	*SetNelconv*	rw	01	Sets the number of elementary conversion to $2^{SetNelconv}$. To compensate for offset the signal is chopped between elementary conversion.

Table 27. RegACCfg0[0x52]

Bit	Name	Mode	Reset	Description
4:2	*SetOsr*	rw	010	Sets the ADC over-sampling rate of an elementary conversion to $2^{3+SetOsr}$.
1	*Continuous*	rw	0	Sets the continuous ADC conversion mode
0	*SampleShiftEn*	rw	0	ADC samples can be read directly on the SPI See **section 9.3.1, page 39**.

Table 28. RegACCfg1[0x53]

Bit	Name	Mode	Reset	Description
7:6	*IbAmpAdc*	rw	11	Bias current selection for the ADC
5:4	*IbAmpPga*	rw	11	Bias current selection for the PGA
3	*Enable*	rw	0	PGA3 enable
2		rw	0	PGA2 enable
1		rw	0	PGA1 enable
0		rw	0	ADC enable

Table 29. RegACCfg2[0x54]

Bit	Name	Mode	Reset	Description
7:6	*SetFs*	rw	00	ADC Sampling Frequency selection
5:4	*Pga2Gain*	rw	00	PGA2 gain selection
3:0	*Pga2Offset*	rw	0000	PGA2 offset selection

Table 30. RegACCfg3[0x55]

Bit	Name	Mode	Reset	Description
7	*Pga1Gain*	rw	0	PGA1 gain selection
6:0	*Pga3Gain*	rw	0001100	PGA3 gain selection

Table 31. RegACCfg4[0x56]

Bit	Name	Mode	Reset	Description
7	*DataReadyEn*	rw	0	Combined SPI MISO and ADC Data Ready signal. 0 : Combined Data Ready mode disabled 1 : Combined Data Ready mode enabled See **section 9.3.2, page 39**.
6:0	*Pga3Offset*	rw	0000000	PGA3 offset selection

Table 32. RegACCfg5[0x57]

Bit	Name	Mode	Reset	Description
7	*Busy*	r	0	ADC activity flag
6	*Def*	rw	0	Selects ADC and PGA default configuration, starts an ADC conversion
5:1	*Amux*	rw	00000	Input channel configuration selector
0	*Vmux*	rw	0	Reference channel selector 0 : VBATT 1 : VREF

10.2.4 Mode Registers

Table 33. RegMode[0x70]

Bit	Name	Mode	Reset	Description
7	-	r	1	reserved
6	-	r	0	reserved
5:4	*Chopper*	rw	00	VREF chopping control. **Note 1** 11 : Chop at NELCONV/2 rate 10 : Chop at NELCONV rate 01 : Chop state=1 00 : Chop state=0
3	*MultForceOn*	rw	0	Force charge pump On. Takes priority. **Note 2**
2	*MultForceOff*	rw	1	Force charge pump Off. **Note 2**
1	*VrefD0Out*	rw	0	Enable VREF output on D0 pin
0	*VrefD1In*	rw	0	Enable external VREF on D1 pin

(1) The chop control is to allow chopping of the internal bandgap reference. This may be useful to help eliminate bandgap related internal offset voltage and 1/f noise. The bandgap chop state may be forced High or Low, or may be set to toggle during conversion at either the same rate or half the rate of the Elementary Conversion. (See Conversion Sequence in the ZoomingADC description).

(2) The internal charge pump may be forced On when *VBATT* supply is below 3V or Off when *VBATT* supply is above 3V. Enabling the charge pump increase the current consumption. If the *ADC* is not being run at full rate or full accuracy then it may operate sufficiently well when *VBATT* is less than 3V and internal charge pump forced Off.

11 Typical Performances

Note	The graphs and tables provided following this note are statistical summary based on limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range and therefore outside the warranted range.

11.1 Input impedance

The *PGAs* of the ZoomingADC are a switched capacitor based blocks (see Switched Capacitor Principle section). This means that it does not use resistors to fix gains, but capacitors and switches. This has important implications on the nature of the input impedance of the block.
Using switched capacitors is the reason why, while a conversion is done, the input impedance on the selected channel of the *PGAs* is inversely proportional to the sampling frequency *fs* and to stage gain as given in **Equation 24**.

$$Z_{in} \geq \frac{1}{(Cg \cdot gain + Cp)} \quad [\Omega]$$

Equation 24

The input impedance observed is the input impedance of the first PGA stage that is enabled or the input impedance of the ADC if all three stages are disabled.

Cg multiplied by *gain* is the equivalent gain capacitor and *Cp* is the parasitic capacitor of the first enabled stage. The values for each ZoomingADC bloc are provided in **Table 34**:

Table 34. Capacitor values

Acquisition Chain Stage	Gain capacitor Cg	Parasitic capacitor Cp	Units
PGA1	0.45	1.04	pF
PGA2	0.54	1.5	pF
PGA3	0.775	1.8	pF
ADC	2.67		pF

Table 34 gives typical impedance values for various gain configurations.

Table 35. Typical Input Impedances

ZIN [MΩ]		PGA1gain		PGA2 gain				PGA3 gain				
		1	10	1	2	5	10	1	2	4	8	10
fs [kHz]	62.5	10.26	2.59	7.95	5.05	2.84	2.24	6.25	4.32	2.86	1.87	1.63
	125	5.14	1.30	3.99	2.54	1.44	1.11	3.13	2.16	1.43	0.94	0.82
	250	2.57	0.65	1.98	1.26	0.71	0.56	1.56	1.08	0.72	0.47	0.41
	500	1.29	0.32	0.99	0.63	0.36	0.28	0.78	0.54	0.36	0.24	0.21

PGA1 (with a gain of 10) and *PGA2* (with a gain of 10) have each a minimum input impedance of 300 kΩ at *fs* = 500 kHz. *PGA3* (with a gain of 10) have a minimum input impedance of 250 kΩ at *fs* = 500 kHz.

Larger input impedance can be obtained by reducing the gain and/or by reducing the over-sampling frequency *fs*. Therefore, with a gain of 1 and a sampling frequency of 62.5 kHz, Zin > 10.2 MΩ for *PGA1*.

The input impedance on channels that are not selected is very high (>10MΩ).

11.1.1 Switched Capacitor Principle

Basically, a switched capacitor is a way to emulate a resistor by using a capacitor. The capacitors are much easier to realize on CMOS technologies and they show a very good matching precision.

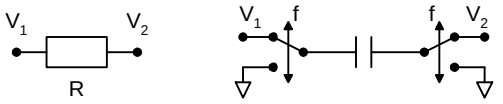


Figure 32. The Switched Capacitor Principle

A resistor is characterized by the current that flows through it (positive current leaves node V_1):

$$I = \frac{V_1 - V_2}{R} \quad [A]$$

Equation 25

One can verify that the mean current leaving node V_1 with a capacitor switched at frequency *f* is:

$$\langle I \rangle = (V1 - V2) \cdot C \quad [A]$$

Equation 26

Therefore as a mean value, the switched capacitor 1/(*f* x *C*) is equivalent to a resistor. It is important to consider that this is only a mean value. If the current is not integrated (low impedance source), the impedance is infinite during the whole time but the transition.
What does it mean for the ZoomingADC?
If the fs clock is reduced, the mean impedance is increased. By dividing the fs clock by a factor 10, the impedance is increased by a factor 10.

One can reduce the capacitor that is switched by using an amplifier set to its minimal gain. In particular if *PGA1* is used with gain 1, its mean impedance is 10x bigger than when it is used with gain 10.

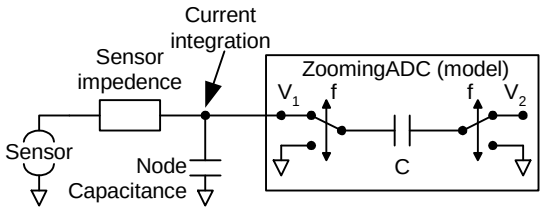


Figure 33. The Switched Capacitor Principle

One can increase the effective impedance by increasing the electrical bandwidth of the sensor node so that the switching current is absorbed through the sensor before the switching period is over. Measuring the sensor node will show short voltage spikes at the frequency fs, but these will not influence the measurement. Whereas if the bandwidth of the node is lower, no spikes will arise, but a small offset can be generated by the integration of the charges generated by the switched capacitors, this corresponds to the mean impedance effect.

Notes:

(1) One can increase the mean input impedance of the ZoomingADC by lowering the acquisition clock *fs*.
(2) One can increase the mean input impedance of the ZoomingADC by decreasing the gain of the first enabled amplifier.
(3) One can increase the effective input impedance of the ZoomingADC by having a source with a high electrical bandwidth (sensor electrical bandwidth much higher than *fs*).

11.2 Frequency Response

The incremental *ADC* is an over-sampled converter with two main blocks: an analog modulator and a low-pass digital filter. The main function of the digital filter is to remove the quantization noise introduced by the modulator. This filter determines the frequency response of the transfer function between the output of the *ADC* and the analog input *VIN*. Notice that the frequency axes are normalized to one elementary conversion period *OSR* / *fs*. The plots of **Figure 34, page 52** also show that the frequency response changes with the number of elementary conversions *NELCONV* performed. In particular, notches appear for *NELCONV* >= 2 These notches occur at:

$$f_{NOTCH} = \frac{i \cdot f_s}{OSR \cdot N_{ELCONV}} \qquad \text{For} \qquad i = 1, 2, \ldots (N_{ELCONV} - 1)$$

Equation 27

and are repeated every fs / OSR.

Information on the location of these notches is particularly useful when specific frequencies must be filtered out by the acquisition system. This chip has no dedicated 50/60 Hz rejection filtering but some rejection can be achieved by using **Equation 27** and setting the appropriate values of *OSR*, *fs* and *NELCONV*.

Table 36. 50/60 Hz Line Rejection Examples

Rejection [Hz]	fNOTCH [Hz]	fs [kHz]	OSR [-]	NELCONV [-]
60	61	125	1024	2
	61	250	1024	4
	61	500	1024	8
50	53	62.5	1024	8
	46	62.5	1024	4
	46	125	1024	8

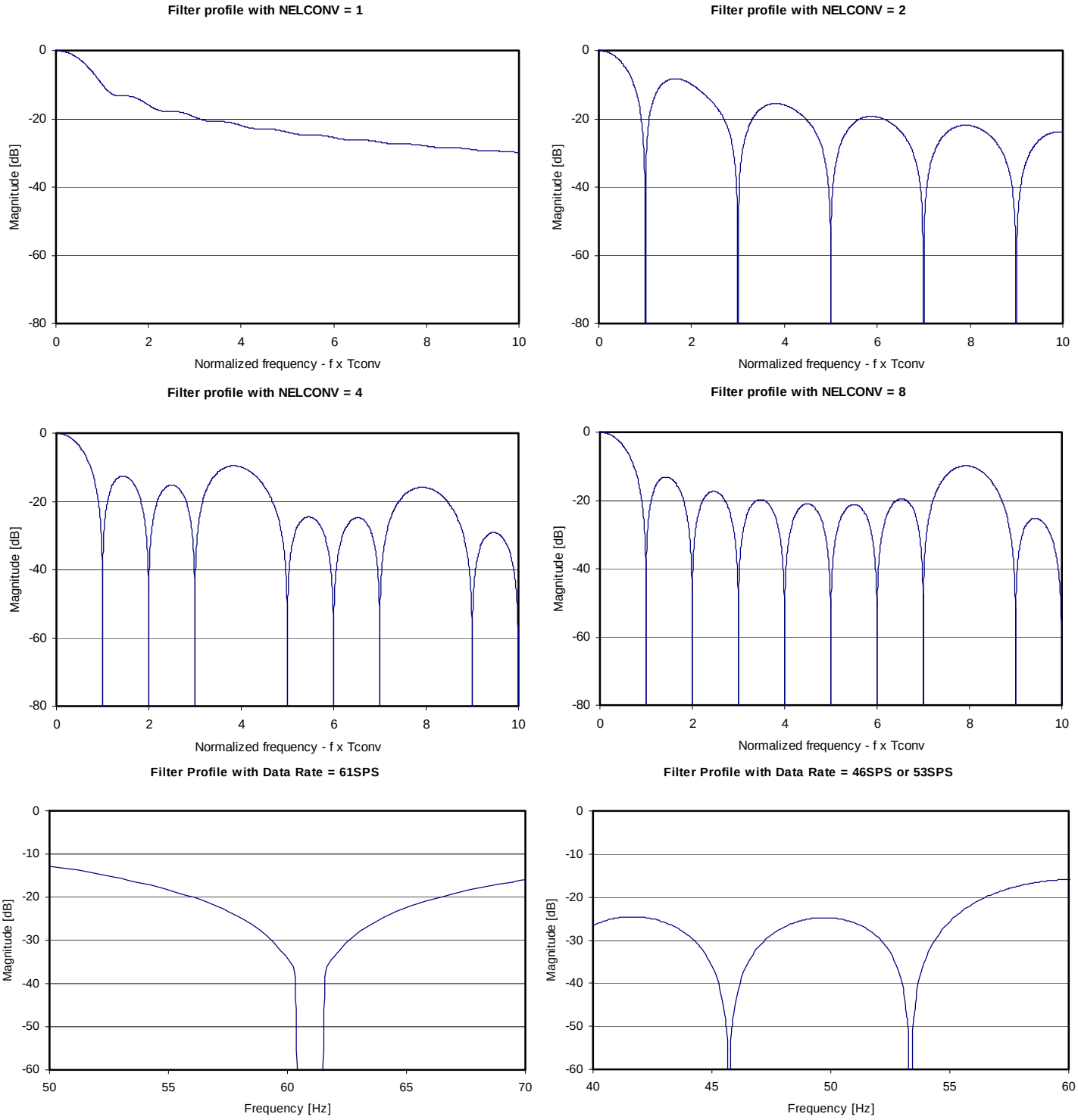


Figure 34. Frequency Response. Normalized Magnitude vs. Frequency for Different NELCONV

11.3 Linearity

11.3.1 Integral Non-Linearity

The different *PGA* stages have been designed to find the best compromise between the noise performance, the integral non-linearity and the power consumption. To obtain this, the first stage has the best noise performance and the third stage the best linearity performance. For large input signals (small *PGA* gains, i.e. up to about 50), the noise added by the *PGA* is very small with respect to the input signal and the second and third stage of the *PGA* should be used to get the best linearity. For small input signals (large gains, i.e. above 50), the noise level in the *PGA* is important and the first stage of the *PGA* should be used.
The following figures show the Integral non linearity for different gain settings over the chip temperature range

11.3.1.1 Gain 1

V_{BATT}=5V; V_{REF}=V_{BATT}; PGAs disabled; OSR=1024; Nelconv=8; fs=250kHz; Resolution=16bits.

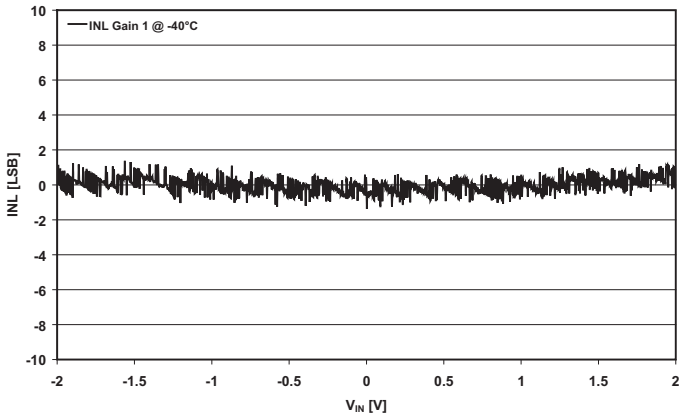


Figure 35. INL -40°C

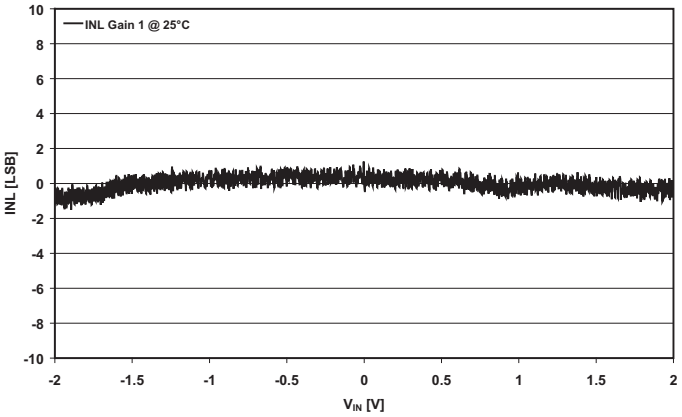


Figure 36. INL 25°C

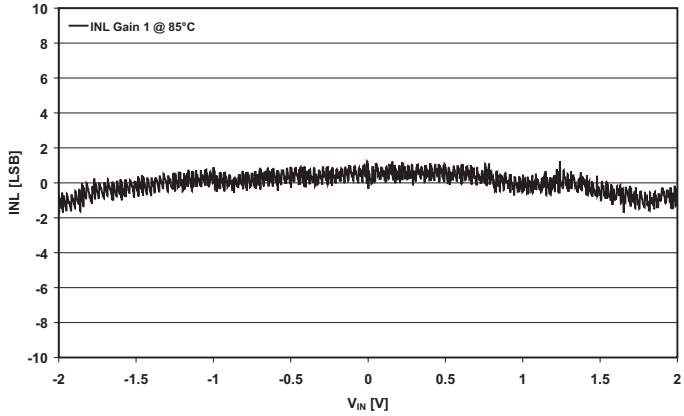


Figure 37. INL 85°C

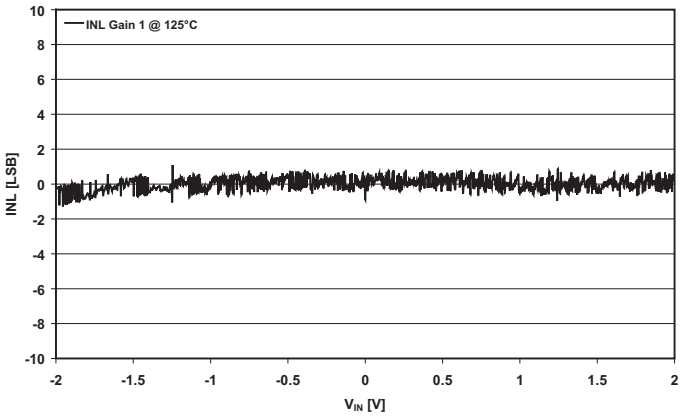


Figure 38. INL 125°C

11.3.1.2 Gain 10

VBATT=5V; VREF=VBATT; ADC and PGA3 enabled; GD3=10; OSR=1024; Nelconv=8; fs=250kHz; Resolution=16bits.

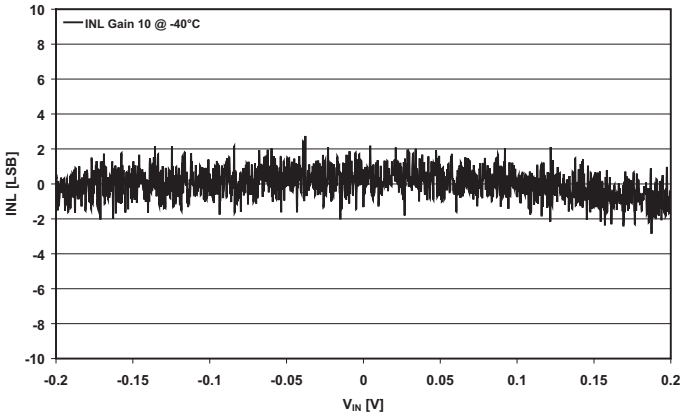


Figure 39. INL -40°C

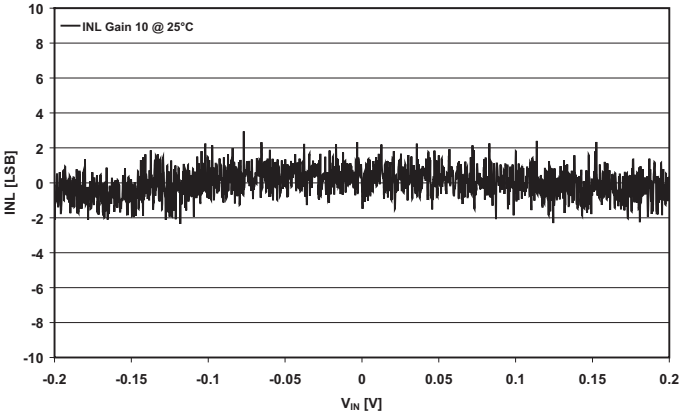


Figure 40. INL 25°C

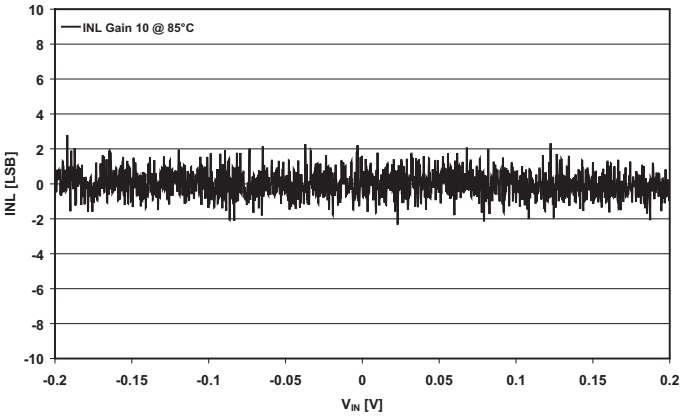


Figure 41. INL 85°C

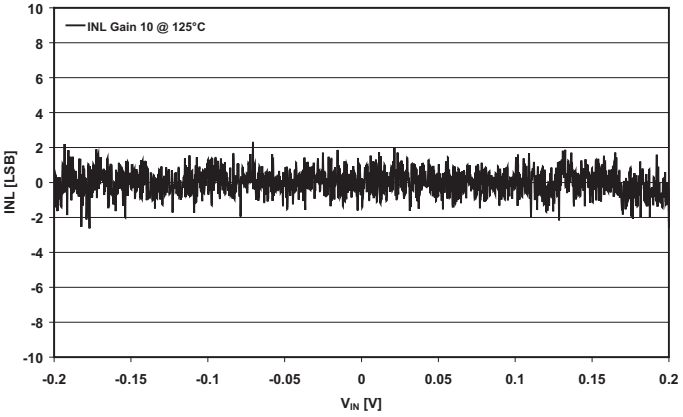
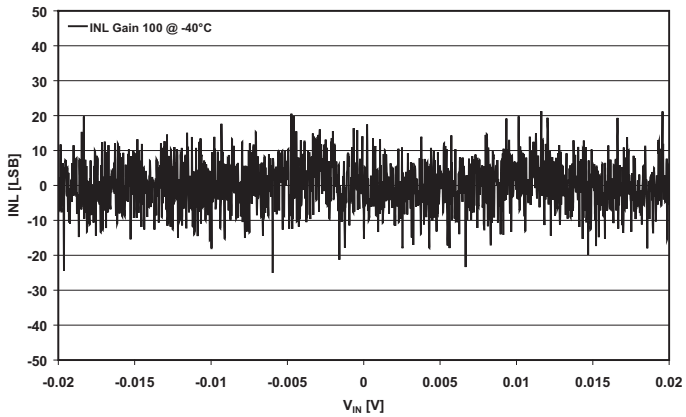


Figure 42. INL 125°C

11.3.1.3 Gain 100

VBATT=5V; VREF=VBATT; ADC, PGA2 and PGA3 enabled; GD2=10; GD3=10; OSR=1024; Nelconv=8; fs=250kHz; Resolution=16bits.



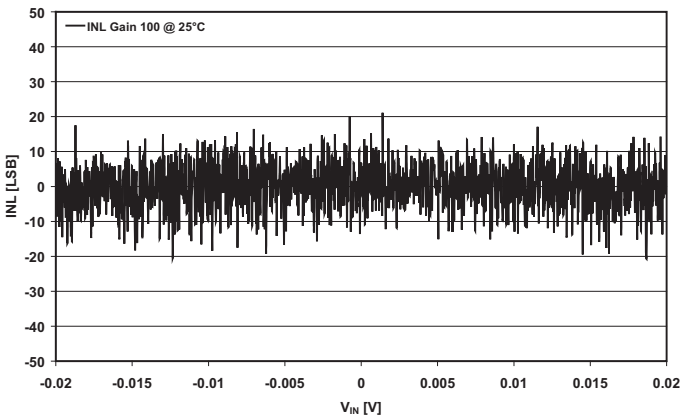


Figure 43. INL -40°C

Figure 44. INL 25°C

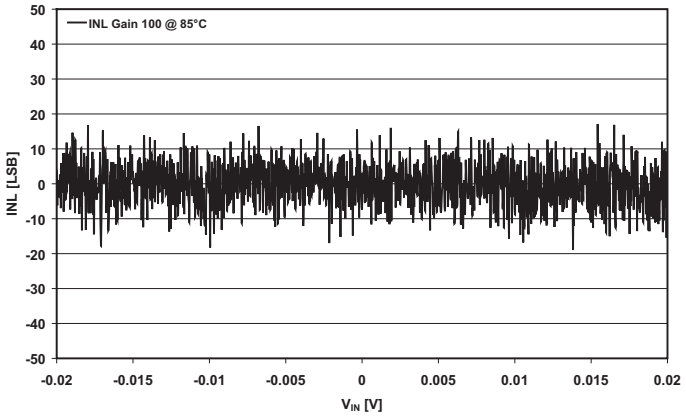


Figure 45. INL 85°C

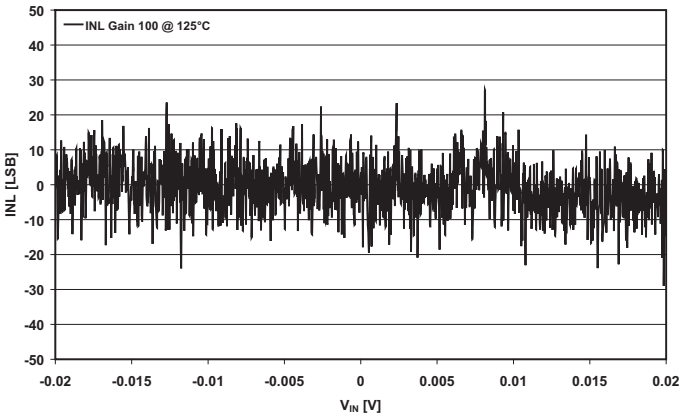


Figure 46. INL 125°C

11.3.1.4 Gain 1000

VBATT=5V; VREF=VBATT; ADC, PGA3, PGA2, PGA1 enabled; GD1=10, GD2=10, GD3=10; OSR=1024; NELCONV=8; fs=250KHz; Resolution=16bits.

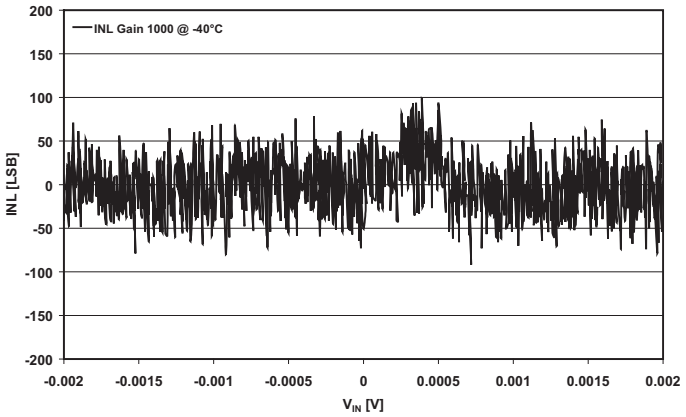


Figure 47. INL -40°C

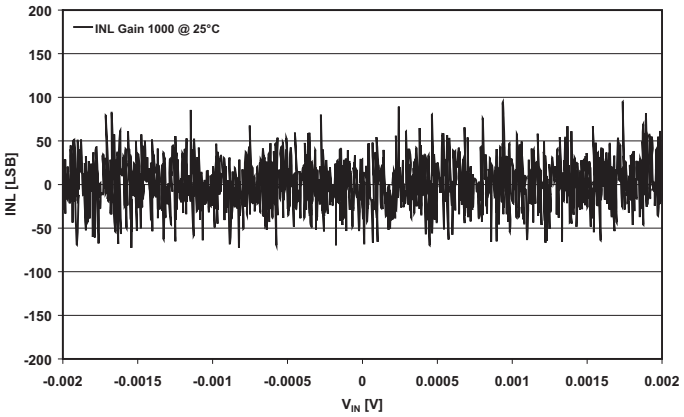


Figure 48. INL 25°C

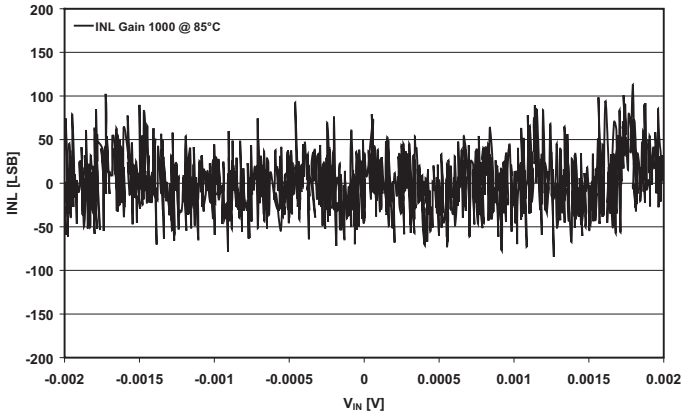


Figure 49. INL 85°C

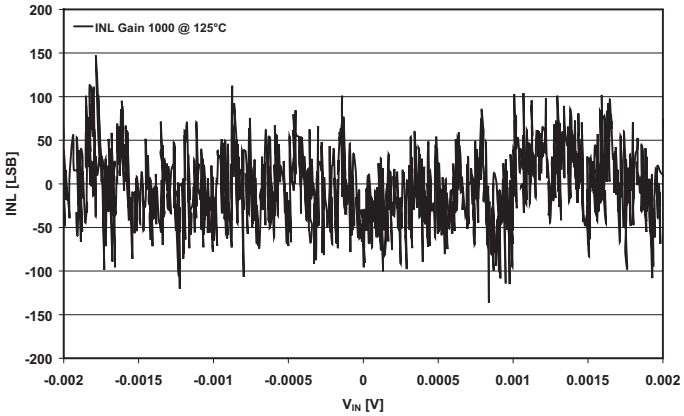


Figure 50. INL 125°C

11.3.2 Differential Non-Linearity

The differential non-linearity is generated by the *ADC*. The *PGA* does not add differential non-linearity. **Figure 51** shows the differential non-linearity.

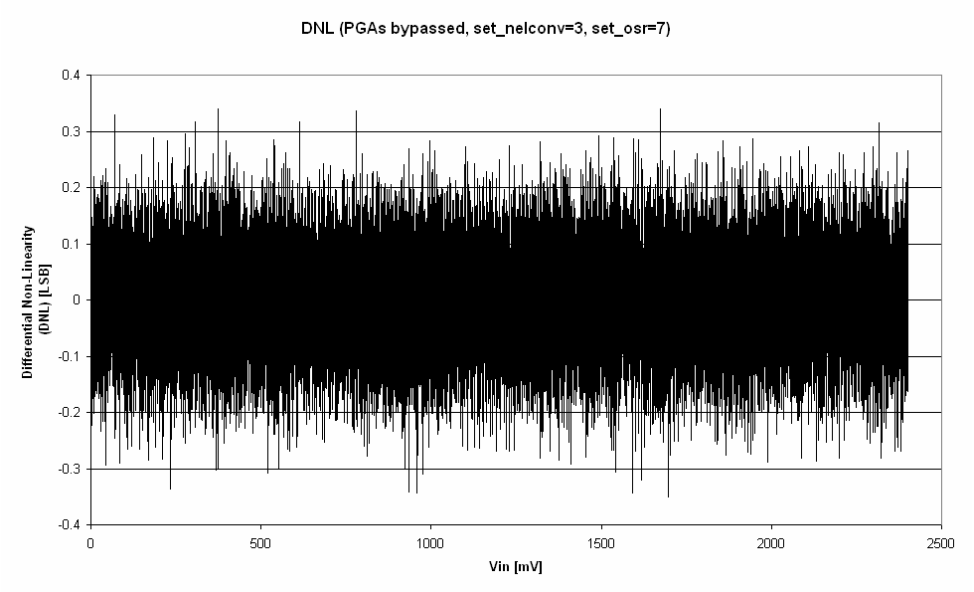


Figure 51. Differential Non-Linearity of the ADC Converter

11.4 Noise

Ideally, a constant input voltage V_{IN} should result in a constant output code. However, because of circuit noise, the output code may vary for a fixed input voltage. Thus, a statistical analysis on the output code of 1200 conversions for a constant input voltage was performed to derive the equivalent noise levels of *PGA1*, *PGA2*, and *PGA3*.

The extracted RMS output noise of *PGA1*, *2*, and *3* are given in **Table 37, page 58**: standard output deviation and output rms noise voltage.

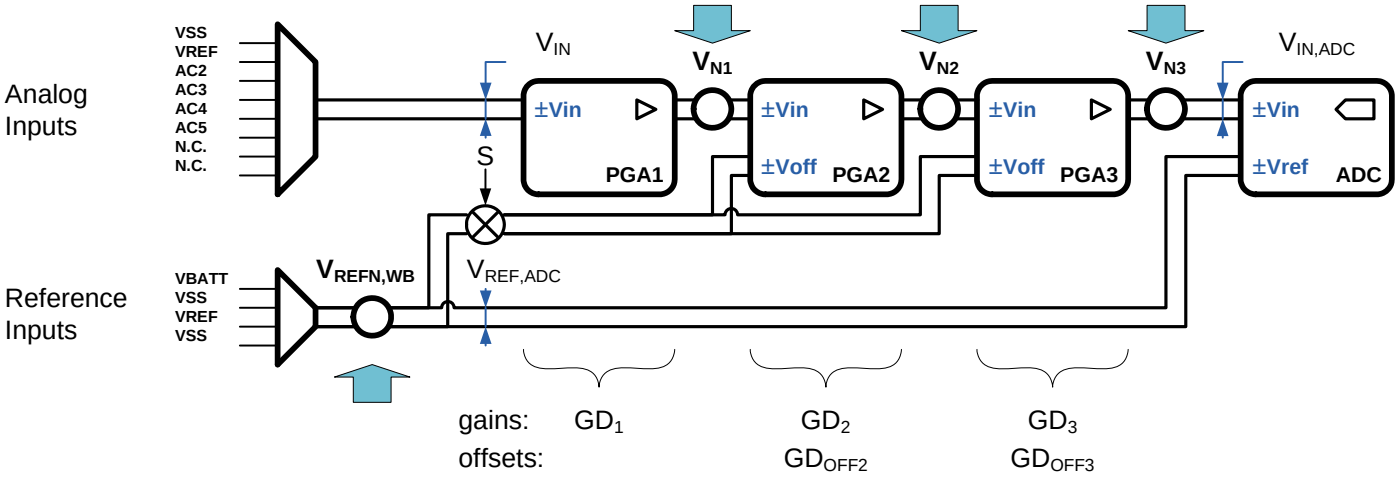


Figure 52. Simple Noise Model for PGAs and ADC

VN1, *VN2*, and *VN3* are the output RMS noise figures of **Table 37**, *GD1*, *GD2*, and *GD3* are the *PGA* gains of stages 1 to 3 respectively. *VREFN,WB* is the wide band noise on the reference voltage.

The simple noise model of **Figure 52** is used to estimate the equivalent input referred RMS noise *VN,IN* of the acquisition chain in the model of **Figure 54, page 58**. This is given by the relationship:

$$V_{N,IN}{}^2 = \frac{\left(\frac{V_{N1}}{GD_1}\right)^2 + \left(\frac{V_{N2}}{GD_1 \cdot GD_2}\right)^2 + \left(\frac{V_{N3}}{GD_{TOT}}\right)^2 + \left(\frac{V_{REFN,WB}\left(GD_2 \cdot GD_{OFF2} + GD_{OFF3}\right)}{GD_{TOT}}\right)^2 + \left(\frac{1}{2} \cdot \frac{V_{REFN,WB}}{GD_{TOT}}\right)^2}{\left(OSR \cdot N_{ELCONV}\right)} \left[V^2 rms\right]$$

Equation 28

On the numerator of **Equation 28**:

1 the first parenthesis is the PGA1 gain amplifier contribution to noise
2 the second parenthesis is the PGA2 gain amplifier contribution to noise
3 the third parenthesis is the PGA3 gain amplifier contribution to noise
4 the fourth parenthesis is PGA2 and PGA3 offset amplifiers contributions to noise
5 the last parenthesis is the contribution of the noise on the references of the ADC

As shown in **Equation 28**, noise can be reduced by increasing *OSR* and *NELCONV* (increases the *ADC* averaging effect, but reduces noise).

Table 37. PGA Noise Measurement (n = 16bits, OSR = 512, NELCONV = 2, VREF = 5V)

Parameter	PGA1	PGA2	PGA3
Output RMS noise [uV]	V_{N1} = 205	V_{N2} = 340	V_{N3} = 365

Figure 53 shows the distribution for the *ADC* alone (*PGA1*, *2*, and *3* bypassed). Quantization noise is dominant in this case, and, thus, the *ADC* thermal noise is below 16 bits.

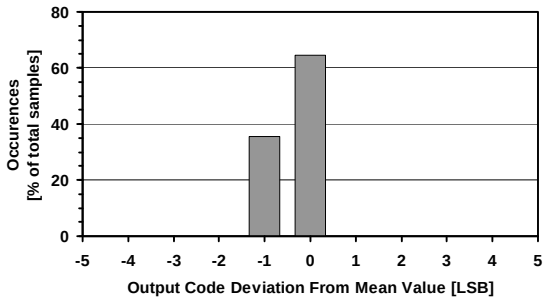


Figure 53. ADC Noise (PGA1, 2 & 3 Bypassed, OSR = 512, NELCONV = 2)

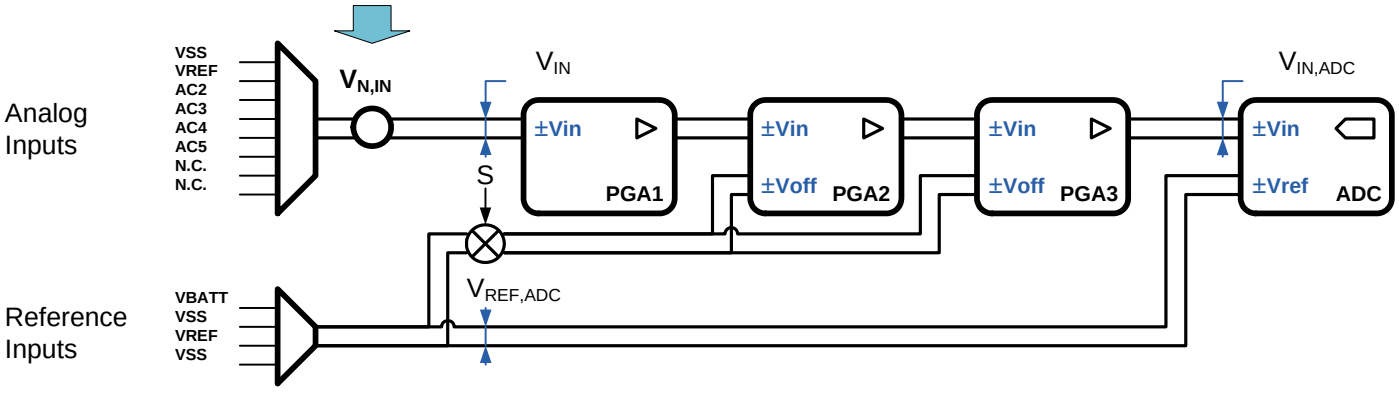


Figure 54. Total Input Referred Noise

As an example, consider the system where: GD_2 = 10 (GD_1 = 1; *PGA3* bypassed), *OSR* = 512, *NELCONV* = 2, *VREF* = 5 V. In this case, the noise contribution V_{N1} of *PGA1* is dominant over that of *PGA2*. Using **Equation 28, page 57**, we get: $V_{N,IN}$ = 6.4 µV (RMS) at the input of the acquisition chain, or, equivalently, 0.85 LSB at the output of the *ADC*. Considering 0.2 V (RMS) maximum signal amplitude, the signal-to-noise ratio is 90dB.

11.5 Gain Error and Offset Error

Gain error is defined as the amount of deviation between the ideal transfer function (theoretical **Equation 19, page 30**) and the measured transfer function (with the offset error removed).

The actual gain of the different stages can vary depending on the fabrication tolerances of the different elements. Although these tolerances are specified to a maximum of ±3%, they will be most of the time around ±0.5%. Moreover, the tolerances between the different stages are not correlated and the probability to get the maximal error in the same direction in all stages is very low. Finally, these gain errors can be calibrated by the software at the same time with the gain errors of the sensor for instance.

Figure 55 shows gain error drift vs. temperature for different *PGA* gains. The curves are expressed in% of Full-Scale Range (*FSR*) normalized to 25°C.

Offset error is defined as the output code error for a zero volt input (ideally, output code = 0). The offset of the *ADC* and the PGA1 stage are completely suppressed if $N_{ELCONV} > 1$.

The measured offset drift vs. temperature curves for different PGA gains are depicted in **Figure 56**. The output offset error, expressed in LSB for 16-bit setting, is normalized to 25°C. Notice that if the *ADC* is used alone, the output offset error is below +/-1 LSB and has no drift.

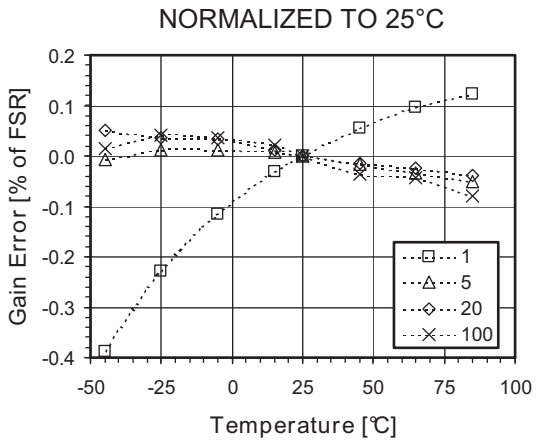


Figure 55. Gain Error vs. Temperature for Different Gains

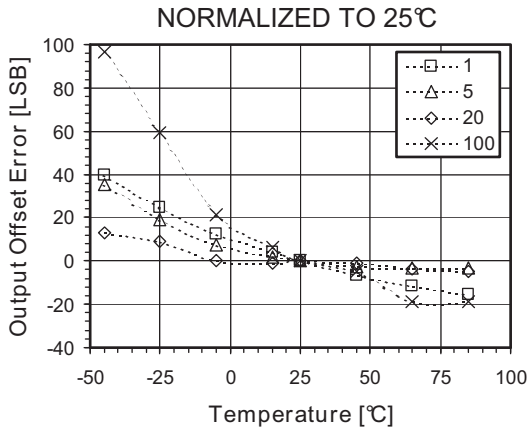


Figure 56. Offset Error vs. Temperature for Different Gains

11.6 Power Consumption

As mentioned in **section 6.4, page 16** the Charge Pump must be enabled if VBATT is below 3V. **Figure 57** plots the variation of current consumption with supply voltage *VBATT*, as well as the distribution between the 3 *PGA* stages and the *ADC* (see **Table 38, page 61**). In this case the Charge Pump is forced ON for VBATT < 4.2V and forced OFF for VBATT > 4.2V.

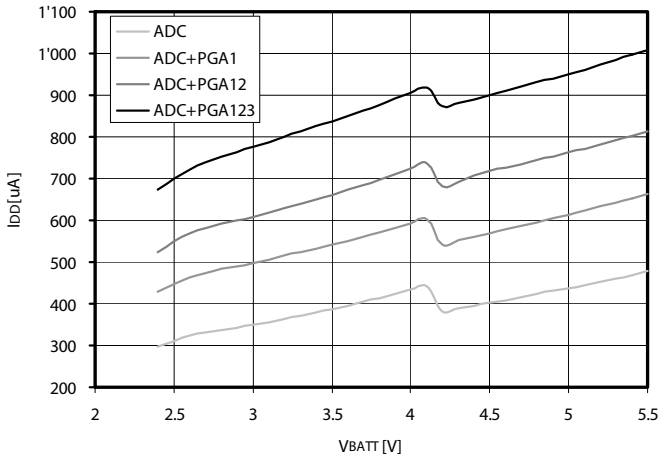


Figure 57. Current Consumption vs. Supply Voltage and PGAs

As shown in **Figure 58**, if lower sampling frequency is used, the current consumption can be lowered by reducing the bias currents of the *PGAs* and the *ADC* with registers *IbAmpPga* and *IbAmpAdc*. (In **Figure 58**, *IbAmpPga/Adc* = '11', '10', '00' for *fs* = 500, 250, 62.5 kHz respectively. In this case the Charge Pump is forced ON for VBATT < 4.2V and forced OFF for VBATT > 4.2V.

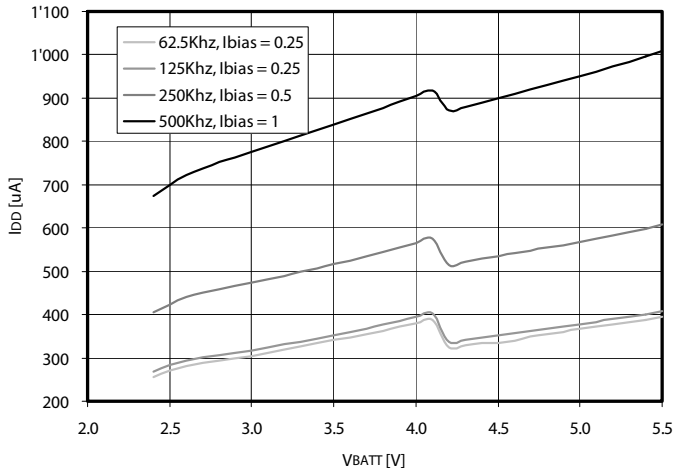


Figure 58. Current Consumption vs. Temperature and ADC Sampling Frequency

Current consumption vs. temperature is depicted in **Figure 59**, showing the increase between -40 and +125°C.

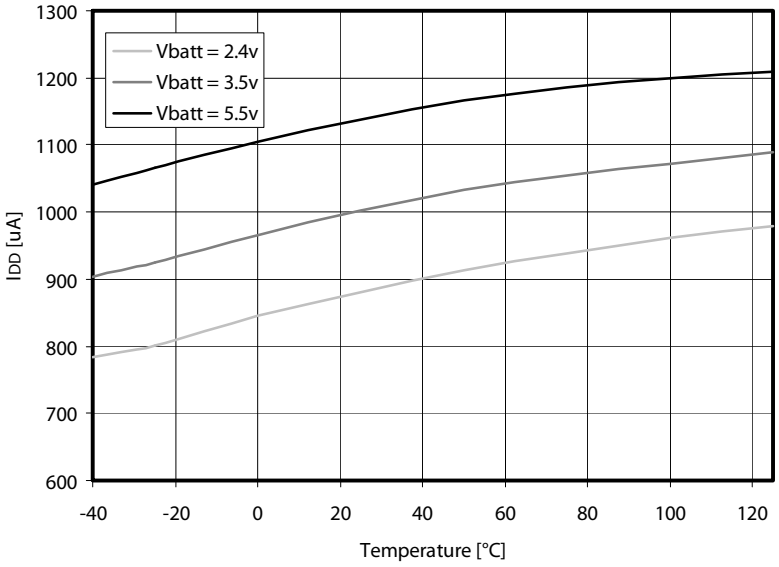


Figure 59. Current Consumption vs. Temperature and Supply Voltage

Table 38. Typical Current Distribution in Acquisition Chain (n = 16 bits, fs = 250kHz)

Supply	ADC	PGA1	PGA2	PGA3	Total	Unit
VBATT = 2.4V	207	70	51	78	406	uA
VBATT = 3.5V	282	82	61	91	516	
VBATT = 5.5V	338	103	67	98	606	

FAMILY OVERVIEW

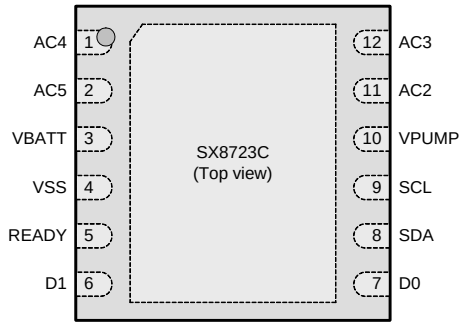
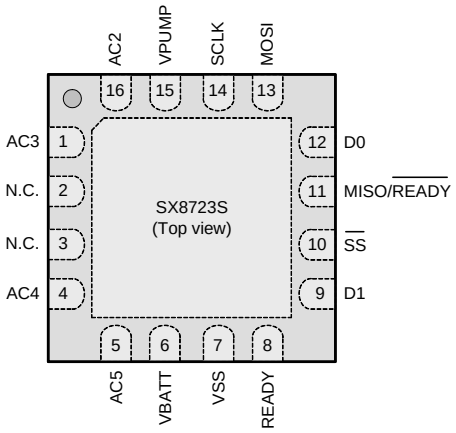
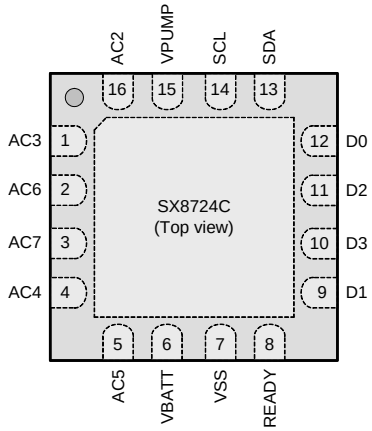
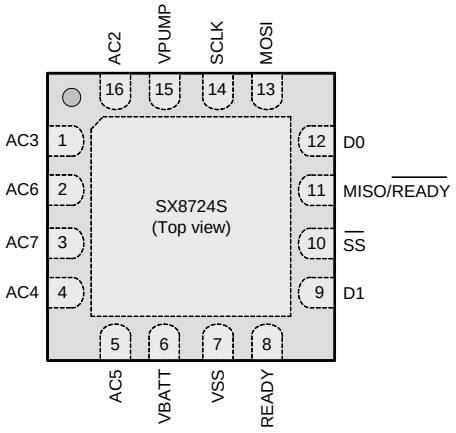
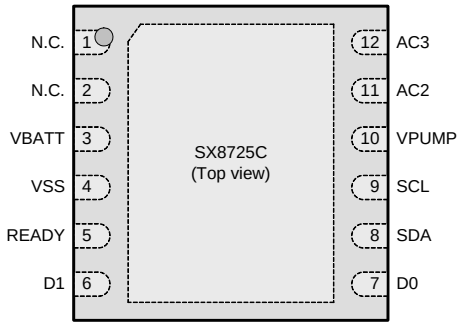
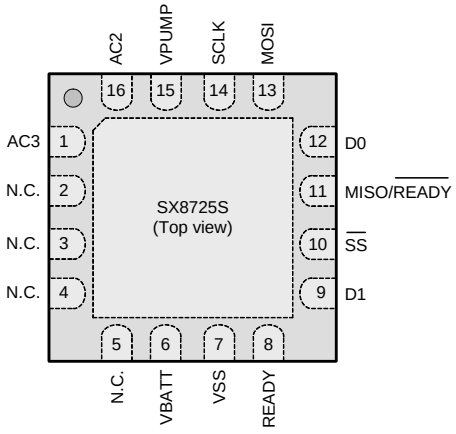
This chapter gives an overview of similar devices based on the ZoomingADC but with different features or packages. Each part is described in it's own datasheet.

12 Comparison Table

Table 39. Family Comparison Table

		Part number					
		SX8723C	**SX8724C**	**SX8725C**	**SX8723S**	**SX8724S**	**SX8725S**
Package		MLPD-W-12 4x4	MLPQ-16 4x4	MLPD-W-12 4x4	MLPQ-16 4x4	MLPQ-16 4x4	MLPQ-16 4x4
Protocol		I2C	I2C	I2C	SPI	SPI	SPI
GPIO	**D0**	I2C addr, Digital IO or Vref OUT	I2C addr, Digital IO or Vref OUT	I2C add, Digital IO or Vref OUT	Digital IO or Vref OUT	Digital IO or Vref OUT	Digital IO or Vref OUT
	D1	I2C addr, Digital IO or Vref IN	I2C addr, Digital IO or Vref IN	I2C addr, Digital IO or Vref IN	Digital IO or Vref OUT.	Digital IO or Vref IN	Digital IO or Vref IN
	D2	N.A.	Digital IO	N.A.	N.A.	N.A.	N.A.
	D3	N.A.	Digital IO	N.A.	N.A.	N.A.	N.A.
Differential input channels		2	3	1	2	3	1

13 Comparison by package pinout

I2C versions	SPI versions
	
	
	

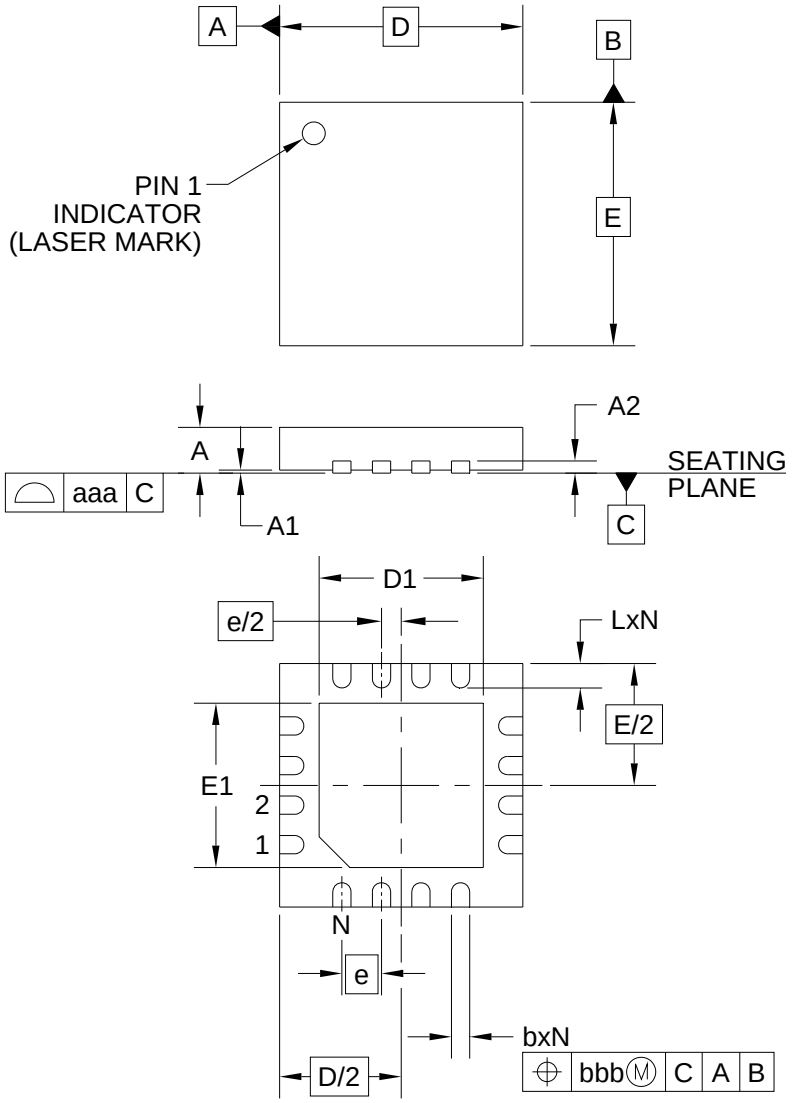
14 PCB Layout Considerations

PCB layout considerations to be taken when using the SX8723S are relatively simple to get the highest performances out of the ZoomingADC. The most important to achieve good performances out the ZoomingADC is to have a good voltage reference. The SX8723S has already an internal reference that is good enough to get the best performances with a minimal amount of external components, but, in case an external reference is needed this one must be as clean as possible in order to get the desired performance. Separating the digital from the analog lines will be also a good choice to reduce the noise induced by the digital lines. It is also advised to have separated ground planes for digital and analog signals with the shortest return path, as well as making the power supply lines as wider as possible and to have good decoupling capacitors.

15 How to Evaluate

For evaluation purposes SX8724SEVK evaluation kit can be ordered. This kit connects to any PC using a USB port. A software gives the user the ability to control the registers as well as getting the raw data from the ZoomingADC and displaying it on the "Graphical User Interface". For more information please look at SEMTECH web site (**http://www.semtech.com/analog-controllers-sensors-converters/**).

16 Package Outline Drawing: MLPQ-W16-4x4-EP1



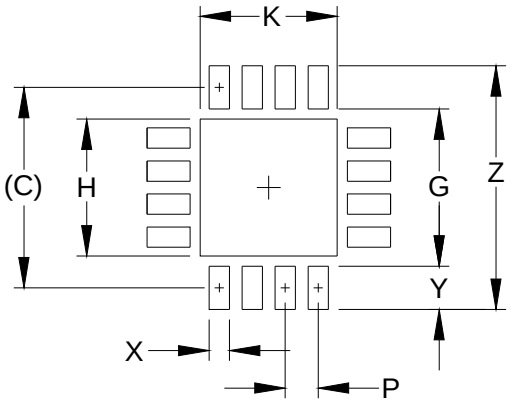
DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	-	0.80
A1	0.00	-	0.05
A2	-	(0.20)	-
b	0.25	0.30	0.35
D	3.90	4.00	4.10
D1	2.55	2.70	2.80
E	3.90	4.00	4.10
E1	2.55	2.70	2.80
e	0.65 BSC		
L	0.30	0.40	0.50
N	16		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 60. Package Outline Drawing

17 Land Pattern Drawing: MLPQ-W16-4x4-EP1



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.156)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.026	0.65
X	.016	0.40
Y	.033	0.85
Z	.189	4.80

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.

Figure 61. Land Pattern Drawing

18 Tape and Reel Specification

MLP/QFN (0.70mm - 1.00mm package thickness)

- Single Sprocket holes
- Tolerances for Ao & Bo are +/- 0.20mm
- Tolerances for Ko is +/- 0.10mm
- Tolerance for Pocket Pitch is +/- 0.10mm
- Tolerance for Tape width is +/-0.30mm
- Trailer and Leader Length are minimum required length
- Package Orientation and Feed Direction

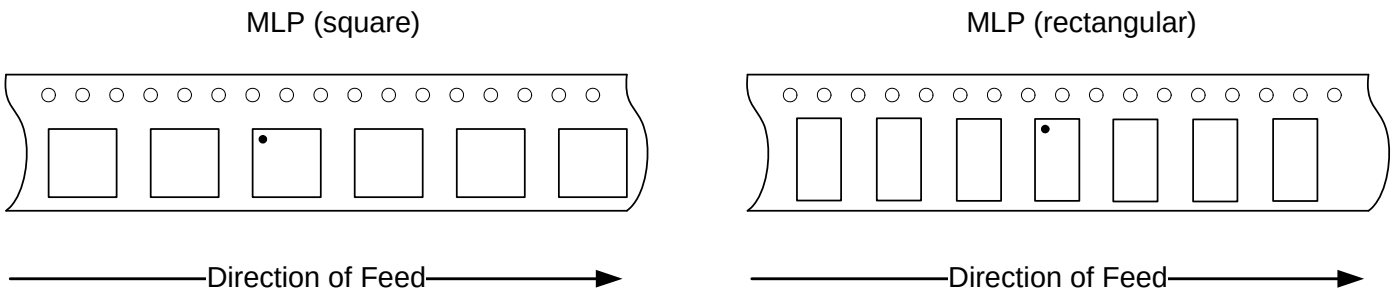


Figure 62. Direction of Feed

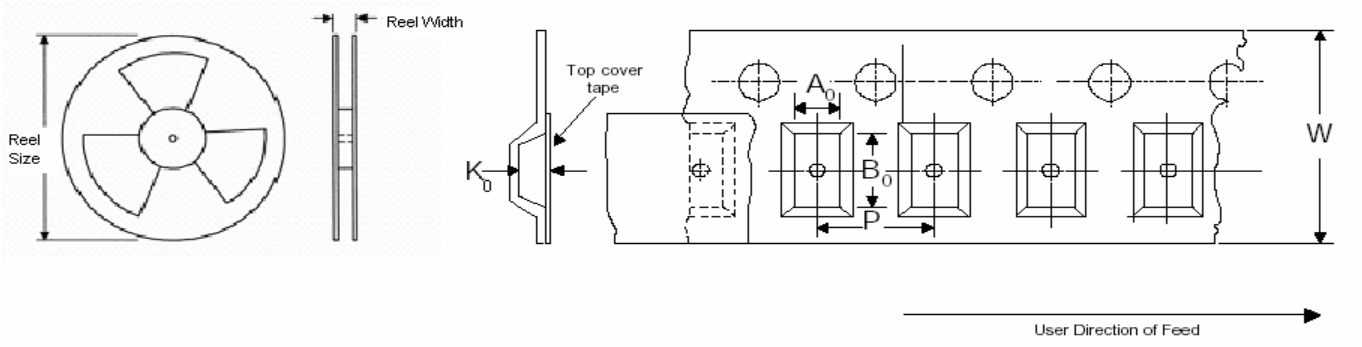


Figure 63. User direction of feed

Table 40. Tape and reel specifications

Pkg size	carrier tape (mm)					Reel				
	Tape Width (W)	Pocket Pitch (P)	Ao	Bo	Ko	Reel Size (in)	Reel Width (mm)	Trailer Length (mm)	Leader Length (mm)	QTY per Reel
4x4	12	8	4.35	4.35	1.10	7/13	12.4	400	400	1000/3000

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