DESCRIPTION

The SX8724C is a data acquisition system based on Semtech's low power ZoomingADC™ technology. It directly connects most types of miniature sensors with a general purpose microcontroller.

With 3 differential inputs, it can adapt to multiple sensor systems. Its digital outputs are used to bias or reset the sensing elements.

FEATURES

- Up to 16-bit differential data acquisition
- Programmable gain: (1/12 to 1000)
- Sensor offset compensation up to 15 times full scale of input signal
- 3 differential or 6 single-ended signal inputs
- Programmable Resolution versus Speed versus Supply current
- Digital outputs to bias Sensors
- Internal or external voltage reference
- Internal time base
- Low-power (250 uA for 16b @ 250 S/s)
- Fast I2C interface with external address option, no clock stretching required

APPLICATIONS

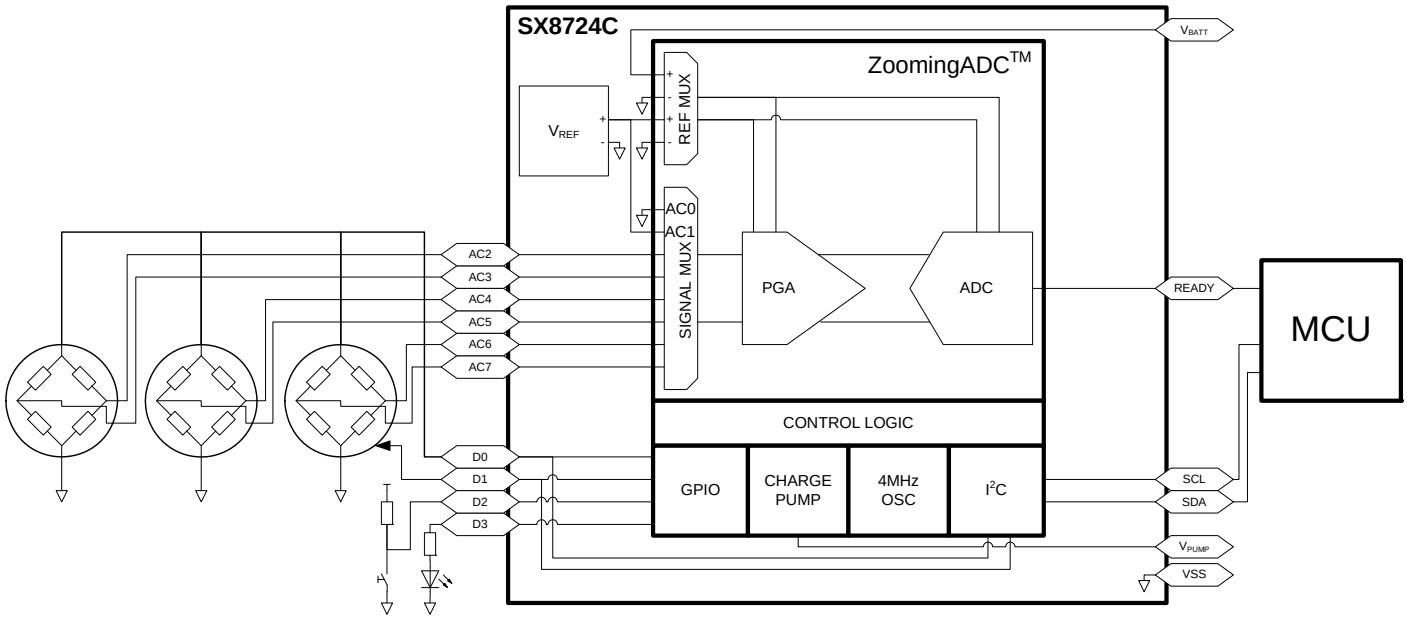
- Industrial pressure sensing
- Industrial temperature sensing
- Industrial chemical sensing
- Barometer
- Compass

ORDERING INFORMATION

DEVICE	PACKAGE	REEL QUANTITY
SX8724CWLTDT	MLPQ-W-16 4x4	1000

- Available in tape and reel only
- WEEE/RoHS compliant, Pb-Free and Halogen Free.

FUNCTIONAL BLOC DIAGRAM



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ELECTRICAL SPECIFICATIONS

1 Absolute Maximum Ratings

Note The Absolute Maximum Ratings, in table below, are stress ratings only. Functional operation of the device at conditions other than those indicated in the Operating Conditions sections of this specification is not implied. Exposure to the absolute maximum ratings, where different to the operating conditions, for an extended period may reduce the reliability or useful lifetime of the product.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Units
Power supply	V_{BATT}		V_{SS} - 0.3	6.5	V
Storage temperature	T_{STORE}		-55	150	°C
Temperature under bias	T_{BIAS}		-40	140	°C
Input voltage	V_{INABS}	All inputs	V_{SS} - 300	V_{BATT} + 300	mV
Peak reflow temperature	T_{PKG}			260	°C
ESD conditions	ESD_{HBM}	Human Body Model ESD	2000		V
Latchup			100		mA

2 Operating Conditions

Unless otherwise specified: *VREF,ADC* = *VBATT*, *VIN* = 0V, Over-sampling frequency *fs* = 250 kHz, *PGA3 on with Gain = 1*, *PGA1&PGA2 off*, offsets *GDOff2* = *GDOff3* = 0. Power operation: normal (*IbAmpAdc[1:0]* = *IbAmpPga[1:0]* = '01').
For resolution n = 12 bits: *OSR* = 32 and *NELCONV* = 4.
For resolution n = 16 bits: *OSR* = 256 and *NELCONV* = 2.
Bandgap chopped at *NELCONV* rate. If *VBATT* < 4.2V, Charge Pump is forced on. If *VBATT* > 4.2V, Charge Pump is forced off.

Table 2. Operating conditions limits

Parameter	Symbol	Comment/Condition	Min	Typ	Max	Unit
Power supply	VBATT		2.4		5.5	V
Operating temperature	TOP		-40		125	°C

.

Table 3. Electrical Characteristics

Parameter	Symbol	Comment/Condition	Min	Typ	Max	Unit
CURRENT CONSUMPTION[1]						
Active current, 5.5V	IOP55	16 b @ 250 Sample/s ADC, fs = 125 kHz		250	350	µA
		16 b @ 1kSample/s PGA3 + ADC, fs = 500 kHz		700	900	
		16 b + gain 1000 @ 1kSample/s PGA3,2,1 + ADC, fs = 500 kHz		1000	1350	
Active current, 3.3V	IOP33	16 b @ 250 Sample/s ADC, fs = 125 kHz		150		µA
		16 b @ 1 kSample/s PGA3 + ADC, fs = 500 kHz		300		
		16 b + gain 1000 @ 1kSample/s PGA3,2,1 + ADC, fs = 500 kHz		850		
Sleep current	ISLEEP	@25°C		75		nA
		up to 85°C		100		
		@125°C		150	200	
TIME BASE						
Max ADC Over-Sampling frequency	fSmax	@25°C	425	500	575	kHz
ADC Over-Sampling frequency drift	fST			0.15		% / °C
DIGITAL I/O						
Input logic high	VIH		0.7			VBATT
Input logic low	VIL				0.3	VBATT
Output logic high	VOH	IOH < 4 mA			VBATT-0.4	V
Output logic low	VOL	IOL < 4 mA	0.4			V
SCL and SDA I/O						
Input logic high	VIH		0.7			VBATT

Table 3. Electrical Characteristics

Parameter	Symbol	Comment/Condition	Min	Typ	Max	Unit
Input logic low	V_{IL}				0.25	V_{BATT}
Leakages currents						
Input leakage current	I_{LeakIn}	Digital input mode, no pull-up or pull-down	-100		100	nA
VREF: Internal Bandgap Reference						
Absolute output voltage	V_{BG}	V_{BATT} > 3V	1.19	1.22	1.25	V
Variation over Temperature	V_{BGT}	V_{BATT} > 3V, over Temperature	-1.5		+1.5	%
Total Output Noise	V_{BGN}	V_{BATT} > 3V			1	mVrms

1. The device can be operated in either active or sleep states. The Sleep state is complete shutdown, but the active state can have a variety of different current consumptions depending on the settings. Some examples are given here: The Sleep state is the default state after power-on-reset. The chip can then be placed into an active state after a valid I2C communication is received.

Table 4. ZoomingADC Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ANALOG INPUT CHARACTERISTICS						
Differential Input Voltage Range $V_{IN} = V_{INP}-V_{INN}$		Gain=1, OSR=32, V_{REF}=5V. **Note 1**	-2.42		+2.42	V
		Gain=100, OSR=32, V_{REF}=5V	-24.2		+24.2	mV
		Gain=1000, OSR=32, V_{REF}=5V	-2.42		+2.42	mV
PROGRAMMABLE GAIN AMPLIFIER						
Total PGA Gain	GD_{TOT}	**Note 1**	1/12		1000	V/V
PGA1 Gain	GD_1	(see **Table 11, page 22**)	1		10	V/V
PGA2 Gain	GD_2	(see **Table 12, page 23**)	1		10	V/V
PGA3 Gain	GD_3	Step = 1/12 V/V (see **Table 13, page 23**)	1/12		127/12	V/V
Gain Settings Precision (each stage)		Gain ≥ 1	-3	±0.5	+3	%
Gain Temperature Dependance				±5		ppm / °C
PGA2 Offset	GD_{OFF2}	Step = 0.2 V/V (see **Table 12, page 23**)	-1		+1	V/V
PGA3 Offset	GD_{OFF3}	Step = 1/12 V/V (see **Table 13, page 23**)	-63/12		+63/12	V/V
Offset Settings Precision (PGA2 or PGA3)		**Note 2**	-3	±0.5	+3	%
Offset Temperature Dependance				±5		ppm / °C
Input Impedance on PGA1 (see **section 11.1, page 47**)		Gain = 1. **Note 3**	1200	1350		kΩ
		Gain = 10. **Note 3**	250	300		kΩ
Input Impedance on PGA2,3		Gain = 1. **Note 3**	150	200		kΩ
Output RMS Noise per over-sample		PGA1. **Note 4**		205		µV
		PGA2. **Note 4**		340		µV
		PGA3. **Note 4**		365		µV

Table 4. ZoomingADC Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ADC STATIC PERFORMANCES						
Resolution (No Missing Codes)	n	**Note 5** **Note 6**	6		16	Bits
Gain Error		**Note 7**		±0.15		%
Offset Error		n = 16 bits. **Note 8**		±1		LSB
Integral Non-Linearity	INL	resolution n = 12 bits. **Note 9**		±0.6		LSB
		resolution n = 16 bits. **Note 9**		±1.5		LSB
Differential Non-Linearity	DNL	resolution n = 12 bits. **Note 10**		±0.5		LSB
		resolution n = 16 bits. **Note 10**		±0.5		LSB
Power Supply Rejection Ratio DC	PSRR	V_{BATT} = 5V +/- 0.3V. **Note 11**		78		dB
		V_{BATT} = 3V +/- 0.3V. **Note 11**		72		dB
ADC DYNAMIC PERFORMANCES						
Conversion Time	T_{CONV}	n = 12 bits. **Note 12**		133		fs cycles
		n = 16 bits. **Note 12**		517		fs cycles
Throughput Rate (Continuous Mode)	$1/T_{CONV}$	n = 12 bits, fs = 250 kHz		1.88		kSps
		n = 16 bits, fs = 250 kHz		0.483		kSps
PGA Stabilization Delay		**Note 13** (see **Table 12, page 23**)		OSR		fs cycles
ZADC ANALOG QUIESCENT CURRENT						
ADC Only Consumption	I_Q	V_{BATT} = 5.5V/3.3V		285/210		µA
PGA1 Consumption		V_{BATT} = 5.5V/3.3V		104/80		µA
PGA2 Consumption		V_{BATT} = 5.5V/3.3V		67/59		µA
PGA3 Consumption		V_{BATT} = 5.5V/3.3V		98/91		µA
ANALOG POWER DISSIPATION : All PGAs & ADC Active						
Normal Power Mode		V_{BATT} = 5.5V/3.3V. **Note 14**		4.0/2.0		mW
3/4 Power Reduction Mode		V_{BATT} = 5.5V/3.3V. **Note 15**		3.2/1.6		mW
1/2 Power Reduction Mode		V_{BATT} = 5.5V/3.3V. **Note 16**		2.4/1.1		mW
1/4 Power Reduction Mode		V_{BATT} = 5.5V/3.3V. **Note 17**		1.5/0.7		mW

(1) Gain defined as overall *PGA* gain *GDTOT* = *GD1* x *GD2* x *GD3*. Maximum input voltage is given by: $V_{IN,MAX} = \pm(V_{REF} / 2) (OSR / OSR+1)$.
(2) Offset due to tolerance on *GDoff2* or *GDoff3* setting. For small intrinsic offset, use only *ADC* and *PGA1*.
(3) Measured with block connected to inputs through *Amux* block. Normalized input sampling frequency for input impedance is f_S = 500 kHz (f_S max, worst case). This figure must be multiplied by 2 for f_S = 250 kHz, 4 for f_S = 125 kHz. Input impedance is proportional to $1/f_S$.
(4) Figure independent from gain and sampling frequency. fs. The effective output noise is reduced by the over-sampling ratio
(5) Resolution is given by n = 2 log2(*OSR*) + log2(N_{ELCONV}). *OSR* can be set between 8 and 1024, in powers of 2. N_{ELCONV} can be set to 1, 2, 4 or 8.
(6) If a ramp signal is applied to the input, all digital codes appear in the resulting *ADC* output data.
(7) Gain error is defined as the amount of deviation between the ideal (theoretical) transfer function and the measured transfer function (with the offset error removed).
(8) Offset error is defined as the output code error for a zero volt input (ideally, output code = 0). For 1 LSB offset, N_{ELCONV} must be at least 2.
(9) INL defined as the deviation of the DC transfer curve of each individual code from the best-fit straight line. This specification holds over the full scale.
(10) DNL is defined as the difference (in LSB) between the ideal (1 LSB) and measured code transitions for successive codes.
(11) Values for Gain = 1. PSRR is defined as the amount of change in the *ADC* output value as the power supply voltage changes.

(12) Conversion time is given by: $T_{CONV} = (N_{ELCONV}(OSR + 1) + 1) / fs$. *OSR* can be set between 8 and 1024, in powers of 2. N_{ELCONV} can be set to 1, 2, 4 or 8.

(13) PGAs are reset after each writing operation to registers **RegACCfg1-5**, corresponding to change of configuration or input switching. The *ADC* should be started only some delay after a change of PGA configuration through these registers. Delay between change of configuration of PGA or input channel switching and ADC start should be equivalent to OSR (between 8 and 1024) number of cycles. This is done by writing bit Start several cycles after *PGA* settings modification or channel switching. This delay does not apply to conversions made without the *PGAs*.

(14) Nominal (maximum) bias currents in *PGAs* and *ADC*, i.e. *IbAmpPga[1:0]* = '11' and *IbAmpAdc[1:0]* = '11'.

(15) Bias currents in *PGAs* and *ADC* set to 3/4 of nominal values, i.e. *IbAmpPga[1:0]* = '10', *IbAmpAdc[1:0]* = '10'.

(16) Bias currents in *PGAs* and *ADC* set to 1/2 of nominal values, i.e. *IbAmpPga[1:0]* = '01', *IbAmpAdc[1:0]* = '01'.

(17) Bias currents in *PGAs* and *ADC* set to 1/4 of nominal values, i.e. *IbAmpPga[1:0]* = '00', *IbAmpAdc[1:0]* = '00'.

2.1 Timing Characteristics

Table 5. General timings

Parameter	Symbol	Comment/Condition	Min	Typ	Max	Unit
ADC INTERRUPT (READY) TIMING SPECIFICATIONS						
READY pulse width	t_{IRQ}	**Note 1**		1		1/fs
STARTUP TIMES						
Startup sequence time at POR	t_{START}				800	µs
Time to enable RC from Sleep after an I2C command	t_{RCEN}				450	µs

(1) The READY pulse indicates End of Conversion. This is a Positive pulse of duration equal to one cycle of the ADC sampling rate in "continuous mode".

See also **Figure 17, page 33**.

2.1.1 POR Waveforms

At device power-on or after a software reset

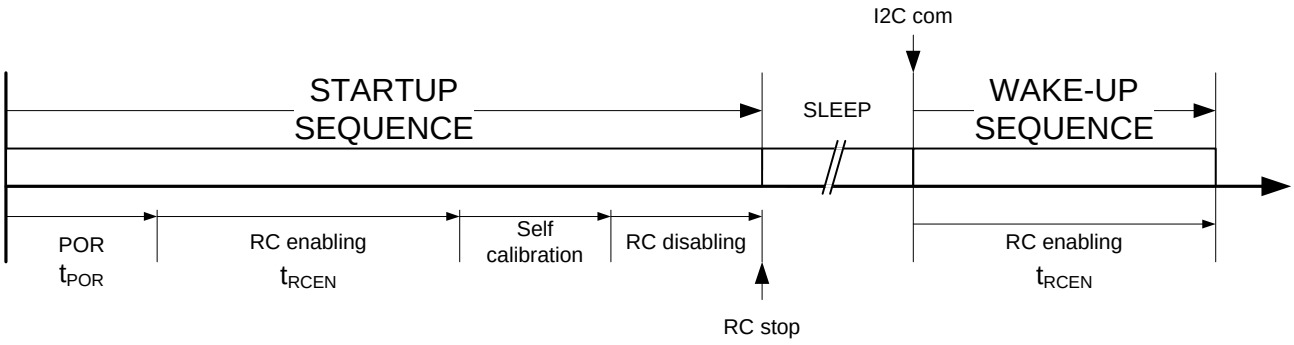


Figure 1. Power-On-Reset waveform

2.1.2 I2C interface timings

Table 6. Digital interface

Parameter	Symbol	STANDARD-MODE			FAST-MODE			Unit
		Min	Typ	Max	Min	Typ	Max	
I2C TIMING SPECIFICATIONS Note 1								
SCL clock frequency	f_{SCL}	0		100	0		400	kHz
SCL timeout (optional mode) **Note 2**	t_{SCLTO}	35			35			ms
SCL Low Pulsewidth	t_L	4.7			1.3			µs
SCL High Pulsewidth	t_H	4.0			0.6			µs
Start Condition Hold Time	t_{SCH}	0.6			0.6			µs
Data Setup Time	t_{DS}	250			100 **Note 3**			ns
Data Hold Time	t_{DH}	0 **Note 4**		3.45	0		0.9	µs
Setup Time for Repeated Start	t_{RSU}	4.7			0.6			µs
Stop Condition Setup Time	t_{PSU}	4.0			0.6			µs
Bus Free Time between a STOP Condition and a START Condition	t_{BF}	4.7			1.3			µs
Pulsewidth of Spike Suppressed	t_{SUP}		100			100		ns
Capacitive load for each bus line	C_B			400			400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{BATT}$			$0.1V_{BATT}$			V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{BATT}$			$0.2V_{BATT}$			V

(1) All timings specifications are referred to VILmin and VIHmax voltage levels defined for the SCL and SDA pins.
(2) The digital interface is reset if the SCL is low more than t_{SCLTO} duration. This is the default mode at startup. The timeout can be disabled by register setting.
(3) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system.
(4) The device internally provides a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(5) Cb = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according to Table 6 are allowed.

2.1.3 I2C timing Waveforms

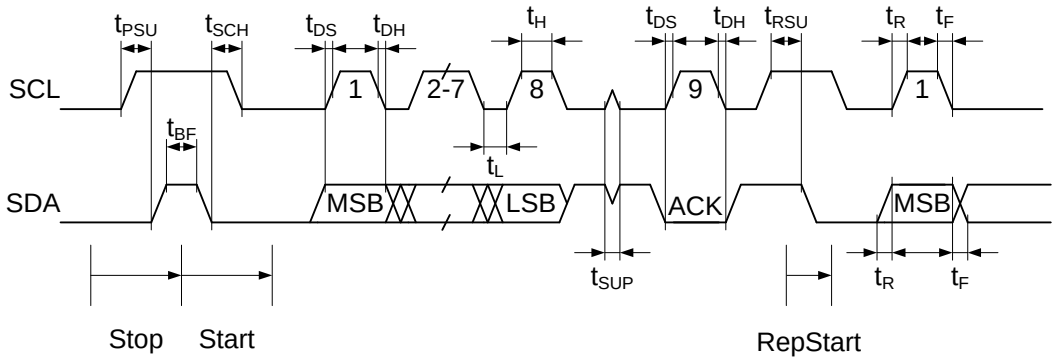
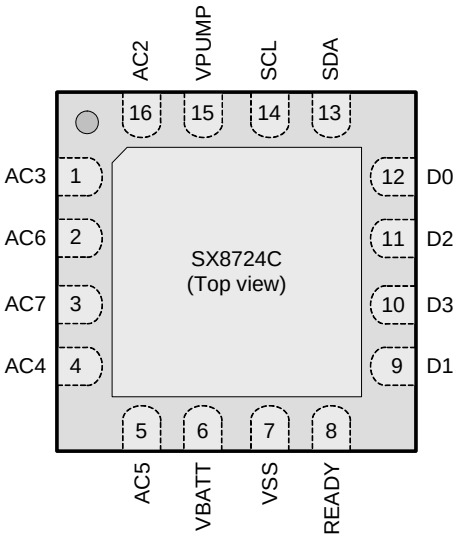
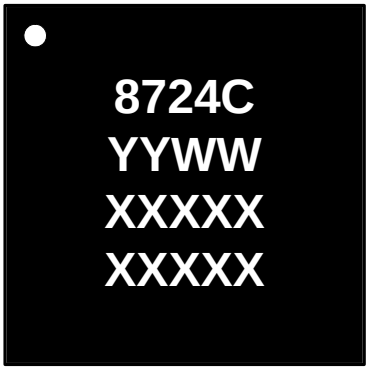


Figure 2. Definition of timing for F/S-mode on the I2C-bus.

3 Pin Configuration



4 Marking Information



nnnnn = Part Number
yyww = Date Code[1]
xxxxx = Semtech Lot Number
xxxxx

1.Date codes and Lot numbers starting with the 'E' character are used for Engineering samples

5 Pin Description

Note The bottom pin is internally connected to *VSS*. It should also be connected to *VSS* on PCB to reduce noise and improve thermal behavior.

Pin	Name	Type	Function
1	AC3	Analog Input	Differential sensor input in conjunction with AC2
2	AC6	Analog Input	Differential sensor input in conjunction with AC7
3	AC7	Analog Input	Differential sensor input in conjunction with AC6
4	AC4	Analog Input	Differential sensor input in conjunction with AC5
5	AC5	Analog Input	Differential sensor input in conjunction with AC4
6	VBATT	Power Input	2.4V to 5.5V power supply
7	VSS	Power Input	Chip ground
8	READY	Digital Output	Conversion complete flag.
9	D1	Digital IO + analog input	Digital output sensor drive (V_{BATT} or V_{SS})
			V_{REF} input in optional operating mode
			I2C address bit 1. Msb address bits are fuse programmed.
10	D3	Digital IO	Digital output sensor drive (V_{BATT} or V_{SS})
11	D2	Digital IO	Digital output sensor drive (V_{BATT} or V_{SS})
12	D0	Digital IO + analog output	Digital output sensor drive (V_{BATT} or V_{SS})
			V_{REF} output in optional operating mode
			I2C address bit 0. MSB address bits are fuse programmed.
13	SDA	Digital IO	I2C data line
14	SCL	Digital IO	I2C clock line. Up to 400 kHz.
15	VPUMP	Power IO	Charge pump output. Raises analog switch supply above V_{BATT} if V_{BATT} supply is too low. Recommended range for capacitor is 1nF to 10 nF. Connect the capacitor to ground.
16	AC2	Analog Input	Differential sensor input in conjunction with AC3

6 General Description

The SX8724C is a complete low-power acquisition path with programmable gain, acquisition speed and resolution.

6.1 Bloc diagram

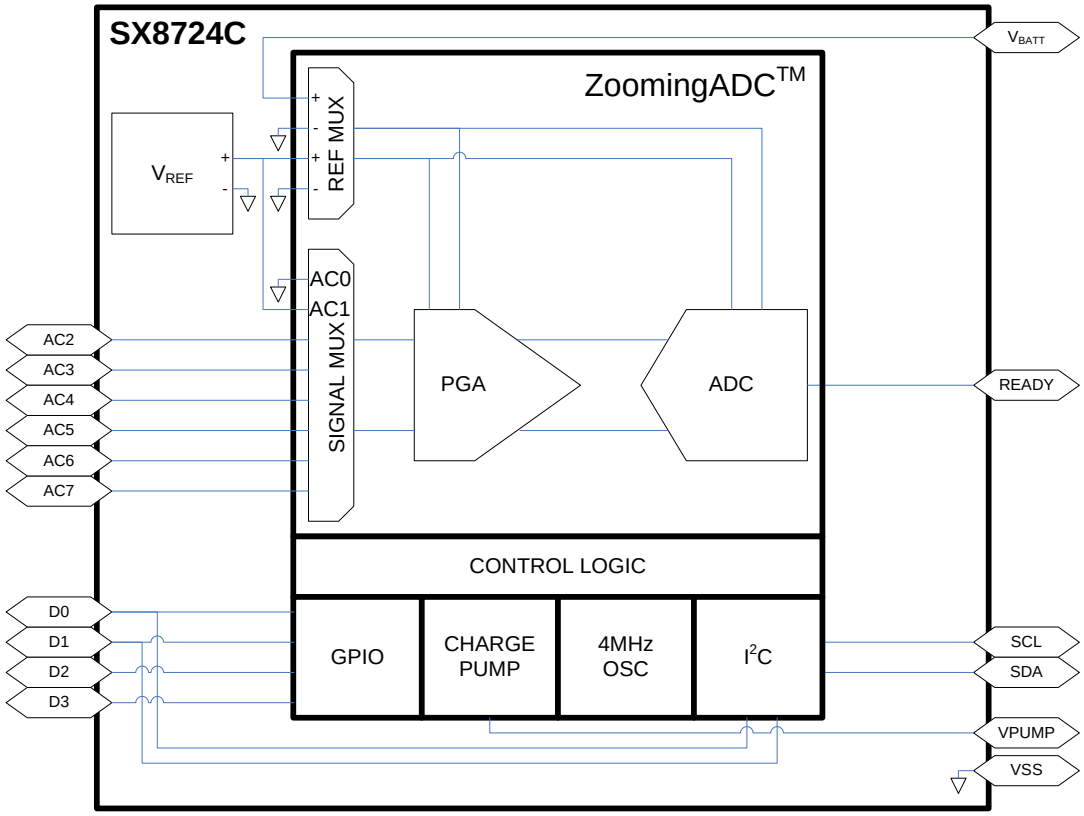


Figure 3. SX8724C bloc diagram

6.2 VREF

The internally generated *VREF* is a trimmed bandgap reference with a nominal value of 1.22V that provides a stable voltage reference for the *ZoomingADC*.

This reference voltage is directly connected to one of the ZoomingADC reference multiplexer inputs.

The bandgap voltage stability is only guaranteed for *VBATT* voltages of 3V and above. As *VBATT* drops down to 2.4V, the bandgap voltage could reduce by up to 50mV.

The bandgap has relatively weak output drive so it is recommended that if the bandgap is required as a signal input then *PGA1* must be enabled with gain = 1.

6.3 GPIO

The *GPIO* block is a multipurpose 4 bit input/output port. In addition to digital behavior, *D0* and *D1* pins can be programmed as analog pins in order to be used as output (reference voltage monitoring) and input for an external

reference voltage (For further details see **Figure 6**, **Figure 7**, **Figure 8** and **Figure 9**). Each port terminal can be individually selected as digital input or output.

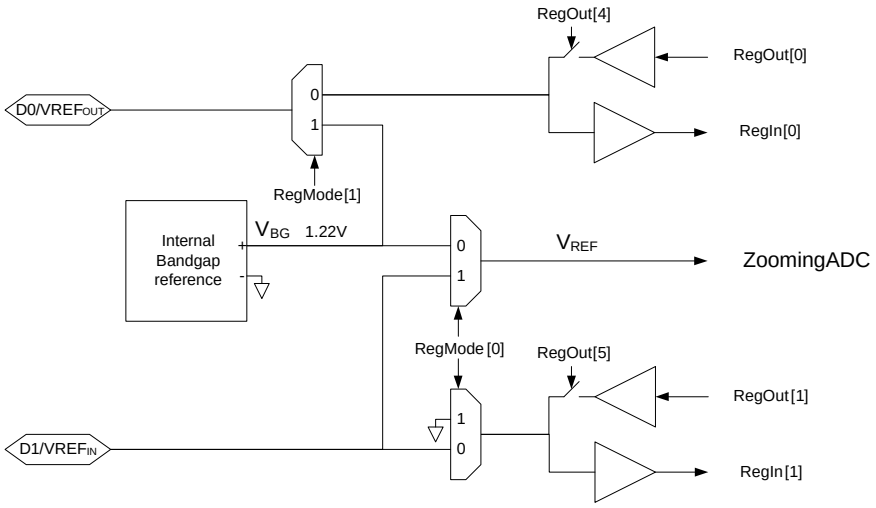


Figure 4. GPIO bloc diagram

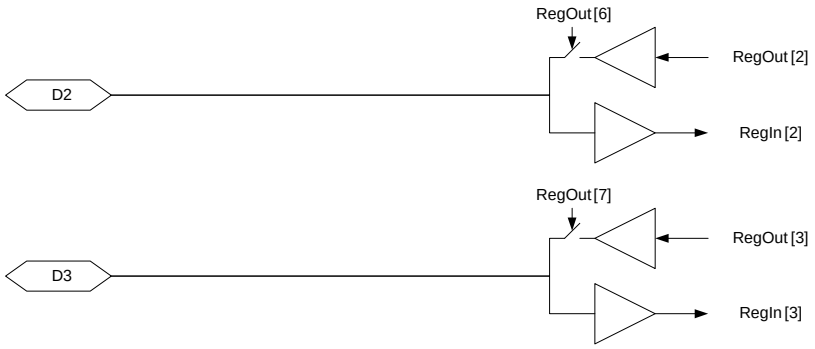


Figure 5. Digital IO bloc diagram

The direction of each bit within the *GPIO* block (input only or input/output) can be individually set using the bits of the **RegOut** (address 0x40) register. If *D[x]Dir* = 1, both the input and output buffer are active on the corresponding *GPIO* block pin. If *D[x]Dir*= 0, the corresponding *GPIO* block pin is an input only and the output buffer is in high impedance. After power on reset the GPIO block pins are in input/output mode (*D[x]Dir* are reset to 1).

The input values of *GPIO* block are available in **RegIn** (address 0x41) register (read only). Reading is always direct - there is no debounce function in the *GPIO* block. In case of possible noise on input signals, an external hardware filter has to be realized. The input buffer is also active when the *GPIO* block is defined as output and the effective value on the pin can be read back.

Data stored in the LSB bits of **RegOut** register are outputted at *GPIO* block if *D[x]Dir= 1*. The default values after power on reset is low (0).
The digital pins are able to deliver a driving current up to 8 mA.

When the bits *VrefD0Out* and *VrefD1In* in the **RegMode** (address 0x70) register are set to 1 the *D0* and *D1* pins digital behavior are automatically bypassed in order to either input or output the voltage reference signals.

6.3.1 Optional Operating Mode: External Vref

D0 and *D1* are multi-functional pins with the following functions in different operating modes (see **RegMode** register for control settings):

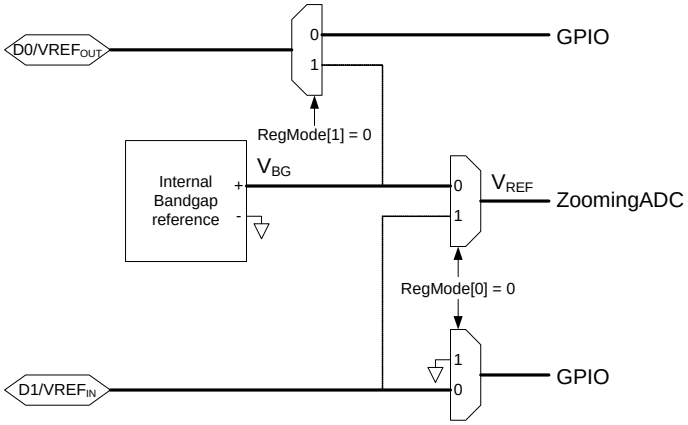


Figure 6. D0 and D1 are Digital Inputs / Outputs

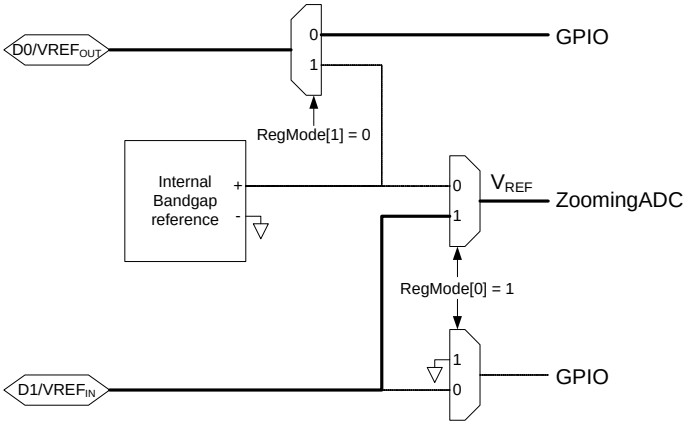


Figure 7. D1 is Reference Voltage Input and D0 is Digital Input / Output

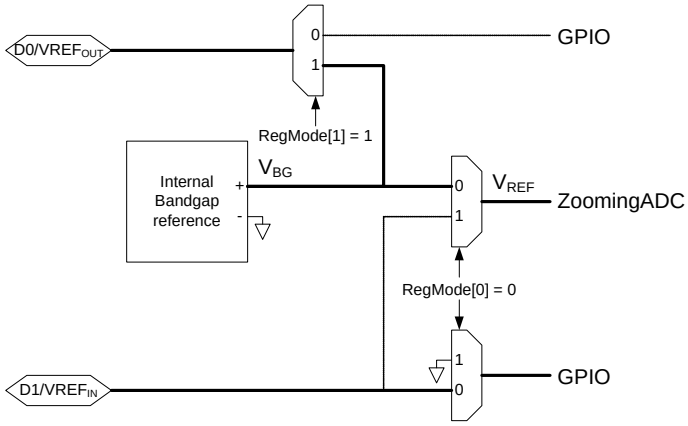


Figure 8. D1 is Digital Input / Output and D0 Reference Voltage Output

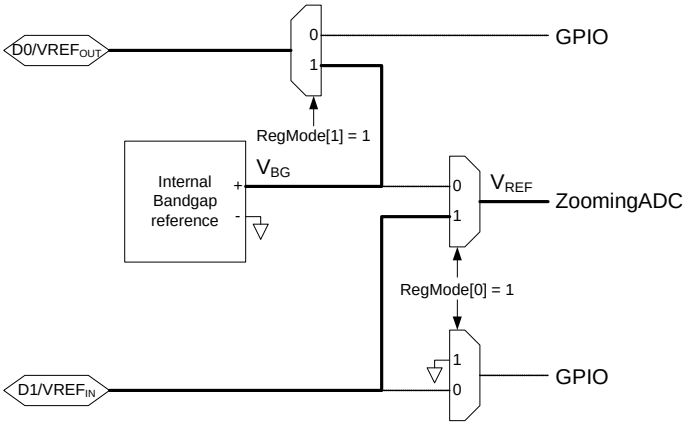


Figure 9. D0 is Reference Voltage Output and D1 is Reference Voltage Input

This allows external monitoring of the internal bandgap reference or the ability to use an external reference input for the *ADC*, or the option to filter the internal V_{REF} output before feeding back as $V_{REF,ADC}$ input. The internally generated V_{REF} is a trimmed as ADC reference with a nominal value of 1.22V. When using an external $V_{REF,ADC}$ input, it may have any value between 0V and V_{BATT}. Simply substitute the external value for 1.22 V in the *ADC* conversion calculations.

6.4 Charge Pump

This block generates a supply voltage able to power the analog switch drive levels on the chip higher than VBATT if necessary.

If *VBATT* voltage drops below 4.2V then the block should be activated. If *VBATT* voltage is greater than 4.2V then *VBATT* may be switched straight through to the *VPUMP* output. If the charge pump is not activated then *VPUMP* = *VBATT.*

If control input bit *MultForceOff* = 1 in **RegMode** (address 0x70) register then the charge pump is disabled and *VBATT* is permanently connected to *VPUMP* output.

If control input bit *MultForceOn* = 1 in **RegMode** register then the charge pump is permanently enabled. This overrides *MultForceOff* bit in **RegMode** register.

An external capacitor is required on *VPUMP* pin. This capacitor should be large enough to ensure that generated voltage is smooth enough to avoid affecting conversion accuracy but not so large that it gives an unacceptable settling time. A recommended value is around 2.2nF.

6.5 RC Oscillator

This block provides the master clock reference for the chip. It produces a clock at 4 MHz which is divided internally in order to generate the clock sources needed by the other blocks.

The oscillator technique is a low power relaxation design and it is designed to vary as little as possible over temperature and supply voltage.

This oscillator is trimmed at manufacture chip test.

The *RC* oscillator will start up after a chip reset to allow the trimming values to be read and calibration registers and I2C address set to their default fused values. Once this has been done, the oscillator will be shut down and the chip will enter a sleep state while waiting for an I2C communication.

The worst case duration from reset (or POR) to the sleep state is 800us.

6.5.1 Wake-up from sleep

When the device is in sleep state, the *RC* oscillator will start up after a communication. The start up sequence for the *RC* oscillator is 450us in worst case.
During this time, the internal blocs using the RC can not be used: no ADC conversion can be started.

7 ZoomingADC

7.1 Overview

The *ZoomingADC* is a complete and versatile low-power analog front-end interface typically intended for sensing applications. In the following text the *ZoomingADC* will be referred as *ZADC*.

The key features of the *ZADC* are:

- Programmable 6 to 16-bit dynamic range over-sampled *ADC*
- Flexible gain programming between 1/12 and 1000
- Flexible and large range offset compensation
- Differential or single-ended input
- 2-channel differential reference inputs
- Power saving modes

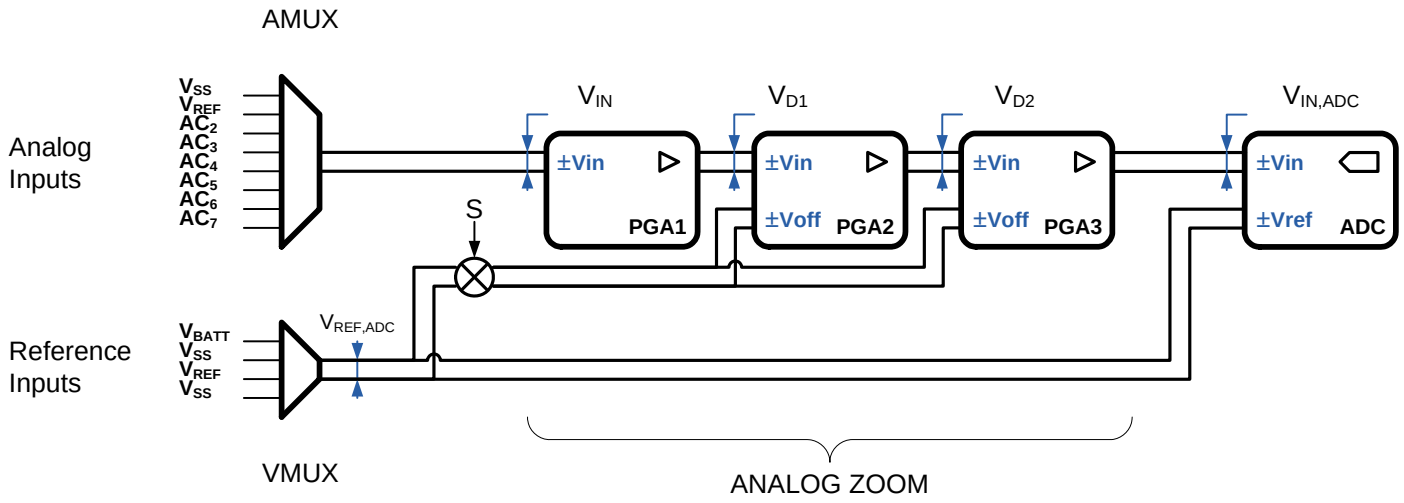


Figure 10. ZADC General Functional Block Diagram

The total acquisition chain consists of an input multiplexer, 3 programmable gain amplifier stages and an over sampled A/D converter. The reference voltage can be selected on two different channels. Two offset compensation amplifiers allow for a wide offset compensation range. The programmable gain and offset allow the application to zoom in on a small portion of the reference voltage defined input range.

7.1.1 Acquisition Chain

Figure 10, page 18 shows the general block diagram of the acquisition chain (*AC*). A control block (not shown in **Figure 10**) manages all communications with the I2C peripheral. The clocking is derived from the internal 4 MHz Oscillator.

Analog inputs can be selected through an 8 input multiplexer, while reference input is selected between two differential channels. It should however be noted that only 7 acquisition channels (including the VREF) are available when configured as single ended since the input amplifier is always operating in differential mode with both positive and negative input selected through the multiplexer.

The core of the zooming section is made of three differential programmable amplifiers (*PGA*). After selection of an input and reference signals VIN and VREF,ADC combination, the input voltage is modulated and amplified through stages 1 to 3. Fine gain programming up to 1'000 V/V is possible. In addition, the last two stages provide programmable offset. Each amplifier can be bypassed if needed.

The output of the cascade of *PGA* is directly fed to the analog-to-digital converter (*ADC*), which converts the signal VIN,ADC into digital.

Like most *ADCs* intended for instrumentation or sensing applications, the ZoomingADC™ is an over-sampled converter [1]. The *ADC* is a so-called incremental converter; with bipolar operation (the *ADC* accepts both positive and negative differential input voltages). In first approximation, the *ADC* output result relative to full-scale (*FS*) delivers the quantity:

$$\frac{OUT_{ADC}}{FS/2} \cong \frac{V_{IN,ADC}}{V_{REF}/2}$$

Equation 1

in two's complement (see **Equation 18** and **Equation 19, page 33** for details). The output code OUTADC is -*FS* / 2 to + *FS* / 2 for VIN,ADC = -VREF,ADC / 2 to + VREF,ADC / 2 respectively. As will be shown, VIN,ADC is related to input voltage VIN by the relationship:

$$V_{IN,ADC} = GD_{TOT} \cdot V_{IN} - GDoff_{TOT} \cdot S \cdot V_{REF} \quad [V]$$

Equation 2

where *GDTOT* is the total *PGA* gain, *GDOFFTOT* is the total magnitude of *PGA* offset and S is the sign of the offset (see **Table 9, page 21**).

7.1.2 Programmable Gain Amplifiers

As seen in **Figure 10, page 18**, the zooming function is implemented with three programmable gain amplifiers (*PGA*). These are:

- *PGA1*: coarse gain tuning
- *PGA2*: medium gain and offset tuning
- *PGA3*: fine gain and offset tuning. Should be set ON for high linearity data acquisition

All gain and offset settings are realized with ratios of capacitors. The user has control over each *PGA* activation and gain, as well as the offset of stages 2 and 3. These functions are examined hereafter.

1. Over-sampled converters are operated with a sampling frequency *fs* much higher than the input signal's Nyquist rate (typically *fs* is 20-1'000 times the input signal bandwidth). The sampling frequency to throughput ratio is large (typically 10-500). These converters include digital decimation filtering. They are mainly used for high resolution, and/or low-to-medium speed applications.

7.1.3 PGA & ADC Enabling

Depending on the application objectives, the user may enable or bypass each *PGA* stage. This is done according to the word *Enable* and the coding given in **Table 7**. To reduce power dissipation, the *ADC* can also be inactivated while idle.

Table 7. ADC and PGA Enabling

Enable (RegACCfg1[3:0])	Block
XXX0 XXX1	ADC disabled ADC enabled
XX0X XX1X	PGA1 disabled PGA1 enabled
X0XX X1XX	PGA2 disabled PGA2 enabled
0XXX 1XXX	PGA3 disabled PGA3 enabled

7.2 ZoomingADC Registers

The system has a bank of eight 8-bit registers: six registers are used to configure the acquisition chain (**RegAcCfg0** to **RegAcCfg5**), and two registers are used to store the output code of the analog-to-digital conversion (**RegAcOutMsb** & **Lsb**).

Table 8. Periferal Registers to Configure the Acquisition Chain (AC) and to Store the Analog-to-Digital Conversion (ADC) Result

Register Name	Bit position							
	7	6	5	4	3	2	1	0
RegACOutLsb	Out[7:0] Note 1							
RegACOutMsb	Out[15:8]							
RegACCfg0 Default values:	Start 0, Note 2	SetNelconv 01, Note 3		SetOsr 010, Note 4			Continuous 0, Note 5	- 0, Note 6
RegACCfg1 Default value:	IbAmpAdc 11, Note 7		IbAmpPga 11, Note 8		Enable 0000, Note 9			
RegACCfg2 Default value:	SetFs 00, Note 10		Pga2Gain 00, Note 12		Pga2Offset 0000, Note 14			
RegACCfg3 Default value:	Pga1Gain 0, Note 11	Pga3Gain 0001100, Note 13						
RegACCfg4 Default value:	- 0	Pga3Offset 0000000, Note 15						
RegACCfg5 Default value:	Busy 0, Note 16	Def 0, Note 17	Amux 00000, Note 18					Vmux 0, Note 19

(r = read; w = write; rw = read & write)

(1) **Out**: (r) digital output code of the analog-to-digital converter. (*MSB = Out[15]*)
(2) **Start**: (w) setting this bit triggers a single conversion (after the current one is finished). This bit always reads back 0.

(3) **SetNelconv**: (rw) sets the number of elementary conversions to $2^{(SetNelconv[1:0])}$. To compensate for offsets, the input signal is chopped between elementary conversions (1,2,4,8).
(4) **SetOsr**: (rw) sets the over-sampling rate (*OSR*) of an elementary conversion to $2^{(3+SetOsr[2:0])}$. *OSR* = 8, 16, 32, ..., 512, 1024.
(5) **Continuous**: (rw) setting this bit starts a conversion. When this bis is 1, A new conversion will automatically begin directly when the previous one is finished.
(6) Reserved
(7) **IbAmpAdc**: (rw) sets the bias current in the *ADC* to 0.25 x (1+ *IbAmpAdc[1:0]*) of the normal operation current (25, 50, 75 or 100% of nominal current). To be used for low-power, low-speed operation.
(8) **IbAmpPga**: (rw) sets the bias current in the PGAs to 0.25 x (1+*IbAmpPga[1:0]*) of the normal operation current (25, 50, 75 or 100% of nominal current). To be used for low-power, low-speed operation.
(9) **Enable**: (rw) enables the *ADC* modulator (bit 0) and the different stages of the *PGAs* (*PGAi* by bit i=1,2,3). *PGA* stages that are disabled are bypassed.
(10) **SetFs**: (rw) These bits set the over sampling frequency of the acquisition chain. Expressed as a fraction of the oscillator frequency, the sampling frequency is given as: 11 ' 500 kHz, 10 ' 250 kHz, 01 ' 125 kHz, 00 ' 62.5 kHz.
(11) **Pga1Gain**: (rw) sets the gain of the first stage: 0 ' 1, 1 ' 10.
(12) **Pga2Gain**: (rw) sets the gain of the second stage: 00 ' 1, 01 ' 2, 10 ' 5, 11 ' 10.
(13) **Pga3Gain**: (rw) sets the gain of the third stage to *Pga3Gain[6:0]* 1/12.
(14) **Pga2Offset**: (rw) sets the offset of the second stage between -1 and +1, with increments of 0.2. The *MSB* gives the sign (0 positive, 1 negative); amplitude is coded with the bits *Pga2Offset[5:0]*.
(15) **Pga3Offset**: (rw) sets the offset of the third stage between -5.25 and +5.25, with increments of 1/12. The *MSB* gives the sign (0 positive, 1 negative); amplitude is coded with the bits *Pga3Offset[5:0]*.
(16) **Busy**: (r) set to 1 if a conversion is running.
(17) **Def**: (w) sets all values to their defaults (*PGA* disabled, max speed, nominal modulator bias current, 2 elementary conversions, over-sampling rate of 32) and starts a new conversion without waiting the end of the preceding one.
(18) **Amux**(4:0): (rw) *Amux[4]* sets the mode (0 ' differential inputs, 1 ' single ended inputs with A0= common reference) *Amux[3]* sets the sign (0 ' straight, 1' cross) *Amux[2:0]* sets the channel.
(19) **Vmux**: (rw) sets the differential reference channel (0 ' V_{BATT}, 1 ' V_{REF}).

7.3 Input Multiplexers (AMUX and VMUX)

The ZoomingADC has analog inputs *AC0* to *AC7* and reference inputs. Let us first define the differential input voltage V_{IN} and reference voltage $V_{REF,ADC}$ respectively as:

$$V_{IN} = V_{INP} - V_{INN} \quad [V]$$

Equation 3

$$V_{REF} = V_{REFP} - V_{REFN} \quad [V]$$

Equation 4

As shown in **Table 9**, the inputs can be configured in two ways: either as 4 differential channels (V_{IN1}= *AC1 - AC0*,... , V_{IN4} = *AC7 - AC6*), or *AC0* can be used as a common reference, providing 7 signal paths all referred to *AC0*. The control word for the analog input selection is *Amux*. Notice that the *Amux* bit 4 controls the sign of the input voltage.

Table 9. Analog Input Selection

Amux (RegACCfg5[5:1])	VINP	VINN
Sign S = 1		
00x00	AC1(VREF)	AC0(VSS)

Amux (RegACCfg5[5:1])	VINP	VINN
Sign S = -1		
01x00	AC1(VSS)	AC0(VREF)

Table 9. Analog Input Selection

Amux (RegACCfg5[5:1])	VINP	VINN	Amux (RegACCfg5[5:1])	VINP	VINN
Sign S = 1			**Sign S = -1**		
00x01	AC3	AC2	01x01	AC2	AC3
00x10	AC5	AC4	01x10	AC4	AC5
00x11	AC7	AC6	01x11	AC6	AC7
10000	AC0(VSS)	AC0(VSS)	11000	AC0(VSS)	AC0(VSS)
10001	AC1(VREF)		11001		AC1(VREF)
10010	AC2		11010		AC2
10011	AC3		11011		AC3
10100	AC4		11100		AC4
10101	AC5		11101		AC5
10110	AC6		11110		AC6
10111	AC7		11111		AC7

Similarly, the reference voltage is chosen among two differential channels (*VREF = VBATT-VSS*, *VREF = VBG-VSS* or *VREF = VREF,IN-VSS*) as shown in **Table 10**. The selection bit is *Vmux*. The reference inputs *VREFP* and *VREFN* (common-mode) can be up to the power supply range.

Table 10. Analog reference Input Selection

Vmux (RegACCfg5[0])	VREFP	VREFN
0	VREF = VBATT	VSS
1	VREF = VBG or VREF,IN[1]	VSS

1. External voltage reference on D1 GPIO pin. See **section 6.3 on page 14** about GPIO and "RegMode[0x70]" on page 46.

7.4 First Stage Programmable Gain Amplifier (PGA1)

The first stage can have a buffer function (unity gain) or provide a gain of 10 (see **Table 11**). The voltage *VD1* at the output of *PGA1* is:

$$V_{D1} = GD_1 \cdot V_{IN} \qquad [V]$$

Equation 5

where *GD1* is the gain of *PGA1* (in V/V) controlled with the *Pga1Gain* bit.

Table 11. PGA1 gain settings

Pga1Gain bit (RegACCfg3[7])	PGA1 gain [V/V] *GD1* [V/V]
0	1
1	10

7.5 Second Stage Programmable Gain Amplifier (PGA2)

The second *PGA* has a finer gain and offset tuning capability, as shown in **Table 12**. The *VD2* voltage at the output of *PGA2* is given by:

$$V_{D2} = GD_2 \cdot V_{D1} - GDoff_2 \cdot S \cdot V_{REF} \quad [V]$$

Equation 6

where *GD2* and *GDOFF2* are respectively the gain and offset of *PGA2* (in V/V). These are controlled with the words *Pga2Gain[1:0]* and *Pga2Offset[3:0]*.

Table 12. PGA2 gain and offset settings

Pga2Gain bitfield (RegACCfg2[5:4])	PGA2 gain [V/V] *GD2* [V/V]
00	1
01	2
10	5
11	10

Pga2Offset bitfield (RegACCfg2[3:0])	PGA2 offset *GDOFF2* [V/V]
0000	0
0001	+0.2
0010	+0.4
0011	+0.6
0100	+0.8
0101	+1
1000	0
1001	-0.2
1010	-0.4
1011	-0.6
1100	-0.8
1101	-1.0

7.6 Third Stage Programmable Gain Amplifier (PGA3)

The finest gain and offset tuning is performed with the third and last *PGA* stage, according to the coding of **Table 13**.

Table 13. PGA3 Gain and Offset Settings

Pga3Gain bitfield (RegACCfg3[6:0])	PGA3 Gain *GD3* [V/V]
0000000	0
0000001	1/12 (=0.083)
...	...
0000110	6/12
...	...
0001100	12/12
0010000	16/12
...	...
0100000	32/12

Pga3Offset bitfield (RegACCfg4[6:0])	PGA3 Offset *GDOFF3* [V/V]
0000000	0
0000001	+1/12 (=0.083)
...	
0010000	+16/12
...	...
0100000	32/12
...	...
0111111	+63/12 (=+5.25)
1000000	0

Table 13. PGA3 Gain and Offset Settings

Pga3Gain bitfield (RegACCfg3[6:0])	PGA3 Gain GD_3 [V/V]
...	...
1000000	64/12
...	...
1111111	127/12 (=10.58)

Pga3Offset bitfield (RegACCfg4[6:0])	PGA3 Offset $GDOFF_3$ [V/V]
1000001	-1/12 (=-0.083)
1000010	-2/12
...	...
1010000	-16/12
...	...
1100000	-32/12
...	...
1111111	-63/12 (=-5.25)

The output of *PGA3* is also the input of the *ADC*. Thus, similarly to *PGA2*, we find that the voltage entering the *ADC* is given by:

$$V_{IN,ADC} = GD_3 \cdot V_{D2} - GDoff_3 \cdot S \cdot V_{REF} \quad [V]$$

Equation 7

where GD_3 and $GDOFF_3$ are respectively the gain and offset of *PGA3* (in V/V). The control words are *Pga3Gain[6:0]* and *Pga3Offset[6:0]*.

To remain within the signal compliance of the *PGA* stages (no saturation), the condition:

$$|V_{IN}|, |V_{D1}|, |V_{D2}| < \frac{V_{BATT}}{2}$$

Equation 8

must be verified.
To remain within the signal compliance of the *ADC* (no saturation), the condition:

$$|V_{IN,ADC}| < \left(\frac{V_{REF}}{2}\right)\left(\frac{OSR-1}{OSR}\right)$$

Equation 9

must be verified.

Finally, combining **Equation 5** to **Equation 7** for the three *PGA* stages, the input voltage *VIN,ADC* of the *ADC* is related to *VIN* by:

$$V_{IN,ADC} = GD_{TOT} \cdot V_{IN} - GDoff_{TOT} \cdot S \cdot V_{REF} \quad [V]$$

Equation 10

where the total *PGA* gain is defined as:

$$GD_{TOT} = GD_3 \cdot GD_2 \cdot GD_1$$

Equation 11

and the total *PGA* offset is:

$$GDoff_{TOT} = GDoff_3 + GD_3 \cdot GDoff_2$$

Equation 12

7.6.1 PGA Ranges

Figure 11 and **Figure 12** illustrates the limits for the maximal conversion precision according to the common mode voltage (VCOMMON), the ADC over-sampling frequency (fs) and PGA gains. The best linearity performances can be

obtained only below these limits, as depicted in **Figure 11** if the supply voltage (V_{BATT}) is below 4.2V and as depicted in **Figure 12** if the supply voltage (V_{BATT}) is above 4.2V.

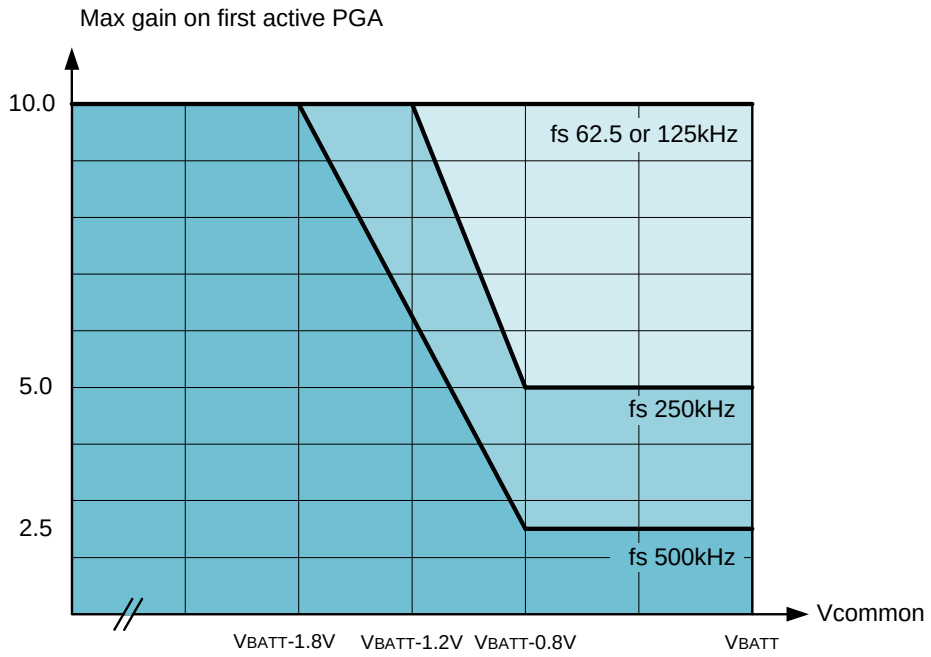


Figure 11. Common mode input range on PGA for V_{BATT} below 4.2V

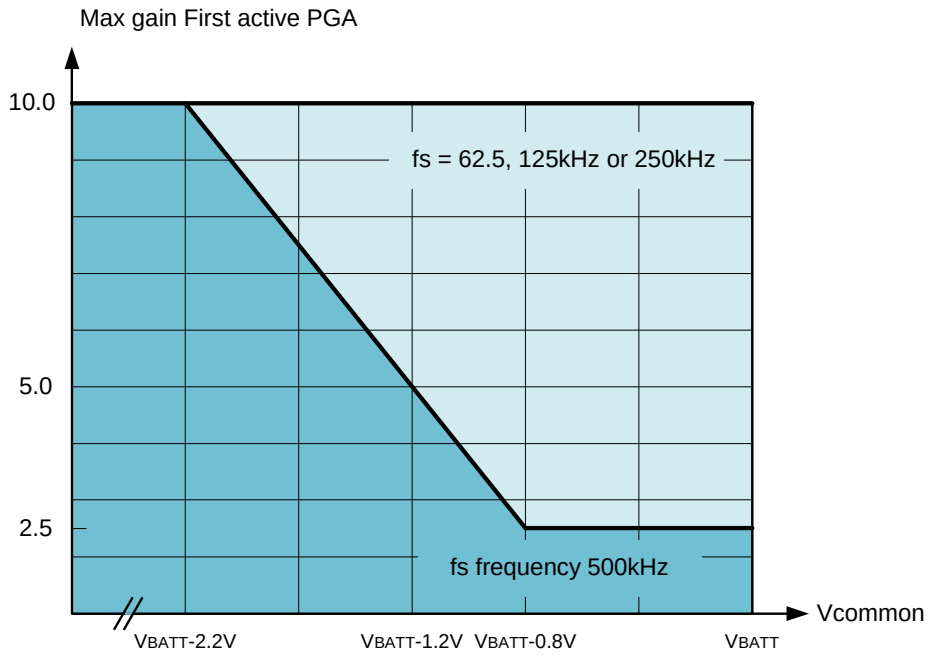


Figure 12. Common mode input range on PGA for VBATT above 4.2V

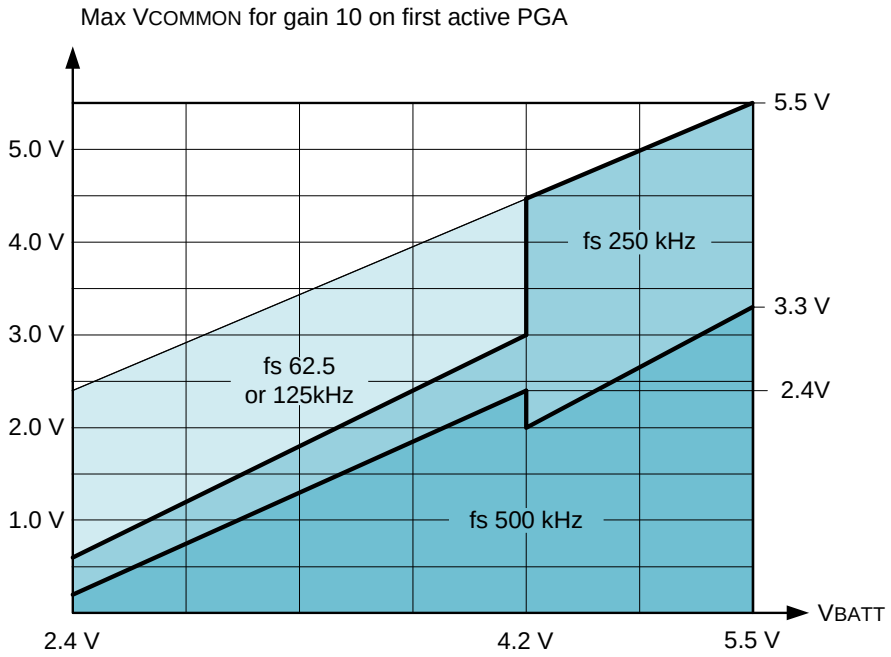


Figure 13. Common mode input range on PGA vs VBATT

7.7 Analog-to-Digital Converter (ADC)

The main performance characteristics of the *ADC* (resolution, conversion time, etc.) are determined by three programmable parameters. The setting of these parameters and the resulting performances are described later.

- *fs* : Over-sampling frequency
- *OSR* : Over-Sampling Ratio
- *NELCONV* : Number of Elementary Conversions

7.7.1 Conversion Sequence

A conversion is started each time the bit *Start* or the *Def* bit is set. As depicted in **Figure 14**, a complete analog-to-digital conversion sequence is made of a set of *NELCONV* elementary incremental conversions and a final quantization step. Each elementary conversion is made of (*OSR*+1) over-sampling periods *Ts*=1/*fs*, i.e.:

$$T_{ELCONV} = (OSR+1) / f_S \quad [s]$$

Equation 13

The result is the mean of the elementary conversion results. An important feature is that the elementary conversions are alternatively performed with the offset of the internal amplifiers contributing in one direction and the other to the output code. Thus, converter internal offset is eliminated if at least two elementary sequences are performed (i.e. if *NELCONV* >= 2). A few additional clock cycles are also required to initiate and end the conversion properly.

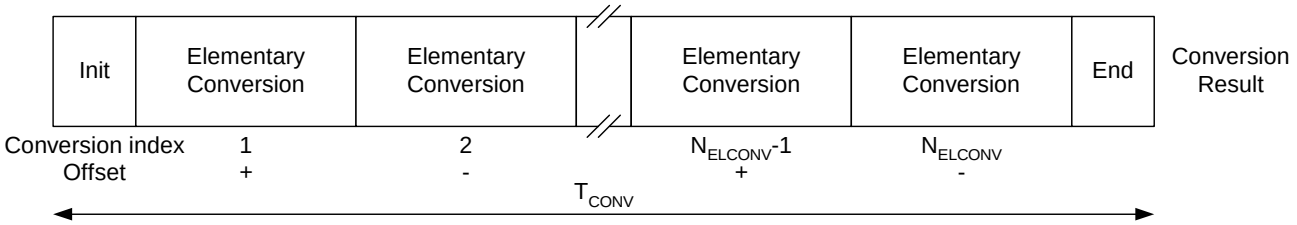


Figure 14. Analog-to-Digital Conversion Sequence

Note	The internal bandgap reference state may be forced High or Low, or may be set to toggle during conversion at either the same rate or half the rate of the Elementary Conversion. This may be useful to help eliminate bandgap related internal offset voltage and 1/*fs* noise.

7.7.2 Over-Sampling Frequency (fs)

The word *SetFs[1:0]* (see **Table 14**) is used to select the over-sampling frequency *fs*. The over-sampling frequency is derived from the 4MHz oscillator clock.

Table 14. Sampling frequency settings

SetFs bitfield (RegACCfg2[7:6])	Over-Sampling Frequency fs [Hz]
00	62.5 kHz
01	125 kHz
10	250 kHz
11	500 kHz

7.7.3 Over-Sampling Ratio (OSR)

The over-sampling ratio (*OSR*) defines the number of integration cycles per elementary conversion. Its value is set with the word *SetOsr[2:0]* in power of 2 steps (see **Table 15**) given by:

$$OSR = 2^{3+\text{SetOsr}[2:0]} \quad [-]$$

Equation 14

Table 15. Over-sampling ratio settings

SetOsr[2:0] (RegACCfg[4:2])	Over-Sampling Ratio OSR [-]
000	8
001	16
010	32
011	64
100	128
101	256
110	512
111	1024

7.7.4 Number of Elementary Conversions (Nelconv)

As mentioned previously, the whole conversion sequence is made of a set of *NELCONV* elementary incremental conversions. This number is set with the word *SetNelconv[1:0]* in power of 2 steps (see **Table 16**) given by:

$$N_{ELCONV} = 2^{\text{SetNelconv}[1:0]} \quad [-]$$

Equation 15

Table 16. Number of elementary conversion

SetOsr[2:0] (RegACCfg[4:2])	# of Elementary Conversion NELCONV [-]
00	1
01	2
10	4
11	8

As already mentioned, *NELCONV* must be equal or greater than 2 to reduce internal amplifier offsets.

7.7.5 Resolution

The theoretical resolution of the *ADC*, without considering thermal noise, is given by:

$$n = 2 \cdot \log_2(OSR) + \log_2(N_{ELCONV}) \quad [bit]$$

Equation 16

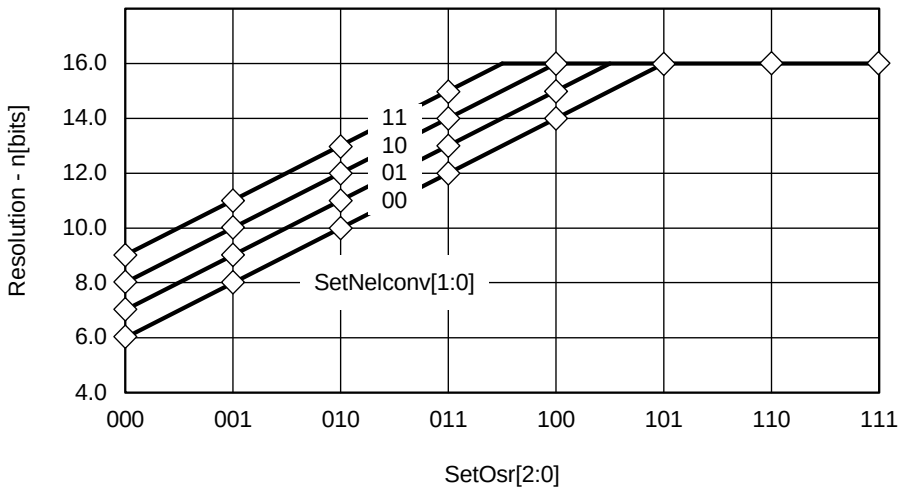


Figure 15. Resolution vs. SetOsr[2:0] and SetNelconv[2:0]

Using look-up **Table 17** or the graph plotted in **Figure 15**, resolution can be set between 6 and 16 bits. Notice that, because of 16-bit register use for the *ADC* output, **practical resolution is limited to 16 bits**, i.e. n = 16. Even if the

resolution is truncated to 16 bit by the output register size, it may make sense to set *OSR* and N_{ELCONV} to higher values in order to reduce the influence of the thermal noise in the PGA .

Table 17. Resolution[1] vs. SetOsr and SetNelconv settings

SetOsr control bits	SetNelconv control bits			
	'00'	**'01'**	**'10'**	**'11'**
'000'	6	7	8	9
'001'	8	9	10	11
'010'	10	11	12	13
'011'	12	13	14	15
'100'	14	15	16	16
'101'	16	16	16	16
'110'	16	16	16	16
'111'	16	16	16	16

1. In shaded area, the resolution is truncated to 16 bits due to output register size **RegACOut[15:0]**

7.7.6 Conversion Time & Throughput

As explained in **Figure 15**, conversion time is given by:

$$T_{CONV} = (N_{ELCONV} \cdot (OSR+1)+1) / f_S \quad [s]$$

Equation 17

and throughput is then simply $1/T_{CONV}$. For example, consider an over-sampling ratio of 256, 2 elementary conversions, and a sampling frequency of 500 kHz (*SetOsr* = "101", *SetNelconv* = "01" and *SetFs* = "00"). In this case, using **Table 18**, the conversion time is 515 sampling periods, or 1.03ms. This corresponds to a throughput of 971Hz in continuous-time mode. The plot of **Figure 16** illustrates the classic trade-off between resolution and conversion time.

Table 18. Normalized conversion time (Tconv x fs) vs. SetOsr and SetNelconv settings[1]

SetOsr bits OSR	SetNelconv control bits NELCONV			
	'00' 1	**'01' 2**	**'10' 4**	**'11' 8**
'000'	10	19	37	73
'001'	18	35	69	137
'010'	34	67	133	265
'011'	66	131	261	521

Table 18. Normalized conversion time (Tconv x fs) vs. SetOsr and SetNelconv settings[1]

SetOsr bits OSR	SetNelconv control bits NELCONV			
	'00' 1	'01' 2	'10' 4	'11' 8
'100'	130	259	517	1033
'101'	258	515	1029	2057
'110'	514	1027	2053	4105
'111'	1026	2051	4101	8201

1. *Normalized to sampling period 1/fs*

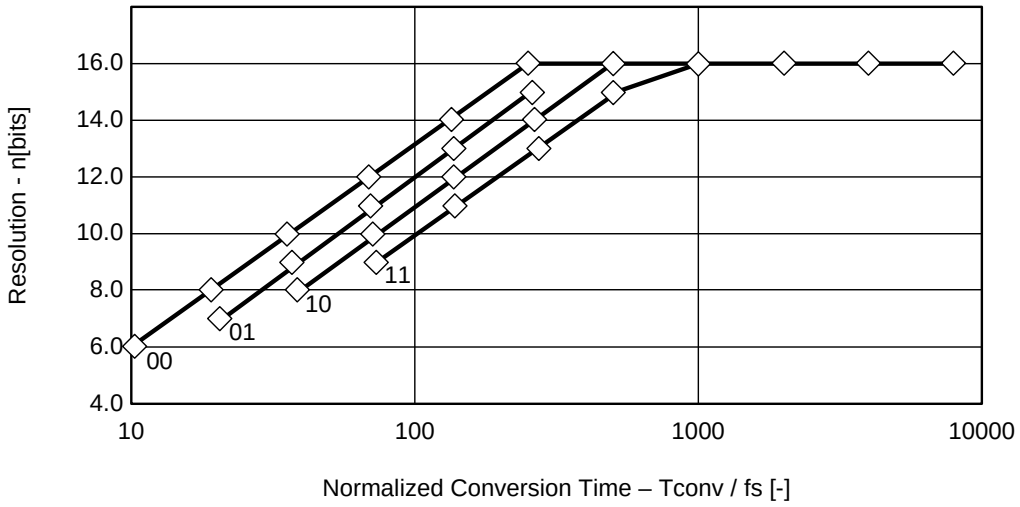


Figure 16. Resolution vs. normalized[1] conversion time for different SetNelconv[1:0]

1. Normalized Conversion Time - TCONV/fs

7.7.7 Continuous-Time vs. On-Request Conversion

The *ADC* can be operated in two distinct modes: "continuous-time" and "on-request" modes (selected using the bit *Continuous*).

In "continuous-time" mode, the input signal is repeatedly converted into digital. After a conversion is finished, a new one is automatically initiated. The new value is then written in the result register, and the corresponding internal trigger pulse is generated. This operation is sketched in **Figure 17**. The conversion time in this case is defined as *TCONV*.

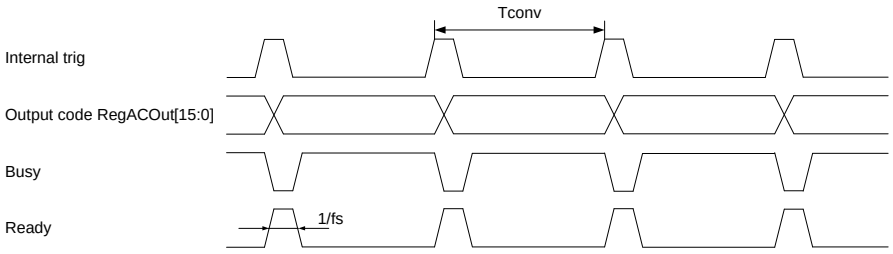


Figure 17. ADC "Continuous-Time" Operation

In the "on-request" mode, the internal behavior of the converter is the same as in the "continuous-time" mode, but the conversion is initiated on user request (with the *Start* bit). As shown in **Figure 18**, the conversion time is also *TCONV*.

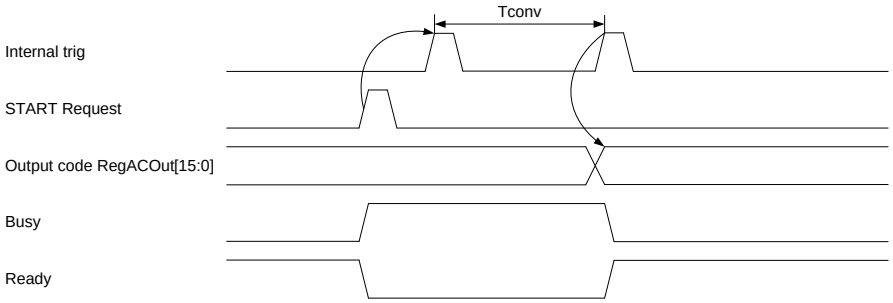


Figure 18. ADC "On-Request" Operation

7.7.8 Output Code Format

The *ADC* output code is a 16-bit word in two's complement format (see **Table 19**). For input voltages outside the range, the output code is saturated to the closest full-scale value (i.e. 0x7FFF or 0x8000). For resolutions smaller than 16 bits, the non-significant bits are forced to the values shown in **Table 20**. The output code, expressed in *LSBs*, corresponds to:

$$OUT_{ADC} = 2^{16} \cdot \frac{V_{IN,ADC}}{V_{REF}} \cdot \frac{OSR + 1}{OSR}$$

Equation 18

Recalling **Equation 10, page 25**, this can be rewritten as:

$$OUT_{ADC} = 2^{16} \cdot \frac{V_{IN}}{V_{REF}} \cdot \left(GD_{TOT} - GDoff_{TOT} \cdot S \cdot \frac{V_{REF}}{V_{IN}} \right) \cdot \frac{OSR+1}{OSR} \quad [LSB]$$

Equation 19

where, from **Equation 11** and **Equation 12**, the total *PGA* gain and offset are respectively:

$$GD_{TOT} = GD_3 \cdot GD_2 \cdot GD_1$$

Equation 20

and:

$$GDoff_{TOT} = GDoff_3 + GD_3 \cdot GDoff_2$$

Equation 21

Table 19. Basic ADC Relationships (example for: VREF = 5V, OSR = 512, n = 16bits)

ADC Input Voltage $V_{IN,ADC}$	% of Full Scale (FS)	Output in LSBs	Hexadecimal Output Code
+2.49505 V	+0.5 x FS	$+2^{15}-1 = 32'767$	7FFF
+2.49497 V	...	$+2^{15}-2 = 32'766$	7FFE
...	...	...	...
+76.145 µV	...	+1	0001
0	0	0	0000
-76.145 µV	...	-1	FFFF
...	...	...	...
-2.49505 V	...	$-2^{15}-1 = -32'767$	8001
-2.49513 V	-0.5 x FS	$-2^{15} = -32'768$	8000

Table 20. Last forced LSBs in conversion output register for resolution settings smaller than 16bits[1]

SetOsr[2:0]	SetNelconv = '00'	SetNelconv = '01'	SetNelconv = '10'	SetNelconv = '11'
'000'	1000000000	100000000	10000000	1000000
'001'	10000000	1000000	100000	10000
'010'	100000	10000	1000	100
'011'	1000	100	10	1
'100'	10	1	-	-
'101'	-	-	-	-
'110'	-	-	-	-
'111'	-	-	-	-

1. (n<16) (RegACOutMsb[7:0] & RegACOutLsb[7:0])

The equivalent *LSB* size at the input of the *PGA* chain is:

$$LSB = \frac{1}{2^n} \cdot \frac{V_{REF}}{GD_{TOT}} \cdot \frac{OSR}{OSR+1} \quad [V/V]$$

Equation 22

Notice that the input voltage $V_{IN,ADC}$ of the *ADC* must satisfy the condition:

$$\left|V_{IN,ADC}\right| \le \frac{1}{2} \cdot (V_{REFP} - V_{REFN}) \cdot \frac{OSR}{OSR+1}$$

Equation 23

to remain within the *ADC* input range.

7.7.9 Power Saving Modes

During low-speed operation, the bias current in the *PGAs* and *ADC* can be programmed to save power using the control words *IbAmpPga[1:0]* and *IbAmpAdc[1:0]* (see **Table 21**). If the system is idle, the *PGAs* and *ADC* can even be disabled, thus, reducing power consumption to its minimum. This can considerably improve battery lifetime.

Table 21. ADC & PGA power saving modes and maximum sampling frequency

IbAmpAdc [1:0]	IbAmpPga [1:0]	ADC Bias Current	PGA Bias Current	Max. fs [kHz]
00		1/4 x I_{ADC}		125
01		1/2 x I_{ADC}		250
11		I_{ADC}		500
	00		1/4 x I_{PGA}	125
	01		1/2 x I_{PGA}	250
	11		I_{PGA}	500

8 Application hints

8.1 Power Reduction

The ZoomingADC is particularly well suited for low-power applications. When very low power consumption is of primary concern, such as in battery operated systems, several parameters can be used to reduce power consumption as follows:

- Operate the acquisition chain with a reduced supply voltage V_{BATT}.
- Disable the *PGAs* which are not used during analog-to-digital conversion with *Enable[3:0]*.
- Disable all *PGAs* and the *ADC* when the system is idle and no conversion is performed.
- Use lower bias currents in the *PGAs* and the *ADC* using the control words *IbAmpPga[1:0]* and *IbAmpAdc[1:0]*.
- Reduce sampling frequency.

Finally, remember that power reduction is typically traded off with reduced linearity, larger noise and slower maximum sampling speed.

8.2 Gain Configuration Flow

The diagram below shows the flow to set the gain of your configuration:

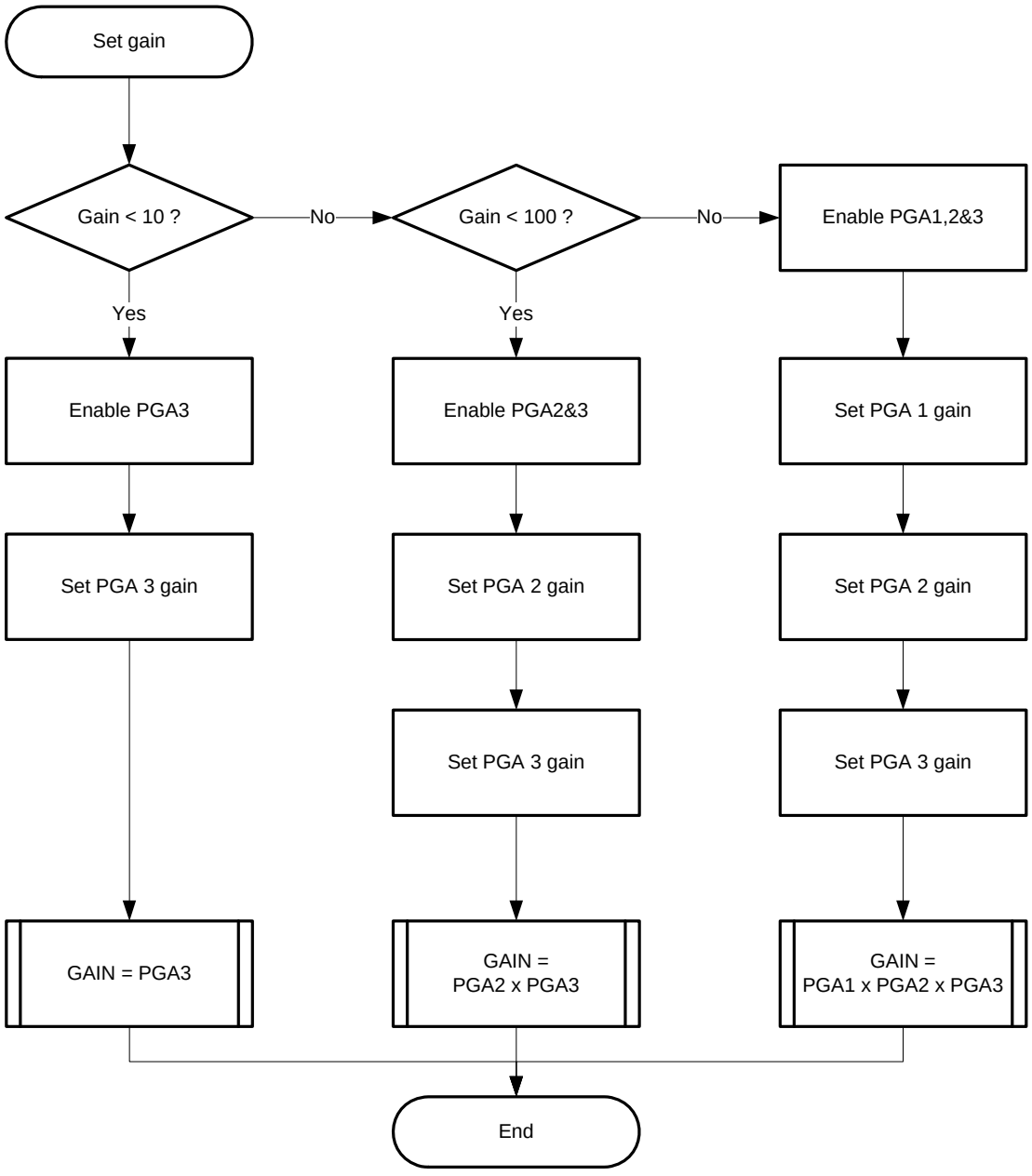


Figure 19. Gain configuration flowchart

9 I2C Interface

The I2C interface gives access to the chip registers. It complies with the I2C protocol specifications, restricted to the slave side of the communication.

The device uses a Generic Fast-Mode (400 KHz) I2C Slave Interface in accordance with the I2C bus standard. Its characteristics can be summarized as follows:

9.1 General Features

- Slave only operation
- Fast mode operation (up to 400 kHz)
- Combined read and write mode support
- General call reset support
- 7-bits default slave address 0x48. Can be changed by fuse and by pinout (D0 and D1).

The interface handles I2C communication at the transaction level. A read transaction is an external request to get the content of system memory location and a write transaction is an external request to write the content of a system memory location.

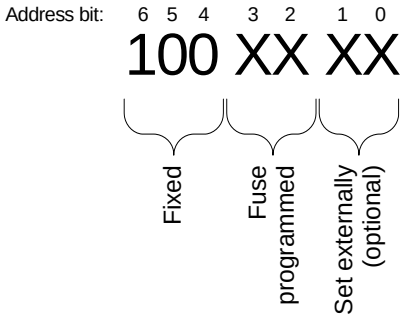
The default I2C slave address is 0x48, 1001000 in binary. This is the standard part I2C slave address. Other addresses between 1000000 and 1001111 are available.

9.2 Other Slave Address Options

Slave address might be diffenciated (2 fuse-programmed bits + 2 LSBs given by 2 GPIO inputs):

- Address bit 3 and bit 2 (100**XX**xx) can be changed in production by fuse. Other values are available by special request. Please contact Semtech Sales for more information. Otherwise, default value is “00”.

- The last significant bits (100xx**XX**) can be defined by the GPIO pin D0 and D1. This mode is not set by default at startup, it must be activated in a register with a command. Default value is “00”.



9.2.1 Address Set Externally

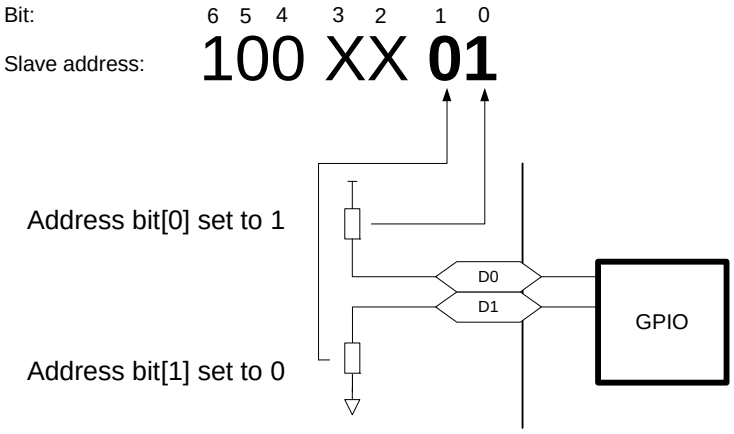


Figure 20. Example of I2C address set by external resistors

The GPIO are set as ouput low at startup, so a resistor should be connected to the pad to avoid shortcut at startup. After startup, the master I2C can send a command (0x96 in RegExtAdd[0x43]) at the default I2C address to change I2C mode and set D0 and D1 as input address bits.

If several SX87xx devices are connected on the same bus, the master MCU must send the command to each device simultaneously using the default address. All SX87xx devices will receive the command at the same time. The master MCU must ensure that the command has been received by asking each slave device at their new address.

9.3 I2C General Call Reset

The device respond to the I2C general call address (0000000) if the eighth bit is '0'. The devices acknowledge the general call address and respond to commands in the second byte. If the second byte is 00000110 (06h), the device reset the internal registers and enter power-down mode.

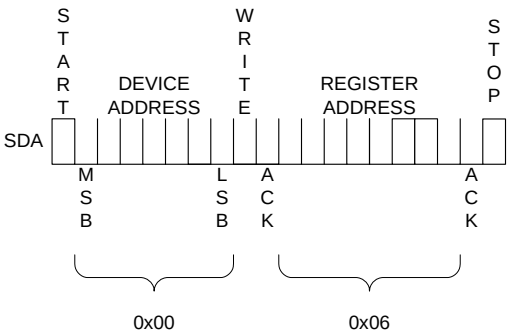


Figure 21. I2C General Call reset frame

9.4 I2C Register Access

9.4.1 Writing a Register

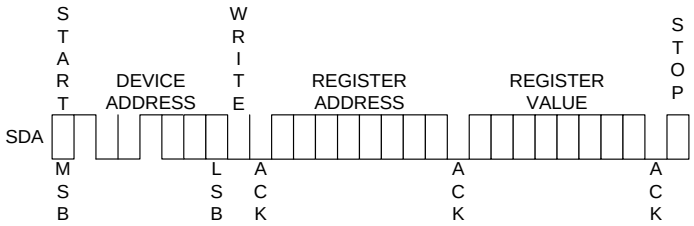


Figure 22. I2C timing diagram for writing to a register

9.4.2 Reading in a Register

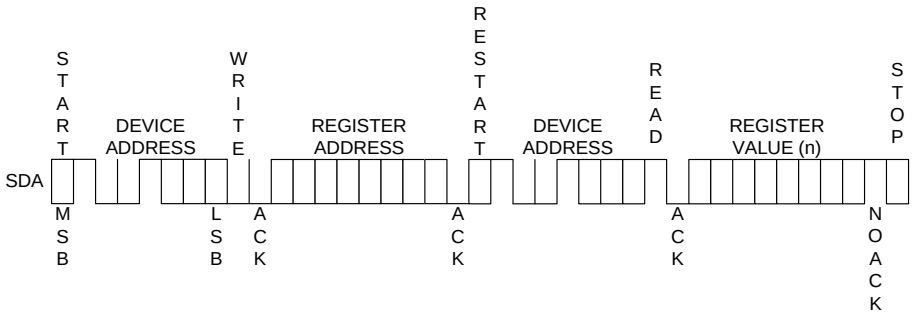


Figure 23. I2C timing diagram for reading from a register

9.4.3 Writing in Several Consecutive Registers

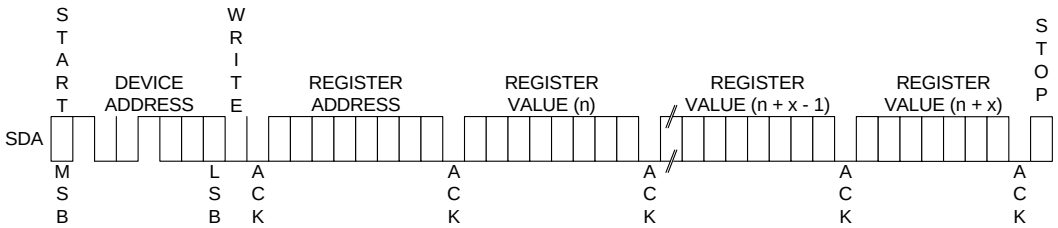


Figure 24. I2C timing diagram for multiple writing to registers

9.4.4 Reading from Several Consecutive Registers

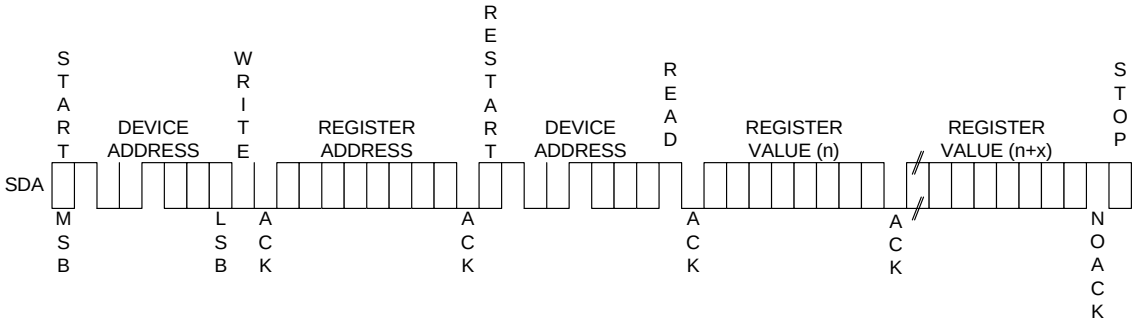


Figure 25. I2C timing diagram for multiple reading from a register

10 Register Memory Map and Description

10.1 Register Map

Table 22 below describes the register/memory map that can be accessed through the I2C interface. It indicates the register name, register address and the register contents.

Table 22. Register Map

Adress	Register	Bit	Description
RC Register			
0x30	RegRCen	1	RC oscillator control
GPIO Registers			
0x40	RegOut	8	D0 to D3 pads data output and direction control
0x41	RegIn	4	D0 to D3 pads input data
0x42	RegTimeout	1	Enable/Disable I2C timeout
0x43	RegExtAdd	8	Set address by external pin
ADC Registers			
0x50	RegACOutLsb	8	LSB of ADC result
0x51	RegACOutMsb	8	MSB of ADC result
0x52	RegACCfg0	7	ADC conversion control
0x53	RegACCfg1	8	ADC conversion control
0x54	RegACCfg2	8	ADC conversion control
0x55	RegACCfg3	8	ADC conversion control
0x56	RegACCfg4	7	ADC conversion control
0x57	RegACCfg5	8	ADC conversion control
Mode Register			
0x70	RegMode	8	Chip operating mode register

10.2 Registers Descriptions

The register descriptions are presented here in ascending order of Register Address. Some registers carry several individual data fields of various sizes; from single-bit values (e.g. flags), upwards. Some data fields are spread across multiple registers. After power on reset the registers will have the values indicated in the tables "Reset" column. Please write the “Reserved” bits with their reset values.

10.2.1 RC Register

Table 23. RegRCen[0x30]

Bit	Bit Name	Mode	Reset	Description
7:1	-	r	0000000	Reserved
0	RCEn	rw	1	Enables RC oscillator. Set 0 for low power mode.

10.2.2 GPIO Registers

Table 24. RegOut[0x40]

Bit	Bit Name	Mode	Reset	Description
7	D3Dir	rw	1	D3 pad direction. 1 : Output 0 : Input
6	D2Dir	rw	1	D2 pad direction. 1 : Output 0 : Input
5	D1Dir	rw	1	D1 pad direction. 1 : Output 0 : Input
4	D0Dir	rw	1	D0 pad direction. 1 : Output 0 : Input
3	D3Out	rw	0	D3 pad output value. Only valid when D3Dir=1
2	D2Out	rw	0	D2 pad output value. Only valid when D2Dir=1
1	D1Out	rw	0	D1 pad output value. Only valid when D1Dir=1 and VrefD1In=0
0	D0Out	rw	0	D0 pad output value. Only valid when D0Dir=1 and VrefD1Out=0

Table 25. RegIn[0x41]

Bit	Bit Name	Mode	Reset	Description
7:4	-	r	0000	Reserved
3	D3In	r	-	D3 pad value
2	D2In	r	-	D2 pad value
1	D1In	r	-	D1 pad value
0	D0In	r	-	D0 pad value

Table 26. RegTimout[0x42]

Bit	Bit Name	Mode	Reset	Description
7:6	-	rw	00	Reserved
5	Timeout	w	0	0 : Disabled 1 : Enabled

Table 26. RegTimout[0x42]

Bit	Bit Name	Mode	Reset	Description
4:0	-	rw	00000	Reserved

Table 27. RegExtAdd[0x43]

Bit	Bit Name	Mode	Reset	Description
7:0	ExternalRd	rw	00000000	Write the 0x96 value into this register to set the two LSbits of the I2C address by external (D0 and D1).

10.2.3 ZADC Registers

Table 28. RegACOutLsb[0x50]

Bit	Name	Mode	Reset	Description
7:0	Out[7:0]	r	00000000	LSB of the ADC result

Table 29. RegACOutMsb[0x51]

Bit	Name	Mode	Reset	Description
7:0	Out[15:8]	r	00000000	MSB of the ADC result

Table 30. RegACCfg0[0x52]

Bit	Name	Mode	Reset	Description
7	Start	rw	0	Starts an ADC conversion
6:5	SetNelconv	rw	01	Sets the number of elementary conversion to $2^{SetNelconv}$. To compensate for offset the signal is chopped between elementary conversion.
4:2	SetOsr	rw	010	Sets the ADC over-sampling rate of an elementary conversion to $2^{3+SetOsr}$.
1	Continuous	rw	0	Sets the continuous ADC conversion mode
0	-	r	0	Reserved

Table 31. RegACCfg1[0x53]

Bit	Name	Mode	Reset	Description
7:6	IbAmpAdc	rw	11	Bias current selection for the ADC
5:4	IbAmpPga	rw	11	Bias current selection for the PGA

Table 31. RegACCfg1[0x53]

Bit	Name	Mode	Reset	Description
3	Enable	rw	0	PGA3 enable
2		rw	0	PGA2 enable
1		rw	0	PGA1 enable
0		rw	0	ADC enable

Table 32. RegACCfg2[0x54]

Bit	Name	Mode	Reset	Description
7:6	SetFs	rw	00	ADC Sampling Frequency selection
5:4	Pga2Gain	rw	00	PGA2 gain selection
3:0	Pga2Offset	rw	0000	PGA2 offset selection

Table 33. RegACCfg3[0x55]

Bit	Name	Mode	Reset	Description
7	Pga1Gain	rw	0	PGA1 gain selection
6:0	Pga3Gain	rw	0001100	PGA3 gain selection

Table 34. RegACCfg4[0x56]

Bit	Name	Mode	Reset	Description
7	-	rw	0	Reserved
6:0	Pga3Offset	rw	0000000	PGA3 offset selection

Table 35. RegACCfg5[0x57]

Bit	Name	Mode	Reset	Description
7	Busy	r	0	ADC activity flag
6	Def	rw	0	Selects ADC and PGA default configuration, starts an ADC conversion
5:1	Amux	rw	00000	Input channel configuration selector
0	Vmux	rw	0	Reference channel selector 0 : V_{BATT} 1 : V_{REF}

10.2.4 Mode Registers

Table 36. RegMode[0x70]

Bit	Name	Mode	Reset	Description
7	-	r	1	reserved
6	-	r	0	reserved
5:4	Chopper	rw	00	V_{REF} chopping control. **Note 1** 11 : Chop at NELCONV/2 rate 10 : Chop at NELCONV rate 01 : Chop state=1 00 : Chop state=0
3	MultForceOn	rw	0	Force charge pump On. Takes priority. **Note 2**
2	MultForceOff	rw	1	Force charge pump Off. **Note 2**
1	VrefD0Out	rw	0	Enable VREF output on D0 pin
0	VrefD1In	rw	0	Enable external VREF on D1 pin

(1) The chop control is to allow chopping of the internal bandgap reference. This may be useful to help eliminate bandgap related internal offset voltage and 1/f noise. The bandgap chop state may be forced High or Low, or may be set to toggle during conversion at either the same rate or half the rate of the Elementary Conversion. (See Conversion Sequence in the ZoomingADC description).

(2) The internal charge pump may be forced On when *VBATT* supply is below 4.2V or Off when *VBATT* supply is above 4.2V. Enabling the charge pump increase the current consumption. If the *ADC* is not being run at full rate or full accuracy then it may operate sufficiently well when *VBATT* is less than 4.2V and internal charge pump forced Off.

11 Typical Performances

Note	The graphs and tables provided following this note are statistical summary based on limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range and therefore outside the warranted range.

11.1 Input impedance

The *PGAs* of the ZoomingADC are a switched capacitor based blocks (see Switched Capacitor Principle section). This means that it does not use resistors to fix gains, but capacitors and switches. This has important implications on the nature of the input impedance of the block.
Using switched capacitors is the reason why, while a conversion is done, the input impedance on the selected channel of the *PGAs* is inversely proportional to the sampling frequency *fs* and to stage gain as given in **Equation 24**.

$$Z_{in} \geq \frac{1}{f_s \cdot (Cg \cdot gain + Cp)} \quad [\Omega]$$

Equation 24

The input impedance observed is the input impedance of the first PGA stage that is enabled or the input impedance of the ADC if all three stages are disabled.

Cg multiplied by *gain* is the equivalent gain capacitor and *Cp* is the parasitic capacitor of the first enabled stage. The values for each ZoomingADC bloc are provided in **Table 37**:

Table 37. Capacitor values

Acquisition Chain Stage	Gain capacitor Cg	Parasitic capacitor Cp	Units
PGA1	0.45	1.04	pF
PGA2	0.54	1.2	pF
PGA3	0.735	1.53	pF
ADC	2.4		pF

PGA1 (with a gain of 10) and *PGA2* (with a gain of 10) have each a minimum input impedance of 300 kOhm at *fs* = 500 kHz. *PGA3* (with a gain of 10) have a minimum input impedance of 250 kOhm at *fs* = 500 kHz. Larger input impedance can be obtained by reducing the gain and/or by reducing the over-sampling frequency *fs*. Therefore, with a gain of 1 and a sampling frequency of 62.5 kHz, Zin > 10.2 MOhm for *PGA1*.

The input impedance on channels that are not selected is very high (>10MOhm).

11.1.1 Switched Capacitor Principle

Basically, a switched capacitor is a way to emulate a resistor by using a capacitor. The capacitors are much easier to realize on CMOS technologies and they show a very good matching precision.

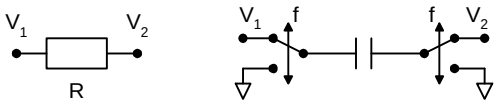


Figure 26. The Switched Capacitor Principle

A resistor is characterized by the current that flows through it (positive current leaves node V_1):

$$I = \frac{V_1 - V_2}{R} \quad [A]$$

Equation 25

One can verify that the mean current leaving node V_1 with a capacitor switched at frequency f is:

$$\langle I \rangle = (V1 - V2) \cdot f \cdot C \quad [A]$$

Equation 26

Therefore as a mean value, the switched capacitor 1/(f x C) is equivalent to a resistor.
It is important to consider that this is only a mean value. If the current is not integrated (low impedance source), the impedance is infinite during the whole time but the transition.
What does it mean for the ZoomingADC?
If the fs clock is reduced, the mean impedance is increased. By dividing the fs clock by a factor 10, the impedance is increased by a factor 10.

One can reduce the capacitor that is switched by using an amplifier set to its minimal gain. In particular if *PGA1* is used with gain 1, its mean impedance is 10x bigger than when it is used with gain 10.

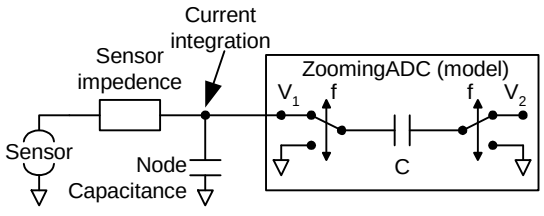


Figure 27. The Switched Capacitor Principle

One can increase the effective impedance by increasing the electrical bandwidth of the sensor node so that the switching current is absorbed through the sensor before the switching period is over. Measuring the sensor node will

show short voltage spikes at the frequency fs, but these will not influence the measurement. Whereas if the bandwidth of the node is lower, no spikes will arise, but a small offset can be generated by the integration of the charges generated by the switched capacitors, this corresponds to the mean impedance effect.

Notes:

(1) One can increase the mean input impedance of the ZoomingADC by lowering the acquisition clock *fs*.

(2) One can increase the mean input impedance of the ZoomingADC by decreasing the gain of the first enabled amplifier.

(3) One can increase the effective input impedance of the ZoomingADC by having a source with a high electrical bandwidth (sensor electrical bandwidth much higher than *fs*).

11.2 Frequency Response

The incremental *ADC* is an over-sampled converter with two main blocks: an analog modulator and a low-pass digital filter. The main function of the digital filter is to remove the quantization noise introduced by the modulator. This filter determines the frequency response of the transfer function between the output of the *ADC* and the analog input *VIN*. Notice that the frequency axes are normalized to one elementary conversion period *OSR* / *fs*. The plots of **Figure 28, page 50** also show that the frequency response changes with the number of elementary conversions *NELCONV* performed. In particular, notches appear for *NELCONV* >= 2 These notches occur at:

$$f_{NOTCH} = \frac{i \cdot f_s}{OSR \cdot N_{ELCONV}} \qquad \text{For} \qquad i = 1, 2, \ldots (N_{ELCONV} - 1)$$

Equation 27

and are repeated every fs / OSR.

Information on the location of these notches is particularly useful when specific frequencies must be filtered out by the acquisition system. This chip has no dedicated 50/60 Hz rejection filtering but some rejection can be achieved by using **Equation 27** and setting the appropriate values of *OSR*, *fs* and *NELCONV*.

Table 38. 50/60 Hz Line Rejection Examples

Rejection [Hz]	fNOTCH [Hz]	fs [kHz]	OSR [-]	NELCONV [-]
60	61	125	1024	2
	61	250	1024	4
	61	500	1024	8
50	53	62.5	1024	8
	46	62.5	1024	4
	46	125	1024	8

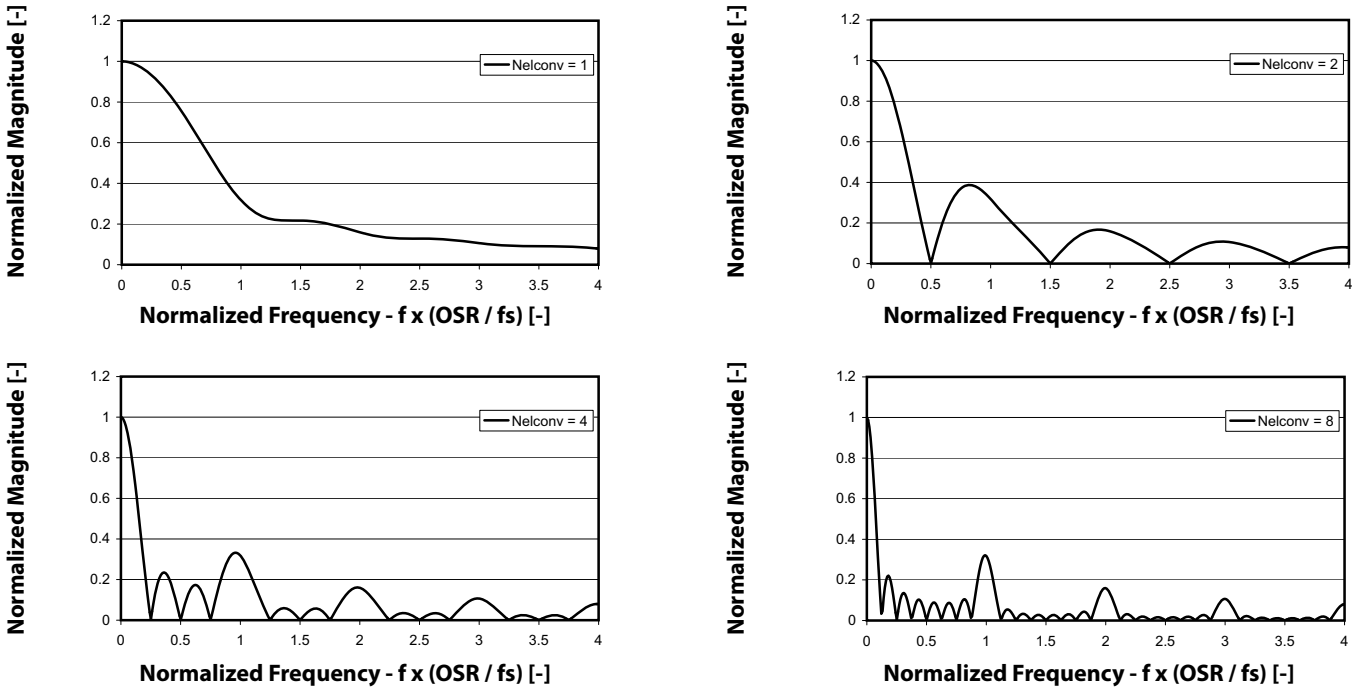


Figure 28. Frequency Response. Normalized Magnitude vs. Frequency for Different NELCONV

11.3 Linearity

11.3.1 Integral Non-Linearity

The different *PGA* stages have been designed to find the best compromise between the noise performance, the integral non-linearity and the power consumption. To obtain this, the first stage has the best noise performance and the third stage the best linearity performance. For large input signals (small *PGA* gains, i.e. up to about 50), the noise added by the *PGA* is very small with respect to the input signal and the second and third stage of the *PGA* should be used to get the best linearity. For small input signals (large gains, i.e. above 50), the noise level in the *PGA* is important and the first stage of the *PGA* should be used.

The following figures show the Integral non linearity for different gain settings over the chip temperature range

11.3.1.1 Gain 1

VBATT=5V ; VREF=VBATT; PGAs disabled; OSR=1024 ; Nelconv=8 ; fs=250kHz; Resolution=16bits.

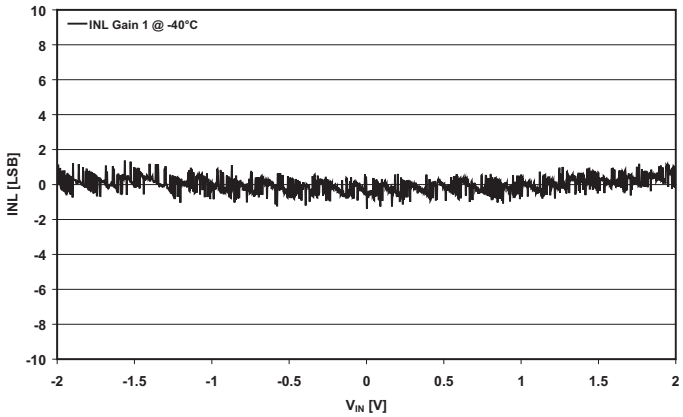


Figure 29. INL -40°C

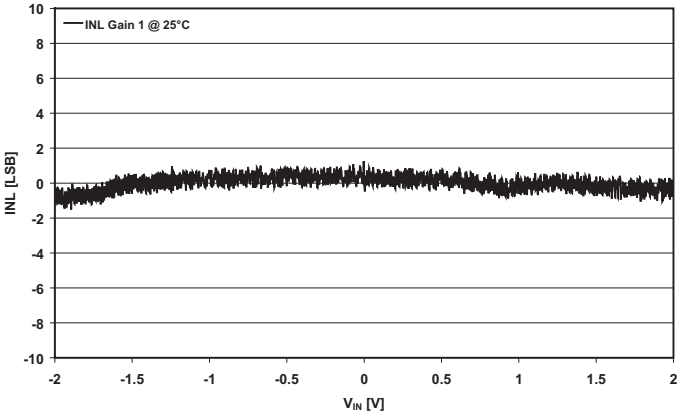


Figure 30. INL 25°C

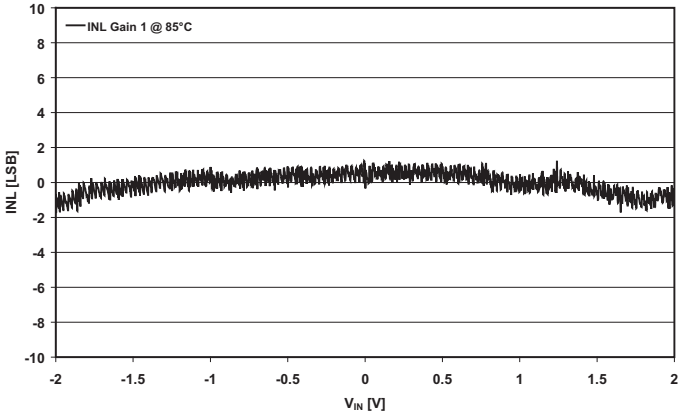


Figure 31. INL 85°C

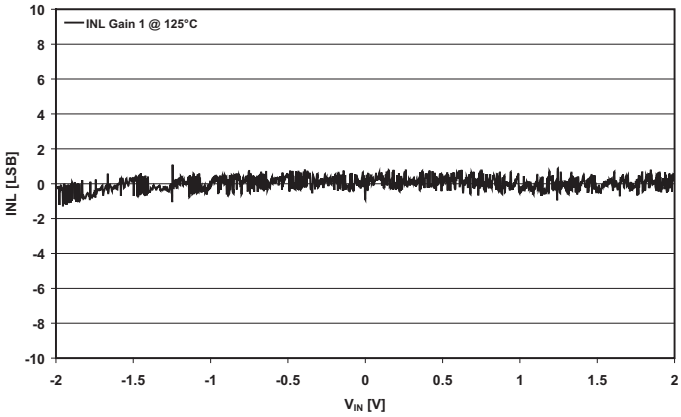


Figure 32. INL 125°C

11.3.1.2 Gain 10

VBATT=5V ; VREF=VBATT; ADC and PGA3 enabled ; GD3=10; OSR=1024 ; Nelconv=8 ; fs=250kHz; Resolution=16bits.

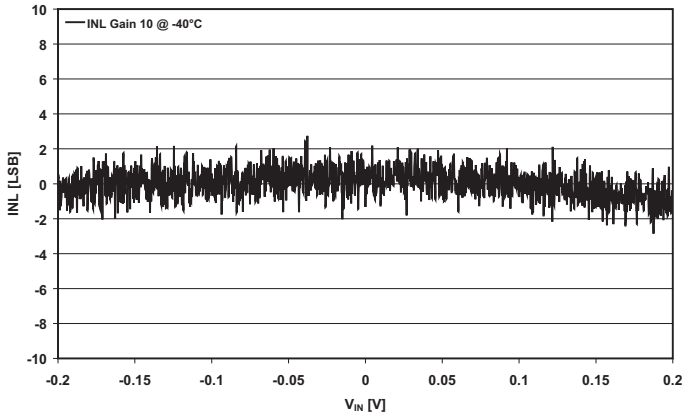


Figure 33. INL -40°C

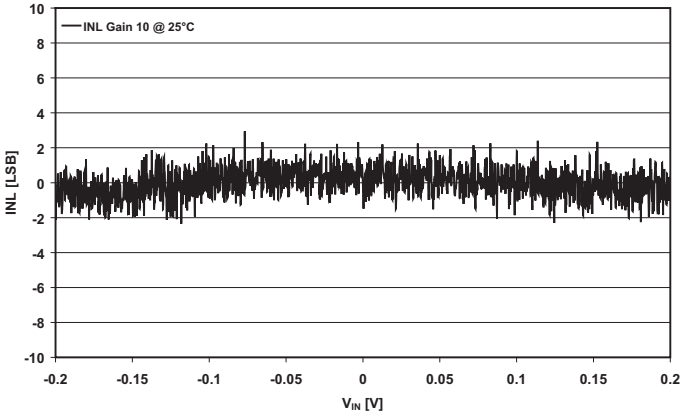


Figure 34. INL 25°C

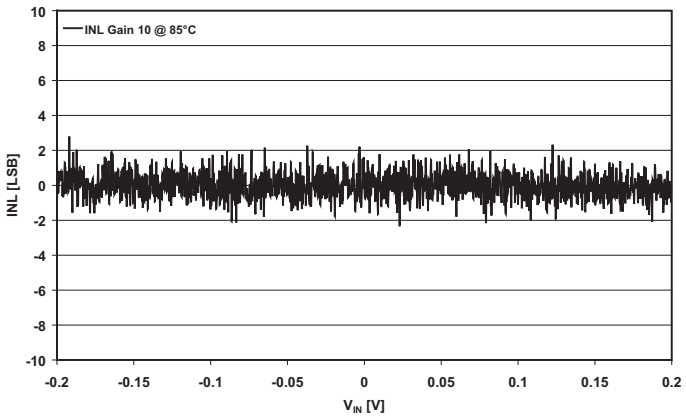


Figure 35. INL 85°C

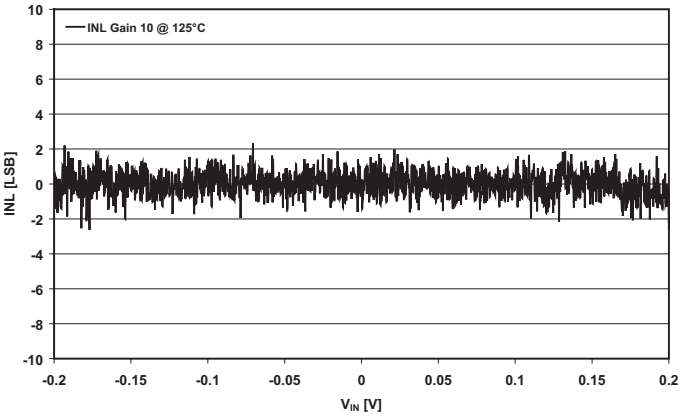


Figure 36. INL 125°C

11.3.1.3 Gain 100

V_{BATT}=5V ; V_{REF}=V_{BATT}; ADC, PGA2 and PGA3 enabled ; GD_2=10; GD_3=10; OSR=1024 ; Nelconv=8 ; fs=250kHz; Resolution=16bits.

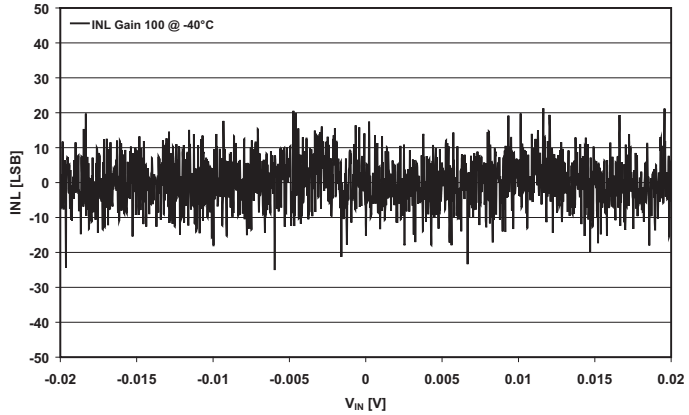


Figure 37. INL -40°C

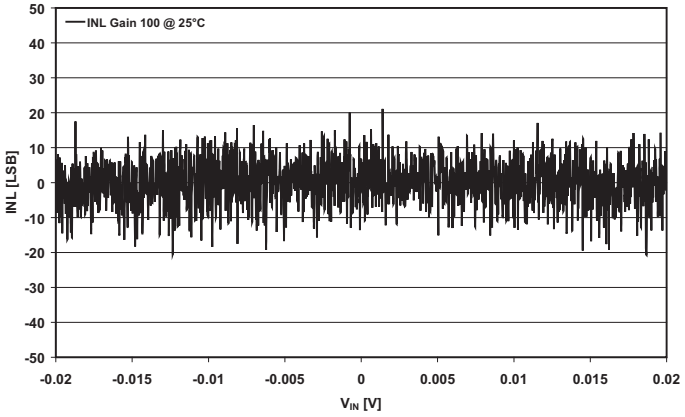


Figure 38. INL 25°C

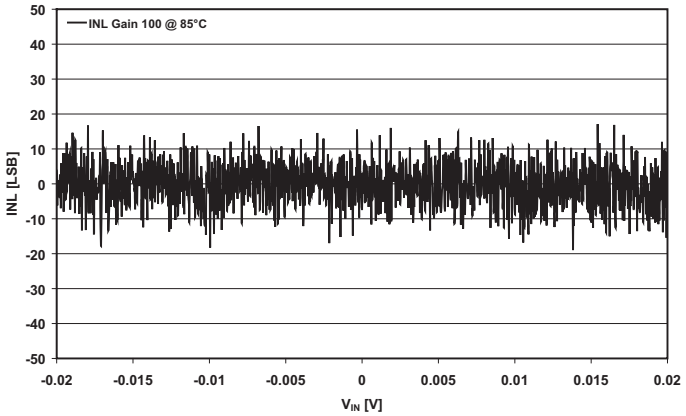


Figure 39. INL 85°C

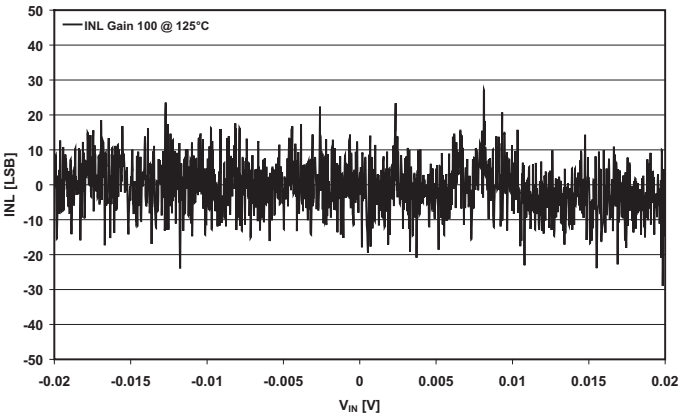


Figure 40. INL 125°C

11.3.1.4 Gain 1000

V_{BATT}=5V ; V_{REF}=V_{BATT}; ADC, PGA3, PGA2, PGA1 enabled; GD_1=10, GD_2=10, GD_3=10; OSR=1024 ; N_{ELCONV}=8 ; fs=250KHz; Resolution=16bits.

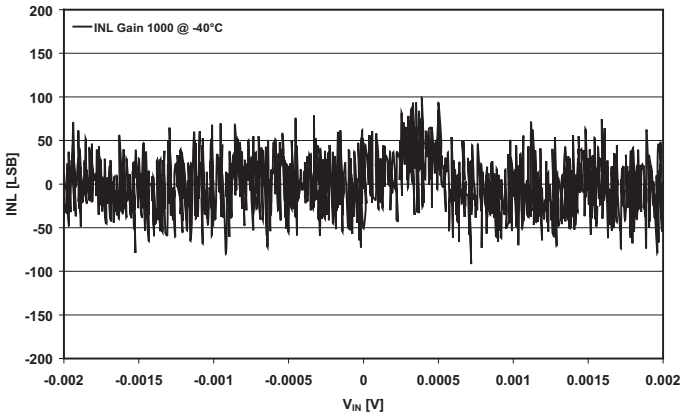


Figure 41. INL -40°C

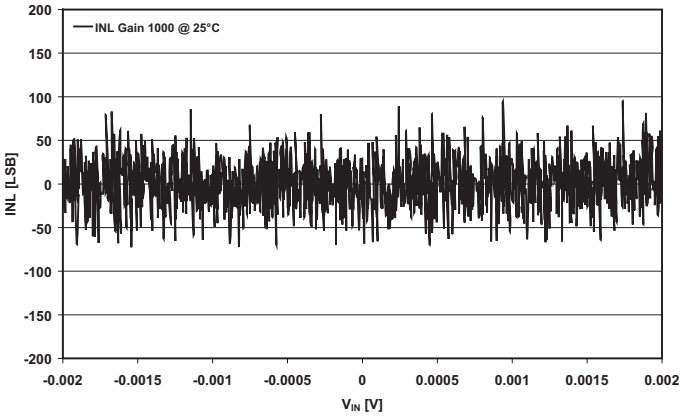


Figure 42. INL 25°C

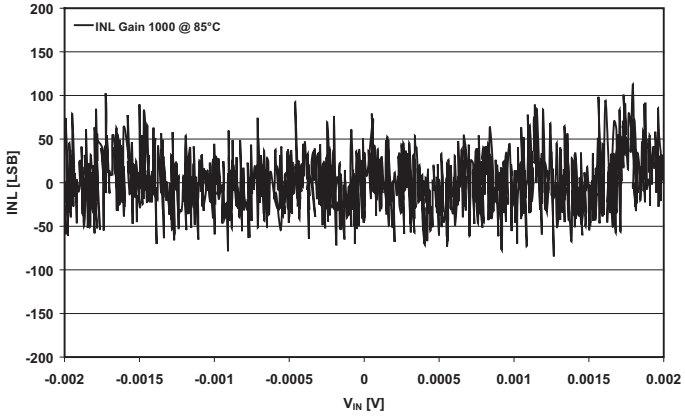


Figure 43. INL 85°C

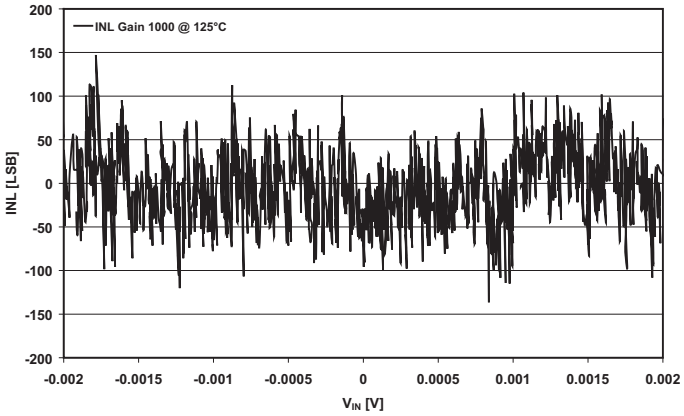


Figure 44. INL 125°C

11.3.2 Differential Non-Linearity

The differential non-linearity is generated by the *ADC*. The *PGA* does not add differential non-linearity. **Figure 45** shows the differential non-linearity.

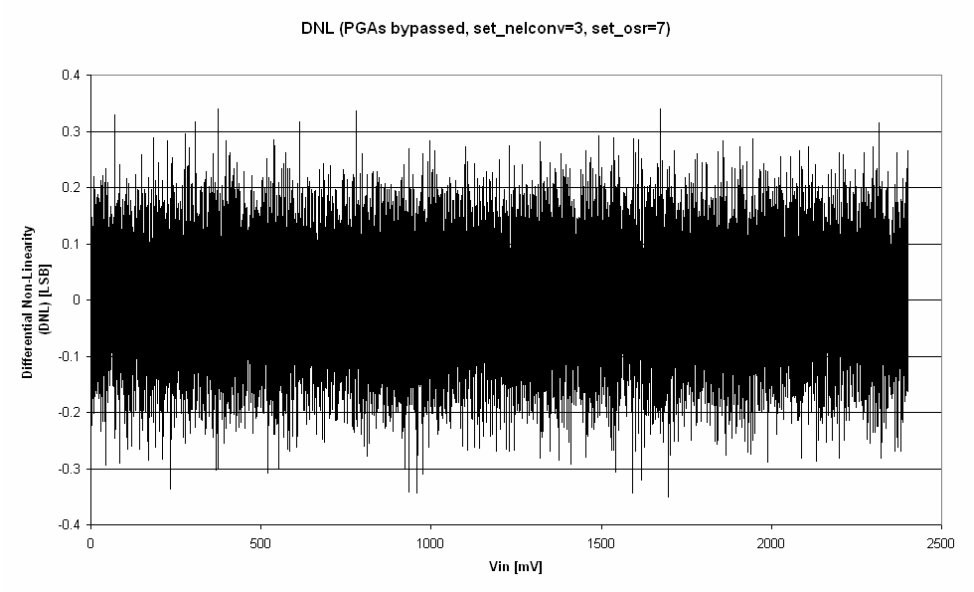


Figure 45. Differential Non-Linearity of the ADC Converter

11.4 Noise

Ideally, a constant input voltage V_{IN} should result in a constant output code. However, because of circuit noise, the output code may vary for a fixed input voltage. Thus, a statistical analysis on the output code of 1200 conversions for a constant input voltage was performed to derive the equivalent noise levels of *PGA1*, *PGA2*, and *PGA3*.

The extracted rms output noise of *PGA1*, *2*, and *3* are given in **Table 39, page 56**: standard output deviation and output rms noise voltage.

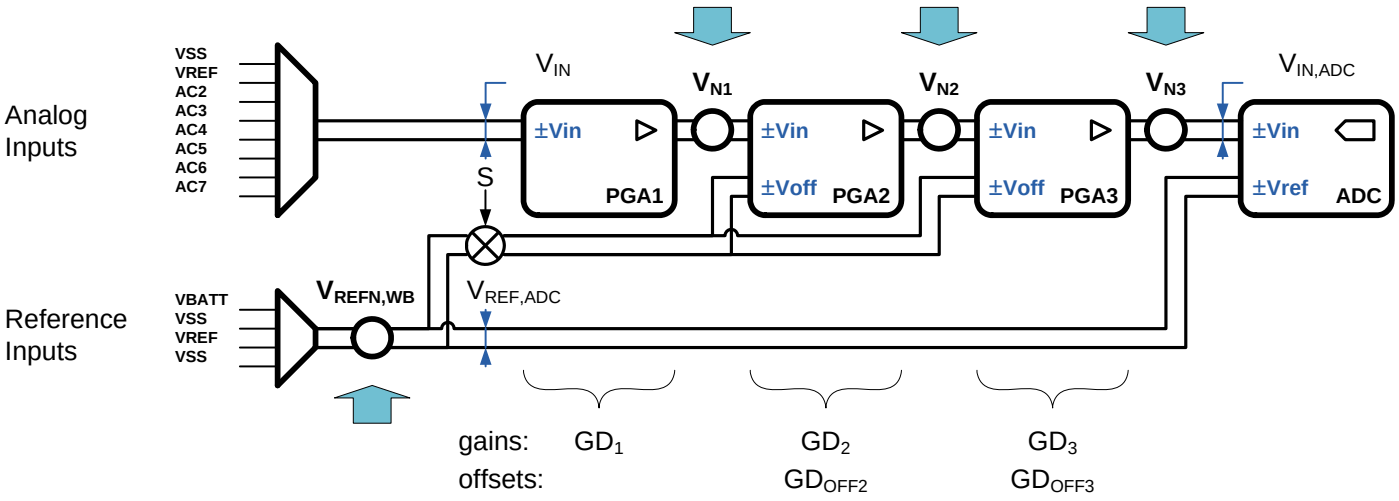


Figure 46. Simple Noise Model for PGAs and ADC

VN1, *VN2*, and *VN3* are the output rms noise figures of **Table 39**, *GD1*, *GD2*, and *GD3* are the *PGA* gains of stages 1 to 3 respectively. *VREFN,WB* is the wide band noise on the reference voltage.

The simple noise model of **Figure 46** is used to estimate the equivalent input referred rms noise *VN,IN* of the acquisition chain in the model of **Figure 48, page 56**. This is given by the relationship:

$$V_{N,IN}{}^2 = \frac{\left(\frac{V_{N1}}{GD_1}\right)^2 + \left(\frac{V_{N2}}{GD_1 \cdot GD_2}\right)^2 + \left(\frac{V_{N3}}{GD_{TOT}}\right)^2 + \left(\frac{V_{REFN,WB}\left(GD_2 \cdot GD_{OFF2} + GD_{OFF3}\right)}{GD_{TOT}}\right)^2 + \left(\frac{1}{2} \cdot \frac{V_{REFN,WB}}{GD_{TOT}}\right)^2}{\left(OSR \cdot N_{ELCONV}\right)} \left[V^2 rms\right]$$

Equation 28

On the numerator of **Equation 28** :

1 the first parenthesis is the PGA1 gain amplifier contribution to noise
2 the second parenthesis is the PGA2 gain amplifier contribution to noise
3 the third parenthesis is the PGA3 gain amplifier contribution to noise
4 the fourth parenthesis is PGA2 and PGA3 offset amplifiers contributions to noise
5 the last parenthesis is the contribution of the noise on the references of the ADC

As shown in **Equation 28**, noise can be reduced by increasing *OSR* and *NELCONV* (increases the *ADC* averaging effect, but reduces noise).

Table 39. PGA Noise Measurement (n = 16bits, OSR = 512, NELCONV = 2, VREF = 5V)

Parameter	PGA1	PGA2	PGA3
Output RMS noise(uV)	V_{N1} = 205	V_{N2} = 340	V_{N3} = 365

Figure 47 shows the distribution for the *ADC* alone (*PGA1*, *2*, and *3* bypassed). Quantization noise is dominant in this case, and, thus, the *ADC* thermal noise is below 16 bits.

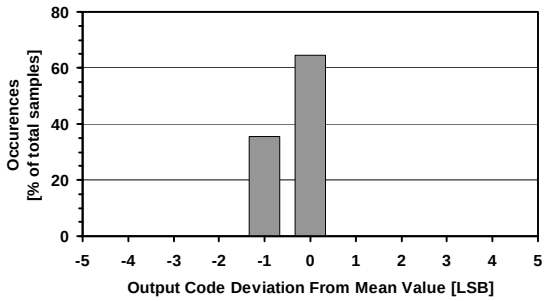


Figure 47. ADC Noise (PGA1, 2 & 3 Bypassed, OSR = 512, NELCONV = 2)

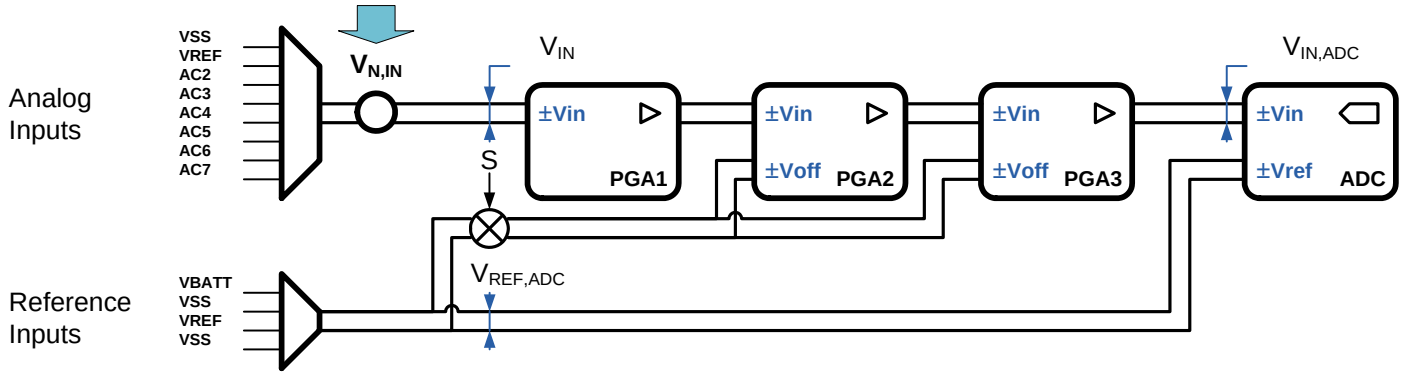


Figure 48. Total Input Referred Noise

As an example, consider the system where: GD_2 = 10 (GD_1 = 1; *PGA3* bypassed), *OSR* = 512, *NELCONV* = 2, V_{REF} = 5 V. In this case, the noise contribution V_{N1} of *PGA1* is dominant over that of *PGA2*. Using **Equation 28, page 55**, we get: $V_{N,IN}$ = 6.4 µV (rms) at the input of the acquisition chain, or, equivalently, 0.85 LSB at the output of the *ADC*. Considering 0.2 V (rms) maximum signal amplitude, the signal-to-noise ratio is 90dB.

11.5 Gain Error and Offset Error

Gain error is defined as the amount of deviation between the ideal transfer function (theoretical **Equation 19, page 33**) and the measured transfer function (with the offset error removed).

The actual gain of the different stages can vary depending on the fabrication tolerances of the different elements. Although these tolerances are specified to a maximum of ±3%, they will be most of the time around ±0.5%. Moreover, the tolerances between the different stages are not correlated and the probability to get the maximal error in the same direction in all stages is very low. Finally, these gain errors can be calibrated by the software at the same time with the gain errors of the sensor for instance.

Figure 49 shows gain error drift vs. temperature for different *PGA* gains. The curves are expressed in % of Full-Scale Range (*FSR*) normalized to 25°C.

Offset error is defined as the output code error for a zero volt input (ideally, output code = 0). The offset of the *ADC* and the PGA1 stage are completely suppressed if $N_{ELCONV} > 1$.

The measured offset drift vs. temperature curves for different PGA gains are depicted in **Figure 50**. The output offset error, expressed in LSB for 16-bit setting, is normalized to 25°C. Notice that if the *ADC* is used alone, the output offset error is below +/-1 LSB and has no drift.

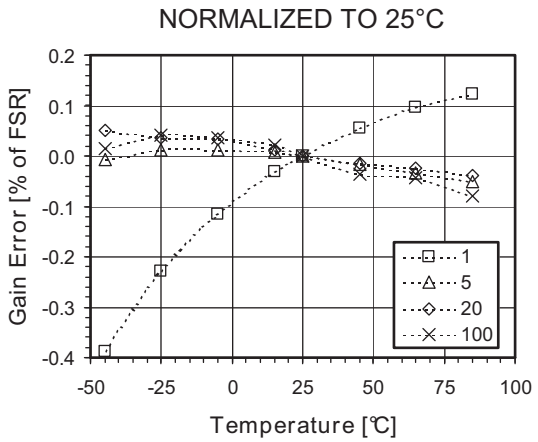


Figure 49. Gain Error vs. Temperature for Different Gains

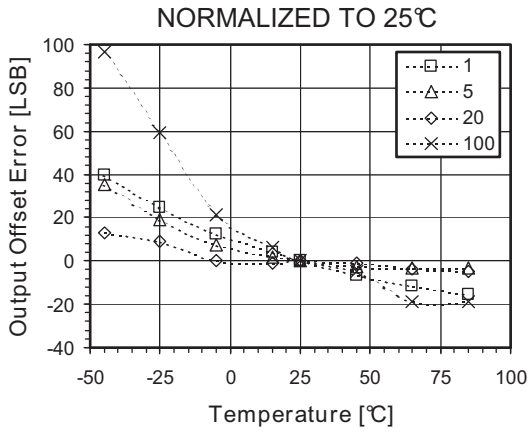


Figure 50. Offset Error vs. Temperature for Different Gains

11.6 Power Consumption

Figure 51 plots the variation of current consumption with supply voltage *VBATT*, as well as the distribution between the 3 *PGA* stages and the *ADC* (see **Table 40, page 60**). The Charge Pump is forced ON for VBATT < 4.2V and forced OFF for VBATT > 4.2V.

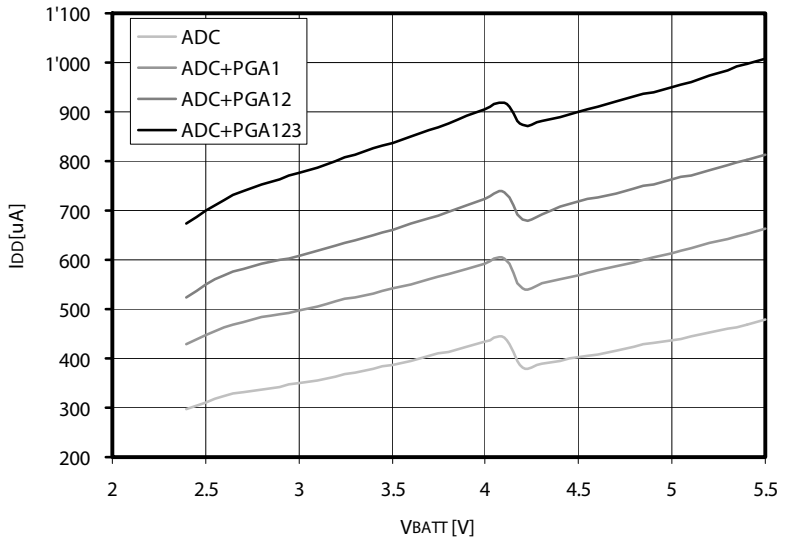


Figure 51. Current Consumption vs. Supply Voltage and PGAs

As shown in **Figure 52**, if lower sampling frequency is used, the current consumption can be lowered by reducing the bias currents of the *PGAs* and the *ADC* with registers *IbAmpPga* and *IbAmpAdc*. (In **Figure 52**, *IbAmpPga/Adc* = '11', '10', '00' for *fs* = 500, 250, 62.5 kHz respectively. The Charge Pump is forced ON for VBATT < 4.2V and forced OFF for VBATT > 4.2V.

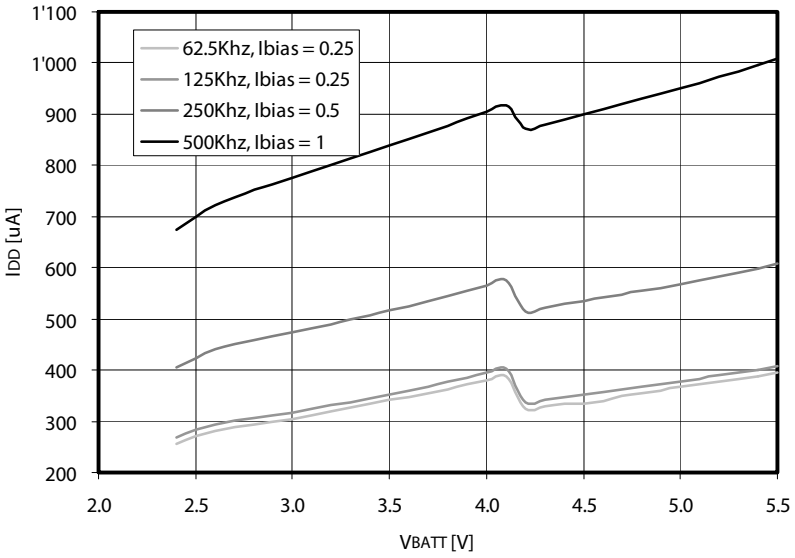


Figure 52. Current Consumption vs Temperature and ADC Sampling Frequency

Current consumption vs. temperature is depicted in **Figure 53**, showing the increase between -40 and +125°C.

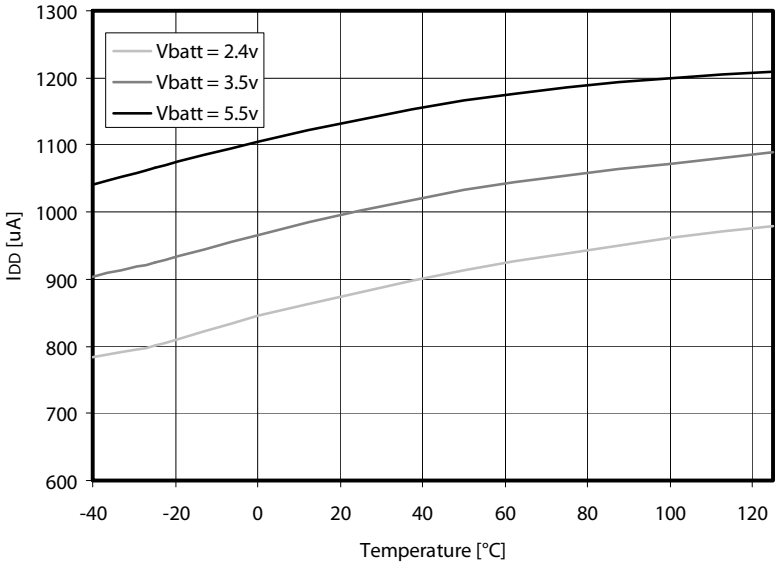


Figure 53. Current Consumption vs Temperature and Supply Voltage

Table 40. Typical Current Distribution in Acquisition Chain (n = 16 bits, fs = 250kHz)

Supply	ADC	PGA1	PGA2	PGA3	Total	Unit
V_{BATT} = 2.4V	207	70	51	78	406	uA
V_{BATT} = 3.5V	282	82	61	91	516	
V_{BATT} = 5.5V	338	103	67	98	606	

FAMILY OVERVIEW

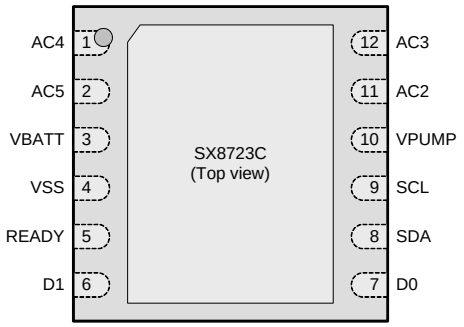
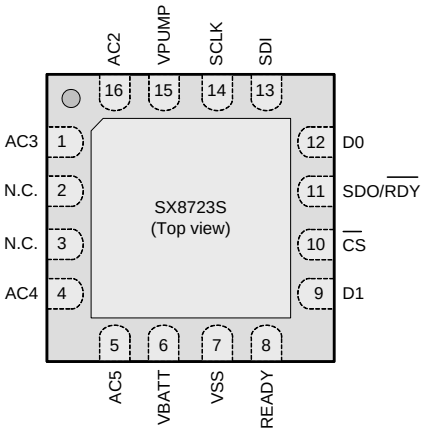
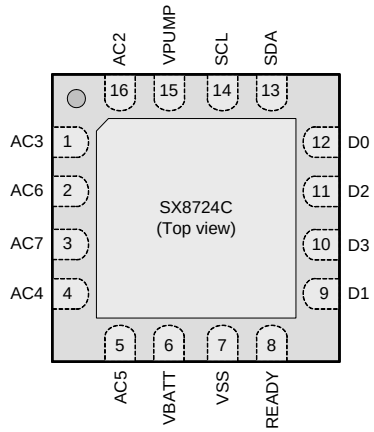
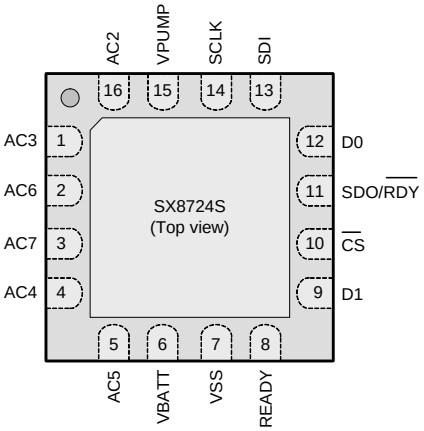
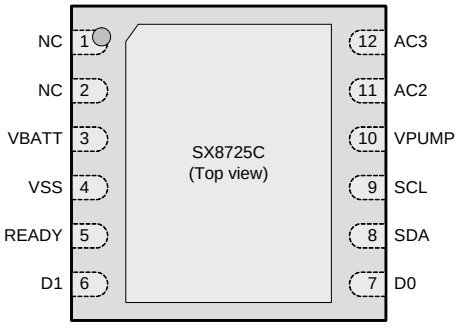
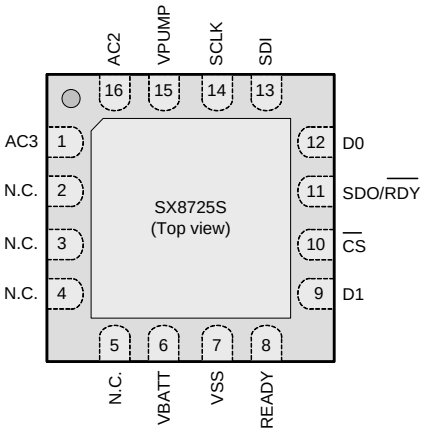
This chapter gives an overview of similar devices based on the ZoomingADC but with different features or packages. Each part is described in it's own datasheet.

12 Comparizon table

Table 41. Family comparizon table

		Part number					
		SX8723C	**SX8724C**	**SX8725C**	**SX8723S**	**SX8724S**	**SX8725S**
Package		MLPD-W-12 4x4	MLPQ-16 4x4	MLPD-W-12 4x4	MLPQ-16 4x4	MLPQ-16 4x4	MLPQ-16 4x4
Protocol		I2C	I2C	I2C	SPI	SPI	SPI
GPIO	**D0**	I2C addr, Digital IO or Vref OUT	I2C addr, Digital IO or Vref OUT	I2C add, Digital IO or Vref OUT	Digital IO or Vref OUT	Digital IO or Vref OUT	Digital IO or Vref OUT
	D1	I2C addr, Digital IO or Vref IN	I2C addr, Digital IO or Vref IN	I2C addr, Digital IO or Vref IN	Digital IO or Vref OUT.	Digital IO or Vref IN	Digital IO or Vref IN
	D2	N.A.	Digital IO	N.A.	N.A.	N.A.	N.A.
	D3	N.A.	Digital IO	N.A.	N.A.	N.A.	N.A.
Differential input channels		2	3	1	2	3	1

13 Comparizon by package pinout

I2C versions	SPI versions
	
	
	

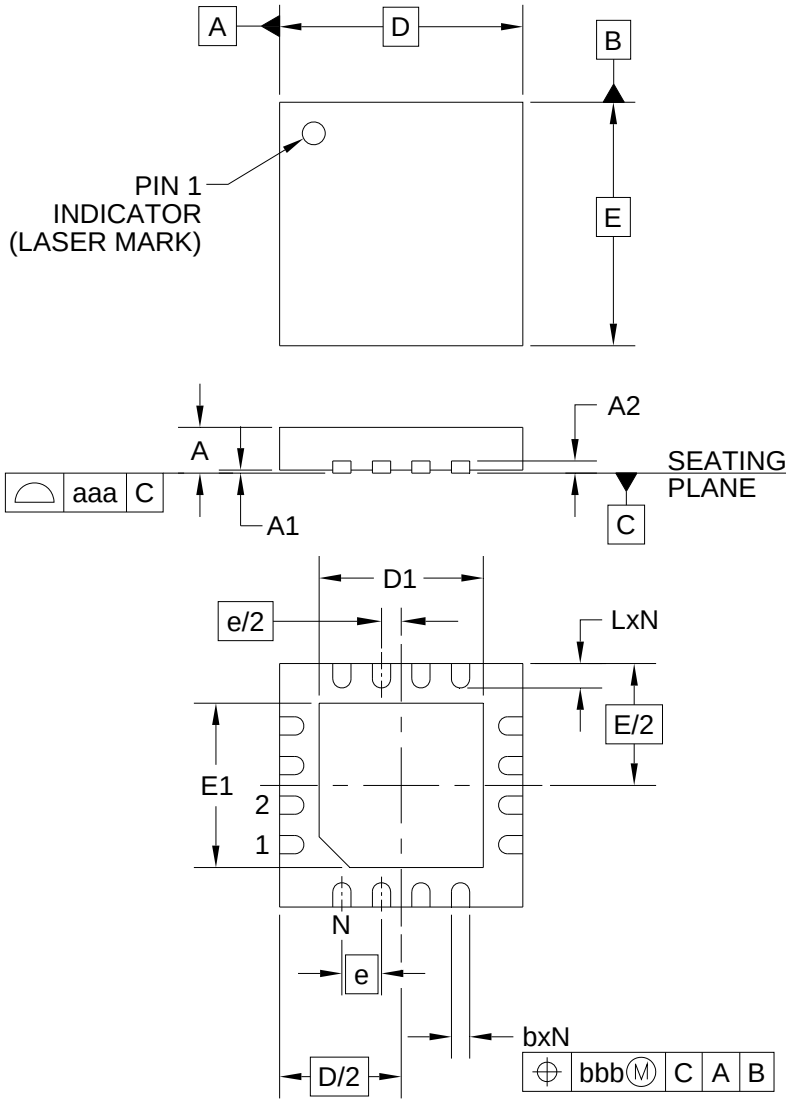
14 PCB Layout Considerations

PCB layout considerations to be taken when using the SX8724C are relatively simple to get the highest performances out of the ZoomingADC. The most important to achieve good performances out the ZoomingADC is to have a good voltage reference. The SX8724C has already an internal reference that is good enough to get the best performances with a minimal amount of external components, but, in case an external reference is needed this one must be as clean as possible in order to get the desired performance. Separating the digital from the analog lines will be also a good choice to reduce the noise induced by the digital lines. It is also advised to have separated ground planes for digital and analog signals with the shortest return path, as well as making the power supply lines as wider as possible and to have good decoupling capacitors.

15 How to Evaluate

For evaluation purposes SX8724CEVK evaluation kit can be ordered. This kit connects to any PC using a USB port. The "SX87xx Evaluation Tools" software gives the user the ability to control the SX8724C registers as well as getting the raw data from the ZoomingADC and displaying it on the "Graphical User interface". For more information please look at SEMTECH web site (**http://www.semtech.com**).

16 Package Outline Drawing: MLPQ-W16-4x4-EP1



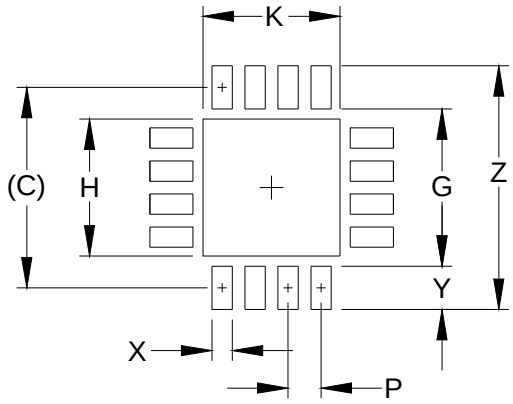
DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	-	0.80
A1	0.00	-	0.05
A2	-	(0.20)	-
b	0.25	0.30	0.35
D	3.90	4.00	4.10
D1	2.55	2.70	2.80
E	3.90	4.00	4.10
E1	2.55	2.70	2.80
e	0.65 BSC		
L	0.30	0.40	0.50
N	16		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 54. Package Outline Drawing

17 Land Pattern Drawing: 4x4MLPQ-W16-EP1



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.156)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.026	0.65
X	.016	0.40
Y	.033	0.85
Z	.189	4.80

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.

Figure 55. Land Pattern Drawing

18 Tape and Reel Specification

MLP/QFN (0.70mm - 1.00mm package thickness)

- Single Sprocket holes
- Tolerances for Ao & Bo are +/- 0.20mm
- Tolerances for Ko is +/- 0.10mm
- Tolerance for Pocket Pitch is +/- 0.10mm
- Tolerance for Tape width is +/-0.30mm
- Trailer and Leader Length are minimum required length
- Package Orientation and Feed Direction

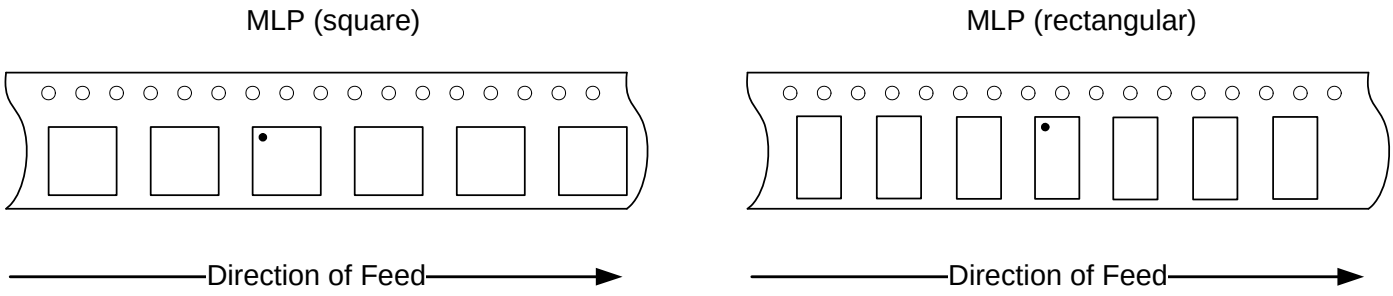


Figure 56. Direction of Feed

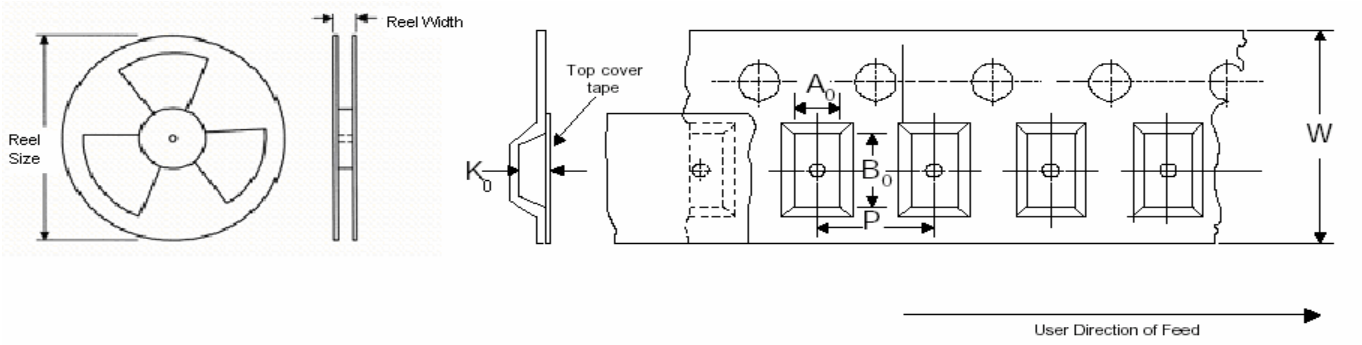


Figure 57. User direction of feed

Table 42. Tape and reel specifications

Pkg size	carrier tape (mm)					Reel				
	Tape Width (W)	Pocket Pitch (P)	Ao	Bo	Ko	Reel Size (in)	Reel Width (mm)	Trailer Length (mm)	Leader Length (mm)	QTY per Reel
4x4	12	8	4.35	4.35	1.10	7/13	12.4	400	400	1000/3000

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