FMA1127DA
Touch Sensor Controller

Overview

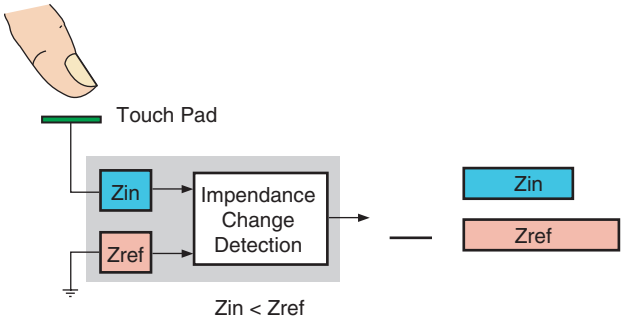
The FMA1127DA is a low-power, compact, flexible touch sensor controller that converts capacitance generated between the human body and a conductive touch pad to digital data without any analog signal processing.

Its programmability increases design flexibility and gives better performance and stability for a broad range of applications.The FMA1127DA's Automatic Impedance Calibration (AIC™) function can be easily configured to support different sensitivities for individual channels independently as well as to change values of parameters, such as calibration intervals. AIC may also be temporarily paused and resumed by a host MCU.

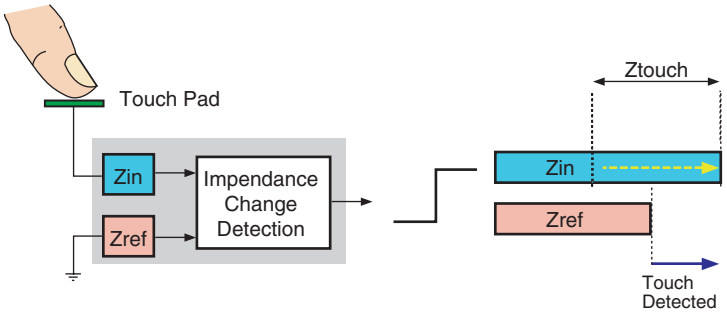
Among the many new features of the FMA1127DA is Adjacent Pattern Interference Suppression (APIS™). APIS is a filtering function that eliminates adjacent key or pattern interference. The FMA1127DA also gives touch-strength output in addition to touch on/off output.There is a number of DIOs depending on the package type that can be configured and programmed to meet a customer's specific needs, giving customers even greater flexibility and value.

The FMA1127DA comes with various package types to support different number of input channels and DIOs.

The FMA1127DA touch sensor controller is developed and owned by ATLab Inc., South Korea, and is distributed by Fujitsu Microelectronics America, Inc.



Touch Pad System Model **Impedance Status**



Touch Pad System Model **Impedance Status**

Features

- Patented full-digital architecture
- Extremely low power consumption (110µA in active mode)
- Supports 12 input channels (40QFN and 30SSOP) or 9 input channels (32QFN and 24SSOP) or 6 input channels (24QFN and 20SSOP)
- Programmable registers to characterize applications
- I²C interface with the host MCU
- Configurable Automatic Impedance Calibration (AIC™)
- Two types of interrupts (GINT for general purpose and TINT for touch detection)
- 8-bit resolution of touch strength data (256 steps)
- Three different modes for Adjacent Pattern Interference Suppression (APIS™).
- Configurable DIO pins as direct touch outputs, extended GPIOs, or external interrupt inputs.
- Beep generation for tactile feeling
- Idle and Sleep modes for power saving
- De-bounced touch outputs

Applications

- Portable devices such as PDAs, cellular phones, MP3 players, remote controllers, and other integrated input devices
- Home appliances and consumer electronic products
- Computer input devices such as mice and keyboards

Touch Sensor Controller

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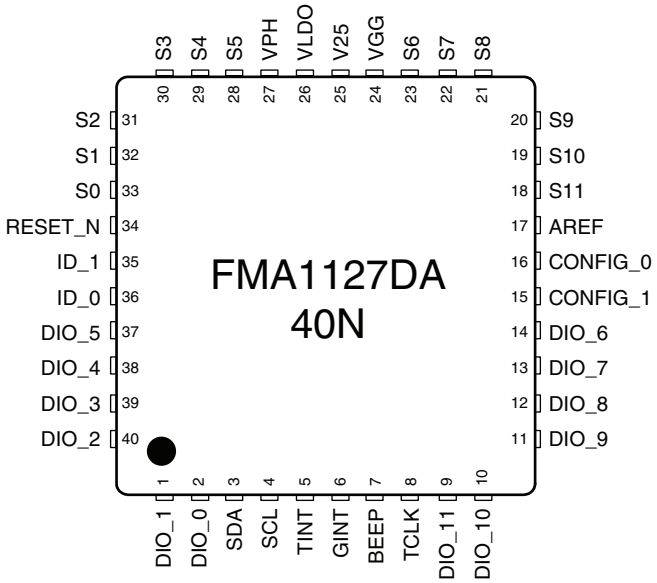
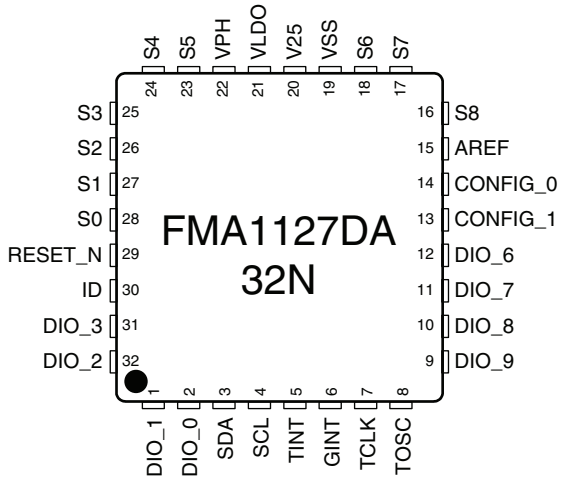
Ordering Information

Product Code	Package Type	Package Dimension	Pin Pitch	Number of Sensor Inputs	Number of Digital Outputs
FMA1127DA-40N	40QFN	5mm x 5mm x 0.85mm	0.4mm	12	12
FMA1127DA-32N	32QFN	4mm x 4mm x 0.9mm	0.4mm	9	8
FMA1127DA-24N	24QFN	4mm x 4mm x 0.85mm	0.5mm	6	3
FMA1127DA-30S	30SSOP	12.7mm x 10.3mm x 2.5mm	0.8mm	12	6
FMA1127DA-24S	24SSOP	8.2mm x 7.8mm x 2.0mm	0.65mm	9	3
FMA1127DA-20S	20SSOP	6.5mm x 6.4mm x 1.85mm	0.65mm	6	2

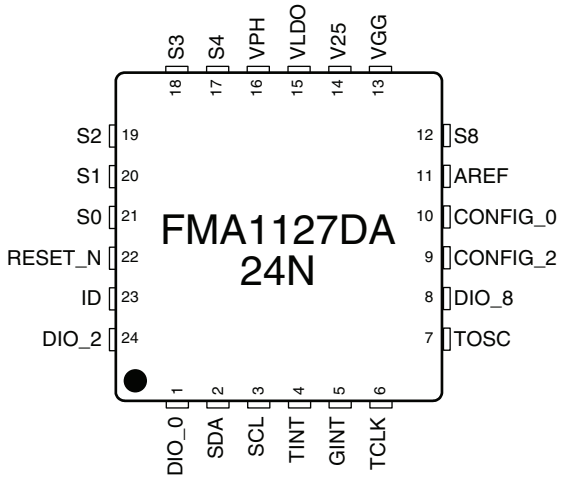
Package Pinouts



40-Pin QFN

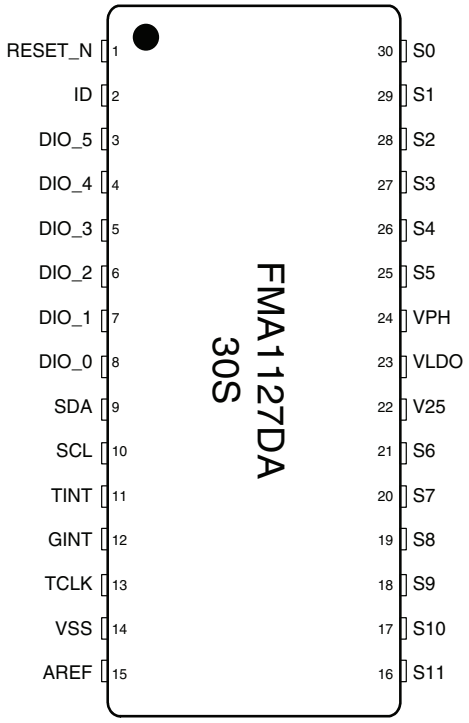


32-Pin QFN

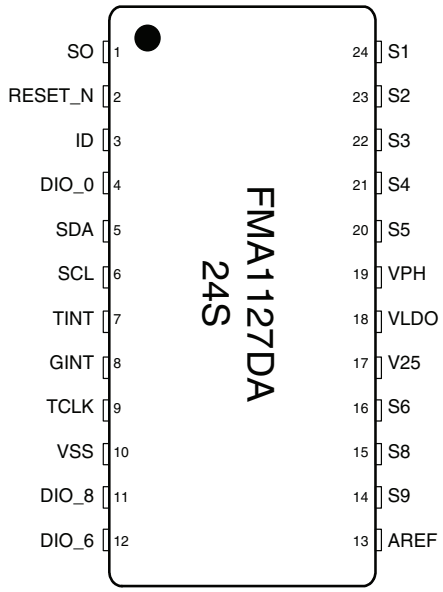


24-Pin QFN

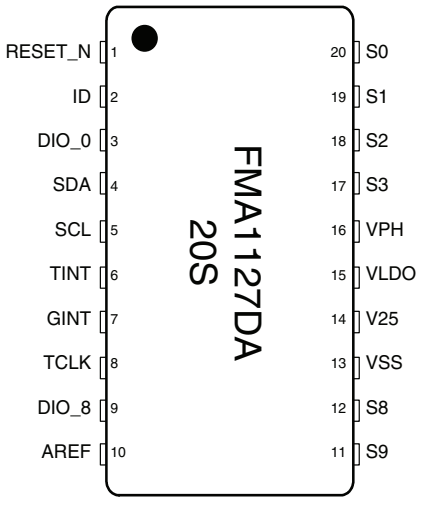
Touch Sensor Controller



30-Pin SSOP



24-Pin SSOP



20-Pin SSOP

Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ABSOLUTE MAXIMUM RATINGS						
Tstg	Storage Temperature		-45		95	^{o}C
Topr	Operating Temperature		-40		90	^{o}C
Hopr	Operating Humidity		5		95	%
VPH	IO Power Supply Voltage	VPH should be higher than 3V when using internal LDO	2.3	3.3	5.5	V
VLDO	Core Power Supply Voltage		2.3	2.5	2.7	V
V25	Core Input Voltage		2.3	2.5	2.7	V
RECOMMENDED OPERATING CONDITIONS						
Toprr	Operating Temperature		-40	25	90	^{o}C
Vddp	Power Supply Voltage (VPH)		2.4		5.3	V
Vddc	Power Supply Voltage (VLDO)		2.4	2.5	2.6	V
Tr_i	Digital Input Rising Time				5	ns
Tf_i	Digital Input Falling Time				5	ns
AC ELECTRICAL SPECIFICATIONS (Typical values at Ta=25^{0}C and VPH=3.3V)						
fsys	System Clock		1.3	1.6	2	MHz
fi	Input frequency (Sensor Clock)	When System Clock is 1.6MHz	2.5		20	KHz
fsmp	Sample frequency	When System Clock is 1.6MHz	10		20,000	Hz
Stch	Touch Sensitivity			0.078		pF
Rs_i	Sensor Input Resistance			15		KΩ
TCsr_i	Tuning Capacitor in Aref or Sin		0		15	pF
Tr_o	Output Rising Time	Load = 100pF		50	60	ns
Tf_o	Output Falling Time	Load = 100pF		50	60	ns
DC ELECTRICAL SPECIFICATIONS (Typical values at Ta=25^{0}C and VPH=3.3V)						
Idd_a	Supply Current (Active mode)	When using internal 2.5V LDO and internal Clock	50	110	170	µA
Idd_i	Supply Current (Idle mode)		20	70	130	µA
Idd_ael	Supply Current (Active mode)	When using external 2.5V LDO and internal Clock	20	80	150	µA
Idd_iel	Supply Current (Idle mode)		35	80	140	µA
Idd_aeo	Supply Current (Active mode)	When using external 2.5V LDO and external Clock	15	70	135	µA
Idd_ieo	Supply Current (Idle mode)		10	30	90	µA
Idd_s	Supply Current (Sleep mode)	When using external 2.5V LDO		0.1	1	µA
Vil	Digital Input Low Voltage				0.7	V
Vih	Digital Input High Voltage		0.8xVPH			V
Vol	Digital Output Low Voltage				0.6	V
Voh	Digital Output High Voltage		VPH-0.5			V
Vldo	Internal LDO Output Voltage		2.3	2.5	3.0	V
Ildo	Internal LDO Driving Current				20	mA
Idr	GPIO Driving Current		-2 (Source)		16 (Sync)	mA
Iol	Digital Output Low Current	At Vol = 0.6V At Vol= 0.4V			8.4 5.7	mA

Operation Principles

Touch Detection

The FMA1127DA touch sensor controller includes the Impedance Change Detection engine within the device. It detects the impedance difference between reference and sensor input.

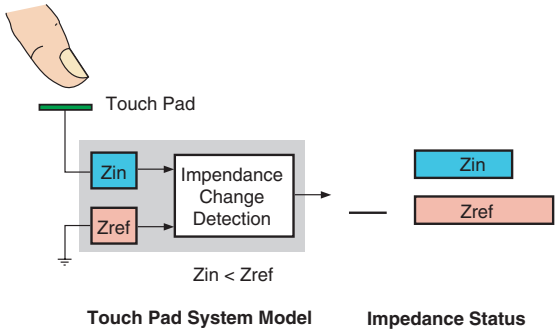


Figure 1: When a Pad is Not Touched.

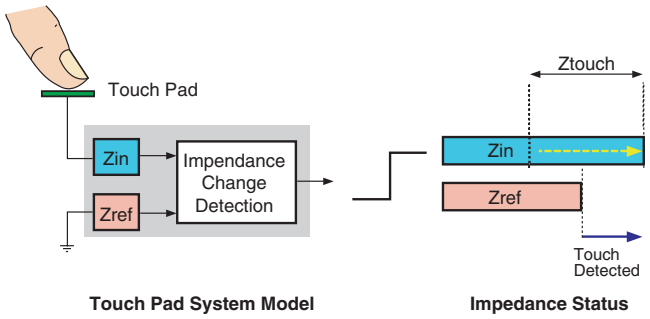


Figure 2: When a Pad is Touched.

As shown in Figure 1, if the pad is not touched, the impedance of the sensor input Zin should be kept less than the impedance of the reference Zref. If the pad is touched, as shown in Figure 2, Zin is increased by Ztouch. When Ztouch by touching becomes greater than the difference of Zin and Zref in the not touched state, i.e., if Zin in touched state becomes greater than Zref by a value higher than 0.078pF, the ICD (Impedance Change Detection) engine within the chip generates the acknowledged output signal indicating it senses the touch.

$$IDC = \begin{cases} 1, \text{ if } Zin - Zref > 0.078pF \\ 0, \text{ otherwise} \end{cases}$$

Notice the value of 0.078pF or higher is needed to maintain stable output against various noises. The sensor input impedance, Zin, includes parasitic capacitance of the input line, tuning capacitance of input pin and on-chip input impedance, while Zref includes on-chip impedance, AIC control values and external tuning capacitance if necessary.

AIC™ (Automatic Impedance Calibration)

Automatic Impedance Calibration (AIC) maintains consistent sensitivity against external environmental changes such as temperature, supply voltage and current, humidity, and system-level variations. This helps users develop their applications more conveniently by providing the actual impedance value of each sensor input. For developers, a Tuning Viewer program is provided, which helps to optimize the PCB design and to decide AIC input parameters. More detailed information is available in the FM1127 Tuning Guide.

The ICD engine residing in the FMA1127DA controls reference impedance values for each sensor input pin by acquiring each input impedance data. It periodically updates all reference impedance values under the condition that all twelve touch pads remain in no-touched status. This auto-calibration function absorbs environmental changes and guarantees product stability.

APIS™ Touch Output

When touch pads are arranged too closely to each other, it is sometimes difficult to identify which pad is touched. APIS™ (Adjacent Pattern Interference Suppression) is a filtering function to identify which pads are intentionally touched. If APIS mode is not defined, all touch data without APIS filtering are transmitted to the MCU. For example, if the application is a numeric keypad, the user can use the APIS mode1 to get the strongest output and filter out all other weakly touched inputs. Without APIS, the host may have to do this filtering function. APIS reduces the burden of the host computing time.

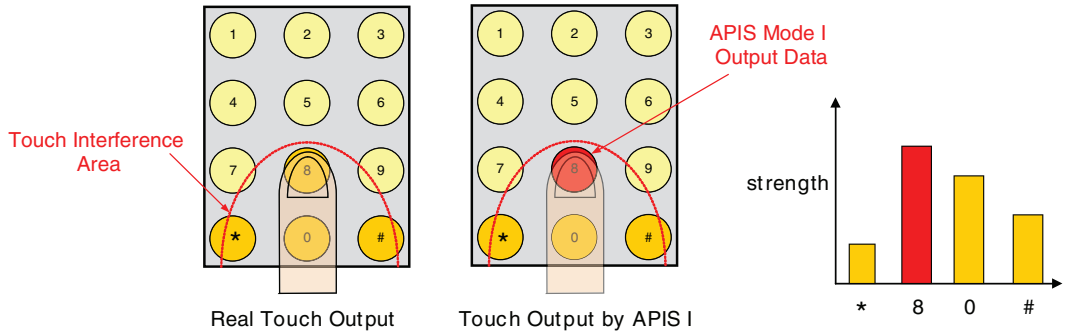
There are three modes in APIS:

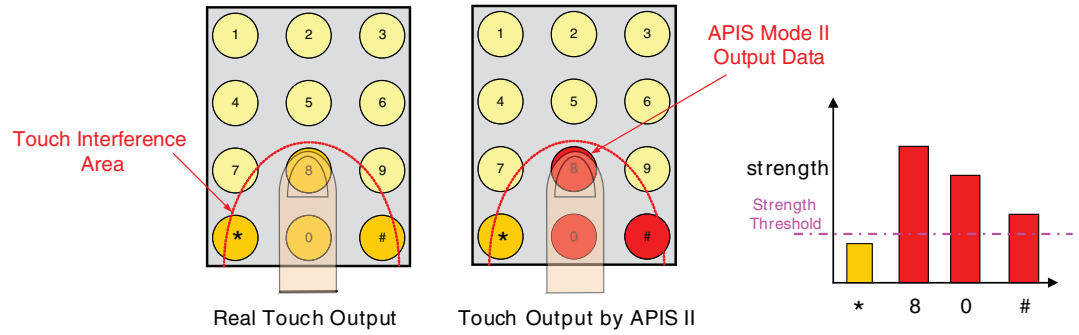
APIS mode 1: reports the strongest output only (Figure 3).

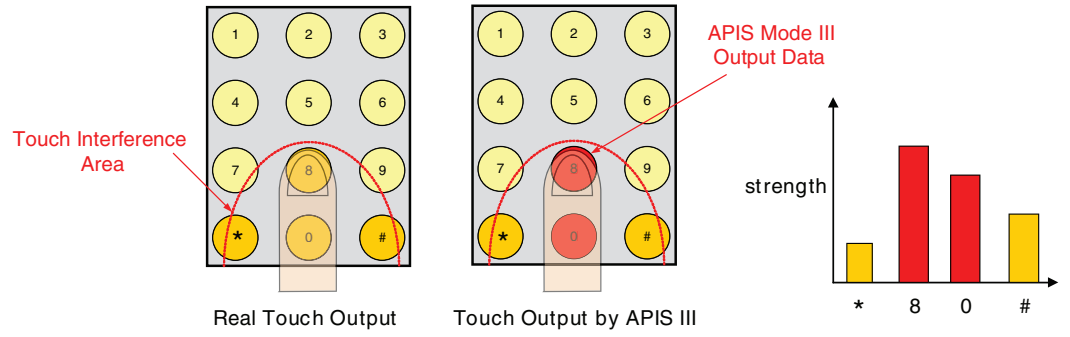
APIS mode 2: reports all outputs that exceeds pre-defined thresholds (value of Strength Threshold register) (Figure 4).

APIS mode 3: reports two strongest outputs (suitable for multi-touch applications) (Figure 5).

All three modes are described in the Figures below. The red-colored circles and bars show the output.







Functional Characteristics

	Active to Idle	Idle to Active	Active to Sleep	Idle to Sleep	Sleep to Active
System Clock: 1.6MHz, Sensor Clock: 20kHz	0.25 x A sec.	Min: 2ns, Max: 10ms	1ns	1ns	10µs
System Clock: 1.6MHz, Sensor Clock: 10kHz	0.5 x A sec.	Min: 2ns, Max: 20ms	1ns	1ns	10µs
System Clock: 800kHz, Sensor Clock: 10kHz	0.5 x A sec.	Min: 2ns, Max: 20ms	1ns	1ns	10µs
System Clock: 800Hz, Sensor Clock: 5kHz	1 x A sec.	Min: 2ns, Max: 40ms	1ns	1ns	10µs
System Clock: 400kHz, Sensor Clock: 5kHz	1 x A sec.	Min: 2ns, Max: 40ms	1ns	1ns	10µs
System Clock: 400kHz, Sensor Clock: 2.5kHz	2 x A sec.	Min: 2ns, Max: 80ms	1ns	1ns	10µs
System Clock: 200kHz, Sensor Clock: 2.5kHz	2 x A sec.	Min: 2ns, Max: 80ms	1ns	1ns	10µs
System Clock: 200kHz, Sensor Clock: 1.25kHz	4 x A sec.	Min: 2ns, Max: 160ms	1ns	1ns	10µs

A = IDLE Time Register Value

Communication Specifications for I²C

Table 1: DC Electrical Specifications for I²C Bus

Symbol	Parameter	Standard-Mode		Fast-Mode		Unit
		Min.	Max.	Min.	Max	
V_{IL}	LOW Level Input Voltage:					
	Fixed Input Levels	-0.5	1.5	n/a	n/a	V
	V_{DD} Related Input Levels	-0.5	0.3 V_{DD}	-0.5	0.3 x V_{DD}(1)	V
V_{IH}	HIGH Level Input Voltage:					
	Fixed Input Levels	3.0	(2)	n/a	n/a	V
	V_{DD} Related Input Levels	0.7 x V_{DD}	(2)	0.7 x V_{DD}	(2)	V
V_{hys}	Hysteresis of Schmitt Trigger Inputs:					
	V_{DD} > 2V	3.0	(2)	n/a	n/a	V
	V_{DD} < 2V	0.7 x V_{DD}	(2)	0.7 x V_{DD}	(2)	V
(6)V_{OL1} (6)V_{OL3}	LOW Level Output Voltage (open drain or collector) at 3mA Sink Current:					
	V_{DD} > 2V	0	0.4	0	0.4	V
	V_{DD} < 2V	n/a	n/a	0	0.2 x V_{DD}	V
Iol	Digital Output Low Current at					
	Vol = 0.6V		8.4		8.4	mA
	Vol = 0.4V		5.7		5.7	mA
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax} with a Bus Capacitance from 10pF to 400pF		250(4)	20 + 0.1Cb(3)		ns
t_{sp}	Pulse Width of Spike Which Must be Suppressed by the Input Filter	n/a	n/a	0	50	ns
I_i	Input Current each I/O Pin with an Input Voltage Between 0.1V_{DD} and 0.9V V_{DDmax}	-10	10	-10(5)	10(5)	µA
C_i	Capacitance for Each I/O Pin		10		10	pF

Note:

1. Devices that use non-standard supply voltages which do not conform to the intended I²C bus system levels must relate their input levels to the V_{DD} voltage to which the pull-up resistors R_p are connected.
2. Maximum V_{IH} = V_{DDmax} + 0.5V.
3. C_b = capacitance of one bus line in pF.
4. The maximum t_f for the SDA and SCL bus lines quoted in Table 2 (300ns) is longer than the specified maximum t_{of} for the output stages (250ns). The allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Figure 6 without exceeding the maximum specified for t_f.
5. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.
6. VIH = 1.21V, VIL = 0.76V. Hence Hysteresis is about 0.45V at the condition of 500kHz input frequncey. Input Impedance C_{in} is about 2pF.

n/a = not applicable.

Table 2. AC Electrical Specifications for I²C Bus

Symbol	Parameter	Standard-Mode		Fast-Mode		Unit
		Min.	Max.	Min.	Max	
f_{SCL}	SCL Clock Frequency	0	100	0	400	kHz
$t_{HD:STA}$	Hold Time (repeated) START Condition. After this Period, the First Clock Pulse is Generated	4.0		0.6		µs
t_{LOW}	LOW Period of the SCL Clock	4.7		1.3		µs
t_{HIGH}	HIGH Period of the SCL Clock	4.0		0.6		µs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	4.7		0.6		µs
$t_{HD:DAT}$	Data Hold Time:					
	For CBUS Compatible Master	5.0	–	–	–	µs
	For I²C Bus Devices	2(2)	3.45(3)	0(2)	0.9(3)	µs
$t_{SU:DAT}$	Data Setup Time	250		100(4)		ns
t_r	Rise Time of Both SDA and SCL Signals		1000	$20 + 0.1C_b$(5)	300	ns
t_f	Fall Time of Both SDA and SCL Signals		300	$20 + 0.1C_b$(5)	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	4.0		0.6		µs
f_{BUF}	Bus Free Time Between a STOP and START Condition	4.7		1.3		µs
C_b	Capacitive Load for Each Bus Line		400		400	pF
V_{nL}	Noise Margin at the LOW Level for Each Connected Device (including Hysteresis)	0.1 x V_{DD}		0.1 x V_{DD}		V
V_{nH}	Noise Margin at the HIGH Level for Each Connected Device (including Hysteresis)	0.2 x V_{DD}		0.2 x V_{DD}		V

Notes:

1. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 1).
2. A device must internally provide a hold time of al least 300ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined regions of the falling edge of SCL.
3. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU:DAT}$ Š 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{max} + t_{SU:DAT} = 1{,}000 + 250 = 1{,}250$ns (according to the Standard-mode I²C bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according the Table 2 are allowed.

n/a = not applicable.

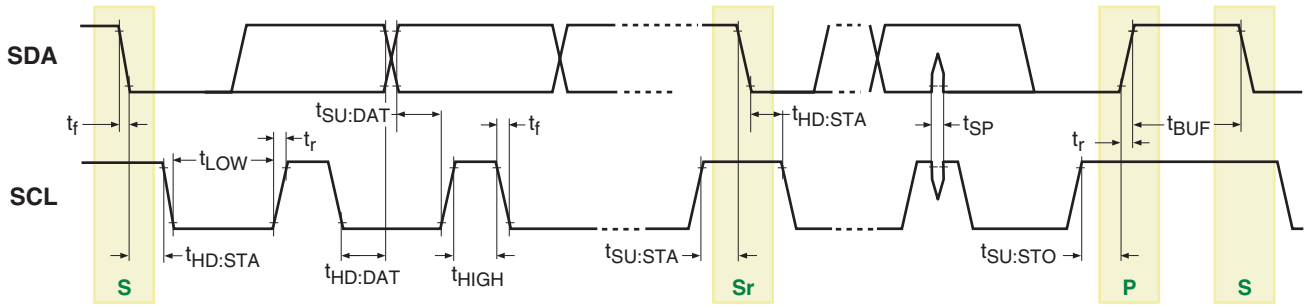
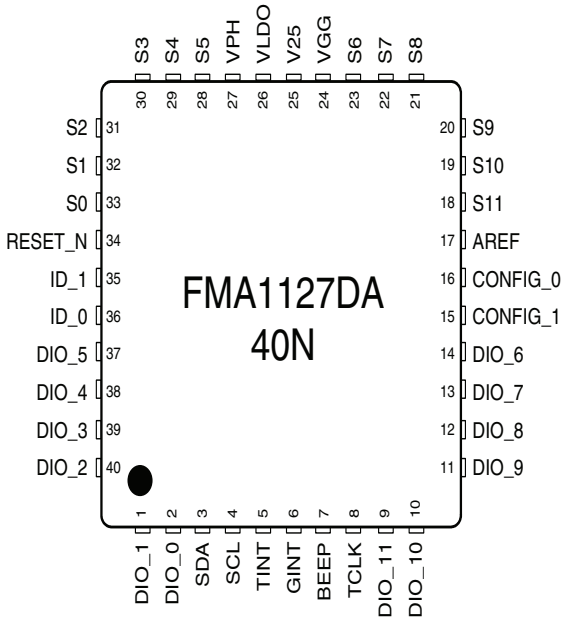


Figure 6: Definition of Timing for F/S-mode Devices on the I²C-Bus

Application Information

Top View of 40-pin Package (40QFN)



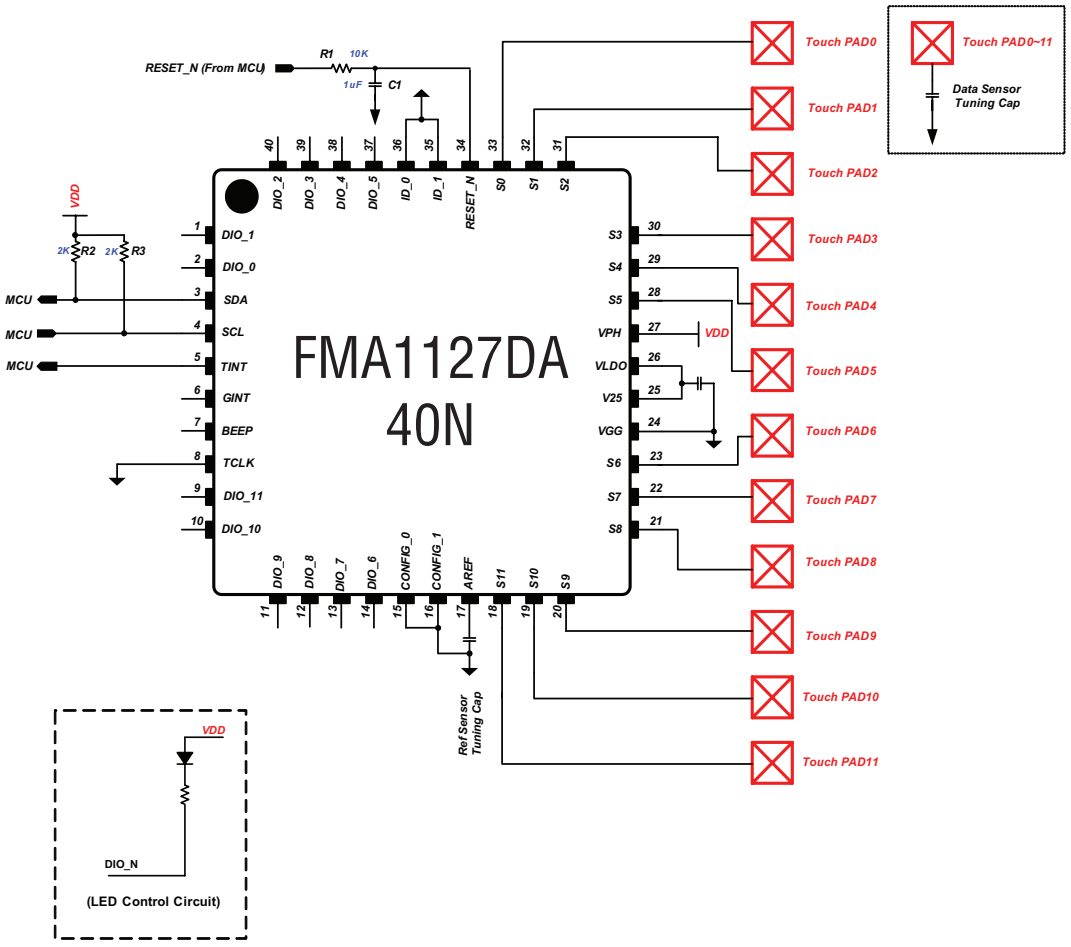
40-Pin QFN

Pin Description

Name	IO	Pin #	Description
RESET_N	I	34	Reset, active LOW
TCLK	I	8	External clock Input. Should be grounded if not used.
S	I	18-23 28-33	Twelve Sensor Inputs from external Touch Pads.
A_REF	I	17	Reference Input.
DIO	IO	1, 2, 9–14, 38–40	Configured by HOST: - extended GPIOs, Direct Button Outputs or External Interrupt inputs
SDA	IO	3	Bidirectional I²C Data from/to Host
SCL	I	4	I²C CLK from Host
TINT	O	5	Touch Interrupt, it can be generated when touch status is changed.
GINT	O	6	General Interrupts including touch interrupt and EINT. Can be masked.
BEEP	O	7	Beep Output.
ID	I	35, 36	I²C Chip ID Select(00:0x58, 01:0x59, 10:0x5A, 11:0x5B)
CONFIG	I	15,16	Test pins. Should be grounded.
VPH	P	27	Power (2.3V-5.5V)
VLDO	O	26	2.5V Regulator Power Output
V25	P	25	2.5V Power Input
VSS	P	24	Ground

Touch Sensor Controller

Typical Application Circuit



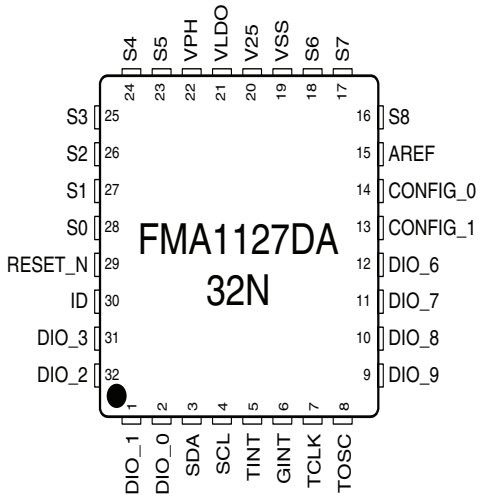
Notes:

- The voltage range of VDD can be from 2.3V to 5.5V. If internal LDO is used, it should be from 3V to 5.5V.
- Pull-Up resistors are required for I2C communication. For 5V application, 2K ohm resistor is typically used. For 3V application, 1K ohm resistor is typically used.
- Each tuning capacitor is an optional component depending on PCB layout environment.
- The circuit above is a typical application circuit using an internal LDO.
- RESET_N pin should be connected to host MCU GPIO and needs an RC filter. (R1=10KΩ, C1=1uF)
- For LED control through DIO ports, sink current circuit is mandatory as shown above.
- I2C has no recovery specification when clk is attacked by noise glitch or ESD. Sometimes 'additional' clock by noise glitch generates unintentional START condition which causes the TSC to wait indefinitely.

  Recommendations to avoid such a noise glitch:

  1. Addition of serial resister on I2C clock line and data line having values ranging from 100ohm to 500ohm.
  2. Addition of about capacitor on I2C clock line and data line and connect other end to ground. This would add some filtering mechanism. The size of capacitor depends on existing parasitic capacitance of the board (~Value ranging from 30pf to 300pf).

Top View of 32-pin Package (32QFN)

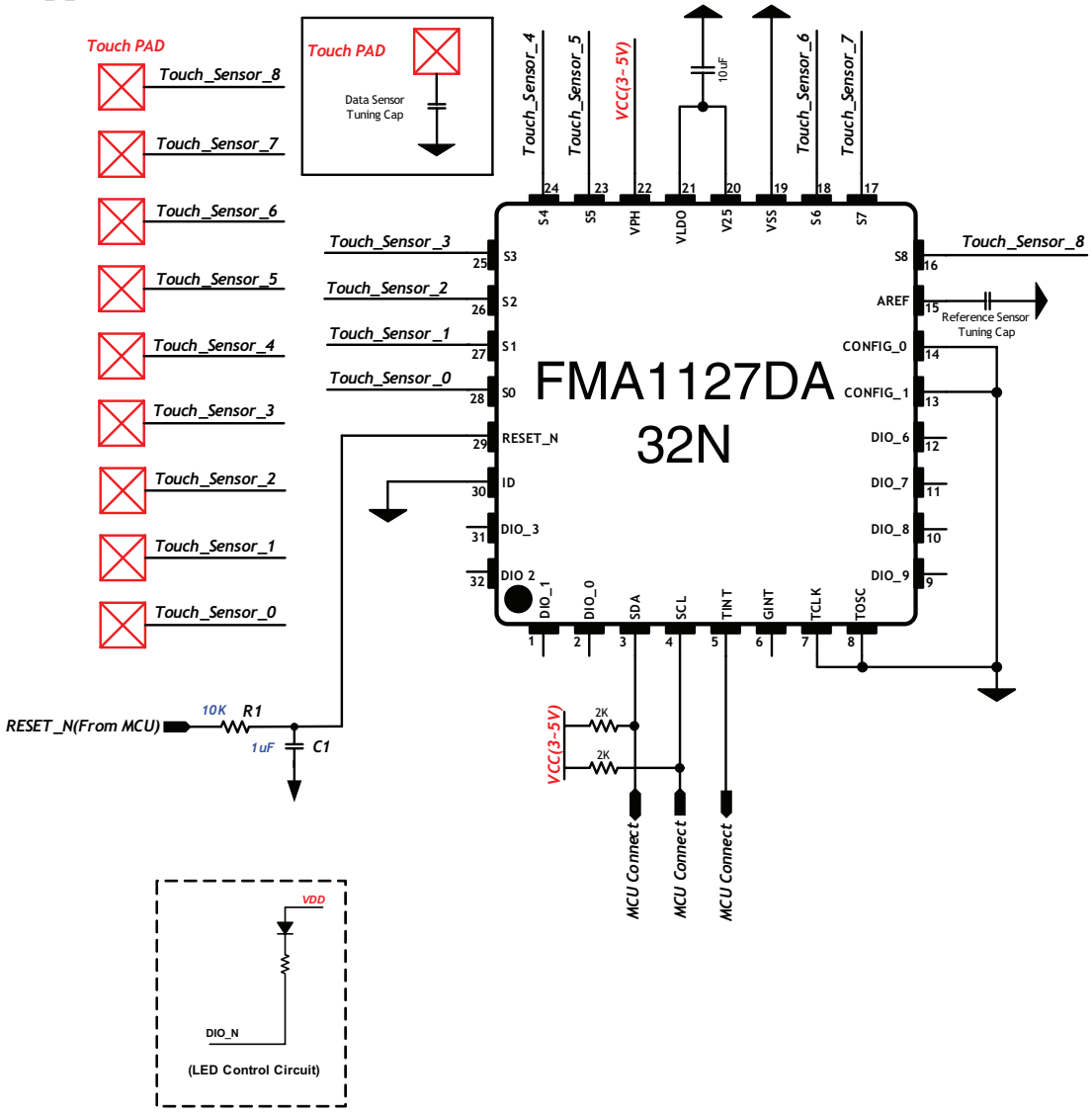


Pin Description

Name	IO	Pin #	Description
RESET_N	I	29	Reset, active LOW
TCLK	I	7	External Clock Input. Should be grounded if not used.
S	I	16–18, 23–28	Nine Sensor Inputs from external Touch Pads.
AREF	I	15	Reference Input.
DIO	IO	1, 2, 9–12, 31, 32	Configured by HOST: - extended GPIOs, Direct Button Outputs or External Interrupt inputs
SDA	IO	3	Bidirectional I²C Data from/to Host
SCL	I	4	I²C CLK from Host
TINT	O	5	Touch Interrupt, it can be generated when touch status is changed.
GINT	O	6	General Interrupts including touch interrupt and EINT. Can be masked.
TOSC	I	8	Test Pin, Should be grounded.
ID	I	30	I²C Chip ID Select(0:0x58, 1:0x5B)
CONFIG	I	13, 14	Test pins. Should be grounded.
VPH	P	22	Power (2.5V~5.5V)
VLDO	O	21	2.5V Regulator Power Output
V25	P	20	2.5V Power Input
VSS	P	19	Ground

Touch Sensor Controller

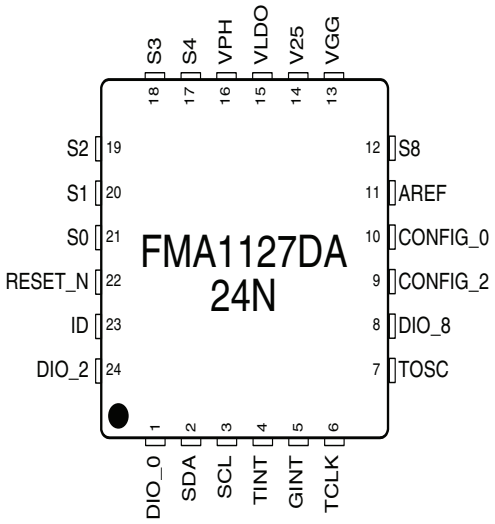
Typical Application Circuit



Notes:

- The voltage range of VDD can be from 2.3V to 5.5V. If internal LDO is used, it should be from 3V to 5.5V.
- Pull-Up resistors are required for I²C communication. For 5V application, 2K ohm resistor is typically used. For 3V application, 1K ohm resistor is typically used.
- Each tuning capacitor is an optional component depending on PCB layout environment.
- The circuit above is a typical application circuit using an internal LDO.
- RESET_N pin should be connected to host MCU GPIO and needs an RC filter. (R1=10KΩ, C1=1uF)
- For LED control through DIO ports, sink current circuit is mandatory as shown above.
- I²C has no recovery specification when clk is attacked by noise glitch or ESD. Sometimes 'additional' clock by noise glitch generates unintentional START condition which causes the TSC to wait indefinitely.
  Recommendations to avoid such a noise glitch:
  1. Addition of serial resister on I²C clock line and data line having values ranging from 100ohm to 500ohm.
  2. Addition of about capacitor on I²C clock line and data line and connect other end to ground. This would add some filtering mechanism. The size of capacitor depends on existing parasitic capacitance of the board (~Value ranging from 30pf to 300pf).

Top View of 24-pin Package (24QFN)

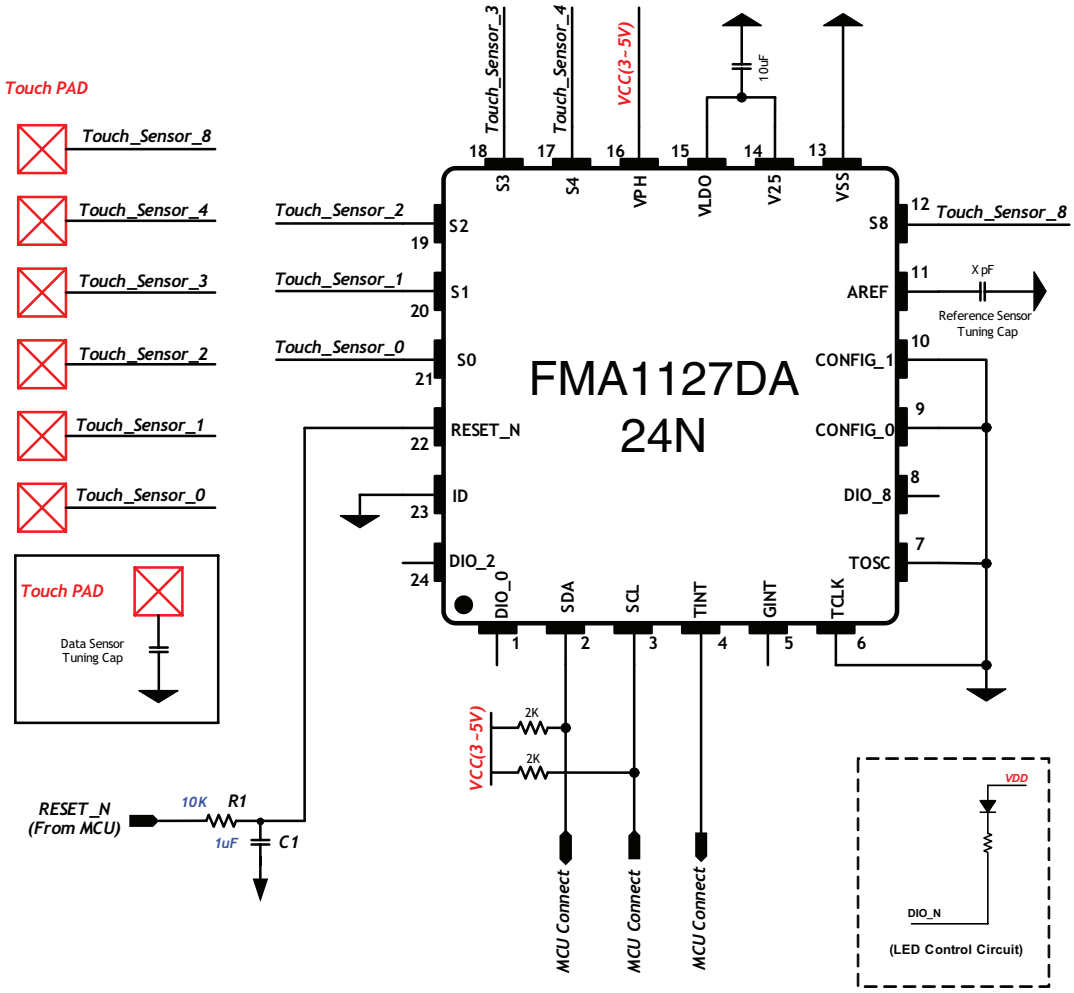


Pin Description

Name	IO	Pin #	Description
RESET_N	I	22	Reset, active LOW
TCLK	I	6	External Clock Input. Should be grounded if not used.
S	I	12, 17-21	Nine Sensor Inputs from external Touch Pads.
AREF	I	11	Reference Input.
DIO	IO	1, 8, 24	Configured by HOST: - extended GPIOs, Direct Button Outputs or External Interrupt inputs
SDA	IO	2	Bidirectional I²C Data from/to Host
SCL	I	3	I²C CLK from Host
TINT	O	4	Touch Interrupt, it can be generated when touch status is changed.
GINT	O	5	General Interrupts including touch interrupt and EINT. Can be masked.
TOSC	I	7	Test Pins. Should be grounded.
ID	I	23	I²C Chip ID Select(0:0x58, 1:0x5B)
CONFIG	I	9, 10	Test pins. Should be grounded.
VPH	P	16	Power (2.5V-5.5V)
VLDO	O	15	2.5V Regulator Power Output
V25	P	14	2.5V Power Input
VSS	P	13	Ground

Touch Sensor Controller

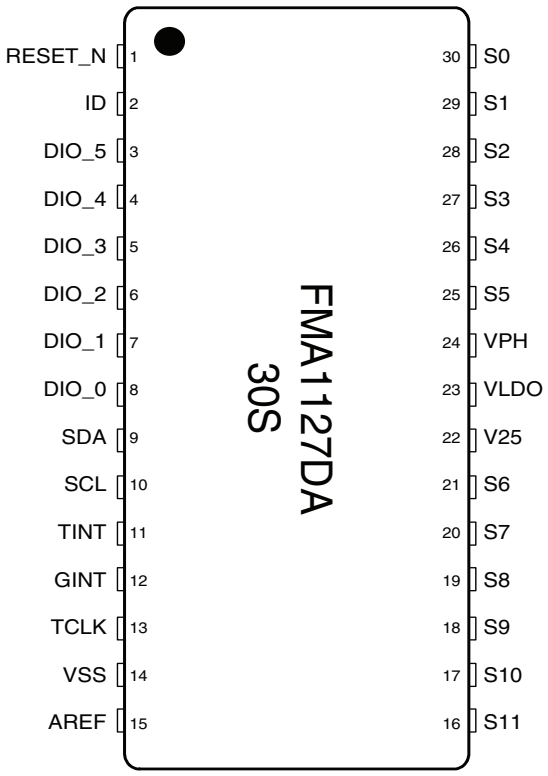
Typical Application Circuit



Notes:

- The voltage range of VDD can be from 2.3V to 5.5V. If internal LDO is used, it should be from 3V to 5.5V.
- Pull-Up resistors are required for I2C communication. For 5V application, 2K ohm resistor is typically used. For 3V application, 1K ohm resistor is typically used.
- Each tuning capacitor is an optional component depending on PCB layout environment.
- The circuit above is a typical application circuit using an internal LDO.
- RESET_N pin should be connected to host MCU GPIO and needs an RC filter. (R1=10KΩ, C1=1uF)
- For LED control through DIO ports, sink current circuit is mandatory as shown above.
- I2C has no recovery specification when clk is attacked by noise glitch or ESD. Sometimes 'additional' clock by noise glitch generates unintentional START condition which causes the TSC to wait indefinitely.
  Recommendations to avoid such a noise glitch:
  1. Addition of serial resister on I2C clock line and data line having values ranging from 100ohm to 500ohm.
  2. Addition of about capacitor on I2C clock line and data line and connect other end to ground. This would add some filtering mechanism. The size of capacitor depends on existing parasitic capacitance of the board (~Value ranging from 30pf to 300pf).

Top View of 30-pin Package (30SSOP)



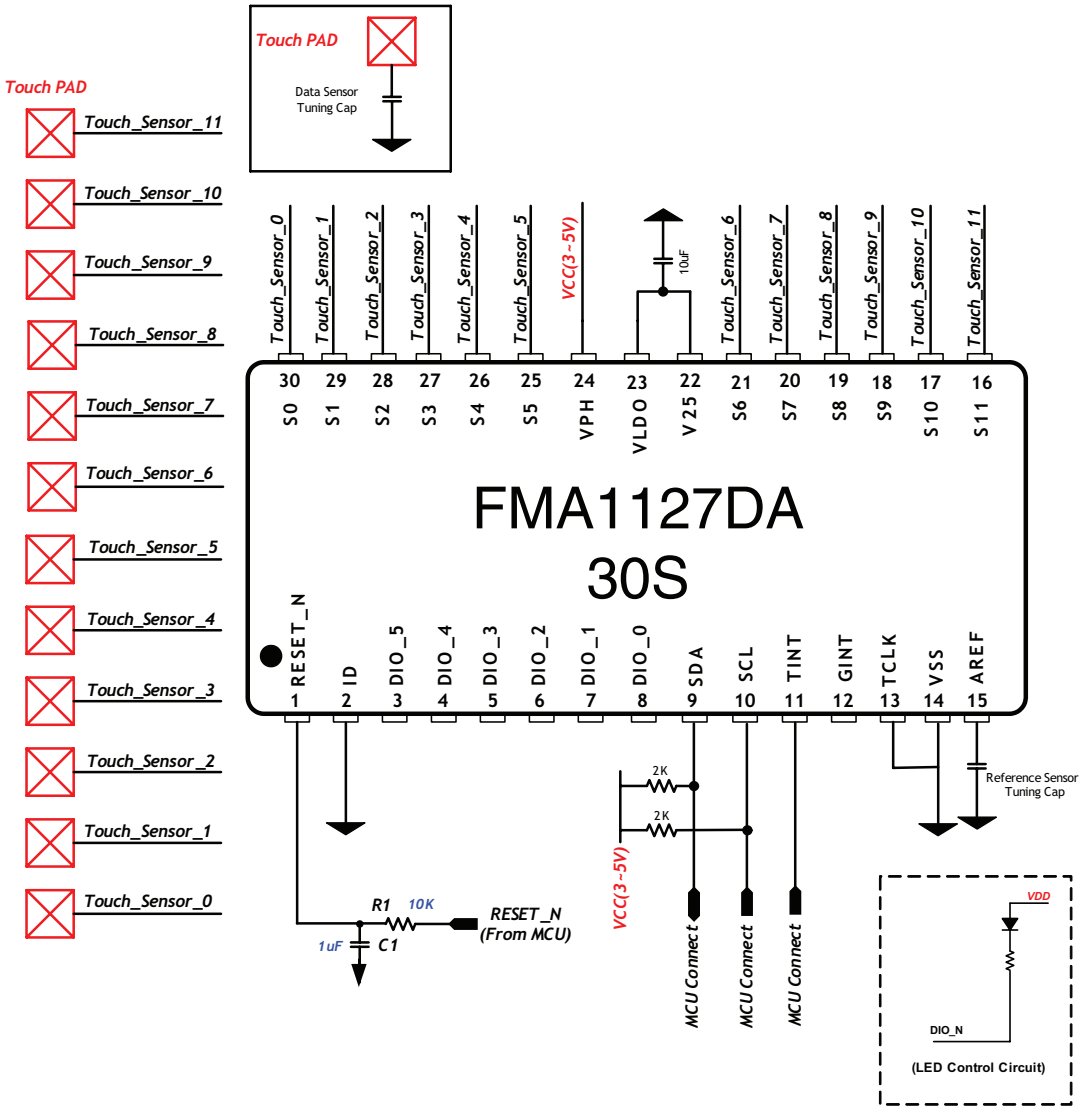
30-Pin SSOP

Pin Description

Name	IO	Pin #	Description
RESET_N	I	1	Reset, active LOW
TCLK	I	13	External Clock Input. Should be grounded if not used.
S	I	16–21, 25–30	Twelve Sensor Inputs from external Touch Pads.
AREF	I	15	Reference Input.
DIO	IO	3–8	Configured by HOST as below: -extended GPIOs, Direct Button Outputs or External Interrupt inputs
SDA	IO	9	Bidirectional I²C Data from/to Host
SCL	I	10	I²C CLK from Host
TINT	O	11	Touch Interrupt, it can be generated when touch status is changed.
GINT	O	12	General Interrupts including touch interrupt and EINT. Can be masked.
ID	I	2	I²C Chip ID Select(0:0x58, 1:0x5B)
VPH	P	24	Power (2.5V~5.5V)
VLDO	O	23	2.5V Regulator Power Output
V25	P	22	2.5V Power Input
VSS	P	14	Ground

Touch Sensor Controller

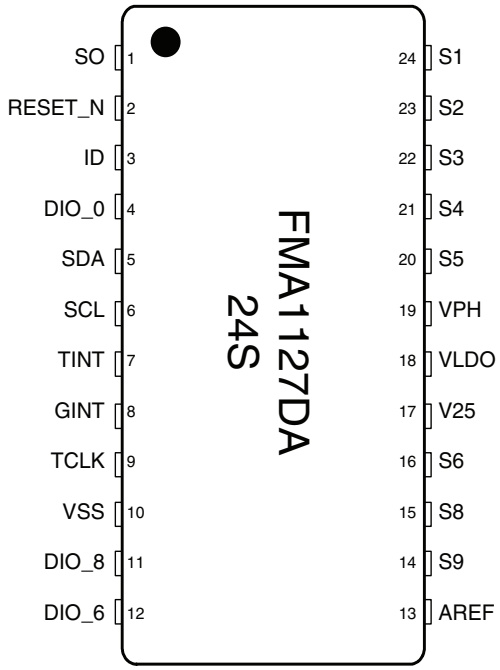
Typical Application Circuit



Notes:

- The voltage range of VDD can be from 2.3V to 5.5V. If internal LDO is used, it should be from 3V to 5.5V.
- Pull-Up resistors are required for I²C communication. For 5V application, 2K ohm resistor is typically used. For 3V application, 1K ohm resistor is typically used.
- Each tuning capacitor is an optional component depending on PCB layout environment.
- The circuit above is a typical application circuit using an internal LDO.
- RESET_N pin should be connected to host MCU GPIO and needs an RC filter. (R1=10KΩ, C1=1uF)
- For LED control through DIO ports, sink current circuit is mandatory as shown above.
- I²C has no recovery specification when clk is attacked by noise glitch or ESD. Sometimes 'additional' clock by noise glitch generates unintentional START condition which causes the TSC to wait indefinitely.
  Recommendations to avoid such a noise glitch:
  1. Addition of serial resister on I²C clock line and data line having values ranging from 100ohm to 500ohm.
  2. Addition of about capacitor on I²C clock line and data line and connect other end to ground. This would add some filtering mechanism. The size of capacitor depends on existing parasitic capacitance of the board (~Value ranging from 30pf to 300pf).

Top View of 24-pin Package (24SSOP)

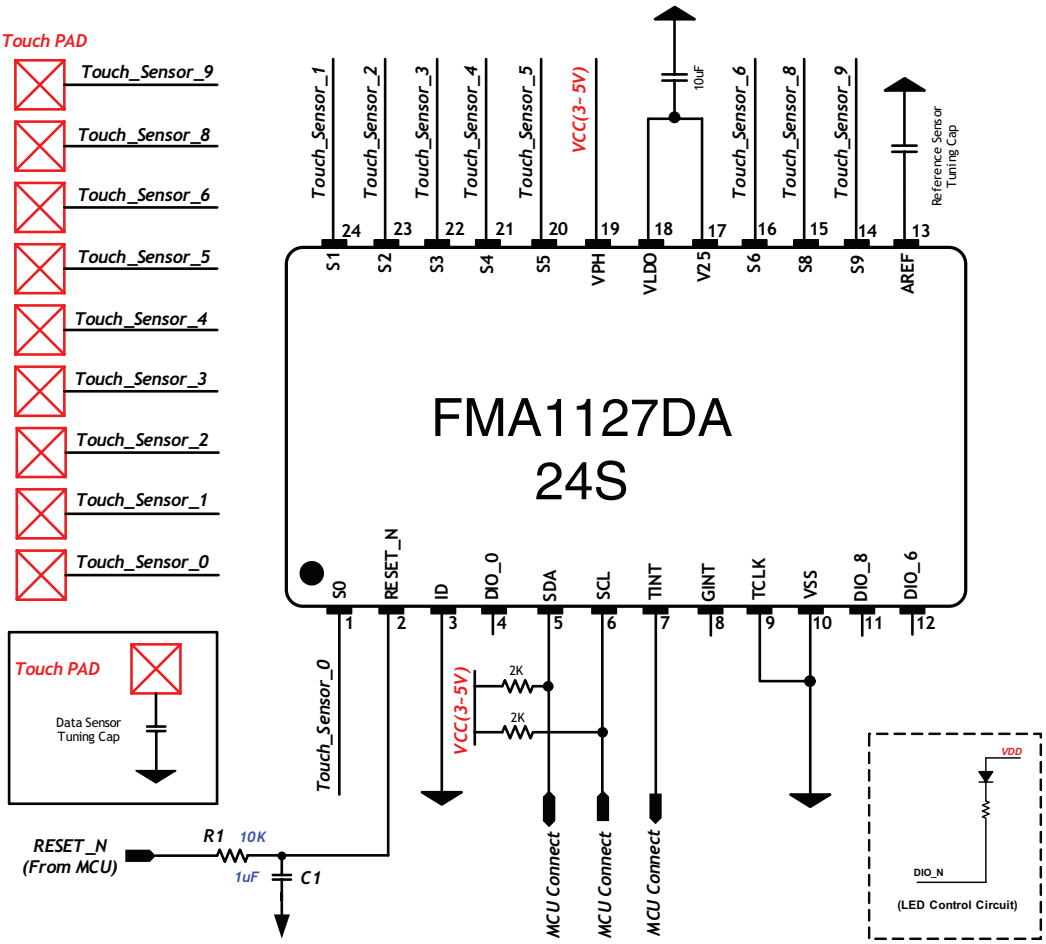


Pin Description

Name	IO	Pin #	Description
RESET_N	I	2	Reset, active LOW
TCLK	I	9	External Clock Input. Should be grounded if not used.
S	I	1, 14–16, 20–24	Nine Sensor Inputs from external Touch Pads.
AREF	I	13	Reference Input.
DIO	IO	4, 11, 12	Configured by HOST: -extended GPIOs, Direct Button Outputs or External Interrupt inputs
SDA	IO	5	Bidirectional I²C Data from/to Host
SCL	I	6	I²C CLK from Host
TINT	O	7	Touch Interrupt, it can be generated when touch status is changed.
GINT	O	8	General Interrupts including touch interrupt, and they can be masked.
ID	I	3	I²C Chip ID Select(0:0x58, 1:0x5B)
VPH	P	19	Power (2.5V-5.5V)
VLDO	O	18	2.5V Regulator Power Output
V25	P	17	2.5V Power Input
VSS	P	10	Ground

Touch Sensor Controller

Typical Application Circuit

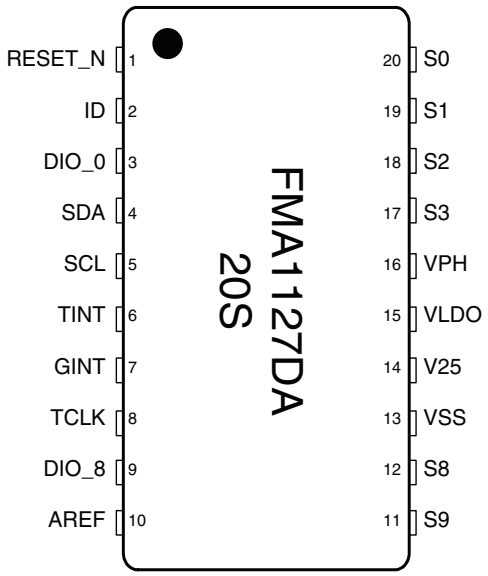


Notes:

- The voltage range of VDD can be from 2.3V to 5.5V. If internal LDO is used, it should be from 3V to 5.5V.
- Pull-Up resistors are required for I²C communication. For 5V application, 2K ohm resistor is typically used. For 3V application, 1K ohm resistor is typically used.
- Each tuning capacitor is an optional component depending on PCB layout environment.
- The circuit above is a typical application circuit using an internal LDO.
- RESET_N pin should be connected to host MCU GPIO and needs an RC filter. (R1=10KΩ, C1=1uF)
- For LED control through DIO ports, sink current circuit is mandatory as shown above.
- I²C has no recovery specification when clk is attacked by noise glitch or ESD. Sometimes 'additional' clock by noise glitch generates unintentional START condition which causes the TSC to wait indefinitely.

  Recommendations to avoid such a noise glitch:
  1. Addition of serial resister on I²C clock line and data line having values ranging from 100ohm to 500ohm.
  2. Addition of about capacitor on I²C clock line and data line and connect other end to ground. This would add some filtering mechanism. The size of capacitor depends on existing parasitic capacitance of the board (~Value ranging from 30pf to 300pf).

Top View of 20-pin Package (20SSOP)

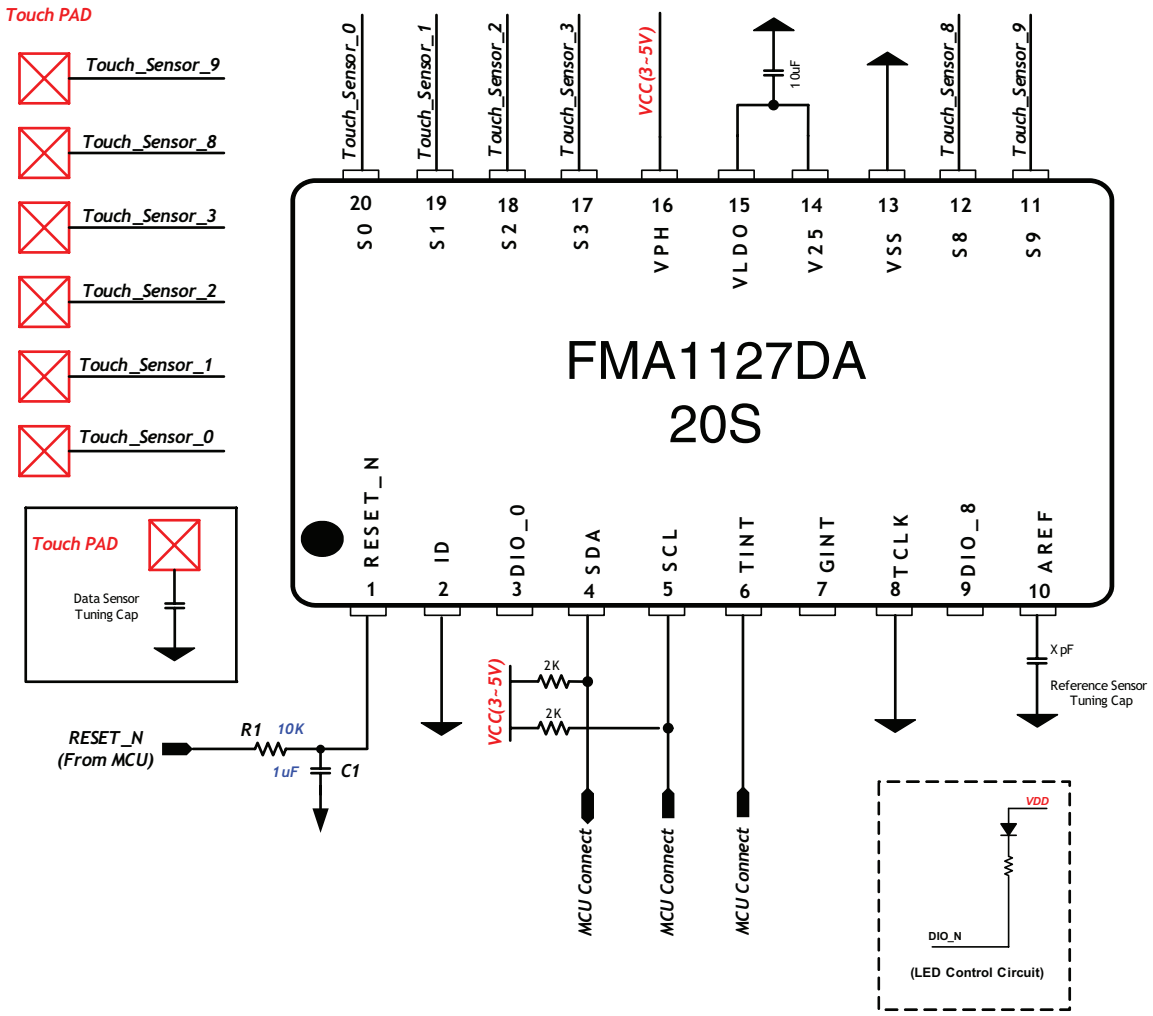


Pin Description

Name	IO	Pin #	Description
RESET_N	I	1	Reset, active LOW
TCLK	I	8	External Clock Input. Should be grounded if not used.
S	I	11-12, 17-20	Six Sensor Inputs from external Touch Pads.
AREF	I	10	Reference Input.
DIO	IO	3, 9	Configured by HOST: -extended GPIOs, Direct Button Outputs or External Interrupt inputs
SDA	IO	4	Bidirectional I²C Data from/to Host
SCL	I	5	I²C CLK from Host
TINT	O	6	Touch Interrupt, it can be generated when touch status is changed.
GINT	O	7	General Interrupts including touch interrupt, and they can be masked.
ID	I	2	I²C Chip ID Select(0:0x58, 1:0x5B)
VPH	P	16	Power (2.5V-5.5V)
VLDO	O	15	2.5V Regulator Power Output
V25	P	14	2.5V Power Input
VSS	P	13	Ground

Touch Sensor Controller

Typical Application Circuit



Notes:

- The voltage range of VDD can be from 2.3V to 5.5V. If internal LDO is used, it should be from 3V to 5.5V.
- Pull-Up resistors are required for I2C communication. For 5V application, 2K ohm resistor is typically used. For 3V application, 1K ohm resistor is typically used.
- Each tuning capacitor is an optional component depending on PCB layout environment.
- The circuit above is a typical application circuit using an internal LDO.
- RESET_N pin should be connected to host MCU GPIO and needs an RC filter. (R1=10KΩ, C1=1uF)
- For LED control through DIO ports, sink current circuit is mandatory as shown above.
- I2C has no recovery specification when clk is attacked by noise glitch or ESD. Sometimes 'additional' clock by noise glitch generates unintentional START condition which causes the TSC to wait indefinitely.

  Recommendations to avoid such a noise glitch:

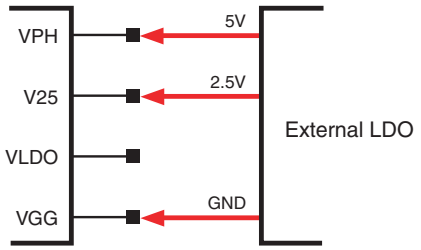
  1. Addition of serial resister on I2C clock line and data line having values ranging from 100ohm to 500ohm.
  2. Addition of about capacitor on I2C clock line and data line and connect other end to ground. This would add some filtering mechanism. The size of capacitor depends on existing parasitic capacitance of the board (~Value ranging from 30pf to 300pf).

Power Connection

There are two methods to supply power to the FMA1127DA touch sensor controller. One is to receive V25 core voltage from internal LDO and the other is to receive core voltage from an external power supply. In the case of using internal LDO, the LDO should be turned on in Sleep mode and hence it will cause slightly higher power consumption than using an external power supply for V25 core voltage.

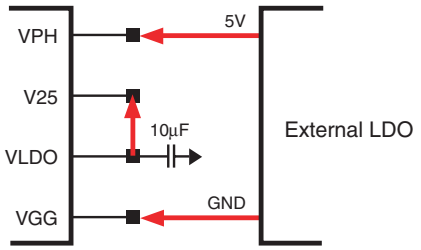
In Case E, if VPH receives 2.5V, internal LDO can not be used because VLDO can not output 2.5V when VPH receives 2.5V from external LDO.

Case A.
VPH: External 5V
VLDO: External 2.5V (Internal LDO Off: Register Control)



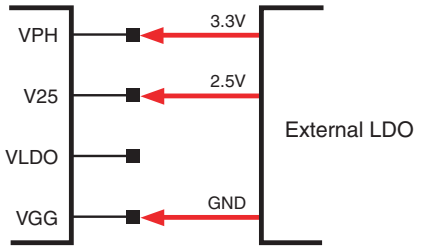
IO interface to over chip is 5V

Case B.
VPH: External 5V
VLDO: Internal LDO 2.5V



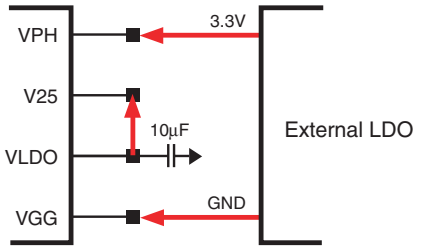
IO interface to over chip is 5V

Case C.
VPH: External 3.3V
VLDO: External 2.5V (Internal LDO Off: Register Control)



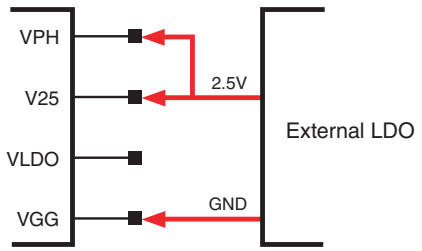
IO interface to over chip is 3.3V

Case D.
VPH: External 3.3V
VLDO: Internal LDO 2.5V



IO interface to over chip is 3.3V

Case E.
VPH: External 2.5V
VLDO: External 2.5V



IO interface to over chip is 2.5V

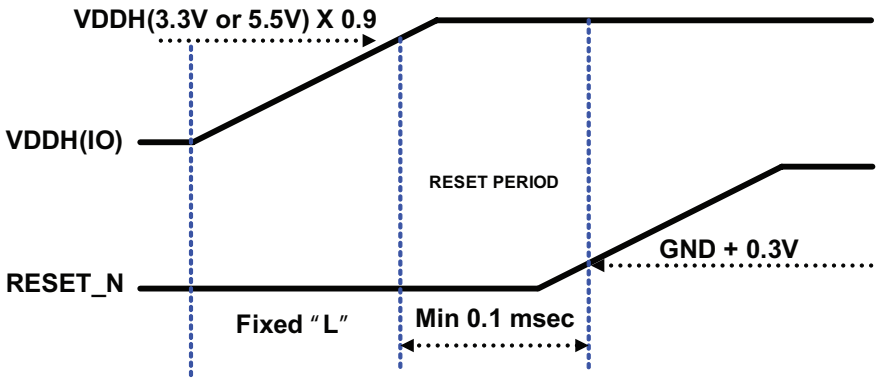
Power Sequence

To initialize the ATA2508DA properly, please refer to the Power Sequence below when the power is given initially during boot-up.

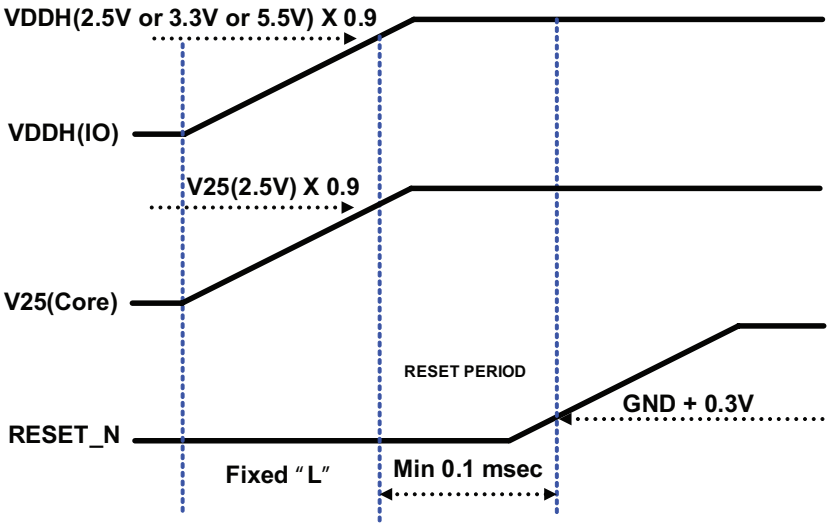
If the reset transition time during power on does not follow the time sequence below, the Internal LDO and oscillator would not operate normally.

The Power Sequence is based on the Power Connection type and is shown in the following example.

Power Connection Type is Case B or Case D



Power Connection type is Case A, Case C, or Case E



In order to delay RESET_N transition about 0.1msec than VDDH transition, 10KO resistor and 1uF capacitor should be attached on RESET_N pin. Please see the typical application circuits described in the previous chapter. Also note that pulse width of RESET_N which is active low and generated by MCU must be longer than 0.1msec to be valid RESET signal.

Register Map Summary

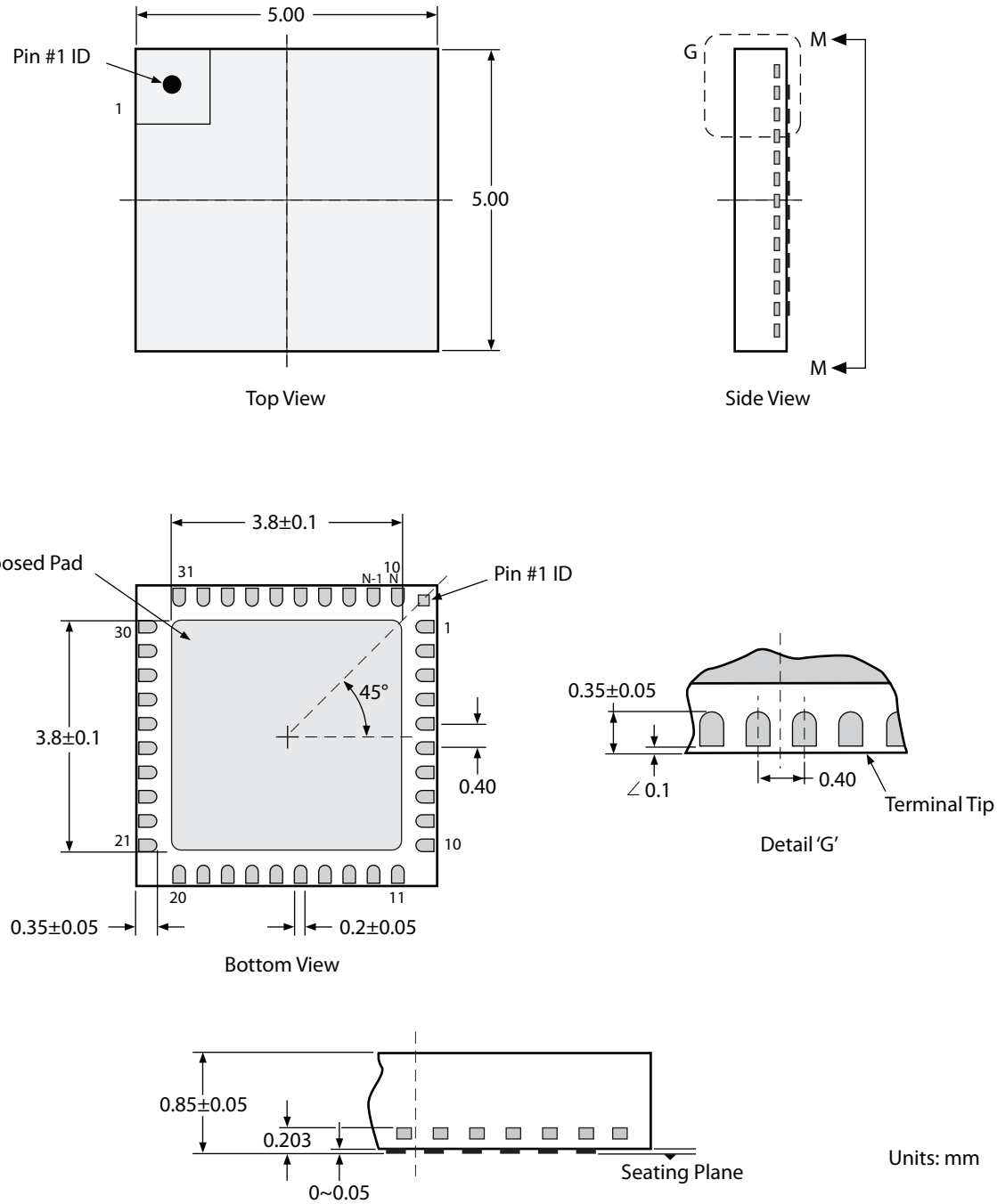
Ads	Reg Name	Ads	Reg Name	Ads	Reg Name
00	Feature	26	Strength Threshold 10	5E	Calibrated Impedance 2
01	ALPHA 0	27	Strength Threshold 11	5F	Calibrated Impedance 3
02	ALPHA 1	28	Sampling Interval	60	Calibrated Impedance 4
03	ALPHA 2	29	Integration Time	61	Calibrated Impedance 5
04	ALPHA 3	2A	IDLE Time	62	Calibrated Impedance 6
05	ALPHA 4	2C	MODE	63	Calibrated Impedance 7
06	ALPHA 5	2D	GPIO REG L	64	Calibrated Impedance 8
07	ALPHA 6	2E	GPIO REG H	65	Calibrated Impedance 9
08	ALPHA 7	2F	GPIO Configuration L	66	Calibrated Impedance 10
09	ALPHA 8	30	GPIO Configuration H	67	Calibrated Impedance 11
0A	ALPHA 9	31	GPIO Direction L	68	Impedance 0
0B	ALPHA 10	32	GPIO Direction H	69	Impedance 1
0C	ALPHA 11	33	Control	6A	Impedance 2
0D	BETA	34	Interrupt Mask	6B	Impedance 3
0E	COT	35	Interrupt Clear	6C	Impedance 4
0F	Reference Delay	36	Interrupt Edge	6D	Impedance 5
10	Hysteresis Delay 0	37	Control 2	6E	Impedance 6
11	Hysteresis Delay 1	38	Beep Period	6F	Impedance 7
12	Hysteresis Delay 2	39	Beep Frequency	70	Impedance 8
13	Hysteresis Delay 3	3A	Calibration Interval	71	Impedance 9
14	Hysteresis Delay 4	3B	EINT Enable	72	Impedance 10
15	Hysteresis Delay 5	3C	EINT Polarity	73	Impedance 11
16	Hysteresis Delay 6	3D	FILTER Period	74	Status
17	Hysteresis Delay 7	3E	FILTER Threshold	75	Touch Byte L
18	Hysteresis Delay 8	50	Strength 0	76	Touch Byte H
19	Hysteresis Delay 9	51	Strength 1	79	Interrupt Pending
1A	Hysteresis Delay 10	52	Strength 2	7A	GPIO IN L
1B	Hysteresis Delay 11	53	Strength 3	7B	GPIO IN H
1C	Strength Threshold 0	54	Strength 4	FA	BIAS OFF
1D	Strength Threshold 1	55	Strength 5	FB	BIAS ON
1E	Strength Threshold 2	56	Strength 6	FC	Wakeup SLEEP
1F	Strength Threshold 3	57	Strength 7	FD	Enter SLEEP
20	Strength Threshold 4	58	Strength 8	FE	Cold Reset
21	Strength Threshold 5	59	Strength 9	FF	Warm Reset
22	Strength Threshold 6	5A	Strength 10		
23	Strength Threshold 7	5B	Strength 11		
24	Strength Threshold 8	5C	Calibrated Impedance 0		
25	Strength Threshold 9	5D	Calibrated Impedance 1		

Notes:

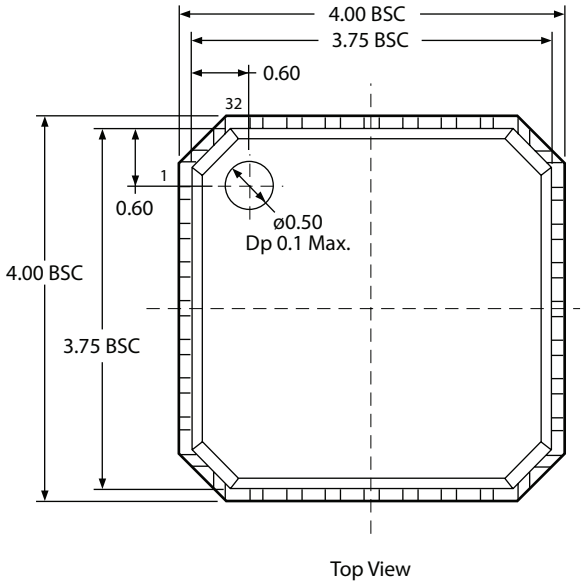
Please refer to the FMA1127DA Application Guide for detailed register descriptions.

Package Dimensions

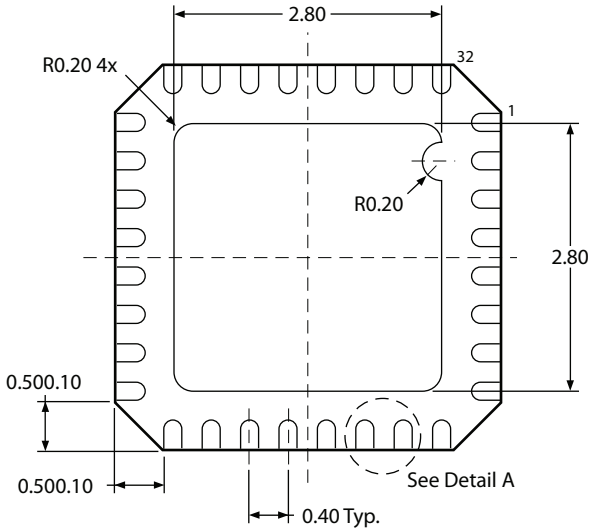
40QFN



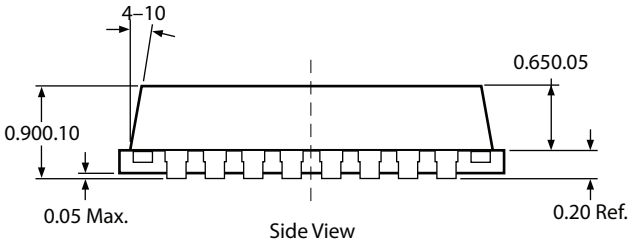
32QFN



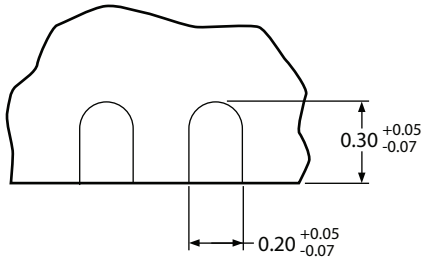
Top View



Bottom View



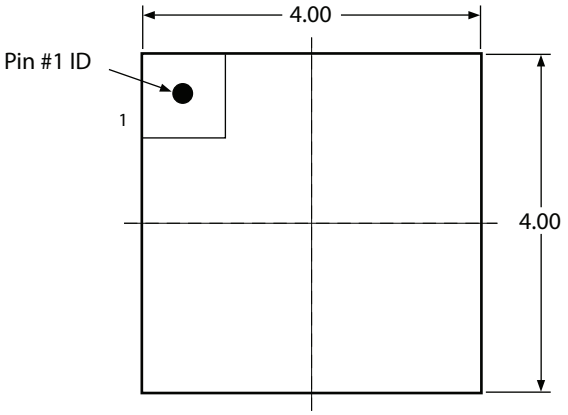
Side View



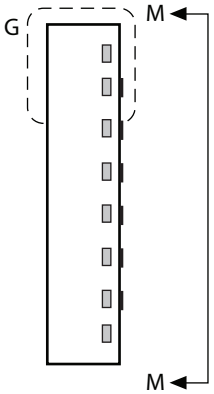
Detail 'A'

Units: mm

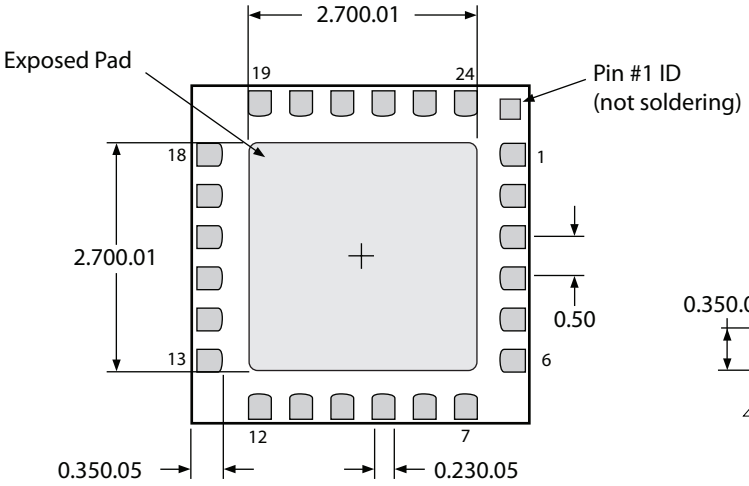
24QFN



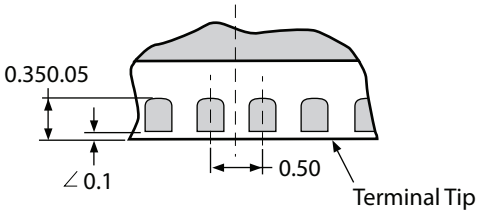
Top View



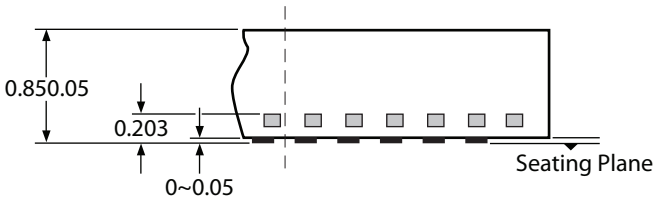
Side View



Bottom View

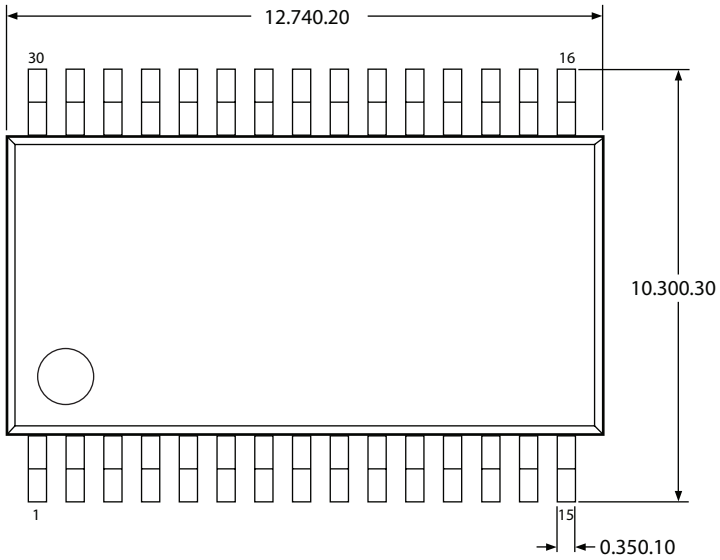


Detail 'G'

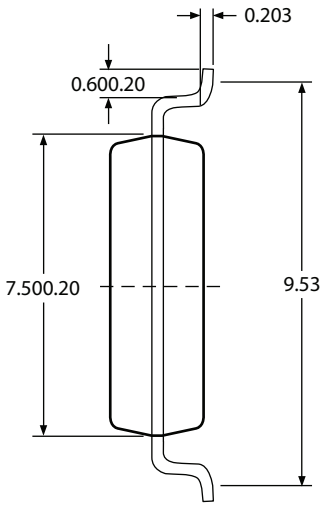


Units: mm

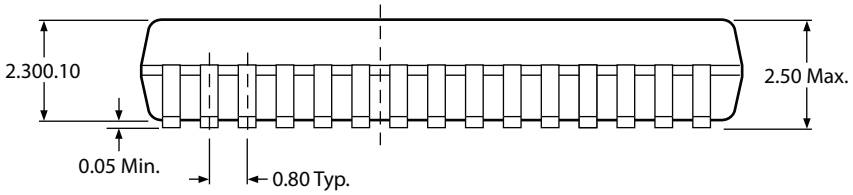
30SSOP



Top View



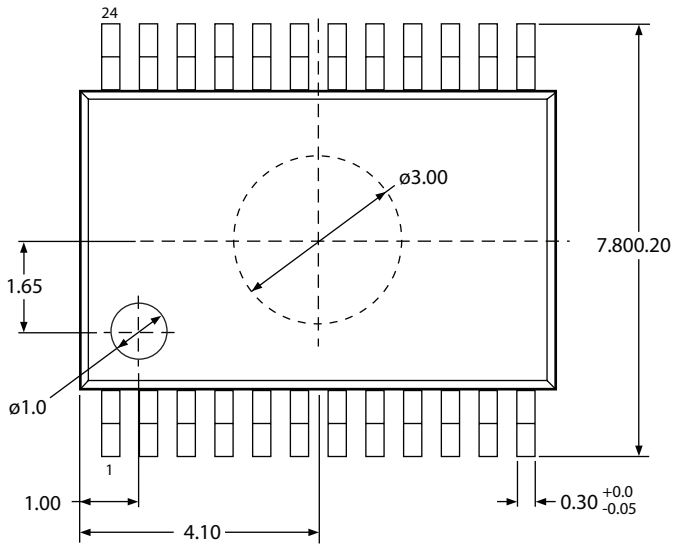
End View



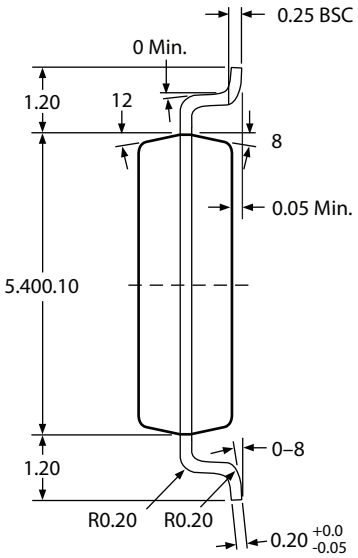
Side View

Units: mm

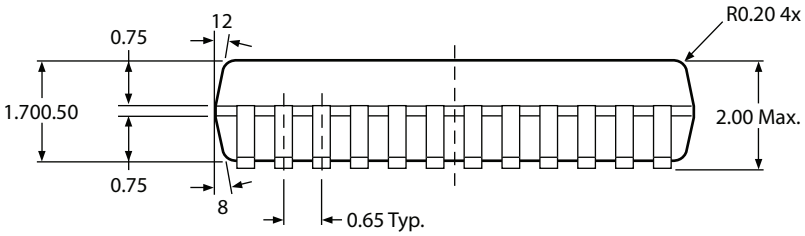
24SSOP



Top View



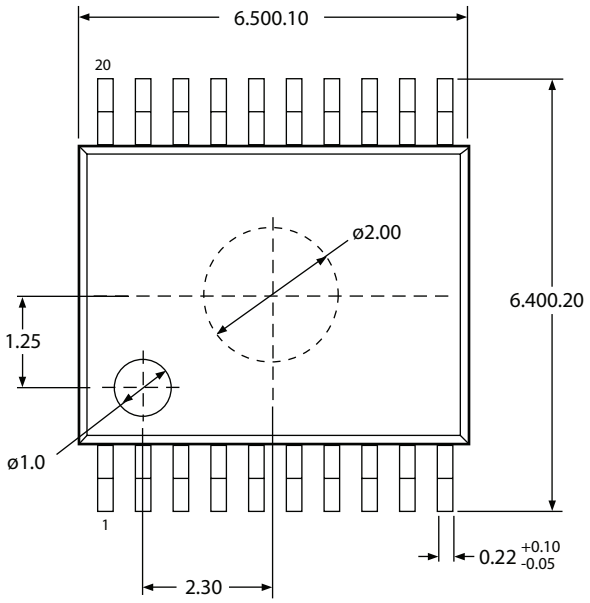
End View



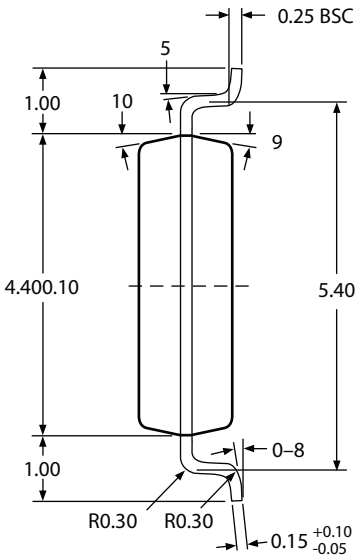
Side View

Units: mm

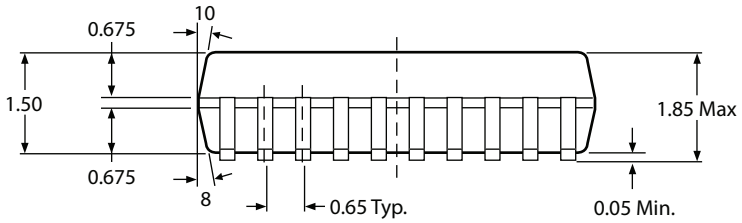
20SSOP



Top View



End View



Side View

Units: mm

Revision History

Date	Revision	Updates
November 16, 2007	V1.0	First Release
June 10, 2008	V1.1	Copy Updates
October 23, 2008	V1.2	Copy Updates
May 1, 2009	V1.3	Part number change
May 29, 2009	V1.4	Additions and updates
June 12, 2009	V2.0	Notations in Electrical Characteristics are changed. Power Sequence is added Notes in Typical Applications are changed. RESET_N pin connection is changed in Typical Applications. Pin descriptions are updated. Iol is added to Electrical Characteristics and I2C DC specification. Note6 is added to I2C DC specification. Cb in I2C AC specification is modified.

The FMA1127DA touch sensor controller is developed and owned by
ATLab Inc., South Korea, and is distributed by Fujitsu Microelectronics America, Inc.

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Printed in U.S.A. MCU-DS-21355-06/2009