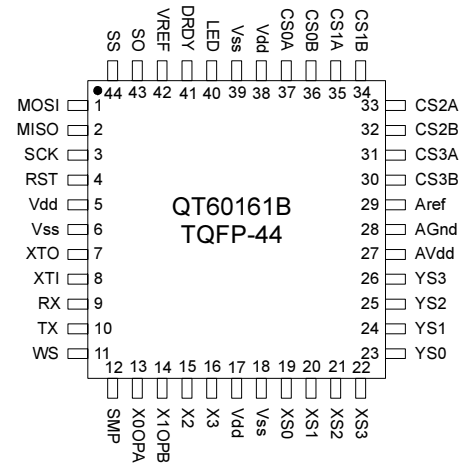# QT60161B
16 KEY QMatrix™ KEYPANEL SENSOR IC

- Advanced second generation QMatrix controller
- 16 touch keys through any dielectric
- 100% autocal for life - no adjustments required
- SPI Slave or Master/Slave interface to a host controller
- Parallel scan interface for electromechanical compatibility
- Keys individually adjustable for sensitivity, response time, and many other critical parameters
- Sleep mode with wake pin
- Synchronous noise suppression
- Mix and match key sizes & shapes in one panel
- Adjacent key suppression feature
- Panel thicknesses to 5 cm or more
- Low overhead communications protocol
- 44-pin TQFP package

Pin diagram (TQFP-44):

Top pins (left to right): SS, SO, VREF, DRDY, LED, Vss, Vdd, CS0A, CS0B, CS1A, CS1B

Left pins (top to bottom):
- MOSI — 1
- MISO — 2
- SCK — 3
- RST — 4
- Vdd — 5
- Vss — 6
- XTO — 7
- XTI — 8
- RX — 9
- TX — 10
- WS — 11

Right pins (top to bottom):
- CS2A — 33
- CS2B — 32
- CS3A — 31
- CS3B — 30
- Aref — 29
- AGnd — 28
- AVdd — 27
- YS3 — 26
- YS2 — 25
- YS1 — 24
- YS0 — 23

Center label: QT60161B TQFP-44

Top pin numbers: 44 43 42 41 40 39 38 37 36 35 34

Bottom pin numbers: 12 13 14 15 16 17 18 19 20 21 22

Bottom pins (left to right): SMP, X0OPA, X1OPB, X2, X3, Vdd, Vss, XS0, XS1, XS2, XS3

APPLICATIONS -

- Security keypanels
- Appliance controls
- ATM machines
- Automotive panels
- Industrial keyboards
- Outdoor keypads
- Touch-screens
- Machine tools

The QT60161B digital charge-transfer ("QT") QMatrix™ IC is designed to detect human touch on up 16 keys when used in conjunction with a scanned, passive X-Y matrix. It will project the keys through almost any dielectric, e.g. glass, plastic, stone, ceramic, and even wood, up to thicknesses of 5 cm or more. The touch areas are defined as simple 2-part interdigitated electrodes of conductive material, like copper or screened silver or carbon deposited on the rear of a control panel. Key sizes, shapes and placement are almost entirely arbitrary; sizes and shapes of keys can be mixed within a single panel of keys and can vary by a factor of 20:1 in surface area. The sensitivity of each key can be set individually via simple functions over the SPI or UART port, for example via Quantum's QmBtn program, or from a host microcontroller. Key setups are stored in an onboard eeprom and do not need to be reloaded with each powerup.

The device is designed specifically for appliances, electronic kiosks, security panels, portable instruments, machine tools, or similar products that are subject to environmental influences or even vandalism. It can permit the construction of 100% sealed, watertight control panels that are immune to humidity, temperature, dirt accumulation, or the physical deterioration of the panel surface from abrasion, chemicals, or abuse. To this end the device contains Quantum-pioneered adaptive auto self-calibration, drift compensation, and digital filtering algorithms that make the sensing function robust and survivable.

The part can scan matrix touch keys over LCD panels or other displays when used with clear ITO electrodes arranged in a matrix. It does not require 'chip on glass' or other exotic fabrication techniques, thus allowing the OEM to source the matrix from multiple vendors. Materials such as such common PCB materials or flex circuits can be used.

External circuitry consists of a resonator and a few capacitors and resistors, all of which can fit into a footprint of less than 6 sq. cm (1 sq. in). Control and data transfer is via either a SPI or UART port; a parallel scan port provides backwards compatibility with scanned electromechanical keys.

The QT60161B makes use of an important new variant of charge-transfer sensing, transverse charge-transfer, in a matrix format that minimizes the number of required scan lines. Unlike some older technologies it does not require one sensing IC per key.

The QT60161B is identical to earlier QT60161 in all respects except that the device exhibits lower signal noise. This device replaces QT60161 parts directly. After December 2003 the QT60161 will no longer be sold.

AVAILABLE OPTIONS

T_A	TQFP Part Number
-40°C to +105°C	QT60161B-AS

Contents

Table 1.1 Device Pin List

Pin	Name	Type	Description
1	MOSI	I/O PP	Master-Out / Slave In SPI line. In Master/Slave SPI mode is used for both communication directions. In Slave SPI mode is the data input (in only).
2	MISO	I/O PP	Master-In / Slave Out SPI line. Not used in Master/Slave SPI mode. In Slave mode outputs data to host (out only).
3	SCK	I/O PP	SPI Clock. In Master mode is an output; in Slave mode is an input
4	RST	I	Reset input, active low reset
5	Vdd	Pwr	+5V supply
6	Vss	Pwr	Ground
7	XTO	O PP	Oscillator drive output. Connect to resonator or crystal.ply
8	XTI	I	Oscillator drive input. Connect to resonator or crystal, or external clock source.
9	RX	I	UART receive input
10	TX	O PP	UART transmit output
11	WS	I	Wake from Sleep / Sync to noise source
12	SMP	O PP	Sample output control
13	X0OPA	I/O PP	X0 Drive matrix scan / Communications option A input
14	X1OPB	I/O PP	X1 Drive matrix scan / Communications option B input
15	X2	O PP	X2 Drive matrix scan
16	X3	O PP	X3 Drive matrix scan
17	Vdd	Pwr	+5V supply
18	Vss	Pwr	Ground
19	XS0	I	XS0 Scan input line
20	XS1	I	XS1 Scan input line
21	XS2	I	XS2 Scan input line
22	XS3	I	XS3 Scan input line
23	YS0	O PP	YS0 Scan output line
24	YS1	O PP	YS1 Scan output line
25	YS2	O PP	YS2 Scan output line
26	YS3	O PP	YS3 Scan output line
27	AVdd	Pwr	+5 supply for analog sections
28	AGnd	Pwr	Analog ground
29	Aref	Pwr	+5 supply for analog sections
30	CS3B	I/O PP	Cs3 control B
31	CS3A	I/O PP	Cs3 control A
32	CS2B	I/O PP	Cs2 control B
33	CS2A	I/O PP	Cs2 control A
34	CS1B	I/O PP	Cs1 control B
35	CS1A	I/O PP	Cs1 control A
36	CS0B	I/O PP	Cs0 control B
37	CS0A	I/O PP	Cs0 control A
38	Vdd	Pwr	+5 supply
39	Vss	Pwr	Ground
40	LED	O PP	Active low LED status drive / Activity indicator
41	DRDY	O OD	Data ready output for Slave SPI mode; active low
42	Vref	I	Vref input for conversion reference
43	SO	O PP	Oscilloscope sync output
44	SS	I/O OD	Slave select for SPI direction control; active low

I/O: I = Input
O = Output
Pwr = Power pin
I/O = Bidirectional line
PP = Push Pull output drive
OD = Open drain output drive

1 Overview

QMatrix devices are digital burst mode charge-transfer (QT) sensors designed specifically for matrix geometry touch controls; they include all signal processing functions necessary to provide stable sensing under a wide variety of changing conditions. Only a few low cost external parts are required for operation. The entire circuit can be built in under 6 square centimeters of PCB area.

Figure 1-1 Field flow between X and Y elements
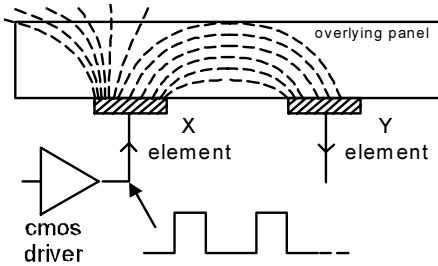
The device has a wide dynamic range that allows for a wide variety of key sizes and shapes to be mixed together in a single touch panel. These features permit new types of keypad features such as touch-sliders, back-illuminated keys, and complex warped panels.

The devices use an SPI interface running at up to 3MHz rates to allow key data to be extracted and to permit individual key parameter setup, or, a UART port which can run at rates to 57.6 Kbaud. The serial interface protocol uses simple commands; the command structure is designed to minimize the amount of data traffic while maximizing the amount of information conveyed.

In addition to normal operating and setup functions the device can also report back actual signal strengths and error codes over the serial interfaces.

QmBtn software for the PC can be used to program the IC as well as read back key status and signal levels in real time.

A parallel scan port is also provided that can be used to directly replace membrane type keypads.

QMatrix technology employs transverse charge-transfer ('QT') sensing, a new technology that senses the changes in an electrical charge forced across an electrode set.

1.1 Field Flows

Figure 1-1 shows how charge is transferred across an electrode set to permeate the overlying panel material; this charge flow exhibits a high dQ/dt during the edge transitions of the X drive pulse. The

Figure 1-2 Field Flows When Touched

Figure 1-3 Fields With a Conductive Film

Figure 1-4 Sample Electrode Geometries
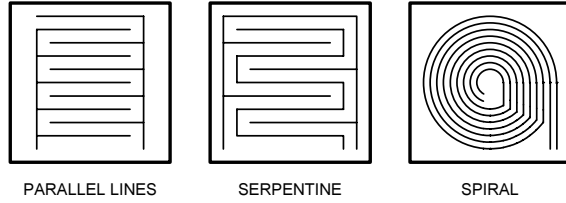
charge driven by the X electrode is partly received onto the corresponding Y electrode which is then processed. The part uses 4 'X' edge-driven rows and 4 'Y' sense columns to sense up to 16 keys.

The charge flows are absorbed by the touch of a human finger (Figure 1-1) resulting in a decrease in coupling from X to Y. Thus, received signals decrease or go negative with respect to the reference level during a touch.

As shown in Figure 1-3, water films cause the coupled fields to increase slightly, making them easy to distinguish from touch.

1.2 Circuit Overview

A basic circuit diagram is shown in Figure 1-5. The 'X' drives are sequentially pulsed in groupings of bursts. At the intersection of each 'X' and 'Y' line in the matrix itself, where a key is desired, should be an interdigitated electrode set similar to those shown in Figure 1-4. See Quantum App Note AN-KD01, or consult Quantum for application assistance.

The device uses fixed external capacitors to acquire charge from the matrix during a burst of charge-transfer cycles; the burst length can be varied to permit digitally variable key signal gains. The charge is converted to digital using a single-slope conversion process.

Burst mode operation permits the use of a passive matrix, reduces RF emissions, and provides excellent response times.

Refer to Section 3 for more details on circuit operation.

1.3 Communications

The device uses two variants of SPI communications, Slave-only and Master-Slave, a UART interface, plus a parallel scan interface. Over the serial interfaces are used a command and data transfer structure designed for high levels of flexibility using minimal numbers of bytes. For more information see Sections 4 and 5.
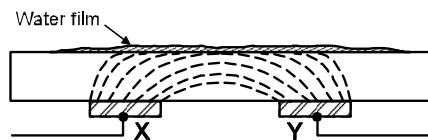
The parallel scan port permits the replacement of electromechanical keypads that would be scanned by a microcontroller; the scan interface mimics an electromechanical keyboard's response.

Figure 1-5 Circuit Block Diagram
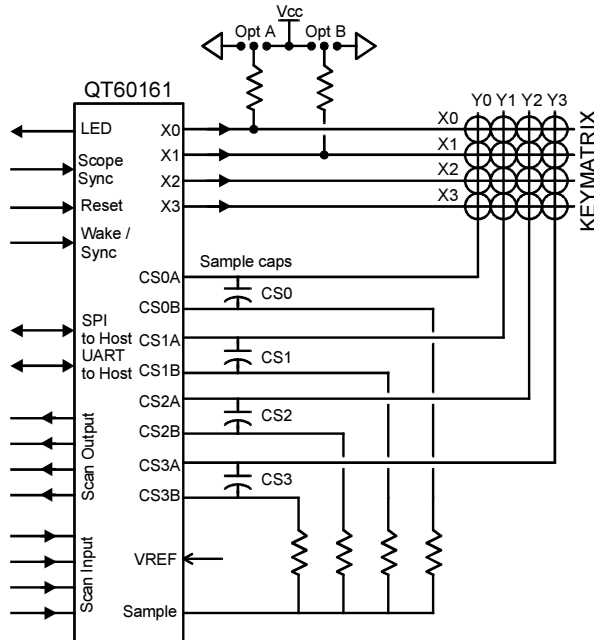
2 Signal Processing

The device calibrates and processes signals using a number of algorithms specifically designed to provide for high survivability in the face of adverse environmental challenges. The QT60161B provides a large number of processing options which can be user-selected to implement very flexible, robust keypanel solutions.

2.1 Negative Threshold

See also command ^A, page 21

The negative threshold value is established relative to a key's signal reference value. The threshold is used to determine key touch when crossed by a negative-going signal swing after having been filtered by the detection integrator (Section 2.6). Larger absolute values of threshold desensitize keys since the signal must travel farther in order to cross the threshold level. Conversely, lower thresholds make keys more sensitive.

As Cx and Cs drift, the reference point drift-compensates for these changes at a user-settable rate (Section 2.4); the threshold level is recomputed whenever the reference point moves, and thus it also is drift compensated.

The threshold is user-programmed on a per-key basis using the setup process (Section 5).

2.2 Positive Threshold

See also command ^B, page 21

The positive threshold is used to provide a mechanism for recalibration of the reference point when a key's signal moves abruptly to the positive. These transitions are described more fully in Section 2.7.

The threshold is user-programmed using the setup process described in Section 5 on a per-key basis.

2.3 Hysteresis

See also command ^C and ^D, page 21

Refer to Figure 1-6. The QT60161B employs programmable hysteresis levels of 12.5%, 25%, or 50% of the delta between the reference and threshold levels. There are different hysteresis settings for positive and negative thresholds which can be set by the user. The percentage refers to the distance between the reference level and the threshold at which the detection will drop out. A percentage of 12.5% is less hysteresis than 25%, and the 12.5% hysteresis point is closer to the threshold level than to the reference level.

The hysteresis levels are set for all keys only; it is not possible to set the hysteresis differently from key to key on either the positive or negative hysteresis levels.

2.4 Drift Compensation

See also commands ^H, ^I, page 22

Signal levels can drift because of changes in Cx and Cs over time. It is crucial that such drift be compensated, else false detections, non- detections, and sensitivity shifts will follow. The QT60161B can compensate for drift using two setups, ^H and ^I.

Drift compensation is performed by making the reference level track the raw signal at a slow rate, but only while there is no detection in effect. The rate of adjustment must be performed slowly, otherwise legitimate detections could be ignored. The devices drift compensate using a slew-rate limited change to the reference level; the threshold and hysteresis values are slaved to this reference.

When a finger is sensed, the signal falls since the human body acts to absorb charge from the cross-coupling between X and Y lines. An isolated, untouched foreign object (a coin, or a water film) will cause the signal to rise very slightly due to the enhanced coupling thus created. These effects are contrary to the way most capacitive sensors operate.

Once a finger is sensed, the drift compensation mechanism ceases since the signal is legitimately detecting an object. Drift compensation only works when the key signal in question has not crossed the negative threshold level (Section 2.1).

The drift compensation mechanism can be made asymmetric if desired; the drift-compensation can be made to occur in one direction faster than it does in the other simply by setting ^H and ^I to different settings.

Figure 1-6 Detection and Drift Compensation
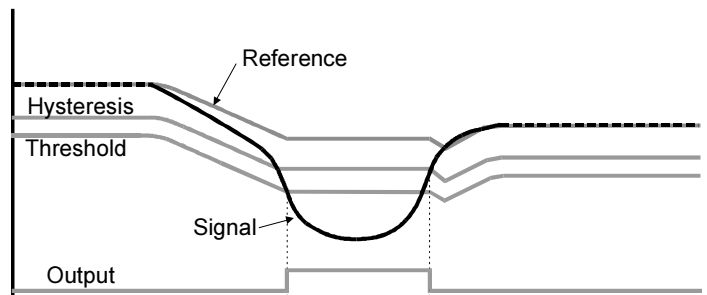
Drift compensation should usually be set to compensate faster for increasing signals than for decreasing signals. Decreasing signals should not be compensated quickly, since an approaching finger could be compensated for partially or entirely before even touching the touch pad. However, an obstruction over the sense pad, for which the sensor has already made full allowance for, could suddenly be removed leaving the sensor with an artificially suppressed reference level and thus become insensitive to touch. In this case, the sensor should compensate for the object's removal by raising the reference level quickly.

The drift compensation rate can be set for each key individually, and can also be disabled completely if desired on a per-key basis.

Drift compensation and the detection time-outs (Section 2.5) work together to provide for robust, adaptive sensing. The time-outs provide abrupt changes in reference location depending on the duration of the signal 'event'.

2.5 Negative Recalibration Delay
See also command ^L, page 23

If a foreign object contacts a key the key's signal may change enough in the negative direction, the same as a normal touch, to create an unintended detection. When this happens it is usually desirable to cause the key to be recalibrated in order to restore its function after a time delay of some seconds.

The Negative Recal Delay timer monitors this detection duration; if a detection event exceeds the timer's setting, the key will be recalibrated so that it can function thereafter. The ^L function can be altered on a key by key basis. It can be disabled if desired by setting the ^L parameter to zero, so that it will never recalibrate automatically.

2.6 Detection Integrator
See also command ^J, page 22

To suppress false detections caused by spurious events like electrical noise, the QT60161B incorporates a 'detection integrator' counter that increments with each detection sample until a user-defined limit is reached, at which point a detection is confirmed. If no detection is sensed on any of the samples prior to the final count, the counter is reset immediately to zero, forcing the process to restart.

When an active key is released, the counter must count down to zero before the key state is set to 'off'. Setting a key's detection integrator target value to zero disables that key although the bursts for that key continue normally.

The detection integrator is extremely effective at reducing false detections at the expense of slower reaction times. In some applications a slow reaction time is desirable; the detection integrator can be used to intentionally slow down touch response in order to require the user to touch longer to operate the key.

There are 16 possible values for this function.

2.7 Positive Recalibration Delay
See also command ^K, page 23

A recalibration can occur automatically if the signal swings more positive than the positive threshold level. This condition can occur if there is positive drift but insufficient positive drift compensation, or if the reference moved negative due to a recalibration, and thereafter the signal returned to normal.

As an example of the latter, if a foreign object or a finger contacts a key for period longer than the Negative Recal Delay, the key is recalibrated to a new lower reference level. Then, when the condition causing the negative swing ceases to exist (e.g. the object is removed) the signal can suddenly swing back positive to near its normal reference.

It is almost always desirable in these cases to cause the key to recalibrate to the new signal level so as to restore normal touch operation. The device accomplishes this by simply setting Reference = Signal.

The time required to detect this condition before recalibrating is governed by the Positive Recalibration Delay command. In order for this feature to operate, the signal must rise through the positive threshold level (Section 2.2) for the proscribed interval determined by Setup ^K.

After the Positive Recal Delay interval has expired and the fast-recalibration has taken place, the affected key will once again function normally. This interval can be set on a per-key basis; it can also be disabled by setting ^K to zero.

2.8 Reference Guardbanding
See also commands ^N, ^O, page 23; 'L', page 24

The QT60161B provides for a method of self-checking that allows the host to ascertain whether one or more key reference levels are 'out of spec'. This feature can be used to determine if an X or Y line has broken, the matrix panel has delaminated from the control panel, or there is a circuit fault.

Reference guardbanding alerts the host when the reference level of a key falls outside of user-defined levels. The reference guardband is determined as a percent deviation from the 'locked' reference level for each individual key. These reference levels can be stored into internal eeprom via the Lock command 'L' during production; deviations in reference levels that fall outside the guardbands centered on these locked reference levels are then reported as key errors.

The amount of guardbanding can be set differently for each signal direction relative to the stored and locked levels. The possible settings are from 0.1% to 25.5% of signal reference in steps of 0.1% as set by commands ^N (positive swings) and ^O (negative swings). A setting of 0 (zero) disables the corresponding guardband direction.

Once the L command has recorded all values of signal reference into eeprom, and if guardbanding is enabled, the part will compare the actual reference level of each key to its corresponding guardbands to see if it falls outside of these limits. If so, either of bits 2 and 3 of command 'e' will be set for that key. The error will also appear in a bitfield reported via command 'E'.

2.9 Adjacent Key Suppression ('AKS')
See also command ^P, page 24

The QT60161B incorporates adjacent key suppression ('AKS') that can be enabled on a per-key basis. AKS permits

the suppression of multiple key presses based on relative signal strengths. AKS assists in solving the problem of surface water which can bridge a key touch to an adjacent key, causing multiple key presses, causing multiple key presses even though only one key was touched. This feature is also useful for panels with tightly spaced keys, where a fingertip can partially overlap an adjacent key.

AKS works for keys that are AKS-enabled anywhere in the matrix and is not restricted to physically adjacent keys; the device has no knowledge of which keys are physically adjacent. When enabled for a key, adjacent key suppression causes detections on that key to be suppressed if any other AKS-enabled key in the panel has a more negative signal deviation from its reference.

This feature does not account for varying key gains (burst length) but ignores the actual negative detection threshold setting for the key. If AKS-enabled keys in a panel have different sizes, it may be necessary to reduce the gains of larger keys relative to smaller ones to equalize the effects of AKS. The signal threshold of the larger keys can be altered to compensate for this without causing problems with key suppression.

AKS works to augment the natural moisture suppression capabilities of the device (Section 3.10), creating a more robust touch panel.

2.10 Full Recalibration
See also command 'b', page 24

The part fully recalibrates one or more keys after the 'b' command has been issued to it, depending on the current scope of the 'b' command. The device recalibrates all keys on powerup, after a hard reset via the RST pin or on power up, or via a reset using the 'r' command. Since the circuit tolerates a very wide dynamic signal range, it is capable of adapting to a wide mix of key sizes and shapes having widely varying Cx coupling capacitances.

If a false calibration occurs due to a key touch or foreign object on the keys during powerup, the affected key will recalibrate again when the object is removed depending on the settings of Positive Threshold and Positive Recal Delay (Sections 2.2 and 2.7).

Calibration requires 9 full burst cycles to complete, and so the time it takes is dependent on the burst spacing parameter (Section 3.8 also, ^G, page 22).

2.11 Device Status & Reporting
See also commands '7', page 19; 'e', page 19; 'E', page 20; 'k', page 20, 'K', page 20

The device can report on the general device status or specific key states including touches and error conditions, depending on the command used.

Usually it is most efficient to periodically request the general device status using command '7' first, as the response to this command is a single byte which reports back on behalf of all keys. '7' indicates if there are any keys detecting, calibrating, or in error.

If command '7' reports a condition requiring further investigation, the host device can then use commands 'e', 'E', 'k' or 'K' to provide further details of the event(s) in progress. This hierarchical approach provides for a concise information

flow using minimal data transfers and low host software overhead.

3 Circuit Operation
A QT60161B reference circuit is shown in Figure 2-1.

3.1 Matrix Scan Sequence
The circuit operates by scanning each key sequentially, key by key. Key scanning begins with location X=0 / Y=0. X axis keys are known as *rows* while Y axis keys are referred to as *columns*. Keys are scanned sequentially by row, for example the sequence Y0X0 Y0X1 Y0X2 Y0X3 Y1X0 etc.

Each key is sampled from 1 to 64 times in a burst whose length is determined by Setup ^F. A burst is completed entirely before the next key is sampled; at the end of each burst the resulting analog signal is converted to digital using a single-slope conversion process. The length of the burst directly impacts on the gain of the key; each key can have a unique burst length in order to allow tailoring of key sensitivity on a key by key basis.

3.2 Signal Path
Refer to Figures 1-5, 3-1, and 3-2.

X-Drives. The X drives are push-pull CMOS lines which drive charge through the matrix keys on the positive and negative edges of X. Only the positive edge of X is used for signal purposes, however the negative edge must cause the charge across the keys to neutralize prior to the next positive edge, else the sampling mechanism will cease after one pulse. The part accomplishes this by holding all Y lines to ground during the falling edge of X.

Charge gate. Only one X row is pulsed during a burst. Charge is coupled across a key's Cx capacitance from the X row to all Y columns. A particular key is chosen by gating the charge from a single Y column into a single one of four possible sampler capacitors. The other three X and three Y lines are clamped to ground during this process.

Dwell time. The dwell time is determined internally and is the same as one oscillator period, i.e. 83.3ns with a 12MHz resonator. The dwell time is set via internal switching action

Figure 3-1 QT60161B Circuit Model
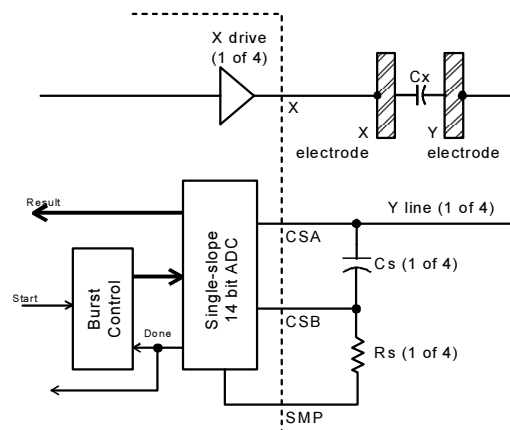
which limits the interval during which charge can be accepted by a Cs capacitor after the rise of an X drive line.

Dwell time has a dramatic effect on the suppression of moisture films as described in Section 3.10.

Cs Charge Integrator capacitor. The Cs capacitors integrate charge arriving through the matrix keys' Cx capacitances, correspondent with the rise of X; to do this a switching arrangement on the Cs control pins permits the charge to accumulate so that the B side of the Cs capacitors becomes negative when the A side is clamped to ground.

Charge conversion. At the end of each burst the voltage on Cs is converted to digital by means of a single-slope conversion process, using one of the external resistors to ramp up the capacitor towards a reference voltage. The elapsed time required to reach the comparison voltage is the digital result. The time required to perform the conversion depends on Cs, Cx, Rs, Aref, and the burst length.

3.3 'X' Electrode Drives
The 'X' lines are directly connected to the matrix without buffering. The positive edges of these signals are used to create the transient field flows used to scan the keys. Only one X line is actively driving the matrix for scanning purposes at a time, and it will pulse repetitively for a 'burst length' for each key as determined by the 'Burst Length' Setups parameter (see command ^F, page 21 and Section 3.5).

3.3.1 RFI FROM X LINES
X drive lines will radiate a small amount of RFI. This can be attenuated if required by using series resistor in-line with each X trace; the resistor should be placed near to the QT60161B. Typical values can range from 100 to 500 ohms. Excessive amounts of R will cause a counterproductive drop in signal strength. RC networks can also be used as shown in Figure 4-6.

Resistance in the X lines also have the positive effect of limiting ESD discharge currents (Section 3.18).

3.3.2 NOISE COUPLING INTO X LINES
External noise, sometimes caused by ground bounce due to injected line noise, can couple into the X lines and cause signal interference in extreme cases. Such noise can be readily suppressed by the use of series resistors as described above. Adding a small capacitor to the matrix line on the QT60161B side of the R, for example 100pF to ground near the QT60161B, will greatly help to reduce such effects.

3.4 'Y' Gate Drives
There are 4 'Y' gate drive pairs (CS0A,B..CS3A,B); only one pair of these lines is used during a burst for a particular key. The magnitude of the voltages accumulated on the Cs capacitors should never exceed 0.25V.

3.4.1 RFI FROM Y LINES
Y lines are nearly 'virtual grounds' and are negligible radiators of RFI; in fact, they act as 'sinks' for RFI emitted by the X lines. Resistors are not required in the Y lines for RFI suppression, and in fact can introduce cross-talk among keys if large enough. However, small resistance values can be beneficial to limit ESD transients and make the circuit more resistant to external RF fields (Section 3.18).

3.4.2 NOISE COUPLING INTO Y LINES
External noise, sometimes caused by ground bounce due to power line noise, can couple into the Y lines and cause signal interference in extreme cases. Such noise can be readily suppressed by adding a 22pF capacitor from each Y line to ground near the QT60161B.

3.5 Burst Length & Sensitivity
See also Command ^F, page 21

The signal gain in volts / pF of Cx for each key is controlled by circuit parameters as well as the burst length.

The burst length is simply the number of times the charge-transfer ('QT') process is performed on a given key. Each QT process is simply the pulsing of an X line once, with a corresponding Y line gated so as to capture the resulting charge passed through the key's capacitance Cx.

QT60161B devices use a finite number of QT cycles which are executed in a short burst. There can be from 1 to 64 QT cycles in a burst, in accordance with the list of permissible values shown on page 21. If a key's burst length is set to zero, that burst is disabled but its time slot in the scanning sequence of all keys is preserved so as to maintain scan timing.

Increasing burst length directly affects key sensitivity. This occurs because the accumulation of charge on Cs is directly linked to the burst length. The burst length of each key can be set individually, allowing for direct digital control over the signal gains of each key, indivually.

Apparent touch sensitivity is also controlled by the Negative Threshold setting (Section 2.1). Burst length and negative threshold interact; normally burst lengths should be kept as short as possible to limit RF emissions, but the threshold setting should normally be kept above a setting of 6 to limit false detections. The detection integrator can also prevent false detections at the expense of slower reaction times (Section 2.6).

The value of Rs also affects sensitivity. Higher values of Rs will lead to larger values of ADC result and higher conversion gains. The side effect of this is that the conversion will take longer and timing conflicts can occur (Section 3.6).

Cs does not significantly affect gain. Smaller values of Cs will have higher delta signal voltages but this gain increase is offset by the decrease in gain caused by a steeper ADC conversion slope. However smaller values of Cs lead to faster conversion times for a given value of Rs, which in turn allows for more relaxed burst timings. Smaller values of Cs also reduce the dynamic range of the system, meaning that the acquisition becomes less tolerant of high values of Cx, due to earlier saturation of the voltage across Cs.

3.6 Burst Acquisition Duration
The total time required to acquire a key's signal depends on the burst length for that key plus the time required to convert the voltage on the corresponding Cs capacitor to digital. The conversion is performed via a single-slope ADC process using one of the external Rs resistors.

If the total time required for the acquisition, i.e. the burst length plus ADC times plus the signal processing and serial interface command handler times exceed the burst spacing setup parameter (Section 3.8), significant timing errors and communications problems can occur.

The time taken by the burst itself is straightforward to quantify, but the time required to do the ADC step is not. The ADC step depends on the value of Vref (pin 42), Cs, Rs, and

Cx. Therefore it is vital that the circuit be checked with an oscilloscope to make sure that burst spacings are unaffected during normal operation.

3.7 Intra-Burst Spacing
See also Command ^M, page 23

The time between X drive pulses during a burst is the intra-burst pulse QT spacing. This timing has no noticeable effect on performance of the circuit, but can have an impact on the nature of RF spectral emissions from the matrix panel. The setting of this function can be from 1μs to 10μs, loosely corresponding to fundamental emission frequencies of from 1MHz to 100kHz respectively.

Longer spacings require more time to execute and can limit the operational settings of burst length and/or burst spacing (Section 5.7).

The intra-burst QT spacing has no effect on sensitivity or water film suppression and is not particularly important to the sensing function other than described above.

3.8 Burst Spacing
See also Command ^G, page 22

The interval of time from the start of one burst to the start of the next is known as the *burst spacing.* This is an alterable parameter which affects all keys.

Shorter spacings result in faster response time, but due to increasing timing restrictions at shorter spacings burst lengths or the conversion resolution may be restricted, limiting the amount of gain that can be obtained; see Sections 3.6 and 5.7. Conversely longer spacings permit higher burst lengths but slow down response time.

Three settings of burst spacing are possible: 500μs, 1ms, and 2ms.

3.9 Sample Capacitors
Charge sampler capacitors Cs should be either ceramic NPO, X7R 5%, or PPS film for stability reasons.

The values of capacitance should not be altered from that shown in the schematic of Figure 3-2 without good reason.

Changes in Cs have only a limited effect on signal gain.

3.10 Water Film Suppression
Water films on the user surface can cause problems with false detection under certain conditions. Water films on their own will not normally cause false detections. The most common problem occurs when surface water bridges over 2 or more keys, and a user touches one of the keys and the water film causing an adjacent key to also trigger. Essentially, the water film transports the touch contact to adjacent keys.

The circuit suppresses water coupling by having a short dwell time, equal to one oscillator period or 83ns. A short dwell time reduces the amount of charge collected via resistive water films, i.e. it suppresses charge from areas adjacent to the scanned key. This effect has nothing to do with the frequency of the burst itself.

Very short dwell times can cause excess suppression of human touch as well. If series resistors are used in line with the X and Y matrix lines for noise and ESD suppression

(Section 3.18), a short dwell time can seriously affect signal gain.

Mechanical measures can also be used to suppress key cross-coupling, for example one can use raised plastic barriers between keys, or placing keys in shallow wells to lengthen the electrical path from key to key.

3.11 Reset Input
The RST' pin can be used to reset the device to simulate a power down cycle, in order to bring the part up into a known state should communications with the part be lost. The pin is active low, and a low pulse lasting at least 10μs must be applied to this pin to cause a reset.

To provide for proper operation during power transitions the devices have an internal brown-out detector set to 4 volts.

A reset command, 'r', is also provided which generates an equivalent hardware reset (page 25).

3.12 Oscillator
The oscillator can use either a quartz crystal or a ceramic resonator. In either case, the XTI and XTO must both be loaded with 22pF capacitors to ground. 3-terminal resonators having onboard ceramic capacitors are commonly available and are recommended. An external TTL-compatible frequency source can also be connected to XTI; XTO should be left unconnected.

The frequency of oscillation should be 12MHz +/-2%.

3.13 Startup / Calibration Times
The QT60161B requires initialization times as follows:

1. From very first powerup to ability to communicate:
   2,000ms (One time event to initialize all of eeprom)

2. Normal cold start to ability to communicate:
   70ms (Normal initialization from any reset)

3. Calibration time per key vs. burst spacings:
   spacing = 500μs: 100ms
   spacing = 1ms: 150ms
   spacing = 2ms: 300ms

   To the above, add 2,000ms or 70ms from (1) or (2) for the total elapsed time from reset to ability to report key detections.

Keys that cannot calibrate for some reason require 5 calibration cycles before they report as errors. However, the device can report back during this interval that the key(s) affected are still in calibration via status function bits.

3.14 Sleep_Wake / Noise Sync Pin (WS)
The Sleep_wake and Noise sync features use input pin WS. The Sleep and Sync features can be used simultaneously; the part can be put into Sleep mode, but awakened by a noise sync signal which is gated in at the time desired.

Sleep mode: *See also command 'Z', page 25.* The device can be put into an ultra low-power sleep mode using the 'Z' command. When this command is received, the WS pin must be placed immediately thereafter into a logic-high state. The part will complete an ongoing burst before entering Sleep. The part can be awakened by a low transition on the WS pin lasting at least 5μs. One convenient way to wake the part is to connect WS to MOSI, and have the host send a null

Figure 3-2 Recommended Circuit Diagram
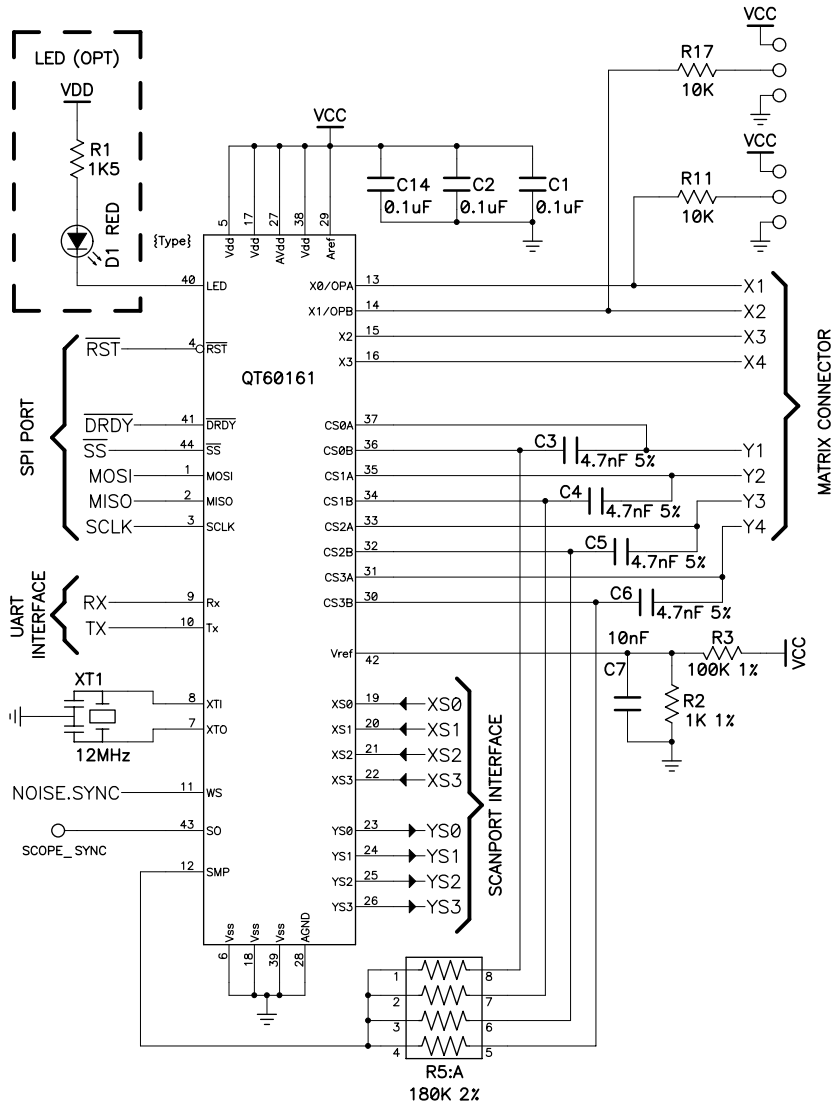
Noise sync: *See also command ^W, page 26.* External fields can cause interference leading to false detections or sensitivity shifts. The strongest external fields usually come from AC power. RF noise sources are heavily suppressed by the low impedance nature of the QT circuitry itself.

External noise only becomes a problem if the noise is uncorrelated with signal sampling; uncorrelated noise can cause aliasing and beat effects in the key signals. To suppress this problem the devices feature a noise sync input which allows bursts to synchronize to the noise source. This same input can also be used to wake the part from a low-power Sleep state.

The device's bursts can be synchronized to an external source of repetitive electrical signal, such as 50Hz or 60Hz, or possibly a video display vertical sync line, using the Sleep_wake / Noise sync line. The noise sync operating mode is set by command ^W. This feature allows dominant external noise signals to be heavily suppressed, since the system and the noise become synchronized and no longer beat or alias with respect to each other. The sync occurs only at the burst for key 0 (X0Y0); the device waits for the sync signal for up to 100ms after the end of a preceding full matrix scan (after key #15), then when a negative sync edge is received, the matrix is scanned in its entirety again.

The sync signal drive should be a buffered logic signal, or perhaps a diode-clamped signal, but never a raw AC signal from the mains.

Since Noise sync is highly effective yet simple and inexpensive to implement, it is strongly advised to take advantage of it anywhere there is a possibility of encountering electric fields. Quantum's QmBtn software can show signal noise caused by nearby AC electric fields and will hence assist in determining the need to make use of this feature.

If the sync feature is enabled but no sync signal exists, the sensor will continue to operate but with a delay of 100ms from the end of one scan to the start of the next, and hence will have a slow response time.

command to the device. The part will wake and the null command will not be processed. The MOSI line in turn requires a pullup resistor to prevent the line from floating low and causing an unintentional wake from sleep.

During Sleep the oscillator is shut down, and the part hibernates with microamp levels of current drain. When the part wakes, the part resumes normal functionality from the point where it left off. It will not recalibrate keys or engage in other unwarranted behavior.

Just before going to sleep the part will respond with a response of 'Z'. In slave-only SPI mode (see Section 4.3), the SS line must be floated high by the host as soon as it receives this response; if SS does not float high, sleep will fail and the device will instead completely reset after about 2 seconds. Upon waking the part will issue another 'Z' byte back to the host.

3.15 LED / Alert Output
Pin 40 is designed to drive a low-current LED, 5mA maximum, in an active-low configuration. Higher currents can cause significant level shifts on the die and are not advised. The LED will glow brightly (i.e. pin 40 will be solid low) during calibration of one or more keys, for example at startup. When a key is detected, the LED will pulse low for the duration of

the burst during which the key is being sensed, i.e. with a very low duty cycle. Each additional key being detected will also create a low pulse for that key's burst. During all other times, the LED pin will be off (high).

This pin can be used to alert the host that there is key activity, in order to further limit the amount of communication between the device and the host. The LED / Alert line should ideally be connected to an interrupt pin on the host that can detect a negative edge, following which the host can proceed to poll the device for keys.

This line also pulls low if there is a key error of any kind.

Note that in sleep mode if the LED was on prior to sleep, it will remain on during sleep.

3.16 Oscilloscope Sync
See also Command ^R, page 26

The 'SO' pin can output an oscilloscope sync signal which is a positive pulse that brackets the burst of a selected key. This feature is controlled by the ^R command. More than one burst can output a sync pulse, for example if the scope of the command when set is a row or column, or is all keys. The ^R command is volatile and does not survive a reset or power down.

This feature is invaluable for diagnostics; without it, observing signals clearly on an oscilloscope for a particular burst is nearly impossible.

This function is supported in QmBtn PC software via a checkbox.

3.17 Power Supply & PCB Layout
Vdd should be 5.0 volts +/- 5%. This can be provided by a common 78L05 3-terminal regulator. LDO type regulators are often fine but can suffer from poor transient load response which may cause erratic signal behavior.

If the power supply is shared with another electronic system, care should be taken to assure that the supply is free of low-level spikes, sags, and surges which can adversely affect the circuit. The devices can track slow changes in Vcc depending on the settings of drift compensation, but signals can be adversely affected by rapid voltage steps and impulse noise on the supply rail.

Supply bypass capacitors of 0.1uF to a ground plane should be used near every supply pin of every active component in the circuit.

PCB layout: The PCB layout should incorporate a ground plane under the entire circuit; this is easily possible with a 2-layer design. The ground plane should be broken up as little as possible. Internal nodes of the circuit can be quite sensitive to external noise and the circuit should be kept away from stray magnetic and electric fields, for example those emanating from mains power components such as transformers and power capacitors. If proximity to such components is unavoidable, an electrostatic shield may be required.

The use of the Sync feature (Section 3.14) can be invaluable in reducing these types of noise sources, but only up to a point.

3.18 ESD / Noise Considerations
In general the QT60161B will be well protected from static discharge during use by the overlying panel. However, even with a dielectric panel transients currents can still flow into scan lines via induction or in extreme cases, dielectric breakdown. Porous or cracked materials may allow a spark to tunnel through the panel. In all cases, testing is required to reveal any potential problems. The IC has diode protected pins which can absorb and protect the device from most induced discharges, up to 5mA.

The X lines are not usually at risk during operation, since they are low-resistance output drives. Diode clamps can be used on the X and Y matrix lines if desired. The diodes should be high speed / high current types such as BAV99 dual diodes, connected from Vdd to Vss with the diode junction connected to the matrix pin. Diode arrays can also be used.

Capacitors placed on the X and Y matrix lines can also help to a limited degree by absorbing ESD transients and lowering induced voltages. Values up to 100pF on the X lines and 22pF on the Y lines can be used.

The circuit can be further protected by inserting series resistors into the X and/or Y lines to limit peak transient current. RC networks as shown in Figures 4-6 and 4-7 can provide enhanced protection against ESD while also limiting the effects of external EMI should this be a problem.

External field interference can occur in some cases; these problems are highly dependent on the interfering frequency and the manner of coupling into the circuit. PCB layout (Section 3.17) and external wiring should be carefully designed to reduce the probability of these effects occurring.

SPI / UART data noise: In some applications it is necessary to have the host MCU at a distance from the sensor, perhaps with the interface coupled via ribbon cable. The SPI link is particularly vulnerable to noise injection on these lines; corrupted or false commands can be induced from transients on the power supply or ground wiring. Bypass capacitors and series resistors can be used to prevent these effects as shown in Figures 4-6 and 4-7.

4 Communications Interfaces
The QT60161B uses parallel, UART, and SPI interfaces to communicate with a host MCU. The serial interfaces use a protocol described in Section 5. Only one interface can be used at a time; the interface type is selected by resistor-coupled jumpers connected to pins X0OPA (pin 13) and X0OPB (pin 14) shown in Table 4-1. See also Figure 3-2.

Further specific information on each interface type is contained in the following sections:

SPI Slave-Only Mode:	Section 4.3
SPI Master-Slave Mode:	Section 4.4
UART Interface:	Section 4.5
Parallel Interface:	Section 4.7

4.1 Serial Protocol Overview
The SPI and UART interface protocols are based entirely on polled data transmission, that is, the part will not send data to the host of its own volition but will do so only in response to specific commands from a host.

Run-time data responses, such as key detection or error information, requires simple single-byte functions to evoke a response from the part.

Setup mode interactions mostly use 2-byte functions from the host to cause the part to alter its behavior; these functions also cause writes to the internal eeprom.

The concept of 'scope' is used to allow functions to operate on individual keys or groupings of keys. The scope of subsequent functions can be altered by short initial scope instructions.

See Section 5 for protocol details.

4.2 SPI Port Specifications
The part has an SPI synchronous serial interface with the following specifications at 12MHz oscillator frequency:

Max clock rate, Fck	3MHz
Data length	8 bits
Host command space, Tcm	$\geq 50\mu s$
Response delay to host, Tdr1	Table 4-1, also, Sec. 6
Drdy delay from response, Tdr2	1µs to 1ms
Multi-byte return spacing, Tdr3	10µs to 2ms

The host can clock the SPI with the part in Slave mode at any rate up to and including the maximum clock rate Fck. The maximum clock rate of the part in Master mode is determined by Setup ^Q (page 25).

The part can operate in either master-slave mode or slave-only mode, and is thus compatible with virtually all SPI-capable microcontrollers.

The SPI interface should not be used over long distances due to problems with signal ringing and introduced noise etc. unless suitably buffered or filtered with RC networks as shown in Figures 4-6 and 4-7. Slower data rates with longer RC timeconstants will provide enhanced resistance to noise and ringing problems.

4.3 SPI Slave-Only Mode
Refer to Figures 4-1, 4-3 and 4-2. In Slave-only mode the host must always be in Master mode, as it controls all SPI activity including the clocking of the interface in both directions. Unlike hardware SPI slaves, the QT60161B needs processing time to respond to functions. DRDY' is used to let the host know when data is ready for collection; it indicates to the host when data is ready in response to a command so that the host can clock over the data.

This mode requires 5 signals to operate:

MOSI - Master out / Slave in data pin; used as an input for data from the host at all times. This pin should be connected to the MOSI pin of the host device.

MISO - Master in / Slave out data pin; used as an output for data to the host at all times. This pin should be connected to the MISO pin of the host device.

SCK - SPI clock - input only clock pin from host. The host must shift out data on the falling edge of SCK; the QT60161B clocks data in on the rising edge of SCK. **Important note:** SCK must idle low just before and after SS' transitions either up or down, or the transmission will fail; between bytes SCK should idle low.

SS' - Slave select - input only; this pin acts as a framing signal to the sensor from the host. This line must go low just before and during reception of data from the host. It must not go high again until the SCK line has returned low; during data or echo response it must not go high until after the host has sensed that DRDY' has gone high from the device. This pin must idle high. The SS' pin has an internal pullup resistor inside.

DRDY' - Data Ready - active-low - indicates to the host that the part is ready to send data back subsequent to a command from the host. This pin idles high. The DRDY' pin has an internal pullup resistor inside.

Internal pullup resistors note: The internal pullup resistors can range from 35k to 120k ohms. If RC filtering is used on the SPI lines per Figure 4-6, this resistance may not be low enough to ensure adequate signal risetime and may need to be augmented with external 10k pullups.

The host must wait until DRDY' goes low before an SPI transfer to retrieve data. For multi-byte responses, the host must observe DRDY' to see when it goes high again after each data byte, then low again, before executing another transfer to get the next data byte. The host should send null bytes (0x00) to retrieve data.

If the DRDY' line does not go low after a command, the command was not properly received or it was inappropriate. The delay to DRDY' low depends on the command and how many bytes of data are being stored into eeprom; Table 4-1 shows the maximum delays encountered in most cases. Absolute worst case delays are found in Section 6-5; these timings occur only rarely, for example if the device happens to be busy with adjacent key suppression calculations, which occurs only at the moment when a key is first detected.

A typical Slave-only function sequence is as follows:

1) The host pulls SS' low, then transfers a command to the sensor. The host then releases SS' to float high. DRDY' is unaffected in this step.

2) For 2-byte functions, (1) is repeated with a ≥50us delay.

3) When the sensor has the command echo or requested data ready to send back to the host, it loads it into its SPI register and pulls DRDY' low.

4) The host detects that the sensor has pulled DRDY' low and in turn the host pulls SS' low.

5) The host obtains the byte from the sensor by transmitting a dummy byte (0x00) to the sensor.

6) The sensor releases DRDY' to float high.

7) After the host detects that DRDY' has floated high the host must allow SS' to also float high.

8) For multi-byte responses, steps (3) through (7) are repeated until the return data is completely sent.

Note that the host must release the SS' line in step (7) even between multiple byte responses because the QT60161B waits for the SS' line to return high before signalling that the next byte is ready for collection.

Note also that the host should check the DRDY' line and wait for it to go high before transmitting another byte. Until the DRDY' line is released the sensor is still processing a data return, even if the complete response data has been fully transferred; the sensor may still be busy when the host finishes the byte transfer and may not be able to digest a new command immediately.

See Section 3.15, page 10, for a description of the Alert pin which can be used to reduce communication traffic.

4.4 SPI Master-Slave Mode

Refer to Figures 4-1, 4-2, and 4-4. In Master-Slave mode the host and the sensor take turns being Master, with the host always leading off in Master mode during an exchange. The current Master always controls all 3 signal lines. The sensor takes a variable amount of time to respond to the host, depending on the nature of the function and its current and pending tasks. The host, like the sensor, must idle in slave mode when not sending a command.

Master/Slave requires 3 signals to operate:

MOSI - Master out / Slave in data pin - bidirectional - an input pin while the host is transmitting data; an output when the sensor is transmitting data. The MOSI of the host and slave should be tied together. The MISO lines are not used on either part and should be left open.

SCK - SPI clock - bidirectional - an input pin when receiving data; an output pin when sending. The host must shift out data on the falling edge of SCK; the QT60161B clocks data in on the rising edge of SCK. **Important note:** SCK from the host must be low before asserting SS' low or high at either end of a byte or the transmission will fail. SCK should idle low; if in doubt, a 10K pulldown resistor should be used. When the sensor returns data it becomes the Master; data is shifted out by it on the falling edge of SCK and should be clocked in by the host on the rising edge.

SS' - Slave select - bidirectional framing control. When the sensor is in slave mode, this pin accepts the SS' control signal from the host. In either data direction, SS' must go low before and any during data transfer; it should not go high again until SCK has returned low at the end of a byte. In Master mode the sensor asserts control over this line, to make the host a slave and to frame the data. This line must idle high; the part includes an internal pullup resistor and should be floated during idle times.

Internal pullup resistor note: The internal pullup resistor on SS' can range from 35k to 120k ohms. If RC filtering is used on the SPI lines per Figure 4-7, this pullup resistance may not be low enough to ensure adequate signal risetime and may need to be augmented with external 10k pullups.

A command may consist of one or two bytes with a $\geq$50us delay between command bytes. At the end of a full command, the Master must go into Slave mode to await a response from the sensor.

The sensor may take some time to process the host command and respond. When it does so, it asserts SS' low and begins clocking its data. For multi-byte responses, the bytes will be sent at intervals which may be somewhat irregular depending on the request and the processing load of the sensor. The host must be prepared to accept the sensor data as it comes or there can be a data overrun in the host. *If the data returns too fast for the host to accept it, the SPI clock rate should be lowered.*

A typical Master-Slave function sequence is as follows:

1) Host enters Master mode. The sensor is already in Slave mode.

Figure 4-1 Communications Option Jumpers
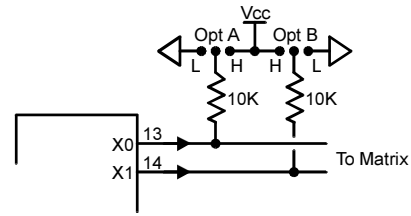
X0OPA (Pin 13)	X0OPB (Pin 14)	Interface Type
Low	Low	SPI, Slave only
Low	High	UART
High	Low	SPI, Master/Slave
High	High	Parallel

2) The host pulls SS' low, then transfers one byte of command to the sensor via MOSI, then releases SS' to float high again.

3) For 2-byte functions, (2) is repeated with $\geq$50us spacings between bytes.

4) The host immediately places its SPI port into Slave mode, floating SCK and MOSI'; SS' stays floating.

5) When the sensor has a command echo or data to send back, it puts its SPI register in Master mode, taking control over MOSI and SCK. SS' remains floating.

6) The sensor pulls SS' low, then clocks out its response byte to the host, then floats SS' high again.

7) The sensor repeats (6) as necessary for multiple byte responses.

8) The sensor returns to slave mode.

After the transmission sequence, the SPI lines float high or are left to float in an indeterminate state (MOSI) until the next transmission sequence is initiated by the host. The host should wait for >1ms after a sequence before initiating another transmission sequence.

See Section 3.15, page 10, for a description of the Alert pin which can be used to reduce communication traffic.

Figure 4-2 SPI Connections
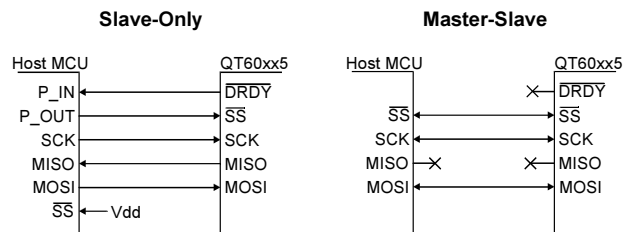
Figure 4-3 SPI Slave-Only Mode Timing
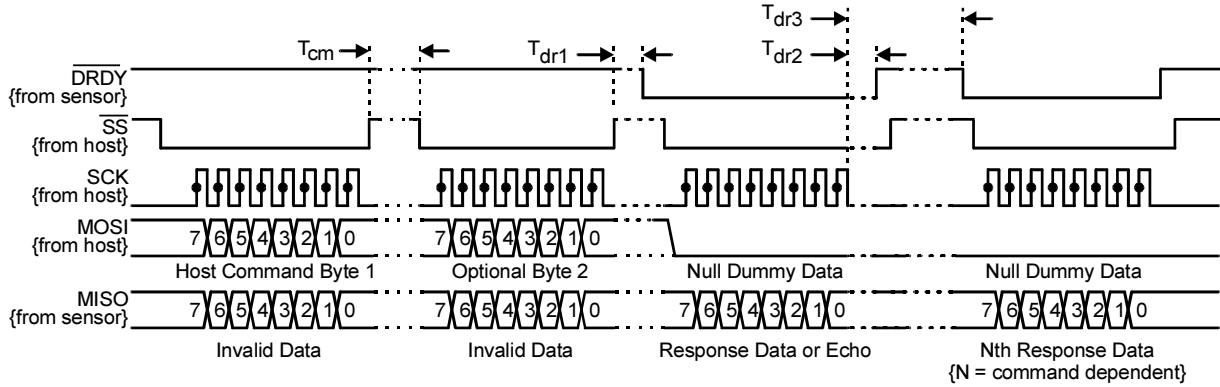
Figure 4-4 SPI Master/Slave Mode Timing
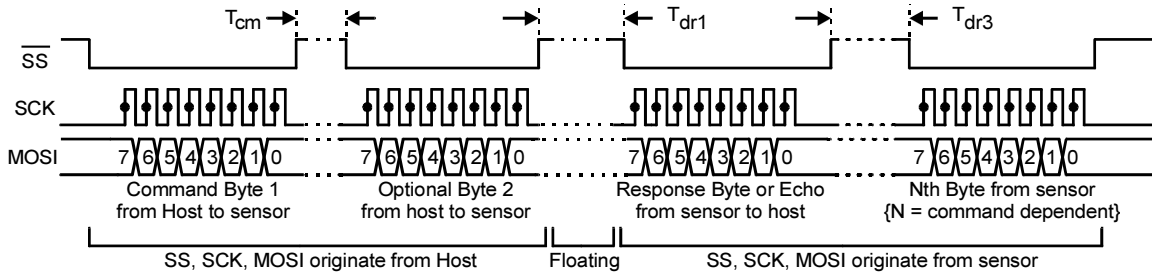
Figure 4-5 UART Timing
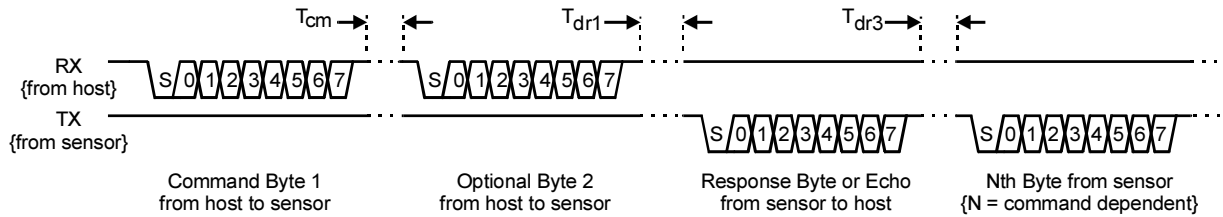
4.5 UART Interface

Refer to Figures 4-1 and 4-5.

UART communications requires only 2 wires, TX and RX to communicate with a host device. All communications must be initiated by the host. The baud rate is determined by Setup ^Q (page 25); the maximum baud rate with a 12MHz oscillator is 57.6K. UART communications uses the following settings:

Table 4-1 Typical Tdr1 Response Delays (100µs sample ramp)

Function Type	Burst Spacing		
	500µs	1ms	2ms
Setup - Put (affect 1 key)	10ms	10ms	10ms
Setup - Put (affect 8 keys)	20ms	20ms	20ms
Setup - Put (affect 16 keys)	65ms	65ms	65ms
Lock reference Level (L)	65ms	65ms	65ms
Calibrate command (all keys)	500µs	500µs	500µs
Get key errors (E)	450µs	450µs	450µs
Get keys pushed (K)	350µs	350µs	350µs
All other commands	350µs	350µs	350µs

Baud rate .... 9,600 - 57,600
Data length .... 8 bits
Parity .... None
Stop bits 1
Host command space, Tcm .... ≥ 50µs
Response delay to host, Tdr1 .... Table 4-1, also, Sec. 6
Multi-byte return spacing, Tdr3 .... 10µs to 2ms

The actual baud rate is determined by Setup ^Q (page 25).

A UART command may consist of one or two bytes with a ≥50us delay between command bytes. At the end of a full command, the host must await a response from the sensor.

The sensor may take some time to process the host command and respond. When it does so, it sends back its data. For multi-byte responses, the bytes will be sent at intervals which may be somewhat irregular depending on the request and the processing load of the sensor. The host must be prepared to accept the sensor data as it comes or there can be a data overrun in the host. *If the data returns too quickly for the host to accept it, the baud rate should be lowered*.

A typical UART communication sequence is as follows:

1) Host sends a byte to the sensor.

2) For 2-byte functions, a ≥50us delay is inserted by the host and then the second byte is sent.

3) If the sensor has a command echo or data to send back, it does so. The delay from step 2 to step 3 is shown in Table 4-1. The delay between successive response bytes (if they occur) is parameter Tdr3 noted above.

4) The sensor repeats (3) as necessary for multiple byte responses.

5) The sensor waits for the next command.

The host should wait for >1ms after a sequence before initiating another transmission sequence to be sure that the sensor has completed any residual activities from the prior command. Commands that are sent to the host prematurely will be ignored.

4.6 Sensor Echo and Data Response
The devices respond to each and every valid command from the host with at least one return byte. In the case of functions that do not send data back to the host, the part returns the command itself as an echo, but only after the function has been processed to completion; this also holds for 2-byte functions where the second byte is an operand: in these cases the return byte is an echo of the command, not the operand.

One important exception to this is the recalibration command 'b' which returns an acknowledgment immediately rather than prior to the actual recalibration.

Commands that return data do not send back a command echo. If desired, the command byte can be verified via the 'l' (lowercase L) function; see page 25.

The host should not transmit a new command until the last command has been processed and responded to completion, plus 1ms.

Commands that are not recognized are ignored, and the host should monitor for timeouts to detect these conditions. If this occurs a new command should not be sent until the specified timeout condition has expired.

The maximum timings shown in Table 4-1 and Section 6-5 are guaranteed provided that the part is operating within its burst timing limitations described in Section 5.7. If the burst timing is in violation, the response time to a command may take considerably longer.

4.7 Parallel Scan Port
The parallel port can be used to directly replace an electro-mechanical or membrane keyboard. The port is electrically equivalent to a 4x4 switch matrix with the exception that the response to a host scan requires up to 100µs. The XS inputs (pins 19..22) are active high; only one XS line should ever be driven high at a time (except for error scan, noted below); the

Figure 4-6 Filtering; SPI Slave-Only Connections
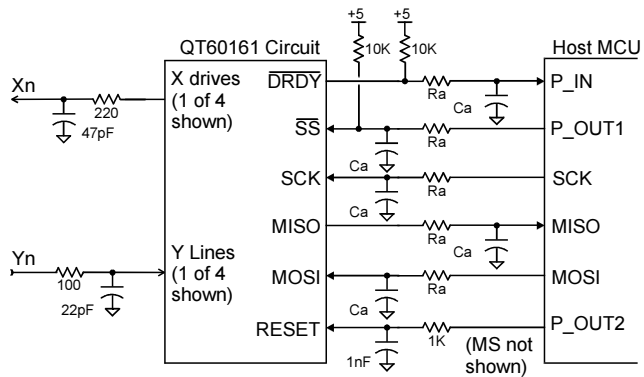
Figure 4-7 Filtering; SPI Master-Slave Connections
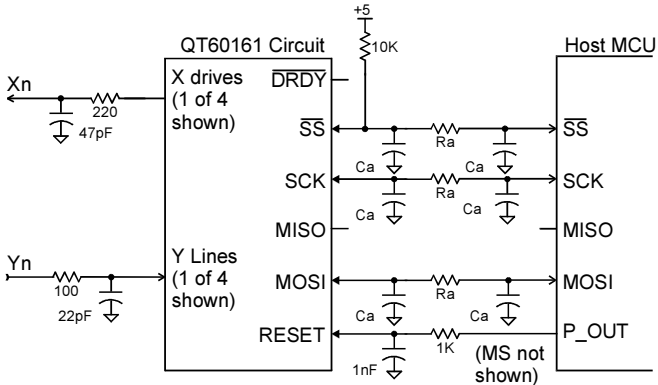
Recommended Values of Ra & Ca for Figures 4-6 and 4-7

SPI Clock Rate	Ra	Ca
3MHz	680	47pF
750kHz	1,000	120pF
187.5kHz	1,000	270pF
93.75kHz	2,200	470pF

output response is found on the YS lines (pins 23..26), and these are also active high. The bit pattern found on the YS lines indicates any keys that are touched; like a real matrix, the device can set multiple bits on the YS lines.

The host should scan to individual lines XS0..XS3. XS0 maps to matrix drive line X0 (pin 13). The response on YS0 maps to matrix line Y0. Thus, the scan port logic exactly mimics the wiring and scanning of the matrix keys.

The parallel scan port operates on a continuous basis, but is slower to react when either serial port is in operation. If either serial port is operational, the scan port updates with every acquisition burst, i.e. 16 times during a complete scan of the matrix.

For a full-time higher speed scan port response, it should be enabled as the sole interface via the option jumper settings shown in Figure 4-1. The port itself is found on pins 19 through 26 (Figure 3-2). In this dedicated mode, the scan port outputs within 100µs of receiving a scan input from the host.

Error scan: The host can extract error information from the scan port by setting all XS lines to logical '1' simultaneously. The part then returns a high level on any YS lines corresponding to Y matrix lines having key errors. Thus a single YS bit, if high, could indicate errors on any or all of 4 keys. Errors are reported for the following conditions:

   a. Key(s) are currently recalibrating
   b. Key(s) tried to calibrate 5 times and failed each time
   c. Key(s) signal references are under- or over- limit

It is not possible to determine the cause of the error or specific key(s) in error via the parallel scan port.

4.8 Eeprom Corruption
The device stores its Setup data in an internal eeprom which can be readily altered via Put mode commands. Sometimes noise on Vdd, the SPI lines or Reset pin can cause eeprom corruption which can be difficult or inconvenient to correct.

The device should always be left in Get mode to prevent spurious commands from corrupting the eeprom. The Get command should ideally be repeated every second or so to ensure that if noise on the SPI lines causes a false Put mode command that it does not last long. Preferably, the 'l' command (lowercase 'L') should be used to verify that the Put command has succeeded.

Flash backup: The part backs up the entire eeprom array into onboard Flash rom after one or more Setup write commands have been issued and the part is then reset. During normal operation the part constantly compares the Flash area with the eeprom array to ensure the two sections match. If an eeprom error is detected, the device sets an error flag (bit 4) in the general device status byte (Command '7', page 19) which can be read by the host device. The LED output also becomes active. If the bit 4 error flag is set, the host should immediately induce a device reset.

Bit 4 is also set if an intentional write has been made to eeprom, but not yet copied into Flash via the reset process. It is perfectly acceptable to continue altering any number of Setup parameters prior to doing the reset, ignoring this bit.

During power up or after a reset, the device compares the Flash area with eeprom, and if there is a discrepancy the eeprom is refreshed from Flash, unless an intentional write was detected in which case the Flash is updated from the

eeprom. As intentional writes in Put mode should only occur during manufacture, it is normally safe to assume that eeprom changes during normal run mode are errors.

The host can also periodically test the checksum of the eeprom as a backup mechanism to the bit 4 error flag.

The uppercase 'L' command, Lock Reference Levels, also writes data to eeprom, and this data also has the potential to become corrupted. This data is also backed up in Flash so that it can be recovered, and an error in this data will also set bit 4 and also alter the checksum. Also, the 'L' command only operates if the device is in Put mode as a further protection.

Flash memory has a limit of 1,000 write cycles, so copy-to-Flash should not be used often.

5 Commands & Functions

The command structure is designed to minimize control and data traffic. All repetitive data and status commands from the host are single-byte, and most commands result in single-byte device responses. Behavioral setup commands involve multiple bytes but these are infrequently used.

Special 'scope' commands exist to restrict subsequent commands to a specific key or range of keys. This control structure permits most matrix keys, which are usually identical in shape and size, to be programmed 'in bulk' using a 'global' scope command, followed by a scope restriction to specific key(s), followed by more key programming, to prevent the need for tedious key-by-key programming across an entire matrix.

There are four types of commands:

Direction - Determine whether subsequent commands are used to get data from or put data to the part;

Scope - Restrict the range of effect of subsequent commands to a specific set of keys;

Status - Cause the part to respond with key information, such as detections, signals, error codes, and the like;

Setup - Modify functionality such as burst length, threshold levels, drift compensation characteristics, etc.

Supervisory - Special functions such as diagnostics, calibration, etc. which affect the part as a whole.

All command types can be intermixed. Even during normal device operation it is possible to use Setup and Supervisory functions to alter key behavior on the fly. There is no special 'setup mode'.

Get/Put, Scope, and many Supervisory functions are volatile and do not persist after a power down or reset cycle. Some Supervisory commands require that the part be reset in order for the new settings to take effect.

Note that the Setup functions write to eeprom and require extra time for a response back to the host. Also note that as with all eeprom memories there is a recommended lifetime limit to the number of writes; this limit is 100,000 cycles.

Command functions are summarized in Section 5-6.

It is highly advised to test the device checksum (command '6', page 18) or individual settings or the general device status ('7') once Setups have been programmed into the part, each time the part is powered up and periodically while running.

The part backs up all eeprom locations into Flash, from which data is restored automatically following a reset if eeprom corruption is detected. The part should also be reset after any Put command(s) in order to force the copy of eeprom data into Flash. See Section 4.8.

5.1 Put / Get Direction Commands

Setup commands can be used to either send control information to the part for programming into its internal eeprom, or to extract the current setting of this information. The same Setup function can do either. To accomplish this the device relies on direction control via the Get and Put commands. In Get mode, a Setup command will return information. In Put mode, the behavior of the device is altered, and often a second operand byte must be sent.

The powerup or reset default mode is Get. The current Get/Put mode persists until countermanded by a different Get/Put command or until the device is reset or powered off.

It is advisable to use Put mode only when actually writing Setups to the device, which will happen infrequently; the part should normally be left in Get mode. Get mode acts as a lock to prevent accidental changes to the internal eeprom.

Multiple direction commands of the same type (g, g, g, g ...) are harmless and can be used to insure that the part does not accidentally enter Put mode for a prolonged period, for example due to noise glitches on the SPI lines. The 'g' command can be repeated every few seconds.

g **0x67 - GET COMMAND**

	Scope	Bytes / Cmd	2nd Byte Range	Returns
Put	n/a	1	n/a	0x67
Get	n/a	n/a	n/a	n/a

Lowercase 'G'. The 'g' command causes the device to treat all subsequent Setup commands as 'Gets'; after, when a Setup command is received from the host the part will respond by sending back the current status of that Setup parameter.

The 'g' command is always single-byte and echoes back itself.

p **0x70 - PUT COMMAND**

	Scope	Bytes / Cmd	2nd Byte Range	Returns
Put	n/a	1	n/a	0x70
Get	n/a	n/a	n/a	n/a

Lower case 'p'. The 'p' command causes the device to treat all subsequent Setup commands as 'Puts'; after, when a 2-byte Setup command is received from the host the part will respond by programming in the desired parameter for the key(s) which are affected.

The 'p' command is always single-byte and echoes back itself.

5.2 Scope Commands

The host should always set the scope parameter when initializing the part during normal operation as well as during setup. Scope commands are persistent and apply to all subsequent functions that are affected by scope, until a different scope command is issued. On powerup or after reset the device defaults to scope = 'all keys'.

Many functions only address one key regardless of the current scope; in these cases the key being addressed is always the key last set by the 's' or 'x' and 'y' commands. If the 's' command was last set to key 9, then even though the 'S' command was issued afterwards the one-key scope will remain key '9'. Similarly if 'x' was set to 2 and 'y' to 3, then the one-key scope will remain key x=2 / y=3 (key #14). This rule operates for either Put or Get commands.

Key numbering convention: The numbering of keys goes by row then column. For example, the key in row X=3, column Y=1 (X3Y1) is key 7. The formula for conversion of an X-Y location to a key number is:

$$\text{key number} = X\_row + (Y\_column \times 4)$$

Row and column numbers are per Fig. 1-5. Keys are acquired in this same burst sequence, i.e. X0Y0, X1Y0, X2Y0 etc.

s **0x73 - SPECIFIC KEY SCOPE**

	Scope	Bytes / Cmd	2nd Byte Range	Returns
Put	n/a	2	0x00..0x0F	0x73
Get	n/a	n/a	n/a	n/a

Lowercase 'S'. Targets a specific individual key for all further functions that are affected by scope. The second byte must contain a binary key number from 0..15.

S **0x53 - ALL KEYS SCOPE**

	Scope	Bytes / Cmd	2nd Byte Range	Returns
Put	n/a	1	n/a	0x53
Get	n/a	n/a	n/a	n/a

Uppercase 'S'. Addresses all keys in the matrix for all further functions that can target a group of keys.

x **0x78 - ROW KEYS SCOPE**

	Scope	Bytes / Cmd	2nd Byte Range	Returns
Put	n/a	2	0x00..0x03	0x78
Get	n/a	n/a	n/a	n/a

Lowercase 'X'. Targets keys in a specific row for functions that can address key groups. The second byte must contain a row number from 0..3.

y **0x79 - COLUMN KEYS SCOPE**

	Scope	Bytes / Cmd	2nd Byte Range	Returns
Put	n/a	2	0x00..0x03	0x79
Get	n/a	n/a	n/a	n/a

Lowercase 'Y'. Targets keys in a specific column for functions that can address key groups. The second byte is a binary column number from 0..3.

5.3 Status Commands

Status commands cause the sensor to report back information related to keys and their signals.

It is not necessary to set the part to Get mode with these commands, although it is advised to leave the part in Get mode as a normal precaution (see Section 5.1)

0 **0x30 - SIGNAL FOR SINGLE KEY**

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	1	1	2	0..0xFFFF

Numeric '0'. Returns the signal level in 16-bit unsigned binary for one key whose location is determined by scope. The least significant byte is returned first.

Note that the signal direction is inverted: decreasing values correspond to more touch due to the physics of key detection described in Section 1.1.

1 **0x31 - DELTA SIGNAL FOR SINGLE KEY**

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	1	1	1	0x00..0xFF

Numeric '1'. Returns the value {Reference - Signal} in unsigned 8-bit binary for one key whose location is determined by scope. If Signal > Reference, the result is truncated to zero. The return value is also limited to 255 (0xFF).

Increasing amounts of this value correspond to increasing amounts of touch as the sign of signal is inverted (see 0x30 above).

2 **0x32 - REFERENCE VALUE**

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	1	1	2	0..0xFFFF

Numeric '2'. Returns the Reference value in unsigned 16-bit binary for one key whose location is determined by scope. The least significant byte is returned first.

5 **0x35 - DETECTION INTEGRATOR COUNTS**

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	1	1	1	0x00..0xFF

Numeric '5'. Returns the Detection Integrator counter value for one key whose location is determined by scope. This function is useful primarily for circuit diagnostics.

6 **0x36 - EEPROM CHECKSUM**

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	n/a	1	1	0x00..0xFF

Numeric '6'. Returns the entire eeprom checksum. This function is useful primarily for diagnostics and should periodically be used to check for valid eeprom contents.

The checksum should be computed when the entire device's settings, including the locked reference levels ('L' command) are known. The host can then periodically test the checksum to validate eeprom integrity. If needed, the eeprom can then

be reprogrammed by the host or the device can be reset to allow the eeprom to be updated from Flash memory (see Section 4.8).

The checksum is a simple 8-bit carry fold-back type. Changes to multiple Setups can generate identical checksums. Changes to one location only will always produce a different checksum. An identical change to 2, 4, 8, or all 16 keys is more prone to generating an identical checksum. A unique checksum can be obtained again by altering any Setup for another key (i.e. an unused key) to be different.

After any Setups change, the checksum will not be valid until after the device has been reset.

Note that the status byte returned by the '7' command contains a bit that is set if there is an error in eeprom data; this feature operates independently of the checksum command.

There is no put version of the command.

7 0x37 - GENERAL DEVICE STATUS

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	n/a	1	1	0x00..0x1F

Section 2.11, p. 7

Numeric '7'. Returns the part's general status byte which is a 4-bit pattern as follows:

    Bit 0: 1= one or more keys are in detection
    Bit 1: 1= one or more keys are recalibrating
    Bit 2: 1= one or more keys are reporting errors
    Bit 3: 1= sync fail; the part is not synchronized to an
             external source (if in that mode; see Section 3.14).
    Bit 4: 1 = Eeprom / Flash contents discrepancy

Higher bits report as 0's and are not used.

This command can be used as a general 1-byte status response; if one or more bits are set, the host can take further relevant action to narrow down the specific issue, such as which key is being touched or in error, via other commands.

<SP> 0x20 - SIGNAL LEVELS FOR GROUP

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	4, 16	1	8 or 32	0..0xFFFF

Space character. Same function as 0x30 above except returns a group response for 4 keys (if Scope = row or column) or 16 keys (if Scope = 'all keys'). If no group scope has been selected, returns data for all keys (32 bytes).

Two bytes are returned for each key; the least significant byte is always returned first.

! 0x21 - DELTA SIGNALS FOR GROUP

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	4, 16	1	4 or 16	0x00..0xFF

Exclamation character. Same function as 0x31 above except returns a group response for 4 or 16 keys depending on scope. If no group scope has been selected, returns data for all 16 keys (16 bytes). The values returned are limited to the range 0..255.

" 0x22 - REFERENCE LEVELS FOR GROUP

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	4, 16	1	8 or 32	0..0xFFFF

Double quote character. Same function as 0x32 above except returns a group response for 4 or 16 keys depending on scope. If no group scope has been selected, returns data for all 16 keys (32 bytes).

% 0x25 - DETECT INTEGRATOR COUNTS FOR GROUP

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	4, 16	1	4 or 16	0x00..0xFF

Percent character. Same function as 0x35 above except returns a group response of 4 bytes (Scope = row or column) or 16 bytes (Scope = 'All keys'). If no group scope has been selected, returns data for all 16 keys.

e 0x65 - ERROR CODE FOR SELECTED KEY

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	1	1	1	0x00..0x0F

Section 2.11, p. 7

Lowercase 'E'. Returns the error byte for a selected key defined by the 's' command. A 4-bit pattern is returned:

b7	b6	b5	b4	b3	b2	b1	b0
u	u	u	u	L	H	R	F

    F: 1= failed last full recalibration attempt
    R: 1= key is in process of full recalibration
    H: 1= key reference is high (above normal bounds)
    L: 1= key reference is low (below normal bounds)
    u: undefined

Refer also to Section 2.10.

F, Bit 0 is set if it failed to calibrate properly during a forced recalibration. The sensor will automatically make 5 sequential attempts at recalibration before setting this flag.

R, Bit 1 is set if the key is in the process of a full recalibration. When bit 1 is set, bits 2 and 3 are cleared.

H, Bit 2 when set indicates that the key's reference level has exceeded the upper boundary described in Section 2.8 and as defined by Command ^N (page 23).

L, Bit 3 when set indicates that the key's reference level falls below the lower boundary described in Section 2.8 and as defined by Command ^O (page 23).

If either H or L are set, it means that the key is probably defective.

E 0x45 - ERROR CODES FOR GROUP

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	1, 4, 16	1	1 or 4	0x00..0xFF

Section 2.11, p. 7

Uppercase 'E'. Returns general error codes for a range of keys defined by scope. Returns either 1 or 4 bytes depending on whether a single key, row, column, or entire matrix are selected.

The bitfields for single key scope are the same as for 'e' above.

The bitfields for a single row (X) are:

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	Y3	Y2	Y1	Y0

The bitfields for a single column (Y) are:

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	X3	X2	X1	X0

The bitfields for a global response are:

	b7	b6	b5	b4	b3	b2	b1	b0
byte1	-	-	-	-	X3Y0 3	X2Y0 2	X1Y0 1	X0Y0 0
byte2	-	-	-	-	X3Y1 7	X2Y1 6	X1Y1 5	X0Y1 4
byte3	-	-	-	-	X3Y2 11	X2Y2 10	X1Y2 9	X0Y2 8
byte4	-	-	-	-	X3Y3 15	X2Y3 14	X1Y3 13	X0Y3 12

Byte 1 is the first returned byte in the sequence.

In all the above examples a '1' in a bit position indicates that there is some type of error associated with the key. The use of the 'e' command (or 'E' with scope set to a specific key) will specify the nature of the error.

k 0x6B - REPORTING OF FIRST TOUCHED KEY

	Scope	Bytes / Cmd	#Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	n/a	1	1	0x00..0xFF

Section 2.11, p. 7

Lowercase 'K'. Returns a byte that indicates which (if any) key has been touched. The byte is structured as follows:

b7	b6	b5	b4	b3	b2	b1	b0
m	-	-	-	k3	k2	k1	k0

Bits are used as follows:
> m - if '1', indicates that yet another key is active
> k0..k3 - indicates the key number of a first detected key, in the range 0..15 (0x00..0x0F).

If a reported key drops out while other keys are active, 'k' will report one of the other active keys, but there is no rule for which of the next keys gets reported in k0..k5.

If the byte returned has a value of 255 (0xFF), then no key has been detected.

K 0x4B - Key Touch Reporting for Group

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	1, 4, 16	1	1 or 4	0x00..0xFF

Section 2.11, p. 7

Uppercase 'K'. Returns 1 or 4 bytes depending on the current scope. The byte(s) returned contain a bit pattern which indicates touched keys. A scope of a single key, a row or a column will return one byte. A scope of all keys will return 4 bytes.

The bitfields for a single key are:

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	key

The bitfields for a single row (scope is X) are:

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	Y3	Y2	Y1	Y0

The bitfields for a single column (scope is Y) are:

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	X3	X2	X1	X0

The bitfields for a global report are:

	b7	b6	b5	b4	b3	b2	b1	b0
byte1	-	-	-	-	X3Y0 3	X2Y0 2	X1Y0 1	X0Y0 0
byte2	-	-	-	-	X3Y1 7	X2Y1 6	X1Y1 5	X0Y1 4
byte3	-	-	-	-	X3Y2 11	X2Y2 10	X1Y2 9	X0Y2 8
byte4	-	-	-	-	X3Y3 15	X2Y3 14	X1Y3 13	X0Y3 12

Byte 1 is the first returned byte in the sequence.

In all the above examples a '1' in a bit position indicates that the key is touched; a '0' indicates no touch.

5.4 Setup Commands

Setup functions are those that alter the behavior a key or a group of keys. The setups are programmed into eeprom locations in the part and ordinarily do not need to be reprogrammed once set. However it is possible to change a setup while the device is in normal operation without interrupting the sensing function of the part.24

Setup functions alter the internal eeprom, and this requires a much longer time to complete than other commands; see Table 4-1.

Setup 'put' commands become effective immediately after the echo response of the command byte unless otherwise noted; some setups require that the key(s) being altered be recalibrated with the 'b' command (page 24) before they take effect.

^A 0x01 - NEGATIVE DETECT THRESHOLD

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	1, 4, 16	2	0x04..0x40	0x01
Get	1	1	n/a	0x04..0x40

Section 2.1, p. 5

Ctrl-A. In Put mode, the command followed by a setting is programmed into eeprom for the key(s) affected by scope.

1, 4, or 16 keys may be affected. Valid decimal values are:

```
4    5    6    7    8    10   12   15
17   20   25   30   35   45   55   64
```

Values other than the above will be rounded down.

In Get mode, the command will return a single byte according to the current scope rules (Section 5.2).

This controls key sensitivity by setting the counts of signal delta needed to cause a detect. Higher = less sensitive. Numbers should be 6 or greater under most conditions to reduce the probability of noise detection. Numbers greater than 20 indicate that the burst length is probably too high. This setup interacts with Burst Length (^F).

^B 0x02 - POSITIVE DETECT THRESHOLD

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	1, 4, 16	2	0x04..0x40	0x02
Get	1	1	n/a	0x04..0x40

Section 2.2, p. 5

Ctrl-B. In Put mode, the command followed by a setting is programmed into eeprom for the key(s) affected by scope. 1, 4, or 16 keys may be affected. Valid decimal values are:

```
4    5    6    7    8    10   12   15
17   20   25   30   35   45   55   64
```

Values other than the above will be rounded down.

In Get mode, the command will return a single byte according to the current scope rules (Section 5.2).

This setup controls the ability of a key to recalibrate quickly should the signal transition positive quickly, as when a touch is prolonged enough to cause a recalibration, and when the key is then 'untouched'. This condition can also be caused by a foreign object being removed from a key. The value should normally be set between 6 and 10 counts. If the value is very

high, the key will still recover by means of the drift compensation process, albeit more slowly.

^C 0x03 - NEGATIVE THRESHOLD HYSTERESIS

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	16	2	0x01..0x03	0x03
Get	16	1	n/a	0x01..0x03

Section 2.3, p. 5

Ctrl-C. In Put mode, the command followed by a setting is programmed into eeprom for all keys only. The value should be from 0 to 3, representing hysteresis as follows:

    0:   50%
    1:   25%
    2:   12.5%
    3:   0% (no hysteresis)

Values other than the above will be rounded down.

The percentage is the distance from the threshold level to the reference level. The hysteresis level is always closer to the threshold point than to the reference point. 25% is a reasonable value under most conditions.

As this parameter is common to all keys, Put and Get operations send or return only one byte.

^D 0x04 - POSITIVE THRESHOLD HYSTERESIS

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	16	2	0x01..0x03	0x04
Get	16	1	n/a	0x01..0x03

Section 2.3, p. 5

Ctrl-D. Identical in operation to ^C above except this applies to positive 'detections' used to recalibrate the sensor (see ^B above for details). Uses same hysteresis values as ^C above.

^F 0x06 - BURST LENGTH

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	1, 4, 16	2	0x00..0x40	0x06
Get	1	1	n/a	0x00..0x40

Section 3.5, p. 8

Ctrl-F. In Put mode the command sets the burst length of one or more keys, according to the current scope. Valid decimal values are:

```
0    1    2    3    4    5    7    10
12   15   20   25   30   40   50   64
```

Values other than the above will be rounded down.

In Get mode, the command will return a single byte according to the current scope rules (Section 5.2).

^F sets the length of the acquisition burst on a key by key basis. This setting is directly proportional to signal gain. This setup interacts with Negative and Positive Threshold (^A and ^B). Increasing ^F can allow for higher threshold levels and more robust signals, at the expense of increased radiated emissions and reduced Cx load capacity.

Special condition: If the value for ^F for a key is set to zero the burst disabled and the key will not function; the key will report back with an error code. The timing for the 'phantom burst' will be preserved so that overall key scan timing will remain unchanged.

^G 0x07 - BURST SPACING

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	16	2	0x00..0x02	0x07
Get	16	1	n/a	0x00..0x02

Section 3.8, p. 9

Ctrl-G. In Put mode, sets the spacing between successive acquire bursts for the entire matrix.

The second byte indicates the spacing to be set according to the following table:

    0:   500µs (0.5ms)
    1:   1000µs (1ms)
    2:   2000µs (2ms)

Values higher than 2 will be truncated to 2.

Longer delay times equate to slower matrix scanning. At lower delay times (faster rep rates) there can be conflicts with long burst lengths and long conversion times which will prevent proper operation; see also Section 3.6, and Section 5.7.

Burst spacing also affects recalibration time; see Section 2.10.

The scope for this function is always 'all keys'.

^H 0x08 - NEGATIVE DRIFT COMPENSATION RATE5

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	1, 4, 16	2	0x01..0x64	0x08
Get	1	1	n/a	0x01..0x64

Section 2.4, p. 5

Ctrl-H. In Put mode, sets the rate of drift compensation used during periods of non-detection, in the negative signal direction. Valid decimal values are:

    1   2   3   4   6   8   10   12
    15   20   25   33   45   60   75   100

Values other than the above will be rounded down.

These numbers correspond to the amount of drift compensation applied, in 100ms/count of reference change, for signals which are negative with respect to the reference level, i.e. in the same direction as legitimate detections. Higher numbers equate to slower drift compensation. Overcompensation (too fast) can result in the suppression of legitimate detections. Under-compensation can result in inadequate compensation for rapid environmental changes. Values of 15 to 45 (1.5 to 4.5 secs/count) are considered normal under most conditions.

Drift compensation does not occur while the signal has passed below the negative threshold level or subsequently remained below the negative hysteresis level.

In Get mode, the command will return a single byte according to the current scope rules (Section 5.2).

The scope in Put mode can be one key, a row or column, or all keys.

^I 0x09 - POSITIVE DRIFT COMPENSATION RATE

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	1, 4, 16	2	0x01..0x64	0x09
Get	1	1	n/a	0x01..0x64

Section 2.4, p. 5

Ctrl-I. Same as ^H above in all respects, except operates only when the signal is positive with respect to the reference level, i.e. in an abnormal direction. It is usually desirable to set this rate much faster than for ^H, i.e. to a lower number. Valid decimal values are:

    1   2   3   4   6   8   10   12
    15   20   25   33   45   60   75   100

Values other than the above will be rounded down.

Values of 4 to 10 (0.4 to 1.0 secs/count) are considered suitable for most systems.

Positive drift compensation continues to operate even if the signal has exceeded the positive threshold.

^J 0x0A - NEGATIVE DETECT INTEGRATOR LIMIT

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	1, 4, 16	2	0x00..0xFF	0x0A
Get	1	1	n/a	0x00..0xFF

Section 2.6, p. 6

Ctrl-J. In Put mode, sets the detection integration limit for one or more keys according to scope.

The unit of measure is a burst, i.e. a setting of 5 means that a detection must be sensed 5 bursts in sequence. A burst for a key occurs once every complete matrix scan. The second byte must be one of the following values (shown in decimal):

    0   1   2   3   5   7   10   15
    20   32   45   60   90   123 175   255

Values other than the above will be rounded down.

In Get mode, the command will return a single byte according to the current scope rules (Section 5.2).

This setup can be used as a noise filter, or as a mechanism to intentionally slow down key reaction time in order to require a long user touch.

Special condition: If the value for ^J is set to zero the key is disabled, but the burst for the key is still generated.

^K 0x0B - POSITIVE RECALIBRATION DELAY

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	1, 4, 16	2	0x00..0xFF	0x0B
Get	1	1	n/a	0x00..0xFF

Section 2.7, p. 6

Ctrl-K. In Put mode, sets the delay until recalibration, timed from when the signal first crosses the positive threshold.

The second byte controls the delay in 100ms increments, and must be one of the following valid values:

```
 0   1   2   3   5   7  10  15
20  32  45  60  90 123 175 255
```

Values other than the above will be rounded down. As an example, a value of 60 will cause a 6-second delay.

In Get mode, the command will return a single byte according to the current scope rules (Section 5.2).

Special condition: If ^K is set to zero this feature is disabled and the key will never auto-recalibrate on positive transitions; however drift compensation will still operate.

^L 0x0C - NEGATIVE RECALIBRATION DELAY

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	1, 4, 16	2	0x00..0xFF	0x0C
Get	1	1	n/a	0x00..0xFF

Section 2.5, p. 6

Ctrl-L. In Put mode, sets the delay until recalibration, timed from when the signal first crosses below the negative threshold as defined by ^A.2.5

The second byte represents the delay in 100ms increments, and must be one of the following valid values:

```
 0   1   2   3   5   7  10  15
20  32  45  60  90 123 175 255
```

Values other than the above will be rounded down. As an example, a setting of 85 will cause delays of 6 seconds.

In Get mode the function returns a single value only; if scope is set to row, column, or all, only the value for the lowest ranking key in the group will be returned.

Special condition: If the value for ^L is set to zero this feature is disabled and the key will never auto-recalibrate after a prolonged touch.

^M 0x0D - INTRA-BURST PULSE SPACING

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	16	2	0x01..0x0A	0x0D
Get	16	1	n/a	0x01..0x0A

Section 3.7, p. 9

Ctrl-M. In Put mode, sets the amount of time between individual pulses in a burst.

The second byte must be in the range of 1 to 10 decimal; other values will be ignored. The setting applies to all keys.

The value corresponds to the timing between pulses within a burst, in microseconds. For example, a setting of 5 will set the pulse spacing to 5 microseconds.

In Get mode the function returns the current value of ^M.

Intra-burst pulse spacing controls the fundamental frequency of the burst and can have a strong effect on radiated emissions from the matrix control panel. It can also have an effect on susceptibility to external EMI if the external fields are close in periodicity to the burst spacing.

^N 0x0E - POSITIVE REFERENCE ERROR BAND

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	16	2	0x00..0xFF	0x0E
Get	16	1	n/a	0x00..0xFF

Section 2.8, p. 6

Ctrl-N. In Put mode, sets the amount of tolerable positive deviation in the reference level for all keys, in tenths of a percent, with regard to the 'locked' reference value for each key. The setup is global in nature and affects all keys equally.

Valid values are from 0 to 255 decimal. The percentage applied is one tenth the operand's decimal value.

In Get mode the function returns the current setting of ^N.

This setup is used to define the limit of possible positive reference deviation with respect to a factory setting, which is used in turn to set an error flag for key(s) whose reference level rises above the designated error band. If for example this setting is set to 50, and the device is calibrated and reference levels are locked (see command 'L', Lock Reference Levels, page 24) into the part by the OEM, then in the future if the reference level of a key should rise 5% over its Locked reference level then the key will report back an error flag via commands 'e' or 'E'.

Guardbands can be used to detect circuit faults as well as extremes of temperature or moisture on the circuitry.

Special condition: If the value is set to zero, this feature is disabled.

^O 0x0F - NEGATIVE REFERENCE ERROR BAND

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	16	2	0x00..0xFF	0x0F
Get	16	1	n/a	0x00..0xFF

Section 2.8, p. 6

Ctrl-O. In Put mode, sets the amount of tolerable negative deviation in the reference level for all keys, in tenths of a percent, with regard to the 'locked' reference value for each key. The setup is global in nature and affects all keys equally.

Valid values are from 0 to 255 decimal. The percentage applied is equal to the decimal value divided by 10, thus, a value of 20 equates to a 2% decrease (i.e. the lower boundary becomes 98% of the locked reference level).

In Get mode the function returns the current setting of ^M.

This setup is identical in nature to ^N except that it governs negative reference deviations.

Special condition: If the value is set to 0, this feature is disabled.

^P **0x10 - ADJACENT KEY SUPPRESSION ('AKS')**

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	1, 4, 16	2	0x00, 0x01	0x10
Get	1	1	n/a	0x00, 0x01

Section 2.9, p. 6

Ctrl-P. In Put mode, instructs logic for the keys specified by the current scope to suppress a pending touch detection under certain signal conditions.

Valid 2nd byte values for this function are:

    0:   AKS off {default}
    1:   AKS on

In Get mode, the command will return a single byte according to the current scope rules (Section 5.2).

AKS functions to suppress detections from water films which can 'spread' a touch signal from the touched key to adjacent keys.

AKS is also useful for panels with tightly spaced keys, where a fingertip can partially overlap an adjacent key. This feature will act to suppress the signals from the unintended key(s).

AKS only operates across keys that have been AKS-enabled; signal strength comparisons are not made with non-AKS-enabled keys.

Unused keys with burst lengths of zero are also ignored for purposes of AKS.

5.5 Supervisory / System Functions

Supervisory functions report or control miscellaneous functions that affect overall chip control, testing, or diagnostics. All supervisory functions ignore scope except where noted.

6 **0x36 - EEPROM CHECKSUM**

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	n/a	1	1	0x00..0xFF

See page 18.

L **0x4C - LOCK REFERENCE LEVELS**

	Scope	Bytes / Cmd	2nd Byte	Returns
Put	16	2	0x00	0x4C
Get	n/a	n/a	n/a	n/a

Section 2.8, p. 6

Uppercase 'L'. This is a put-only command that locks the reference levels of the device into eeprom for all keys, for boundary checking purposes over the product's life.

The whole command – 'L' followed by a null (0x00) - must be received within 100ms without any intervening byte, or the command will fail. The part must be in Put mode for this command to work.

The scope of this command is always 'all keys'.

This function records to eeprom the signal reference for all keys. The locked reference levels are used to compute boundary checks immediately after the command has finished. The results of this command to not take effect until the part has been reset.

Due to the large number of bytes written to eeprom by this command, there is a significant delay from the second byte until the return echo is sent back to the host.

This command should be used only during production. There is no get version of the command.

b **0x62 - RECALIBRATE KEYS**

	Scope	Bytes / Cmd	2nd Byte	Returns
Put	1, 4, 16	1	n/a	0x62
Get	n/a	n/a	n/a	n/a

Section 2.10, p. 7; Section 3.13.

Lowercase 'B'. This is a put-only command that causes the keys selected by scope to recalibrate. The part must be in Put mode for this command to work.

The return byte is sent before the keys have calibrated. While keys are in recalibration, status of the keys can be determined using the 'e' or 'E' commands.

If 'b' is sent while key(s) are already in the middle of recalibration, the affected key(s) will abandon the old calibration cycle and start a new one.

There is no get version of the command.

I 0x6C - RETURN LAST COMMAND CHARACTER

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	n/a	1	1	0x00..0xFF

Lowercase 'L'. This get-only command reports back with the value of the prior command received by the part. The command also reports back any erroneous commands, allowing the host device to verify that a command was correctly received.

If this command is repeated, the second and subsequent instances of 'l' will report back with 0x6C.

There is no put version of the command.

r 0x72 - RESET DEVICE

	Scope	Bytes / Cmd	2nd Byte	Returns
Put	n/a	2	0x00	0x72
Get	n/a	n/a	n/a	n/a

Section 3.11, p. 9

Lowercase 'R'. This put-only command hard-resets the part. The command 0x72 must be followed by a null (0x00) within 100ms or the command will fail. The part must be in Put mode for this command to work.

A reset occurs about 16ms after the echo byte 0x72 is transmitted back to the host. The part will resume communication and sensing in accordance with the timing shown in Section 3.13.

If for some reason the part is unable to send back the echo character 0x72, the command will fail.

There is no get version of the command.

V 0x56 - RETURN PART VERSION

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	n/a	1	1	0x00..0xFF

Uppercase 'V'. This get-only command returns the part version number.

There is no put version of the command.

W 0x57 - RETURN PART SIGNATURE

	Scope	Bytes / Cmd	# Bytes Rtnd	Returns
Put	n/a	n/a	n/a	n/a
Get	n/a	1	1	0x10

Uppercase 'W'. This get-only command returns the part signature as follows:

    0x10   (16 decimal)

There is no put version of this command.

Z 0x5A - ENTER SLEEP

	Scope	Bytes / Cmd	2nd Byte	Returns
Put	n/a	2	0x00	*0x5A, 0x5A
Get	n/a	n/a	n/a	n/a

Section 3.14, p. 9

Uppercase 'Z'. This put-only command forces the device to enter sleep mode. The command 0x5A must be followed by a null (0x00) within 100ms or the command will fail. The part must be in Put mode for this command to work.

The command returns 0x5A immediately before going to sleep, and a second 0x5A upon waking up.

If for some reason the device is unable to transmit the first return 'Z' character back to the host, for example due to the host not releasing the SS line, the part will completely reset after about 2 seconds.

The part will reawaken after a logic low is detected for 10μs on pin 11 (RST' pin, see Section 3.11). The device then sends a second 'Z' back to the host, and resumes from its prior state before it went to sleep without the need for recalibration. The device resumes in Get mode only.

There is no get version of the command.

^Q 0x11 - DATA RATE SELECTION

	Scope	Bytes / Cmd	2nd Byte Range	Returns
Put	n/a	2	0x00..0x04	0x11
Get	n/a	1	n/a	0x00..0x04

Section 4, p. 11

Ctrl-Q. This is a put-only command that sets the UART baud rate and the SPI clock rate. All timings assume a 12MHz oscillator. The part must be in Put mode for this command to work.

SPI Settings -

The acceptable values of the operand for SPI use are:

    0:    93.75 kHz
    1:    187.5 kHz
    2:    750 kHz
    3:    3 MHz

These values define the maximum SPI clock rate in Master mode (part originates the clock).

Note that when the part is receiving data, the host can send to the device at rates up to 3MHz even if the rate setting of ^Q is slower.

Refer to Sections 4.3 and 4.4 for SPI timing details.

New settings do not become effective until the device has been powered off and back on again or after the reset ('r') command.

UART Settings -

The acceptable values of the operand for UART use are:

    0:    9600 baud
    1:    14400 baud
    2:    19200 baud
    3:    38400 baud
    4:    57600 baud

There is no get version of this function.

Refer to Section 4.5for UART details.

New settings do not become effective until the device has been powered off and back on again or after the reset ('r') command.

^R **0x12 - OSCILLOSCOPE SYNC**

	Scope	Bytes / Cmd	2nd Byte Range	Returns
Put	1, 4, 16	2	0x00, 0x01	0x12
Get	1, 4, 16	1	n/a	0x00, 0x01

Section 3.16, p. 11

Ctrl-R. In Put mode, controls the oscilloscope sync function of Pin 43. The settings of this function are:

    0:   off {factory default}
    1:   on

When on, Pin 43 outputs a pulse that brackets the acquire burst(s) for the keys targeted by scope. Without this it is virtually impossible to view signals on an oscilloscope corresponding to a specific key.

Pin 43 idles low and pulses high during a sync pulse.

^R is volatile, that is, it does not persist after a power down.

^W **0x17 - NOISE SYNC**

	Scope	Bytes / Cmd	Byte 2 Range	Returns
Put	-	2	0x00, 0x01	0x17
Get	-	1	n/a	0x00, 0x01

Section 3.14, p. 9

Ctrl-W. In Put mode, sets whether the noise sync feature is enabled or disabled. The part must be in Put mode for this command to work.

The settings are:

    0:   off {factory default}
    1:   on

This function has global scope. The default value is 0 (off).

In Get mode this function returns the current setting of ^W.

The setting of ^W does not become effective until the device has been powered off and back on again or after the reset ('r') command has been issued.

5.6 Function Summary Table

Char	Hex	Name	Description	P/G	Put Mode Scope	Put Mode Bytes/Put	Put Mode Operand Range	Put Mode Returns	Get Mode Scope	Get Mode Bytes returned	Get Mode Return range	Default setting	Page
Direction Commands													
g	0x67	Get	all subsequent Setup commands become 'Gets'	P	-	1		0x67				Get	17
p	0x70	Put	all subsequent Setup commands become 'Puts'	P	-	1		0x70				Get	17
Scope Commands													
s	0x73	Set one key scope	targets a specific key in range 0..15	P	-	2	0x00..0x0F	0x73				undefined	18
S	0x53	Set all keys scope	targets all keys in the matrix	P	-	1		0x53				undefined	18
x	0x78	Set row keys scope	targets keys in a designated row, range 0..3	P	-	2	0x00..0x03	0x78				undefined	18
y	0x79	Set column keys scope	targets keys in a designated column, range 0..3	P	-	2	0x00..0x03	0x79				undefined	18
Status Commands													
0	0x30	signal for 1 key	get signal strength for 1 key	G					1	2	0..0xFFFF	-	18
1	0x31	delta signal for 1 key	get Reference-Signal for 1 key	G					1	1	0..0xFF	-	18
2	0x32	reference for 1 key	get Reference level for 1 key	G					1	2	0..0xFFFF	-	18
0	0x35	Det Integrator for 1 key	get detect integrator for 1 key	G					1	1	0..0xFF	-	18
6	0x36	eeprom checksum	get eeprom checksum of entire eeprom	G					-	1	0..0xFF	-	18
7	0x37	general device status	get device status of entire device	G					-	1	0..0x1F	-	19
<sp>	0x20	signals for group	get signal for group	G					4, 16	8, 32	0..0xFFFF	-	19
!	0x21	delta signals for group	get Reference-Signal for group	G					4, 16	4, 16	0..0xFF	-	19
"	0x22	references for group	get References levels for group	G					4, 16	8, 32	0..0xFFFF	-	19
%	0x25	Det integrator for group	get detection integrators for group	G					4, 16	4, 16	0..0xFF	-	19
e	0x65	error code for 1 key	get error code for 1 key	G					1	1	0..0x0F	-	19
E	0x45	error codes for group	get error bits for group	G					1, 4, 16	1, 4	0..0x0F	-	20
k	0x6B	report 1st key	get indication of first touched key	G					-	-	0..0xFF	-	20
K	0x4B	report touches for group	get indication of all touched keys	G					1, 4, 16	1, 4	0..0x0F	-	20

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Char	Hex	Name	Description	P/G	Put Mode				Get Mode			Default setting	Page
					Scope	Bytes/Put	Operand Range	Returns	Scope	Bytes returned	Return range		
Setup Commands													
^A	0x01	Negative threshold	Signal threshold; fewer counts = more sensitive 4, 5, 6, 7, 8, 10, 12, 15, 17, 20, 25, 30, 35, 45, 55, 64	P/G	1, 4, 16	2	0x04..0x40	0x01	1	1	0x04..0x40	0x0C	21
^B	0x02	Positive threshold	sensitivity to positive signals for recalibration 4, 5, 6, 7, 8, 10, 12, 15, 17, 20, 25, 30, 35, 45, 55, 64	P/G	1, 4, 16	2	0x04..0x40	0x02	1	1	0x04..0x40	0x08	21
^C	0x03	Negative hysteresis	hysteresis for negative threshold 50%, 25%, 12.5%, 0%	P/G	16	2	0x00..0x03	0x03	16	1	0x00..0x03	0x01 (25%)	21
^D	0x04	Positive hysteresis	hysteresis for positive threshold 50%, 25%, 12.5%, 0%	P/G	16	2	0x00..0x03	0x04	16	1	0x00..0x03	0x01 (25%)	21
^F	0x06	Burst length	sets number of QT cycles / burst; zero disables burst 0, 1, 2, 3, 4, 5, 7, 10, 12, 15, 20, 25, 30, 40, 50, 64	P/G	1, 4, 16	2	0x00..0x40	0x06	1	1	0x01..0x40	0x0C	21
^G	0x07	Burst spacing	time from start of one burst to start of next burst 500us, 1ms, 2ms	P/G	16	2	0x00..0x02	0x07	16	1	0x00..0x02	0 (500us)	22
^H	0x08	Neg drift comp rate	rate of drift compensation for negative signal swings 0.1, 0.2, 0.3, 0.4, 0.6, 0.8, 1.0, 1.2, 1.5, 2.0, 2.5, 3.3, 4.5, 6.0, 7.5, 10 secs	P/G	1, 4, 16	2	0x01..0x64	0x08	1	1	0x01..0x64	0x1E (3s)	22
^I	0x09	Pos drift comp rate	rate of drift compensation for positive signal swings 0.1, 0.2, 0.3, 0.4, 0.6, 0.8, 1.0, 1.2, 1.5, 2.0, 2.5, 3.3, 4.5, 6.0, 7.5, 10 secs	P/G	1, 4, 16	2	0x01..0x64	0x09	1	1	0x01..0x64	0x0A (1s)	22
^J	0x0A	Neg det int limit	number of detections required to register a touch, counted in bursts of detection; zero disables a key. 0, 1, 2, 3, 5, 7, 10, 15, 20, 32, 45, 60, 90, 123, 175, 255 counts	P/G	1, 4, 16	2	0x00..0xFF	0x0A	1	1	0x00..0xFF	0x03	22
^K	0x0B	Pos recal delay	time required to trigger a recal from a positive signal excursion in 0.1s increments; zero disables recal. 0, 0.1, 0.2, 0.3, 0.5, 0.7, 1.0, 1.5, 2.0, 3.2, 4.5, 6, 9, 12.3, 17.5, 25.5 secs	P/G	1, 4, 16	2	0x00..0xFF	0x0B	1	1	0x00..0xFF	0x0A (1s)	23
^L	0x0C	Neg recal delay	time required to trigger a recal from a detection, in 0.1s increments. Zero disables recal. 0, 0.1, 0.2, 0.3, 0.5, 0.7, 1.0, 1.5, 2.0, 3.2, 4.5, 6, 9, 12.3, 17.5, 25.5 secs	P/G	1, 8, 64	2	0x00..0xFF	0x0C	1	1	0x00..0xFF	0x3C (9s)	23
^M	0x0D	Intra-burst spacing	period of QT pulses, in microseconds 1, 2, 3, 4, 5, 6, 7, 8, 9, 10us	P/G	16	2	0x01..0x0A	0x0D	64	1	0x02..0x0A	0x02	23
^N	0x0E	Pos error band	tolerable positive reference deviation with respect to Locked reference values, step 0.1%. Zero disables.	P/G	16	2	0x00..0xFF	0x0E	16	1	0x00..0xFF	0 (off)	23
^O	0x0F	Neg error band	tolerable negative reference deviation with respect to Locked reference values, step 0.1%. Zero disables.	P/G	16	2	0x00..0xFF	0x0F	16	1	0x00..0xFF	0 (off)	23
^P	0x10	Key suppression	adjacent key suppression feature; 1 = on	P/G	1, 4, 16	2	0x00, 0x01	0x10	1	1	0x00, 0x01	0 (off)	24

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Char	Hex	Name	Description	P/G	Put Mode					Get Mode			Default setting	Page
					Scope	Bytes/Put	Operand Range	Returns		Scope	Bytes returned	Return range		
Supervisory Commands														
6	0x36	Eeprom checksum	returns checksum of internal eeprom	G						-	1	0x00..0xFF	-	18
L	0x4C	Lock references	locks reference levels into eeprom for future boundary checks. 'L' must be followed by 0x00 (null) 100ms after the command byte	P	16	2	0x00	0x4C					-	24
b	0x62	Recal keys	fully recalibrate keys; return byte is sent prior to calibration	P	1, 4, 16	1		0x62					-	24
l	0x6C	Return last command	send back last command byte received	G						-	1	0x00..0xFF	-	25
r	0x72	Reset device	hard reset the device. 'r' must be followed by a null within 100ms.	P	-	2	0x00	0x72					-	25
V	0x56	Version	returns part version number	G						-	1	0x00..0xFF	-	25
W	0x57	Signature	returns part signature number	G						-	1	0x10	-	25
Z	0x5A	Sleep	force device into Sleep mode. 'Z' must be followed by a null within 100ms. 0x5A returned before and after entering Sleep	P	-	2	0x00	0x5A, 0x5A					-	25
^Q	0x11	Data rate	sets the Master mode SPI clock rate and UART rate; reset via 'r' command or hard reset to take effect SPI: 93.75kHz, 187.5kHz, 750kHz, 3MHz UART: 9.6k, 14.4k, 19.2k, 38.4k, 57.6k	P/G	-	2	0x00..0x04	0x11		-	1	0x00..0x04	0 (93.75k, 9600)	25
^R	0x12	Scope sync	oscilloscope sync control. 1 = on. feature is volatile - does not survive reset	P/G	1, 4, 64	2	0x00, 0x01	0x12		-	1	0x00, 0x01	0 (off)	26
^W	0x17	Noise sync	noise sync enable; 1 = on device must be reset to take effect	G/P	-	2	0x00, 0x01	0x17		-	1	0x00, 0x01	0 (off)	26

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5.7 Timing Limitations
The device requires processing time between bursts, as well as time to handle communications with the host. With short burst spacings, long burst lengths, and long intra-burst pulse spacings, the device can simply run out of available processing time. When this happens, burst timing and host communications slow down and become erratic.

It is important that burst spacings be verified on an oscilloscope with an actual keymatrix during development to be certain that the device timings are preserved and are constant. If not, the burst length and/or pulse spacing should be reduced.

Table 5-2 Permissible Burst Lengths (BL's)
Cs = 4.7nF, Cx = 5pF, Rs = 180K; 100µs ramp time

Pulse Spacing = 2µs		Pulse Spacing = 3µs		Pulse Spacing = 4µs		Pulse Spacing = 5µs		Pulse Spacing = 6µs	
Burst Spacing	Max BL	Burst Spacing	Max BL	Burst Spacing	Max BL	Burst Spacing	Max BL	Burst Spacing	Max BL
500	64	500	64	500	50	500	40	500	30
1,000	64	1,000	64	1,000	64	1,000	64	1,000	64
2,000	64	2,000	64	2,000	64	2,000	64	2,000	64

Pulse Spacing = 7µs		Pulse Spacing = 8µs		Pulse Spacing = 9µs		Pulse Spacing = 10µs	
Burst Spacing	Max BL	Burst Spacing	Max BL	Burst Spacing	Max BL	Burst Spacing	Max BL
500	30	500	25	500	20	500	20
1,000	50	1,000	50	1,000	40	1,000	40
2,000	64	2,000	64	2,000	64	2,000	64

5.8 Erratta / Notes
4 April 2003 - The QT60xx5 version 1.05 datasheet erroneously showed negative recalibration timeouts in the range from 1..255 seconds. The correct range is 0.1..25.5 seconds. From datasheet version 1.06 on, this document change has been made. The devices themselves are not affected.

6 Electrical Specifications

6.1 Absolute Maximum Specifications

Operating temp. . . . . -40°C to +105°C
Storage temp. . . . . -55°C to +125°C
V$_{DD}$. . . . . -0.5 to +5.5V
Max continuous pin current, any control or drive pin. . . . . ±10mA
Short circuit duration to ground, any pin. . . . . infinite
Short circuit duration to V$_{DD}$, any pin. . . . . infinite
Voltage forced onto any pin. . . . . -0.6V to (Vdd + 0.6) Volts
Frequency of operation. 16MHz
Eeprom maximum writes. . . . . 100,000 write cycles

6.2 Recommended operating conditions

V$_{DD}$. . . . . +4.75 to 5.25V
Supply ripple+noise. . . . . 5mV p-p max
Cx transverse load capacitance per key. . . . . 0 to 20pF
Fosc oscillator frequency. . . . . 12MHz +/-2%

6.3 DC Specifications

Vdd = 5.0V, Cs = 4.7nF, Freq = 12MHz, Ta = recommended range, unless otherwise noted

Parameter	Description	Min	Typ	Max	Units	Notes
I$_{DDR}$	Supply current, running			25	mA	Not including external components
I$_{DDS}$	Supply current, sleep		20		µA	Not including external components
V$_{IL}$	Low input logic level			0.8	V	
V$_{HL}$	High input logic level	2.2			V	
V$_{OL}$	Low output voltage			0.6	V	4mA sink
V$_{OH}$	High output voltage	Vdd-0.7			V	1mA source
I$_{IL}$	Input leakage current			±1	µA	
A$_R$	Acquisition resolution		10	16	bits	
R$_P$	Pullup resistors	35		120	kohms	Drdy, SS' pins

6.4 Protocol Timing

Parameter	Description	Min	Typ	Max	Units	Notes
T$_{PR}$	Parallel port response delay			100	µS	
T$_{DR}$2	Tdr delay from response	1		1,000	µS	
T$_{DR}$3	Multi-byte return spacing	15		2,000	µS	

6.5 Maximum Drdy Response Delays

... with adjacent key suppression disabled:

Function Type	Burst Spacing		
	500µs	1ms	2ms
Setup - put (affect 1 key)	10ms	10ms	10ms
Setup - put (affect 4 keys)	20ms	20ms	20ms
Setup - put (affect 16 keys)	65ms	65ms	65ms
Lock reference Level (L)	65ms	65ms	65ms
Calibrate command (all keys)	2ms	2ms	1.1ms
Get key errors (E), Get keys pushed (K)	1.5ms	2ms	1ms
All other commands	1.5ms	1ms	1ms

... with adjacent key suppression enabled:

Function Type	Burst Spacing		
	500µs	1ms	2ms
Setup - put (affect 1 key)	10ms	10ms	10ms
Setup - put (affect 4 keys)	20ms	20ms	20ms
Setup - put (affect 16 keys)	65ms	65ms	65ms
Lock reference Level (L)	65ms	65ms	65ms
Calibrate command (all keys)	2.5ms	2ms	1.2ms
Get key errors (E), Get keys pushed (K)	2ms	2ms	1.1ms
All other commands	1.5ms	2ms	1.1ms

Preliminary Data: All specifications subject to change.

7 Mechanical

7.1 Dimensions
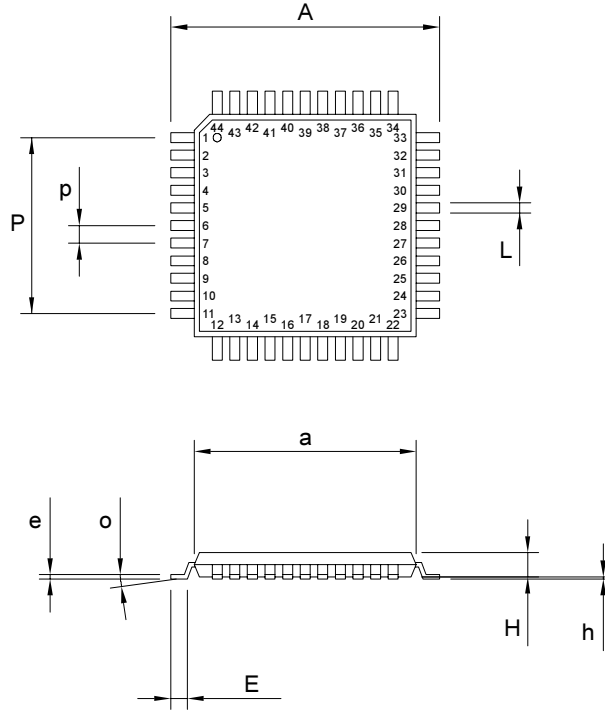
Package Type: 44 Pin TQFP						
SYMBOL	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
a	9.90	10.10	SQ	0.386	0.394	SQ
A	11.75	12.21	SQ	0.458	0.478	SQ
e	0.09	0.20		0.003	0.008	
E	0.45	0.75		0.018	0.030	
h	0.05	0.15		0.002	0.006	
H	-	1.20		-	0.047	
L	0.30	0.45		0.012	0.018	
p	0.80	0.80	BSC	0.031	0.031	BSC
P	8.00	8.00	BSC	0.315	0.315	BSC
o	0	7		0	7	

7.2 Marking

T_A	TQFP Part Number	Marking
-40^{0}C to +105^{0}C	QT60161B-AS	QT60161B-A

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