DATA SHEET

Part No.	AN12960A
Package Code No.	UBGA015-W-2020AEA

Contents

AN12960A

Monaural Class-D amplifier IC with built-in AGC

■ Overview

AN12960A is a Class-D audio amplifier IC for mobile devices such as mobile phone and so on.
AGC circuit which prevents sound distortion due to output saturation caused by excessive input is embedded. This IC is equipped with Auto SP Save function which automatically detects non-signal input condition and stops speaker amplifier, and noise at non-signal input can be reduced.
Either I^2C bus control mode or parallel control mode can be selected.

■ Features

1. High power efficiency by Class-D power amplifier (85%, 500 mW output power with 8 Ω load)
2. The original AGC circuit makes low distortion whether AGC is active or not.
   The ON level and attack/recovery time of the AGC can be selected with I^2C bus control.
3. Auto SP Save function
   In case of non-signal input, the auto SP save function automatically turns off speaker amplifier, and PWM output is stopped. When larger input signal than set detection level is input, SP Save mode is automatically deactivated and speaker amplifier starts and signal is output. The detection level and detection time for the function to be active are selectable.
4. EVR (Electric volume) function : 0 dB to –47 dB by 1 dB
5. Gain Selection : 3-pattern of +16 dB, +19 dB, +22 dB
6. I^2C bus control mode and parallel control mode (changed by High/Low voltage of a pin) can be used for IC control.

■ Applications

- Audio amplifier for mobile devices, such as a cellular phone

■ Package

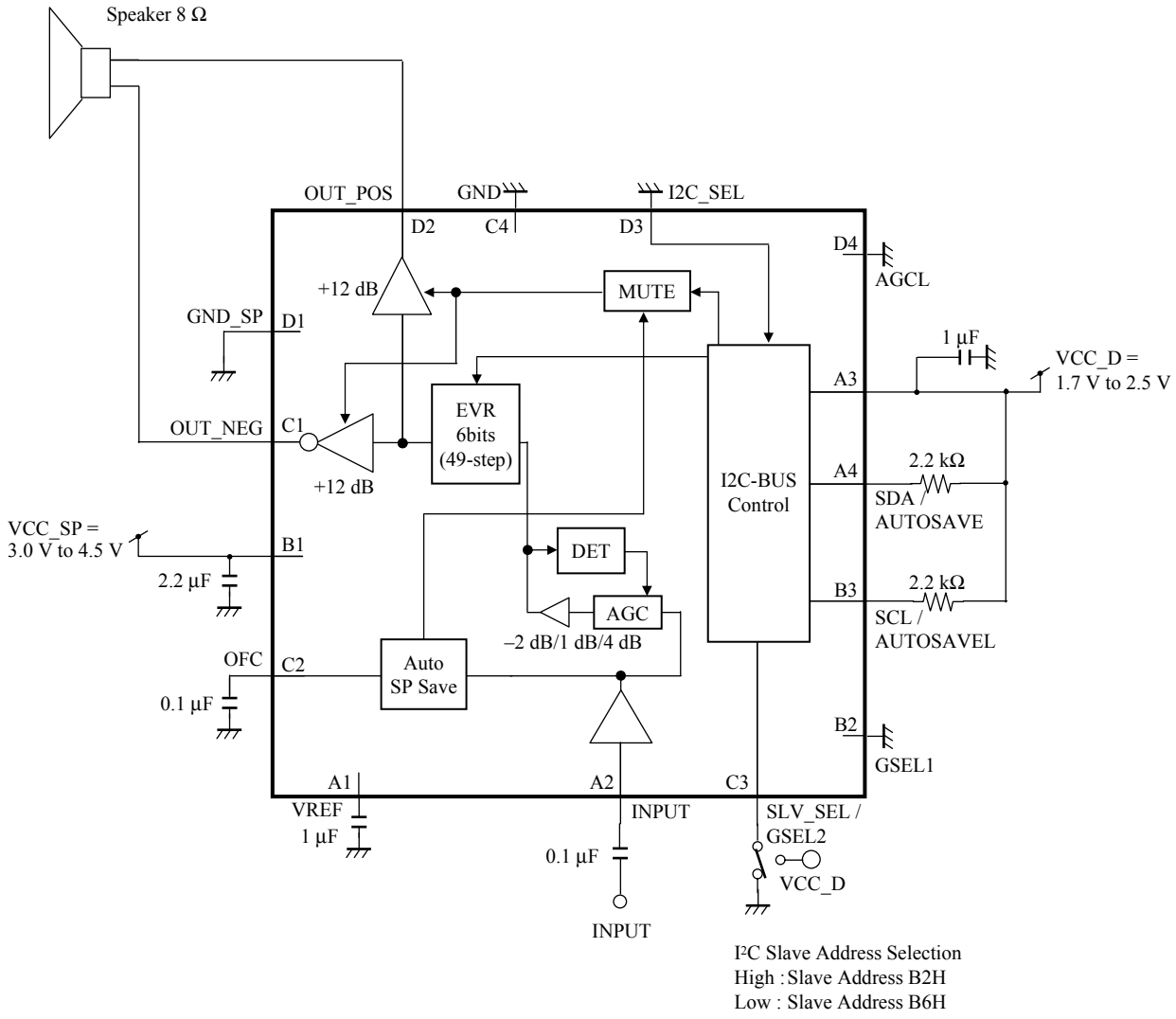
- 15 pin wafer level chip size package (WLCSP)
  Size : 1.96 × 1.96 mm (0.5 mm pitch)

■ Type

- Bi–CMOS IC

■ Application Circuit Example (Block Diagram)

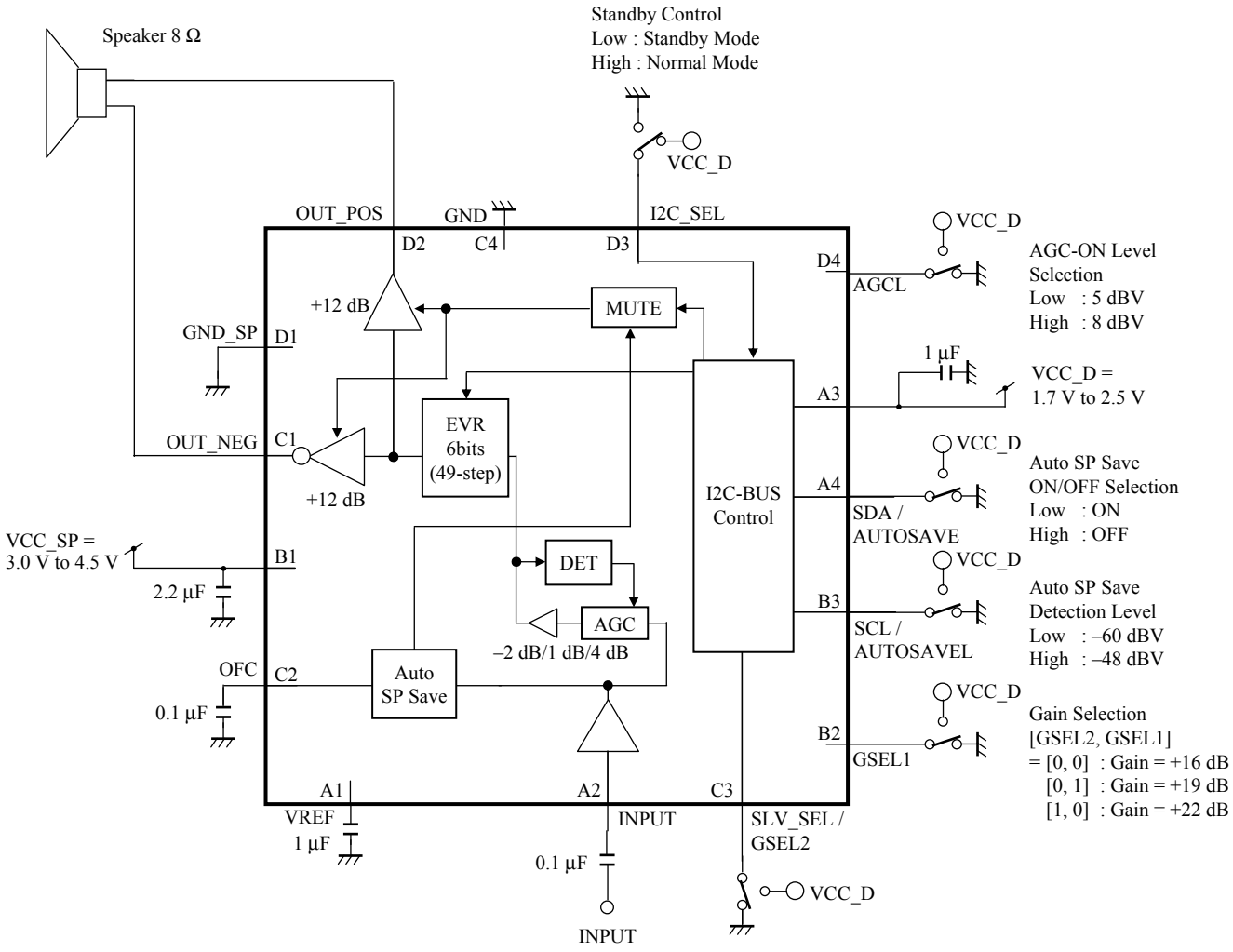
- I²C Control Mode



Notes)
- This application circuit is shown as an example but does not guarantee the design for mass production set.
- This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.
- The threshold voltages of Pin C3 and Pin D3 depend on VCC_D.
- Pin C3 and Pin D3 are floating condition at open, so please apply either High level or Low level voltage to them.

■ Application Circuit Example (Block Diagram) (continued)

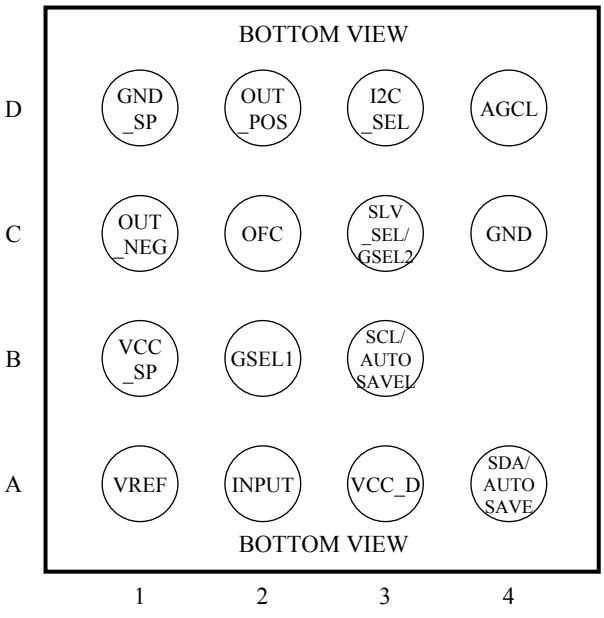
- Parallel Control Mode



Notes)
- This application circuit is shown as an example but does not guarantee the design for mass production set.
- This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.
- The threshold voltages of Pin C3, B2, B3, A4, D4, D3 depend on VCC_D.
- The pins C3, B2, B3, A4, D4, D3 are floating condition at open, so please apply either High level or Low level voltage to them.

■ Pin Descriptions

Pin No.	Pin name	Type	Description
A1	VREF	Output	Reference Voltage
A2	INPUT	Input	Signal Input
A3	VCC_D	Power Supply	Power Supply for Logic circuit
A4	SDA / AUTOSAVE	Input / Output	I^2C Control Mode: SDA of I^2C-bus Parallel Control Mode: Auto SP Save ON/OFF switch
B1	VCC_SP	Power Supply	Power supply for Speaker Amplifier
B2	GSEL1	Input	I^2C Control Mode: No Function (Connect to GND) Parallel Control Mode: Gain Selection 1
B3	SCL / AUTOSAVEL	Input	I^2C Control Mode: SCL of I^2C-bus Parallel Control Mode: Auto SP Save Non-signal Threshold Level Selection
C1	OUT_NEG	Output	Speaker Output (Negative Phase)
C2	OFC	Input / Output	Offset Cancel for Auto SP Save
C3	SLV_SEL / GSEL2	Input	I^2C Control Mode: I^2C Slave Address Selection Parallel Control Mode: Gain Selection 2
C4	GND	Ground	Ground
D1	GND_SP	Ground	Ground for Speaker Amplifier
D2	OUT_POS	Output	Speaker Output (Positive Phase)
D3	I2C_SEL	Input	I^2C Control Mode: No Function (Connect to GND) Parallel Control Mode: Standby Control
D4	AGCL	Input	I^2C Control Mode: No Function (Connect to GND) Parallel Control Mode: AGC-ON Level Selection



■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which are not destructed, and are not the values to which operation is guaranteed.

A No.	Parameter	Symbol	Range	Unit	Notes
1	Supply voltage	VCC_D	3.6	V	*1
		VCC_SP	5.5		
2	Supply current	I_{CC}	—	A	—
3	Power dissipation	P_D	80	mW	*2
4	Operating ambient temperature	T_{opr}	–30 to +85	°C	*3
5	Storage temperature	T_{stg}	–55 to +150	°C	

Notes) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : The power dissipation shown is the value at T_a = 85°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the P_D-T_a diagram in the ■ Technical Data standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3 :Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

■ Operating supply voltage range

Parameter	Symbol	Range	Unit	Note
Supply voltage range	VCC_D	1.7 to 2.5	V	*1
	VCC_SP	3.0 to 4.5		

Note) *1 :The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

■ Allowed Voltage Ranges

Notes)
- Allowable current and voltage ranges are limit ranges which are not destructed, and are not the ranges to which operation is guaranteed.
- Voltage values, unless otherwise specified, are with respect to GND.
  GND is voltage for GND and GND_SP. GND = GND_SP
- Do not apply external currents or voltages to any pin not specifically mentioned.

Pin No.	Pin name	Range	Unit	Notes
A1	VREF	– 0.3 to 2.9	V	
A2	INPUT	– 0.3 to 2.9	V	
A3	VCC_D	0 to 3.6	V	—
A4	SDA/AUTOSAVE	– 0.5 to (VCC_D + 0.5)	V	*1
B1	VCC_SP	0 to 5.5	V	—
B2	GSEL1	– 0.3 to (VCC_D + 0.3)	V	*1
B3	SCL/AUTOSAVEL	– 0.5 to (VCC_D + 0.5)	V	*1
C3	SLV_SEL/GSEL2	– 0.3 to (VCC_D + 0.3)	V	*1
D3	I2C_SEL	– 0.3 to (VCC_D + 0.3)	V	*1
D4	AGCL	– 0.3 to (VCC_D + 0.3)	V	*1

Note) *1 : (VCC_D + 0.5) V ≤ 3.6 V.

■ Electrical Characteristics at VCC_D = 1.8 V, VCC_SP = 3.8 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
Circuit Current								
1	Circuit current 1 at non-signal (VCC_SP)	IVCC2A	Non-signal, STB = OFF, SP = ON, AGC = ON	—	7	20	mA	—
2	Circuit current 2 at non-signal (VCC_D)	IVCC3A	Non-signal, STB = OFF, SP = ON, AGC = ON	—	1	10	µA	—
3	Circuit current 1 in standby mode (VCC_SP)	IVCC2B	Non-signal, STB = ON, SP = OFF, AGC = ON	—	0.1	1.0	µA	—
4	Circuit current 2 in standby mode (VCC_D)	IVCC3B	Non-signal, STB = ON, SP = OFF, AGC = ON	—	0.1	1.0	µA	—
5	Circuit current 1 in speaker save mode (VCC_SP)	IVCC2C	Non-signal, STB = OFF, SP = OFF, AGC = ON	—	3.5	5.5	mA	—
6	Circuit current 2 in speaker save mode (VCC_D)	IVCC3C	Non-signal, STB = OFF, SP = OFF, AGC = ON	—	0.1	10	µA	—
Input-Output Characteristics								
7	SP reference output level	VSPO	Vin = –19.0 dBV , f = 1 kHz RL = 8 Ω, GAIN = +19 dB	–1.5	0.0	1.5	dBV	—
8	SP reference output distortion	THSPO	Vin = –19.0 dBV, f = 1 kHz RL = 8 Ω, GAIN = +19 dB to THD5th	—	0.05	0.5	%	—
9	SP output noise voltage	VNSPO	Non-Signal, using A curve filter GAIN = +19 dB	—	–79	–72	dBV	—
10	SP maximum rating output	VMSPO	THD = 10% , f = 1 kHz RL = 8 Ω, AGC = OFF	500	900	—	mW	—
11	SP Output level at power save	VSSPO	Vin = –19.0 dBV, f = 1 kHz RL = 8 Ω, GAIN = +19 dB using A curve filter	—	–110	–90	dBV	—

■ Electrical Characteristics (continued) at VCC_D = 1.8 V, VCC_SP = 3.8 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
I²C bus (Internal I/O stage characteristics)								
12	SCL, SDA signal input Low level	V_{IL}	—	– 0.5	—	0.3 × VCC_D	V	*1
13	SCL, SDA signal input High level	V_{IH}	—	0.7 × VCC_D	—	VCC_D_{max} + 0.5	V	*1
14	SDA output signal Low level	V_{OL}	Open drain, sink current : 3 mA	0	—	0.2 × VCC_D	V	—
15	SCL, SDA signal input current	I_i	入力電圧 : 0.1VCC_D_{max} to 0.9VCC_D_{max} input voltage : 0.1VCC_D_{max} to 0.9VCC_D_{max}	–10	—	10	μA	—
16	SCL maximum frequency of signal input	f_{SCL}	—	0	—	400	kHz	—

■ Electrical Characteristics (Reference value for design) at VCC_D = 1.8 V, VCC_SP = 3.8 V

Note) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Reference values			Unit	Notes
				Min	Typ	Max		
AGC Characteristics								
17	SP AGC output level	VSPOA	Vin = –7.0 dBV, f = 1 kHz RL = 8 Ω, GAIN = +19 dB AGC-Level = 5 dBV	4.0	5.0	6.0	dBV	—
Control Pin Input Level								
18	SLV_SEL input Low level	Vslvl	—	—	—	0.1 × VCC_D	V	—
19	SLV_SEL input High level	Vslvh	—	0.9 × VCC_D	—	—	V	—
20	I2C_SEL input Low level	VI2Cl	—	—	—	0.1 × VCC_D	V	—
21	I2CSEL input High level	VI2Ch	—	0.9 × VCC_D	—	—	V	—
22	GSEL1 input Low level	Vgs1l	I2C_SEL = High	—	—	0.1 × VCC_D	V	—
23	GSEL1 input High level	Vgs1h	I2C_SEL = High	0.9 × VCC_D	—	—	V	—
24	GSEL2 input Low level	Vgs2l	I2C_SEL = High	—	—	0.1 × VCC_D	V	—
25	GSEL2 input High level	Vgs2h	I2C_SEL = High	0.9 × VCC_D	—	—	V	—
26	AUTOSAVE input Low level	Vasl	I2C_SEL = High	—	—	0.1 × VCC_D	V	—
27	AUTOSAVE input High level	Vash	I2C_SEL = High	0.9 × VCC_D	—	—	V	—
28	AUTOSAVEL input Low level	Vasll	I2C_SEL = High	—	—	0.1 × VCC_D	V	—
29	AUTOSAVEL input High level	Vaslh	I2C_SEL = High	0.9 × VCC_D	—	—	V	—
30	AGCL input Low level	Vagcll	I2C_SEL = High	—	—	0.1 × VCC_D	V	—
31	AGCL input High level	Vagclh	I2C_SEL = High	0.9 × VCC_D	—	—	V	—

■ Electrical Characteristics (Reference value for design) (continued) at VCC_D = 1.8 V, VCC_SP = 3.8 V

Note) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
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B No.	Parameter	Symbol	Conditions	Reference values			Unit	Notes
				Min	Typ	Max		
I²C bus (Bus line specifications)								
32	Bus free time between a condition of stop and a condition of start	t_{BUF}	—	1.3	—	—	µs	*2
33	Setup time of a condition of start	$t_{SU;STA}$	—	0.6	—	—	µs	*2
34	Hold time of a condition of start	$t_{HD;STA}$	The first clock pulse is generated after $t_{HD;STA.}$	0.6	—	—	µs	*2
35	Low period of SCL clock	t_{Low}	—	1.3	—	—	µs	*2
36	High period of SCL clock	t_{High}	—	0.6	—	—	µs	*2
37	Rising time of SDA, SCL signal	t_R	—	$20 + 0.1 \times C_b$	—	0.3	µs	*2
38	Fall time of SDA, SCL signal	t_F	—	$20 + 0.1 \times C_b$	—	0.3	µs	*2
39	Data setup time	$t_{SU;DAT}$	—	0.1	—	—	µs	*2
40	Data hold time	$t_{HD;DAT}$	—	0	—	0.9	µs	*2
41	Setup time of a condition of stop	$t_{SU;STO}$	—	0.6	—	—	µs	*2

■ Electrical Characteristics (Reference value for design)(continued) at VCC_D = 1.8 V, VCC_SP = 3.8 V

Note) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
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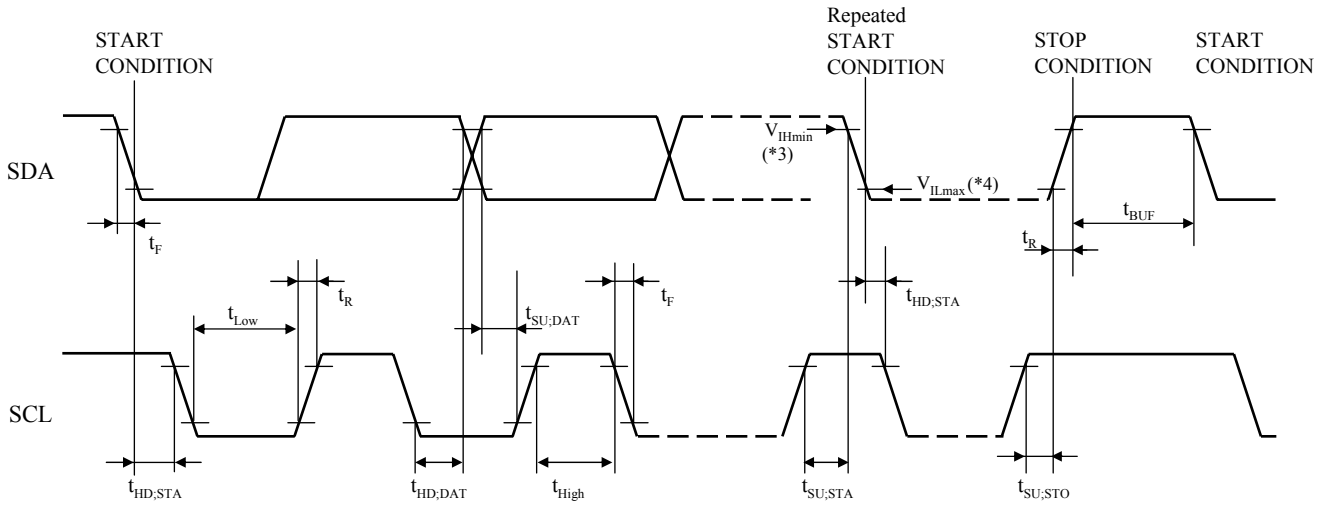
B No.	Parameter	Symbol	Conditions	Reference values			Unit	Notes
				Min	Typ	Max		
I²C bus (Internal I/O stage characteristics)								
42	Hysteresis of Schmitt trigger input	V_{hys}	Hysteresis of SDA, SCL	0.05 × VCC_D	—	—	V	*2
43	Fall time from V_{IHmax} to V_{ILmin}	t_{of}	Bus capacitance : 10 pF to 400pF $I_P \leq 6$ mA (V_{OLmax} = 0.6 V) I_P : Max. sink current	20 + 0.1 × Cb	—	250	ns	*2
44	Pulse width of spike which must be suppressed by the input filter	t_{sp}	—	0	—	50	ns	*2
45	Capacitance for each I/O pin	Ci	—	—	—	10	pF	*2
I²C bus (Bus line specifications) (continued)								
46	Capacitive load for each bus line	Cb	—	—	—	400	pF	*2
47	Noise margin at the Low-level for each connected device (including hysteresis)	V_{aL}	—	0.1 × VCC_D	—	—	V	*2
48	Noise margin at the High-level for each connected device (including hysteresis)	V_{aH}	—	0.2 × VCC_D	—	—	V	*2

■ Electrical Characteristics (Reference value for design)(continued) at VCC_D = 1.8 V, VCC_SP = 3.8 V

Note) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.



Notes) *1 : The input threshold voltage of I²C bus (Vth) is linked to VCC_D (I²C bus I/O stage supply voltage).
In case the pull-up voltage is not VCC_D, the threshold voltage (Vth) is fixed to ((VCC_D / 2) ± (Schmitt width) / 2) and High-level, Low-level of input voltage are not specified.
In this case, pay attention to Low-level (max.) value (V_{ILmax}).
It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (VCC_D).
*2 : All values are V_{IHmin} (*3) and V_{ILmax} (*4) level reference.
*3 : V_{IHmin} is the minimum limit of the signal input high level (it indicates to Page_No.10).
*4 : V_{ILmax} is the maximum limit of the signal input low level (it indicates to Page_No.10).

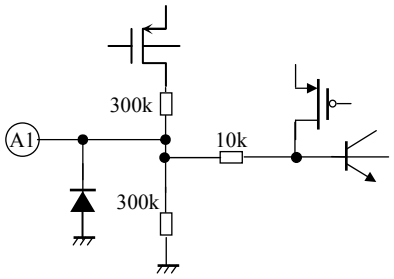
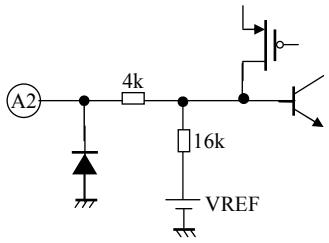
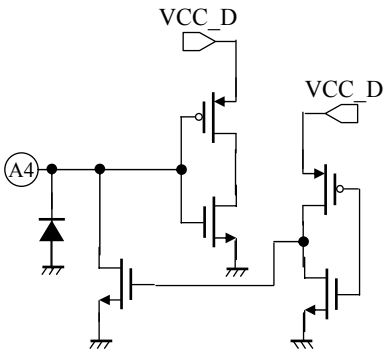
■ Electrical Characteristics Test Procedures

C No.	Parameter	I²C-bus data setting					Notes
		Sub-address					
		00H	01H	02H	03H	04H	
Circuit current							
1	Circuit current 1 at non-signal (VCC_SP)	2EH	92H	00H	00H	00H	—
2	Circuit current 2 at non-signal (VCC_D)	2EH	92H	00H	00H	00H	—
3	Circuit current 1 in standby mode (VCC_SP)	28H	92H	00H	00H	00H	—
4	Circuit current 2 in standby mode (VCC_D)	28H	92H	00H	00H	00H	—
5	Circuit current 1 in speaker save mode (VCC_SP)	2AH	92H	00H	00H	00H	—
6	Circuit current 2 in speaker save mode (VCC_D)	2AH	92H	00H	00H	00H	—
Input-Output characteristic							
7	SP reference output level	2EH	92H	00H	00H	00H	—
8	SP reference output distortion	2EH	92H	00H	00H	00H	—
9	SP output noise voltage	2EH	92H	00H	00H	00H	—
10	SP maximum rating output	26H	92H	00H	00H	00H	—
11	SP output level at power save	2AH	92H	00H	00H	00H	—
I²C bus (Internal I/O stage characteristics)							
12	SCL, SDA signal low-level input	—	—	—	—	—	—
13	SCL, SDA signal high-level input	—	—	—	—	—	—
14	SDA signal low-level output	—	—	—	—	—	—
15	SCL, SDA signal input current	—	—	—	—	—	—
16	SCL signal allowable input max. frequency	—	—	—	—	—	—
AGC Characteristics							
17	SP AGC output level	2EH	92H	00H	00H	00H	—

■ Technical Data (continued)

• I/O block circuit diagram and pin function descriptions

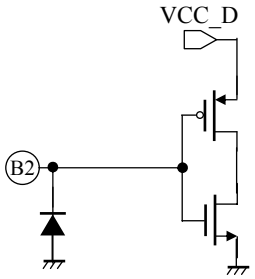
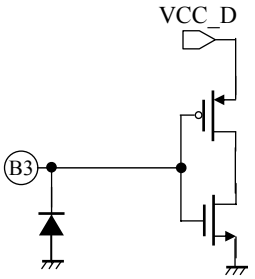
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
A1	VREF DC 1.35 V		Input impedance = About 150 kΩ	Reference Voltage The reference voltage terminal for determining DC bias of input stage. Please connect an external capacitor to remove a ripple.
A2	INPUT DC 1.35 V		Input impedance = About 20 kΩ	Signal Input Please insert the capacitor of 0.1 µF in series.
A3	VCC_D 1.8 V (typ.)	—	—	Power Supply for Logic Circuit
A4	SDA/ AUTOSAVE Hi-Z		Input impedance = Hi-Z	I^2C Control Mode: I^2C-Bus SDA Parallel Control Mode: Auto SP Save ON/OFF Switch Please don't make this pin open.

■ Technical Data (continued)

• I/O block circuit diagram and pin function descriptions

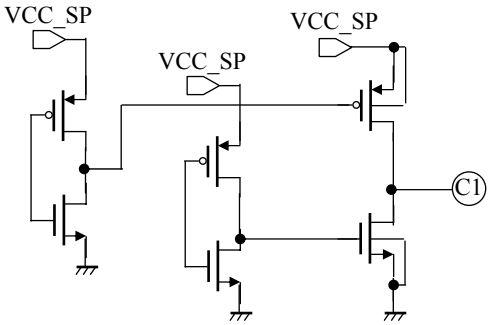
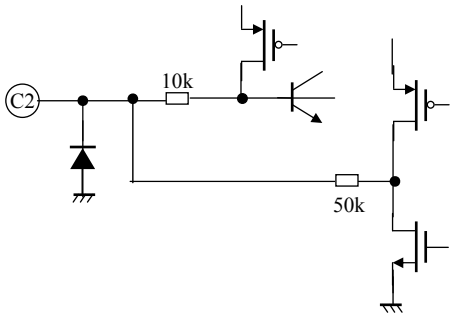
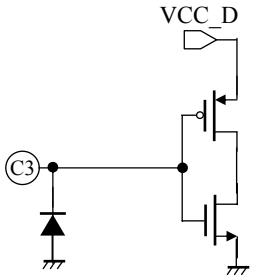
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
B1	VCC_SP 3.8 V (typ.)	—	—	Power Supply for Speaker Amplifier
B2	GSEL1 0 V or 1.8 V (typ.) 0 V or 2.5 V (max.)		Input impedance = Hi-Z	Gain Selection 1 Please don't make this pin open.
B3	SCL / AUTOSAVEL Hi-Z		Input impedance = Hi-Z	I^2C Control Mode: I^2C-Bus SCL Parallel Control Mode: Auto SP Save Non-signal Threshold Level Selection Please don't make this pin open.

■ Technical Data (continued)

- I/O block circuit diagram and pin function descriptions

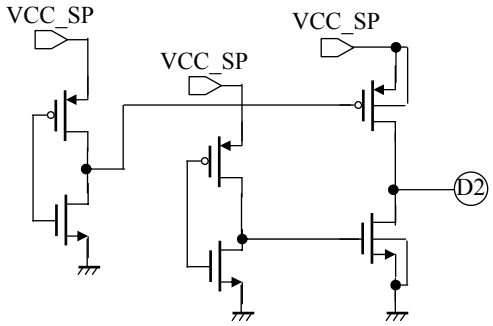
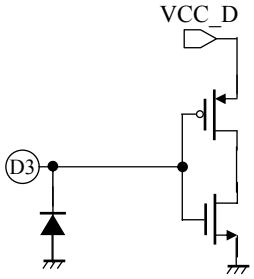
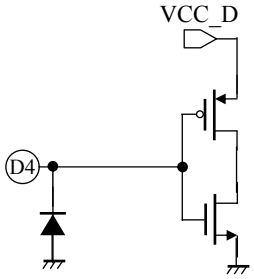
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
C1	OUT_NEG 0 V to 3.8 V (typ.)		Output impedance = Equal to or less than 1 Ω	Speaker Output (Negative Phase)
C2	DET_OFC DC 1.35 V		Input impedance = About 50 kΩ	Offset cancel terminal for Auto SP Save function
C3	SLV_SEL / GSEL2 0 V or 1.8 V (typ.) 0 V or 2.5 V (max.)		Input impedance = Hi-Z	I^2C Control Mode: I^2C Slave Address Selection High level: B2H Low level: B6H Parallel Control Mode: Gain Selection 2 Please don't make this pin open.
C4	GND DC 0 V	—	—	Ground

■ Technical Data (continued)

• I/O block circuit diagram and pin function descriptions

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

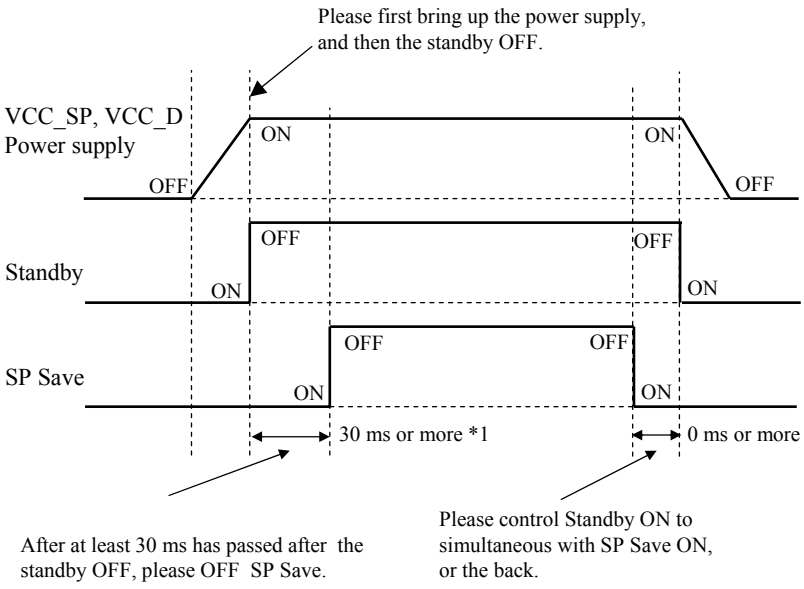
Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
D1	GND_SP	—	—	Ground for Speaker Amplifier
D2	OUT_POS 0 V to 3.8 V (typ.)		Output impedance = Equal to or less than 1 Ω	Speaker Output (Positive Phase)
D3	I2C_SEL 0 V or 1.8 V (typ.) 0 V or 2.5 V (max.)		Input impedance = Hi-Z	I^2C Control Mode: No Function (Connect to GND) Parallel Control Mode: Standby Control Please don't make this pin open.
D4	AGCL 0 V or 1.8 V (typ.) 0 V or 2.5 V (max.)		Input impedance = Hi-Z	AGC-ON Level Selection Low level: 5 dBV High level: 8 dBV Please don't make this pin open.

■ Technical Data (continued)

- The power supply and logic sequence

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.
The timing control of power-ON/OFF and each logic according to the procedure below should be recommended for the best pop performance caused in switching.

1) The sequence of power supply and logic in I²C control mode



The basic procedure at the power-on

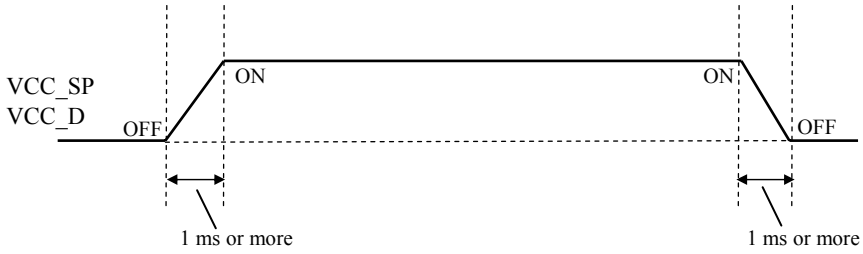
1. The power OFF condition
   Both the standby and the SP Save are ON.
2. Power ON
3. Standby OFF
4. SP Save OFF

The basic procedure at the power-off

1. The power ON condition
   Both the standby and the SP Save are OFF.
2. SP Save ON (= Standby ON)
3. Standby ON
4. Power OFF

2) The sequence of VCC_SP and VCC_D

This IC have not a standup and falling order in VCC_SP and VCC_D. The standup and falling time of VCC_SP and VCC_D recommend 1 ms or more.



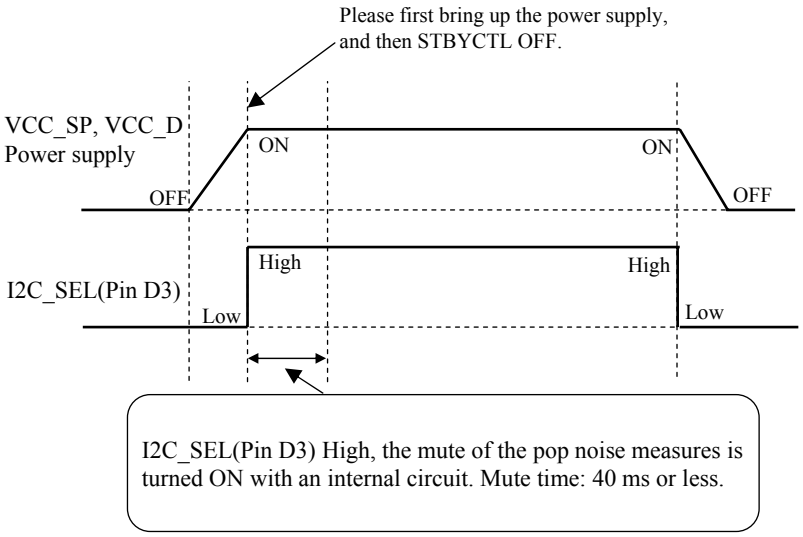
Note) *1 : This IC contains the pre-charge circuit, It is time until each bias is stabilized from Standby OFF.
It depends for this time on the capacity value linked to a standard voltage terminal (VREF), and the capacity value and resistance linked to an input terminal (IN).
It is a recommendation value in a constant given in the example of an application circuit (block diagram).

■Technical Data (continued)

- The power supply and logic sequence (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.
The timing control of power-ON/OFF and each logic according to the procedure below should be recommended for the best pop performance caused in switching.

3) The sequence of power supply and I2C_SEL pin(Pin D3) in parallel control mode



The basic procedure at the power-on

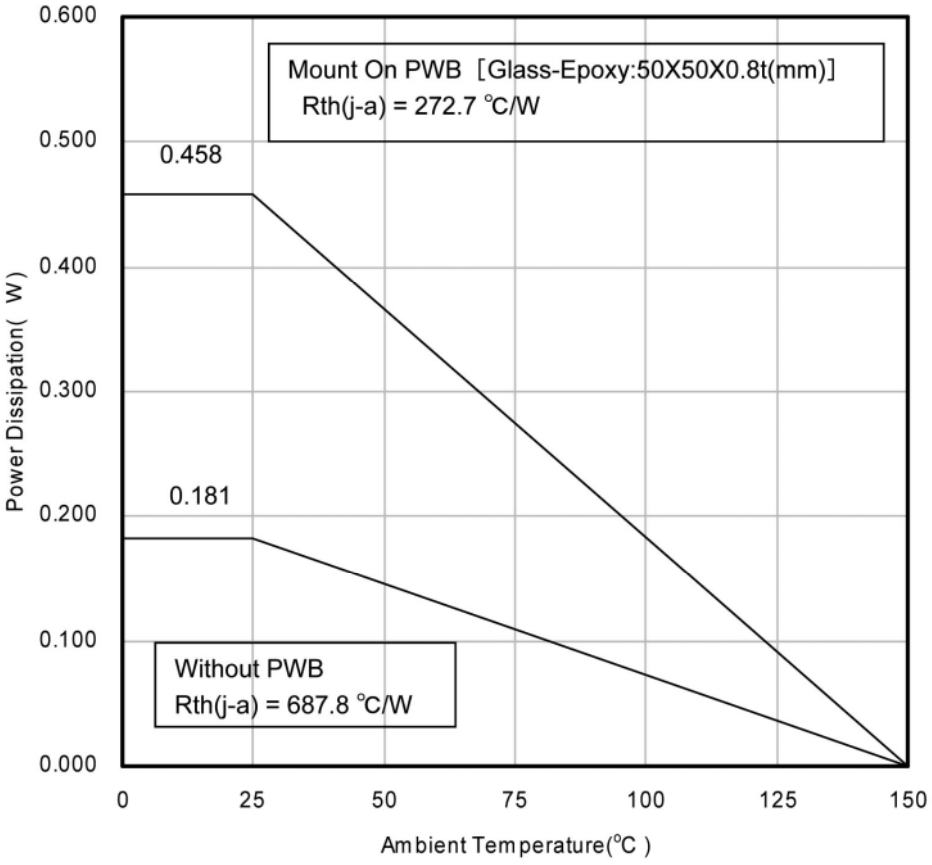
1. The power OFF condition
   STBYCTL is ON.
2. Power ON
3. I2C_SEL(Pin D3): High

The basic procedure at the power-off

1. The power ON condition
   STBYCTL is OFF .
2. I2C_SEL(Pin D3) : Low
3. Power OFF

■ Technical Data (continued)

• P_D — T_a diagram



■ Usage Notes

• Special attention and precaution in using

1. This IC is intended to be used for general electronic equipment [cellular phones].
   Consult our sales staff in advance for information on the following applications:
   ・Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   ・Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required

2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-V_{CC} short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .
   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

6. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

7. When using the LSI for new models, verify the safety including the long-term reliability for each product.

8. When the application system is designed by using this LSI, be sure to confirm notes in this book.
   Be sure to read the notes to descriptions and the usage notes in the book.

9. Please carry out the thermal design with sufficient margin such that the power dissipation will not be exceeded, based on the conditions of power supply, load and surrounding temperature. Although indicated also in the column of the maximum rating, the maximum rating becomes an instant and the marginal value which must not exceed. It sufficiently evaluates, and I use-wish-do so that it may not exceed certainly. Moreover, don't impress neither voltage nor current to PIN which is not indicated. It may destroy in both cases.

10. If SDA/AUTOSAVE (Pin A4), GSEL1(Pin B2), SCL/AUTOSAVEL (Pin B3), SLV_SEL/GSEL2(Pin C3), I2C_SEL(Pin D3), I2C_SEL(Pin D3) and AGCL (Pin D4) are open, their inputs are arbitrary. Don't make them open.

■ Usage Notes (continued)

• Special attention and precaution in using (continued)

11. Due to unshielded structure of this IC, under exposure of light, function and characteristic of the product cannot be guaranteed. During normal operation or even under testing condition, please ensure that IC is not exposed to light.

12. Basically, chip surface is ground potential. Please design to ensure no contact between chip surface and metal shielding.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this book for any special application, unless our company agrees to your using the products in this book for any special application.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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