National Semiconductor

# LH0036 Instrumentation Amplifier

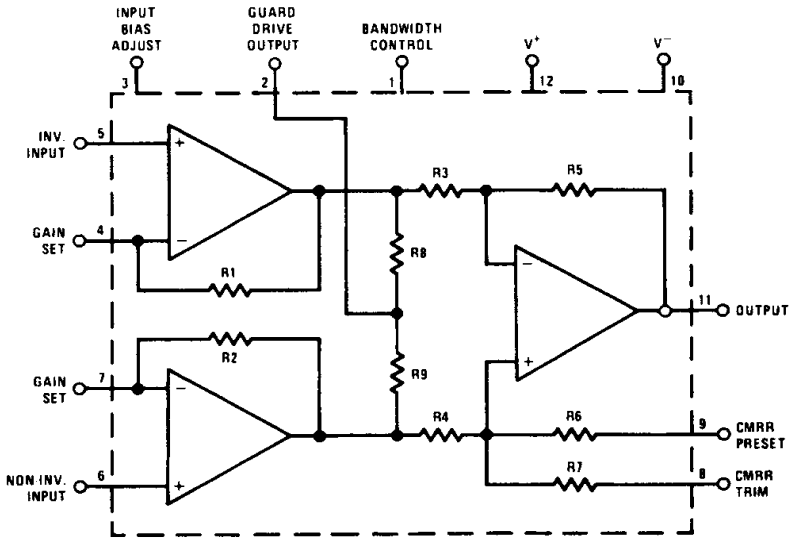
## General Description

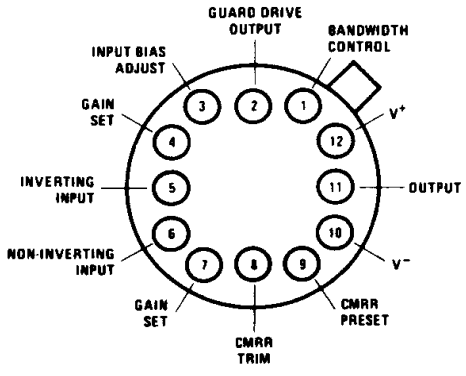
The LH0036C is a micro power instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable from 1 to 1000 with a single external resistor. Power supply operating range is between ±1V and ±18V. Input bias current and output bandwidth are both externally adjustable or can be set by internally set values. The LH0036C is specified for operation over the −25°C to +85°C temperature range.

## Features

| | |
|---|---|
| ■ High input impedance | 300 MΩ |
| ■ High CMRR | 100 dB |
| ■ Single resistor gain adjust | 1 to 1000 |
| ■ Low power | 90 μW |
| ■ Wide supply range | ±1V to ±18V |
| ■ Adjustable input bias current | |
| ■ Adjustable output bandwidth | |
| ■ Guard drive output | |

## Equivalent Circuit and Connection Diagrams




TOP VIEW

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**Order Number LH0036CG**
**See NS Package Number G12B**

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## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)**

| | |
|---|---|
| Supply Voltage | ±18V |
| Differential Input Voltage | ±30V |
| Input Voltage Range | $\pm V_S$ |
| Shield Drive Voltage | $\pm V_S$ |
| CMRR Preset Voltage | $\pm V_S$ |
| CMMR Trim Voltage | $\pm V_S$ |
| Power Dissipation (Note 3) | 1.5W |
| Short Circuit Duration | Continuous |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

## Operating Temperature Range

LH0036C −25°C to +85°C

ESD rating to be determined.

## Electrical Characteristics (Notes 1 and 2)

| Parameter | Conditions | Limits LH0036C Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage ($V_{IOS}$) | $R_S$ = 1.0 kΩ, $T_A$ = 25°C | | 1.0 | 2.0 | mV |
| | $R_S$ = 1.0 kΩ | | | 3.0 | mV |
| Output Offset Voltage ($V_{OOS}$) | $R_S$ = 1.0 kΩ, $T_A$ = 25°C | | 5.0 | 10 | mV |
| | $R_S$ = 1.0 kΩ | | | 12 | mV |
| Input Offset Voltage Tempco ($\Delta V_{IOS}/\Delta T$) | $R_S \leq$ 1.0 kΩ | | 10 | | µV/°C |
| Output Offset Voltage Tempco ($\Delta V_{OOS}/\Delta T$) | | | 15 | | µV/°C |
| Overall Offset Referred to Input ($V_{OS}$) | $A_V$ = 1.0 | | 6.0 | | mV |
| | $A_V$ = 10<br>$A_V$ = 100<br>$A_V$ = 1000 | | 1.5<br>1.05<br>1.005 | | mV<br>mV<br>mV |
| Input Bias Current ($I_B$) | $T_A$ = 25°C | | 50 | 125 | nA |
| | | | | 200 | nA |
| Input Offset Current ($I_{OS}$) | $T_A$ = 25°C | | 20 | 50 | nA |
| | | | | 100 | nA |
| Input Voltage Range | Differential | ±10 | ±12 | | V |
| | Common Mode | ±10 | ±12 | | V |
| Gain Nonlinearity | | | 0.03 | | % |
| Deviation From Gain Equation Formula | $A_V$ = 1 to 1000 (Note 4) | | ±1.0 | ±3.0 | % |

## Electrical Characteristics (Notes 1 and 2) (Continued)

| Parameter | Conditions | Limits | | | Units |
|---|---|---|---|---|---|
| | | LH0036C | | | |
| | | Min | Typ | Max | |
| PSRR | $\pm 5.0V \le V_S \le \pm 15V$, $A_V = 1.0$<br>$\pm 5.0V \le V_S \le \pm 15V$, $A_V = 100$ | | 1.0<br>0.10 | 5.0<br>0.50 | mV/V<br>mV/V |
| CMRR | $A_V = 1.0$ DC to<br>$A_V = 10$ 100 Hz<br>$A_V = 100$ $\Delta R_S = 1.0k$ | | 2.5<br>0.25<br>50 | 5.0<br>0.50<br>100 | mV/V<br>mV/V<br>$\mu$V/V |
| Output Voltage | $V_S = \pm 15V$, $R_L = 10\ k\Omega$<br>$V_S = \pm 1.5V$, $R_L = 100\ k\Omega$ | $\pm 10$<br>$\pm 0.6$ | $\pm 13.5$<br>$\pm 0.8$ | | V<br>V |
| Output Resistance | | | 0.5 | | $\Omega$ |
| Supply Current | | | 400 | 600 | $\mu$A |
| Small Signal Bandwidth | $A_V = 1.0$, $R_L = 10\ k\Omega$<br>$A_V = 10$, $R_L = 10\ k\Omega$<br>$A_V = 100$, $R_L = 10\ k\Omega$<br>$A_V = 1000$, $R_L = 10\ k\Omega$ | | 350<br>35<br>3.5<br>350 | | kHz<br>kHz<br>kHz<br>Hz |
| Full Power Bandwidth | $V_{IN} = \pm 10V$, $R_L = 10k$, $A_V = 1$ | | 5.0 | | kHz |
| Equivalent Input Noise Voltage | 0.1 Hz < f < 10 kHz,<br>$R_S < 50\Omega$ | | 20 | | $\mu$V/p-p |
| Slew Rate | $\Delta V_{IN} = \pm 10V$,<br>$R_L = 10\ k\Omega$, $A_V = 1.0$ | | 0.3 | | V/$\mu$S |
| Settling Time | To $\pm 10$ mV, $R_L = 10\ k\Omega$,<br>$\Delta V_{OUT} = 1.0V$<br>$A_V = 1.0$<br>$A_V = 100$ | | <br><br>3.8<br>180 | | <br><br>$\mu$S<br>$\mu$S |

**Note 1:** Unless otherwise specified, all specifications apply for $V_S = \pm 15V$, Pins 1, 3, and 9 grounded, $-25°C$ to $+85°C$.

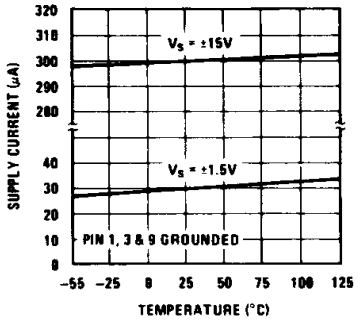
**Note 2:** All typical values are for $T_A = 25°C$.

**Note 3:** The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 90°C/W.

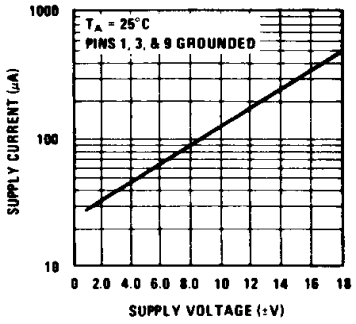
**Note 4:** $A_V = 1000$ guaranteed by design and testing at $A_V = 100$.

## Typical Performance Characteristics

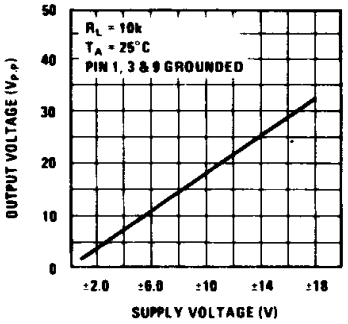
**Supply Current vs Temperature**



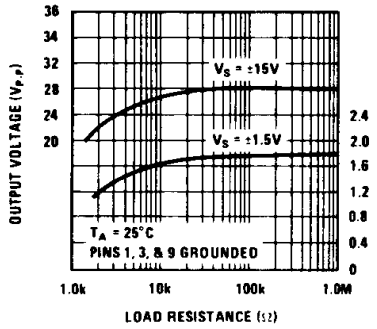

**Supply Current vs Supply Voltage**



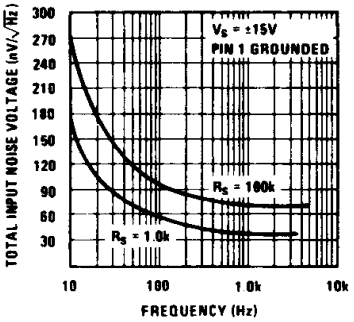

**Output Voltage Swing vs Supply Voltage**



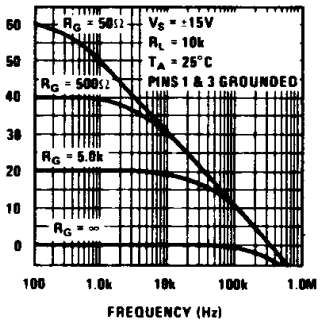

**Peak to Peak Output Voltage Swing vs $R_L$**




**Total Input Noise Voltage* vs Frequency**

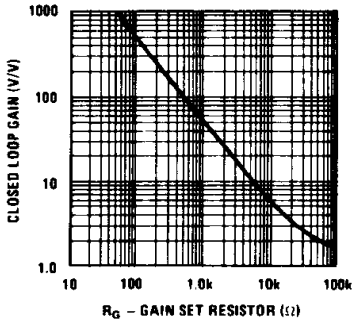



**Closed Loop Voltage Gain vs Frequency**

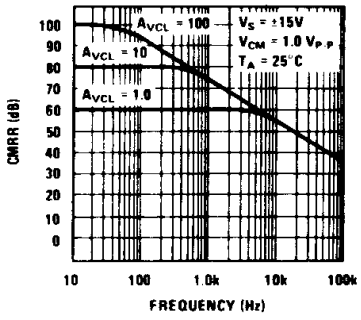



*Noise voltage includes contribution from source resistance

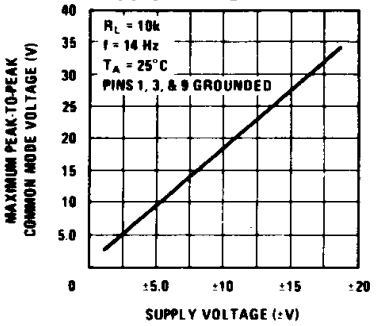
**Closed Loop Voltage Gain**



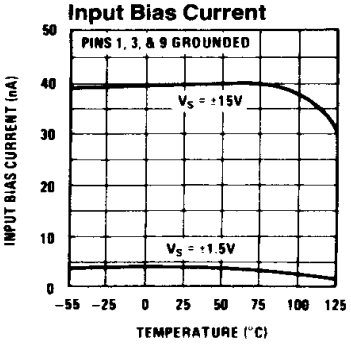

**CMRR vs Frequency**



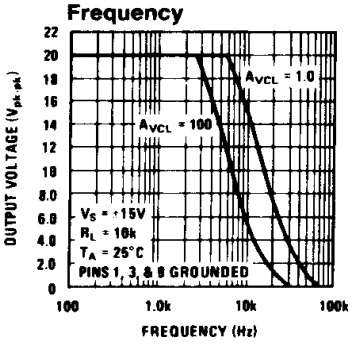

**Common Mode Voltage vs Supply Voltage**



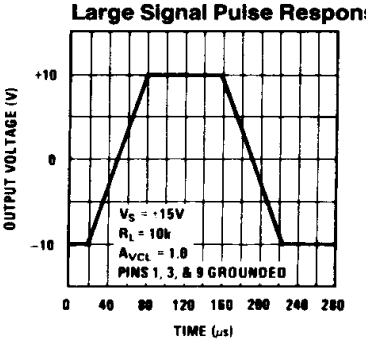

**Input Bias Current**




**Output Voltage Swing vs Frequency**




**Large Signal Pulse Response**

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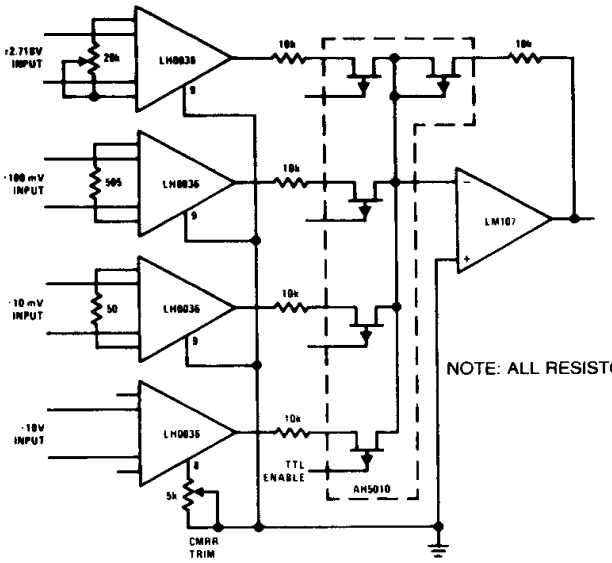
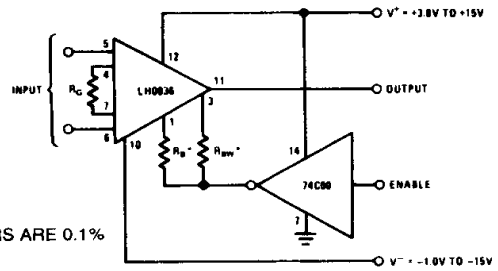
# Typical Applications

### Pre MUX Signal Conditioning

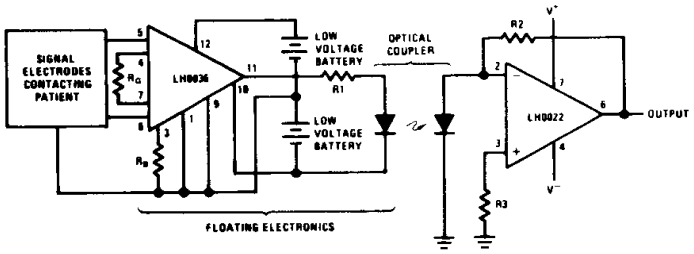



### Instrumentation Amplifier with Logic Controlled Shut-Down

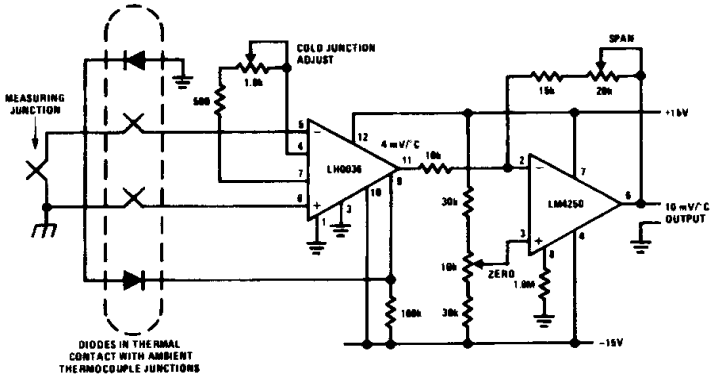



*$R_{BW}$ AND $R_B$ ARE OPTIONAL BANDWIDTH AND INPUT BIAS CURRENT CONTROLLING RESISTORS.

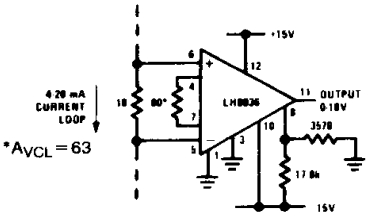
### Isolation Amplifier for Medical Telemetry



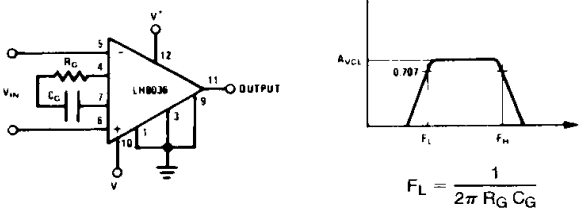

### Thermocouple Amplifier with Cold Junction Compensation




### Process Control Interface




### High Pass Filter




$$F_L = \frac{1}{2\pi R_G C_G}$$

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$F_H$ = A FUNCTION OF SELECTED $A_{VCL}$, $R_S$ AND $R_{SW}$

# Applications Information

## THEORY OF OPERATION

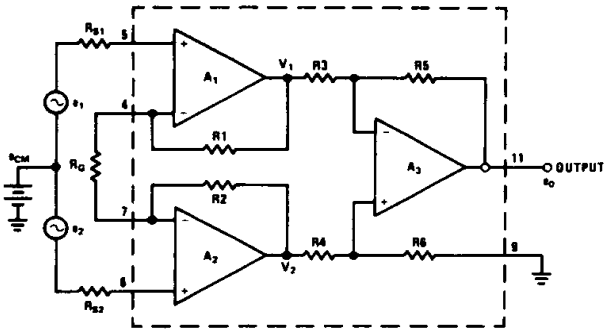


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**FIGURE 1. Simplified LH0036**

The LH0036 is a 2 stage amplifier with a high input impedance gain stage comprised of $A_1$ and $A_2$ and a differential to single-ended unity gain stage, $A_3$. Operational amplifier, $A_1$, receives differential input signal, $e_1$, and amplifies it by a factor equal to $(R1 + R_G)/R_G$.

$A_1$ also receives input $e_2$ via $A_2$ and R2. $e_2$ is seen as an inverting signal with a gain of $R1/R_G$. $A_1$ also receives the common mode signal $e_{CM}$ and processes it with a gain of $+1$.

Hence:

$$V_1 = \frac{R1+R_G}{R_G} e_1 - \frac{R1}{R_G} e_2 + e_{CM} \quad (1)$$

By similar analysis $V_2$ is seen to be:

$$V_2 = \frac{R2 + R_G}{R_G} e_2 - \frac{R2}{R_G} e_1 + e_{CM} \quad (2)$$

For $R1 = R2$:

$$V_2 - V_1 = \left[\left(\frac{2R1}{R_G}\right) + 1\right](e_2 - e_1) \quad (3)$$

Also, for $R3 = R5 = R4 = R6$, the gain of $A_3 = 1$, and:

$$e_0 = (1)(V_2 - V_1) = (e_2 - e_1)\left[1 + \left(\frac{2R1}{R_G}\right)\right] \quad (4)$$

As can be seen for identically matched resistors, $e_{CM}$ is cancelled out, and the differential gain is dictated by equation (4).

For the LH0036, equation (4) reduces to:

$$A_{VCL} = \frac{e_0}{e_2 - e_1} = 1 + \frac{50k}{R_G} \quad (5a)$$

The closed loop gain may be set to any value from 1 ($R_G = \infty$) to 1000 ($R_G \cong 50\Omega$). Equation (5a) re-arranged in more convenient form may be used to select $R_G$ for a desired gain:

$$R_G = \frac{50k}{A_{VCL} - 1} \quad (5b)$$

## USE OF BANDWIDTH CONTROL (pin 1)

In the standard configuration, pin 1 of the LH0036 is simply grounded. The amplifier's slew rate in this configuration is typically 0.3V/μS and small signal bandwidth 350 kHz for $A_{VCL} = 1$. In some applications, particularly at low frequency, it may be desirable to limit bandwidth in order to minimize the overall noise bandwidth of the device. A resistor $R_{BW}$ may be placed between pin 1 and ground to accomplish this purpose. *Figure 2* shows typical small signal bandwidth versus $R_{BW}$.

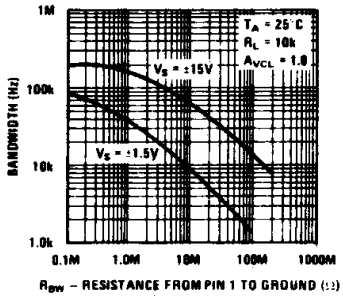


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**FIGURE 2. Bandwidth vs $R_{BW}$**

It also should be noted that large signal bandwidth and slew rate may be adjusted down by use of $R_{BW}$. *Figure 3* is plot of slew rate versus $R_{BW}$.

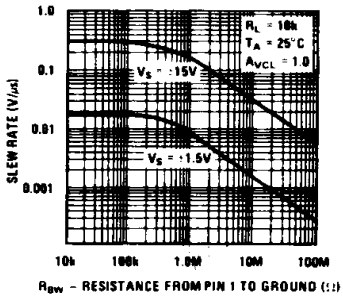


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**FIGURE 3. Output Slew Rate vs $R_{BW}$**

## CMRR CONSIDERATIONS

### Use of Pin 9, CMRR Preset

Pin 9 should be grounded for nominal operation. An internal factory trimmed resistor, R6, will yield a CMRR in excess of 80 dB (for $A_{VCL} = 100$). Should a higher CMRR be desired, pin 9 should be left open and the procedure, in this section followed.

### DC Off-set Voltage and Common Mode Rejection Adjustments

Off-set may be nulled using the circuit shown in *Figure 4*.

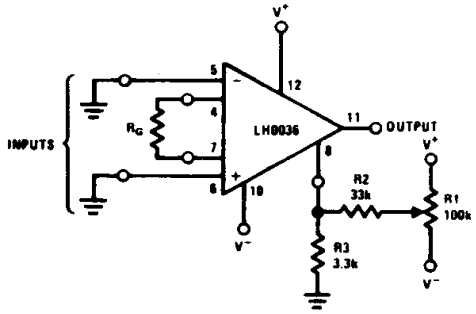


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**FIGURE 4. $V_{OS}$ Adjustment Circuit**

## Applications Information (Continued)

Pin 8 is also used to improve the common mode rejection ratio as shown in *Figure 5*. Null is achieved by alternately applying ±10V (for $V^+$ & $V^-$ = 15V) to the inputs and adjusting R1 for minimum change at the output.

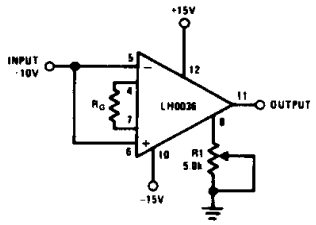


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**FIGURE 5. CMRR Adjustment Circuit**

The circuits of *Figure 4* and *5* may be combined as shown in *Figure 6* to accomplish both $V_{OS}$ and CMRR null. However, the $V_{OS}$ and CMRR adjustment are interactive and several iterations are required. The procedure for null should start with the inputs grounded.

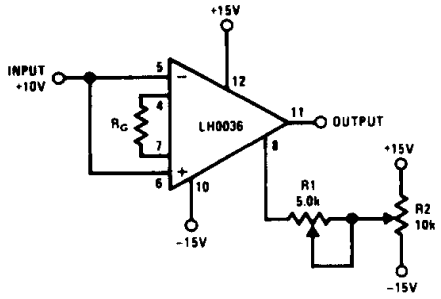


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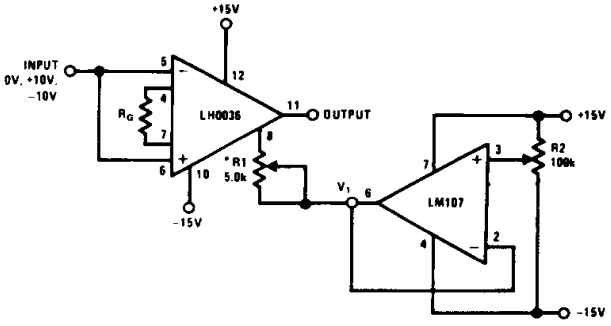
**FIGURE 6. Combined CMRR, $V_{OS}$ Adjustment Circuit**

R2 is adjusted for $V_{OS}$ null. An input of +10V is then applied and R1 is adjusted for CMRR null. The procedure is then repeated until the optimum is achieved.

A circuit which overcomes adjustment interaction is shown in *Figure 7*. In this case, R2 is adjusted first for output null of the LH0036. R1 is then adjusted for output null with +10V input. It is always a good idea to check CMRR null with a −10V input. The optimum null achievable will yield the highest CMRR over the amplifiers common mode range.

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*Note: Nominal value R1 to Achieve Optimum CMRR is 3.0 kΩ

**FIGURE 7. Improved $V_{OS}$, CMRR Nulling Circuit**

### AC CMRR Considerations

The ac CMRR may be improved using the circuit of *Figure 8*.

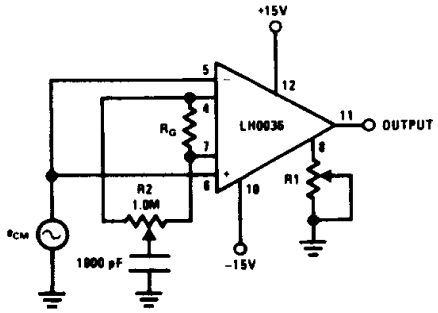


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**FIGURE 8. Improved AC CMRR Circuit**

After adjusting R1 for best dc CMRR as before, R2 should be adjusted for minimum peak-to-peak voltage at the output while applying an ac common mode signal of the maximum amplitude and frequency of interest.

### INPUT BIAS CURRENT CONTROL

Under nominal operating conditions (pin 3 grounded), the LH0036 requires input currents of 40 nA. The input current may be reduced by inserting a resistor ($R_B$) between 3 and ground or, alternatively, between 3 and $V^-$. For $R_B$ returned to ground, the input bias current may be predicted by:

$$I_{BIAS} \cong \frac{V^+ - 0.5}{4 \times 10^8 + 800\, R_B} \qquad (6a)$$

or

$$R_B = \frac{V^+ - 0.5 - (4 \times 10^8)\,(I_{BIAS})}{800\, I_{BIAS}} \qquad (6b)$$

Where:

$I_{BIAS}$ = Input Bias Current (nA)
$R_B$ = External Resistor connected between pin 3 and ground (Ohms)
$V^+$ = Positive Supply Voltage (Volts)

*Figure 9* is a plot of input bias current versus $R_B$.

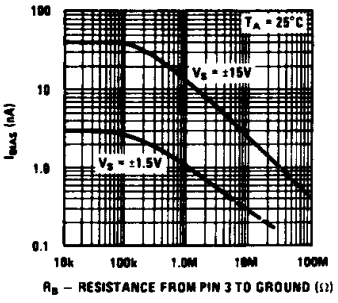


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**FIGURE 9. Input Bias Current as a Function of $R_B$**

As indicated above, $R_B$ may be returned to the negative supply voltage. Input bias current may then be predicted by:

$$I_{BIAS} \cong \frac{(V^+ - V^-) - 0.5}{4 \times 10^8 + 800\, R_B}$$

## Applications Information (Continued)

or

$$R_B \cong \frac{(V^+ - V^-) - 0.5 - (4 \times 10^8)(I_{BIAS})}{800\ I_{BIAS}} \quad (8)$$

Where:

$I_{BIAS}$ = Input Bias Current (nA)
$R_B$ = External resistor connected between pin 3 and $V^-$ (Ohms)
$V^+$ = Positive Supply Voltage (Volts)
$V^-$ = Negative Supply Voltage (Volts)

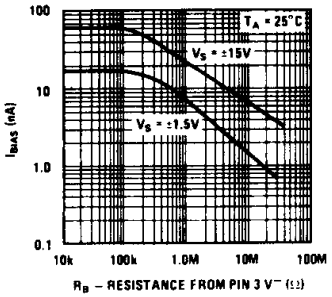


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**FIGURE 10. Input Bias Current as a Function of $R_B$**

*Figure 10* is a plot of input bias current versus $R_B$ returned to $V^-$ it should be noted that bandwidth is affected by changes in $R_B$. *Figure 11* is a plot of bandwidth versus $R_B$.

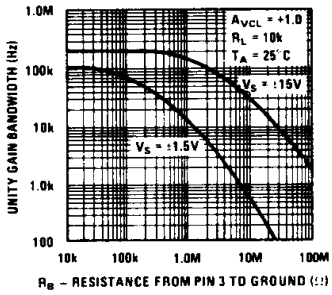


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**FIGURE 11. Unity Gain Bandwidth as a Function of $R_B$**

### BIAS CURRENT RETURN PATH CONSIDERATIONS

The LH0036 exhibits input bias currents typically in the 40 nA region in each input. This current must flow through $R_{ISO}$ as shown in *Figure 12*.

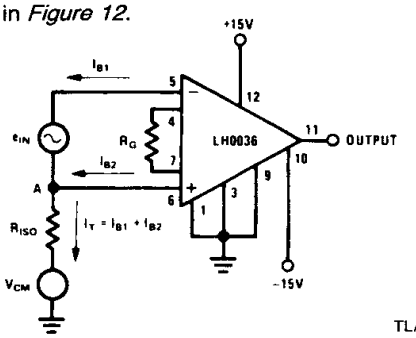


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**FIGURE 12. Bias Current Return Path**

In a typical application, $V_S = \pm 15V$, $I_{B1} \cong I_{B2} \cong 40$ nA, the total current, $I_T$, would flow through $R_{ISO}$ causing a voltage rise at point A. For values of $R_{ISO} \geq 150$ MΩ, the voltage at point A exceeds the +12V common range of the device. Clearly, for $R_{ISO} = \infty$, the LH0036 would be driven to positive saturation.

The implication is that a finite impedance must be supplied between the input and power supply ground. The value of the resistor is dictated by the maximum input bias current, and the common mode voltage. Under worst case conditions:

$$R_{ISO} \leq \frac{V_{CMR} - V_{CM}}{I_T} \quad (9)$$

Where:

$V_{CMR}$ = Common Mode Range (10V for the LH0036)
$V_{CM}$ = Common Mode Voltage
$I_T = I_{B1} + I_{B2}$

**In applications in which the signal source is floating, such as a thermocouple, one end of the source may be grounded directly or through a resistor.**

### GUARD OUTPUT

Pin 2 of the LH0036 is provided as a guard drive pin in those stringent applications which require very low leakage and minimum input capacitance. Pin 2 will always be biased at the input common mode voltage. The source impedance looking into pin 2 is approximately 15 kΩ. Proper use of the guard/shield pin is shown in *Figure 13*.

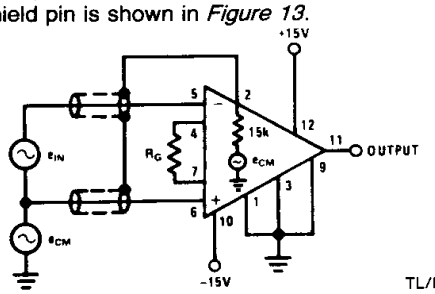


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**FIGURE 13. Use of Guard**

For applications requiring a lower source impedance than 15 kΩ, a unity gain buffer, such as the LH0002 may be inserted between pin 2 and the input shields as shown in *Figure 14*.

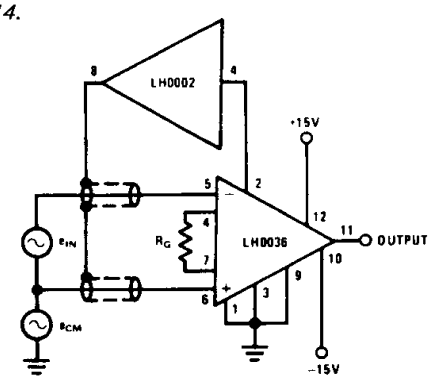


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**FIGURE 14. Guard Pin With Buffer**

## Definition of Terms

**Bandwidth:** The frequency at which the voltage gain is reduced to 0.707 of the low frequency (dc) value.

**Closed Loop Gain, $A_{VCL}$:** The ratio of the output voltage swing to the input voltage swing determined by $A_{VCL} = 1 + (50k/R_G)$. Where: $R_G$ = Gain Set Resistor.

**Common Mode Rejection Ratio:** The ratio of input voltage range to the peak-to-peak change in offset voltage over this range.

**Gain Equation Accuracy:** The deviation of the actual closed loop gain from the predicted closed loop gain, $A_{VCL} = 1 + (50k/R_G)$ for the specified closed loop gain.

**Input Bias Current:** The current flowing at pin 5 and 6 under the specified operating conditions.

**Input Offset Current:** The difference between the input bias current at pins 5 and 6; i.e. $I_{OS} = |I_5 - I_6|$.

**Input Stage Offset Voltage, $V_{IOS}$:** The voltage which must be applied to the input pins to force the output to zero volts for $A_{VCL} = 100$.

**Output Stage Offset Voltage, $V_{OOS}$:** The voltage which must be applied to the input of the output stage to produce zero output voltage. It can be measured by measuring the overall offset at unity gain and subtracting $V_{IOS}$.

$$V_{OOS} = \left[V_{OS}\Big|_{A_{VCL}=1}\right] - \left[V_{OS}\Big|_{A_{VCL}=1000}\right]$$

**Overall Offset Voltage:**

$$V_{OS} = V_{IOS} + \frac{V_{OOS}}{A_{VCL}}$$

**Power Supply Rejection Ratio:** The ratio of the change in offset voltage, $V_{OS}$, to the change in supply voltage producing it.

**Resistor, $R_B$:** An optional resistor placed between pin 3 of the LH0036 and ground (or $V^-$) to reduce the input bias current.

**Resistor, $R_{BW}$:** An optional resistor placed between pin 1 of the LH0036 and ground (or $V^-$) to reduce the bandwidth of the output stage.

**Resistor, $R_G$:** A gain setting resistor connected between pins 4 and 7 of the LH0036 in order to program the gain from 1 to 1000.

**Settling Time:** The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.