19-3872; Rev 0; 3/06

EVALUATION KIT AVAILABLE

2A, 76V, High-Efficiency MAXPower Step-Down DC-DC Converters

General Description

The MAX5090A/B/C easy-to-use, high-efficiency, high-voltage step-down DC-DC converters operate from an input voltage up to 76V, and consume only 310μA quiescent current at no load. This pulse-width-modulated (PWM) converter operates at a fixed 127kHz switching frequency at heavy loads, and automatically switches to pulse-skipping mode to provide low quiescent current and high efficiency at light loads. The MAX5090 includes internal frequency compensation simplifying circuit implementation. The device can also be synchronized with external system clock frequency in a noise-sensitive application. The MAX5090 uses an internal low on-resistance and a high-voltage DMOS transistor to obtain high efficiency and reduce overall system cost. This device includes undervoltage lockout, cycle-by-cycle current limit, hiccup-mode output short-circuit protection, and overtemperature shutdown.

The MAX5090 delivers up to 2A output current. External shutdown is included, featuring 19μA (typ) shutdown current. The MAX5090A/MAX5090B versions have fixed output voltages of 3.3V and 5V, respectively, while the MAX5090C features an adjustable 1.265V to 11V output voltage.

The MAX5090 is available in a space-saving 16-pin thin QFN package (5mm x 5mm) and operates over the automotive temperature range (-40°C to +125°C).

Applications

Automotive

Industrial

Distributed Power

Features

- ♦ Wide Input Voltage Range: 6.5V to 76V
- ♦ Fixed (3.3V, 5V) and Adjustable (1.265V to 11V) Output-Voltage Versions
- ♦ 2A Output Current
- ♦ Efficiency Up to 92%
- ♦ Internal 0.26Ω High-Side DMOS FET
- ♦ 310μA Quiescent Current at No Load
- ♦ 19μA Shutdown Current
- ♦ Internal Frequency Compensation
- ♦ Fixed 127kHz Switching Frequency
- ♦ External Frequency Synchronization
- ♦ Thermal Shutdown and Short-Circuit Current Limit
- ♦ -40°C to +125°C Automotive Temperature Range
- ♦ 16-Pin (5mm x 5mm) Thin QFN Package
- ♦ Capable of Dissipating 2.67W at +70°C

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE*	OUTPUT VOLTAGE (V)
MAX5090AATE+	-40°C to +125°C	16 TQFN-EP**	3.3
MAX5090AATE	-40°C to +125°C	16 TQFN-EP**	3.3
MAX5090BATE+	-40°C to +125°C	16 TQFN-EP**	5.0
MAX5090BATE	-40°C to +125°C	16 TQFN-EP**	5.0

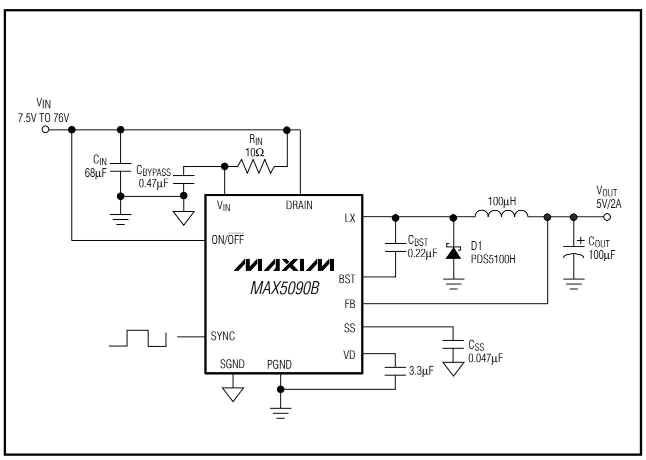
Ordering Information continued at end of data sheet.

**The package code is T1655-3.*

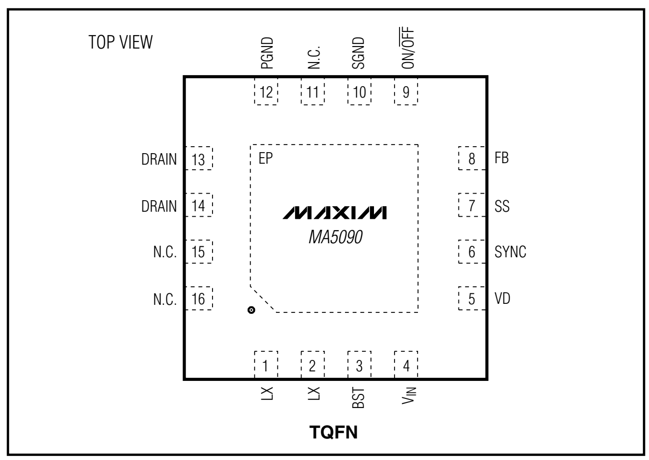
***EP = Exposed pad.*

+Denotes lead-free package.

Typical Operating Circuit



Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to PGND, unless otherwise specified.)
V_{IN}, DRAIN ....-0.3V to +80V
SGND, PGND..........-0.3V to +0.3V
LX..........-0.8V to (V_{IN} + 0.3V)
BST ....-0.3V to (V_{IN} + 10V)
BST to LX..........-0.3V to +10V
ON/$\overline{OFF}$..........-0.3V to (V_{IN} + 0.3V)
VD, SYNC ....-0.3V to +12V
SS..........-0.3 to +4V
FB
MAX5090A/MAX5090B..........-0.3V to +15V
MAX5090C ....1mA (internally clamped to +2V, -0.3V)

V_{OUT} Short-Circuit Duration..........Continuous
VD Short-Circuit Duration..........Continuous
Continuous Power Dissipation (T_A = +70°C)*
16-Pin TQFN (derate 33.3mW/°C above +70°C) 2.667W
Operating Junction Temperature Range..........-40°C to +125°C
Storage Temperature Range ....-65°C to +150°C
Junction Temperature..........+150°C
Lead Temperature (soldering, 10s) ....+300°C

**As per JEDEC 51 Standard Multilayer Board.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +12V, $V_{ON/\overline{OFF}}$ = +12V, V_{SYNC} = 0V, I_{OUT} = 0, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. See the *Typical Operating Circuit.*) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			6.5		76.0	V
Undervoltage Lockout	UVLO	V_{IN} rising		5.70	6.17	6.45	V
UVLO Hysteresis	$UVLO_{HYS}$				0.5		V
Output Voltage	V_{OUT}	MAX5090A	V_{IN} = 6.5V to 76V, I_{OUT} = 0 to 2A	3.20	3.3	3.39	V
		MAX5090B	V_{IN} = 7.5V to 76V, I_{OUT} = 0 to 2A	4.85	5.0	5.15	
		MAX5090B	V_{IN} = 7V to 76V, I_{OUT} = 0 to 1A	4.85	5.0	5.15	
Output Voltage Range	V_{OUT}	MAX5090C only		1.265		11.000	V
Feedback Voltage	V_{FB}	MAX5090C, V_{IN} = 6.5V to 76V		1.191	1.228	1.265	V
Efficiency	η	MAX5090A	V_{IN} = 12V, I_{OUT} = 1A		80		%
		MAX5090B	V_{IN} = 12V, I_{OUT} = 1A		88		
		MAX5090C	V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1A		88		
Quiescent Supply Current (Note 2)	I_Q	MAX5090A	V_{IN} = 6.5V to 28V		310	550	µA
		MAX5090B	V_{IN} = 7V to 28V		310	550	
		MAX5090C	V_{IN} = 6.5V to 28V		310	550	
Quiescent Supply Current (Note 2)	I_Q	MAX5090A	V_{IN} = 6.5V to 40V		310	570	µA
		MAX5090B	V_{IN} = 7V to 40V		310	570	
		MAX5090C	V_{IN} = 6.5V to 40V		310	570	
Quiescent Supply Current (Note 2)	I_Q	MAX5090A	V_{IN} = 6.5V to 76V		310	650	µA
		MAX5090B	V_{IN} = 7V to 76V		310	650	
		MAX5090C	V_{IN} = 6.5V to 76V		310	650	
Shutdown Current	I_{SHDN}	$V_{ON/\overline{OFF}}$ = 0V, V_{IN} = 14V			19	45	µA
SOFT-START							
Default Internal Soft-Start Period		C_{SS} = 0			700		µs
Soft-Start Charge Current	I_{SS}			4.5	10	16.0	µA

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +12V, $V_{ON/\overline{OFF}}$ = +12V, V_{SYNC} = 0V, I_{OUT} = 0, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. See the *Typical Operating Circuit*.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Soft-Start Reference Voltage	$V_{SS(REF)}$		1.23	1.46	1.65	V
INTERNAL SWITCH/CURRENT LIMIT						
Peak Switch Current Limit	I_{LIM}	(Note 3)	2.4	3.3	5.0	A
Switch Leakage Current	I_{OL}	V_{IN} = 76V, $V_{ON/\overline{OFF}}$ = 0V, V_{LX} = 0V	-10		+10	µA
Switch On-Resistance	$R_{DS(ON)}$	I_{SWITCH} = 1A		0.26	0.4	Ω
PFM Threshold	I_{PFM}	Minimum switch current in any cycle	1	60	300	mA
PFM Threshold	I_{PFM}	Minimum switch current in any cycle at T_J ≤ +25°C (Note 4)	14		300	mA
FB Input Bias Current	I_B	MAX5090C, V_{FB} = 1.2V	-150	+0.1	+150	nA
ON/$\overline{\text{OFF}}$ CONTROL INPUT						
ON/$\overline{\text{OFF}}$ Input-Voltage Threshold	$V_{ON/\overline{OFF}}$	Rising trip point	1.180	1.38	1.546	V
ON/$\overline{\text{OFF}}$ Input-Voltage Hysteresis	V_{HYST}			100		mV
ON/$\overline{\text{OFF}}$ Input Current	$I_{ON/\overline{OFF}}$	$V_{ON/\overline{OFF}}$ = 0V to V_{IN}		10	100	nA
OSCILLATOR/SYNCHRONIZATION						
Oscillator Frequency	f_{OSC}		106	127	150	kHz
Synchronization	f_{SYNC}		119		200	kHz
Maximum Duty Cycle	D_{MAX}	V_{IN} = 6.5V to 76V, V_{OUT} ≤ 11V	80	95		%
SYNC High-Level Voltage			2.0			V
SYNC Low-Level Voltage					0.8	V
SYNC Minimum Pulse Width					350	ns
SYNC Input Leakage			-1		+1	µA
INTERNAL VOLTAGE REGULATOR						
Regulator Output Voltage	VD	V_{IN} = 9V to 76V, I_{OUT} = 0	7.0	7.8	8.4	V
Dropout Voltage		6.5V ≤ V_{IN} ≤ 8.5V, I_{OUT} = 15mA		0.5		V
Load Regulation	$\Delta VD/\Delta I_{VD}$	0 to 15mA		10		Ω
PACKAGE THERMAL CHARACTERISTICS						
Thermal Resistance (Junction to Ambient)	θ_{JA}	TQFN package (JEDEC 51)		30		°C/W
THERMAL SHUTDOWN						
Thermal-Shutdown Junction Temperature	T_{SH}	Temperature rising		+175		°C
Thermal-Shutdown Hysteresis	T_{HYST}			20		°C

Note 1: All limits at -40°C are guaranteed by design, not production tested.
Note 2: For total current consumption during switching (at no load), also see the *Typical Operating Characteristics*.
Note 3: Switch current at which the current-limit circuit is activated.
Note 4: Limits are guaranteed by design.

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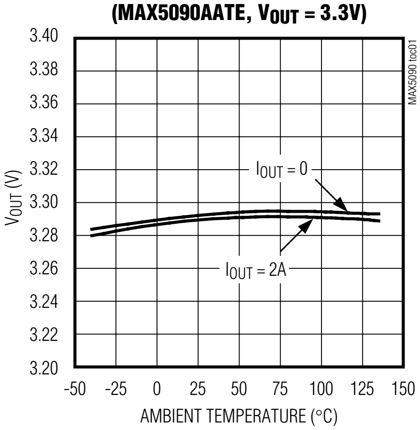
2A, 76V, High-Efficiency MAXPower Step-Down DC-DC Converters

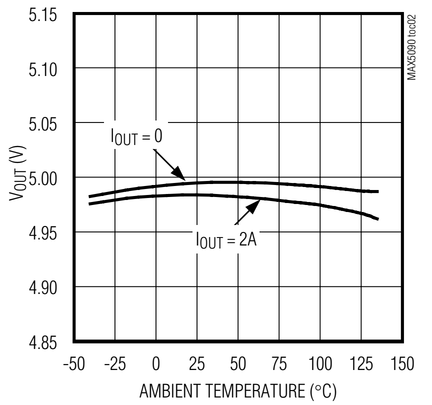
Typical Operating Characteristics

(V_{IN} = 12V, $V_{ON/\overline{OFF}}$ =12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. See the *Typical Operating Circuit,* if applicable.)

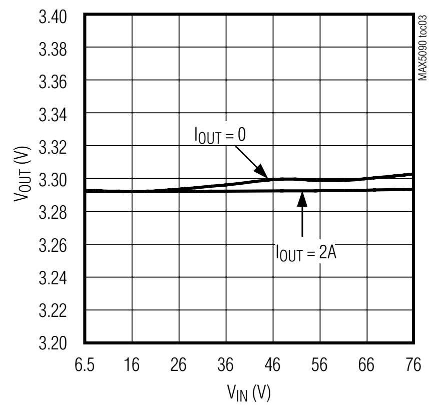
V_{OUT} vs. TEMPERATURE (MAX5090AATE, V_{OUT} = 3.3V)



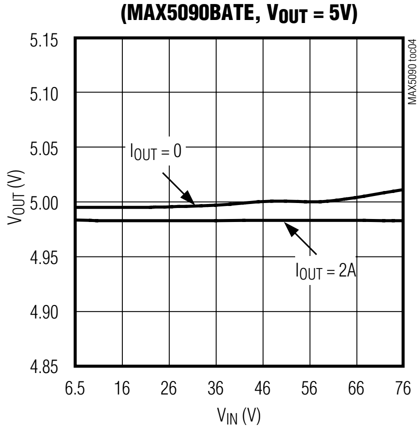
V_{OUT} vs. TEMPERATURE (MAX5090BATE, V_{OUT} = 5V)



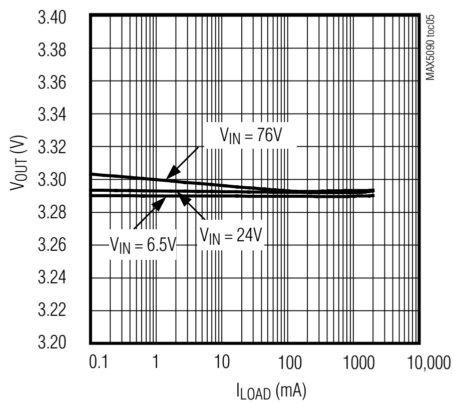
LINE REGULATION (MAX5090AATE, V_{OUT} = 3.3V)



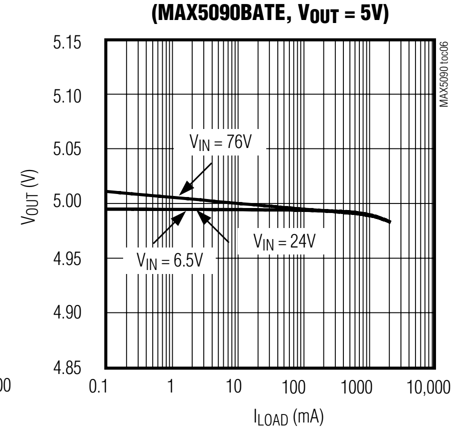
LINE REGULATION (MAX5090BATE, V_{OUT} = 5V)



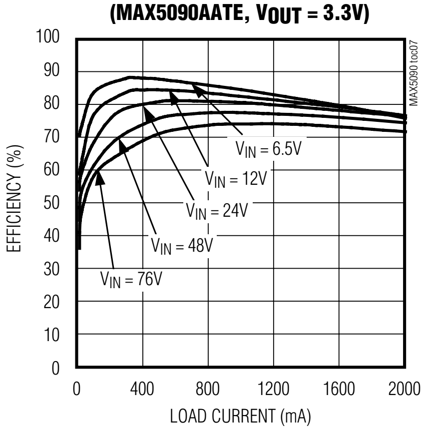
LOAD REGULATION (MAX5090AATE, V_{OUT} = 3.3V)



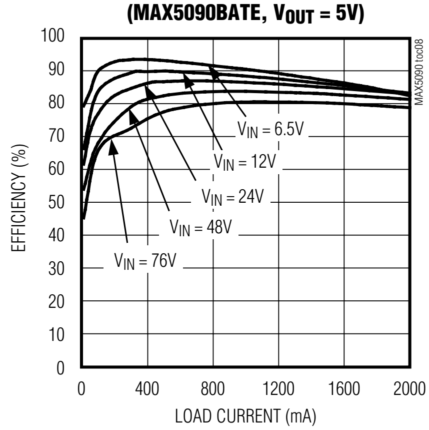
LOAD REGULATION (MAX5090BATE, V_{OUT} = 5V)



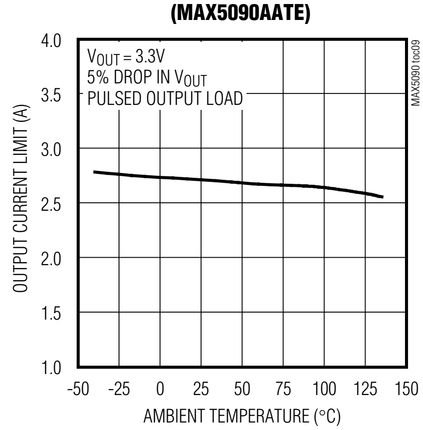
EFFICIENCY vs. LOAD CURRENT (MAX5090AATE, V_{OUT} = 3.3V)



EFFICIENCY vs. LOAD CURRENT (MAX5090BATE, V_{OUT} = 5V)



OUTPUT CURRENT LIMIT vs. TEMPERATURE (MAX5090AATE)



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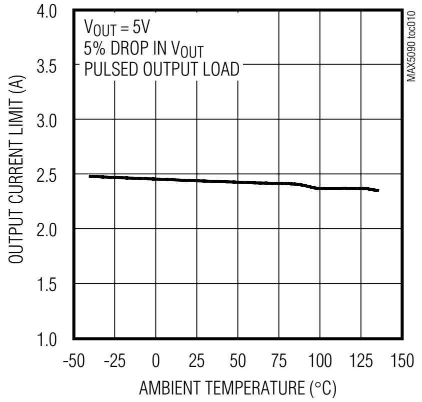
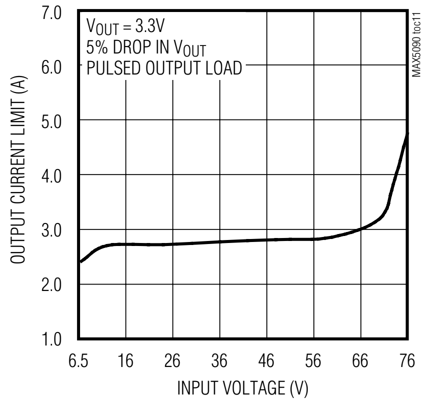
Typical Operating Characteristics (continued)

(V_{IN} = 12V, $V_{ON/\overline{OFF}}$ = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. See the *Typical Operating Circuit,* if applicable.)

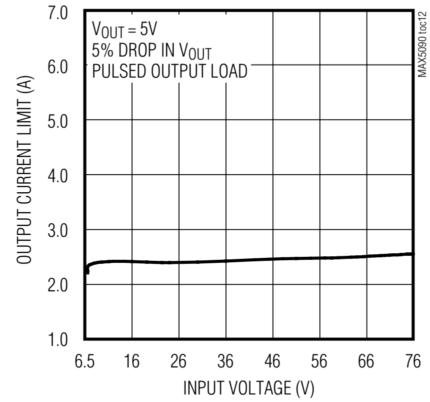
OUTPUT CURRENT LIMIT vs. TEMPERATURE (MAX5090BATE)



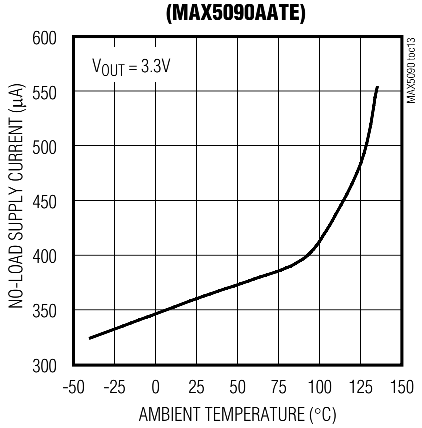
OUTPUT CURRENT LIMIT vs. INPUT VOLTAGE (MAX5090AATE)



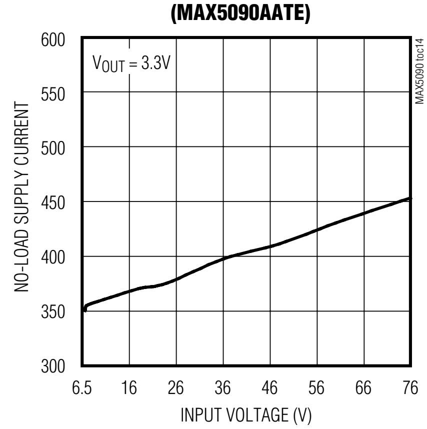
OUTPUT CURRENT LIMIT vs. INPUT VOLTAGE (MAX5090BATE)



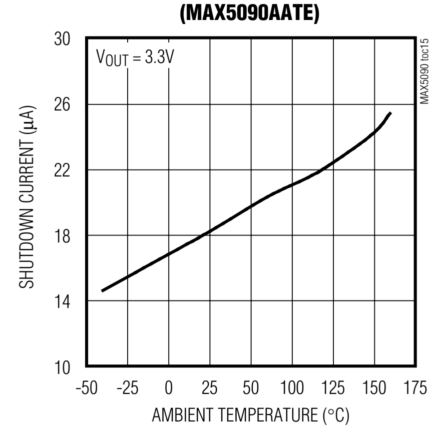
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE (MAX5090AATE)



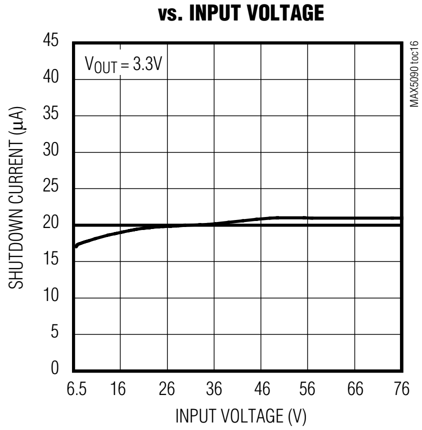
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (MAX5090AATE)



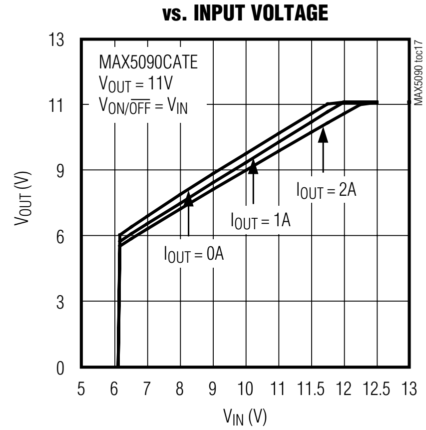
SHUTDOWN CURRENT vs. TEMPERATURE (MAX5090AATE)



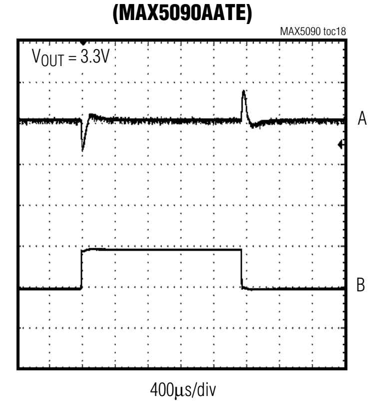
SHUTDOWN CURRENT vs. INPUT VOLTAGE



OUTPUT VOLTAGE vs. INPUT VOLTAGE



LOAD-TRANSIENT RESPONSE (MAX5090AATE)



A: V_{OUT}, 200mV/div, AC-COUPLED
B: I_{OUT}, 1A/div, 1A TO 2A

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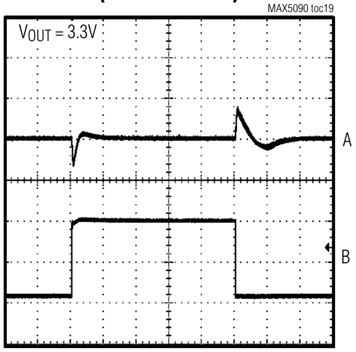
2A, 76V, High-Efficiency MAXPower Step-Down DC-DC Converters

Typical Operating Characteristics (continued)

(V_{IN} = 12V, $V_{ON/\overline{OFF}}$ =12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. See the *Typical Operating Circuit,* if applicable.)

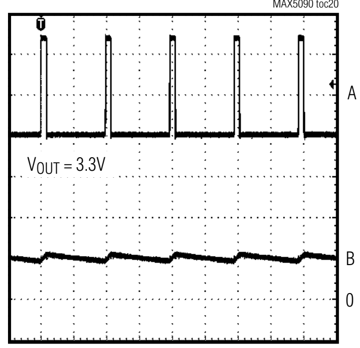
LOAD-TRANSIENT RESPONSE (MAX5090AATE)



400µs/div

A: V_{OUT}, 200mV/div, AC-COUPLED
B: I_{OUT}, 500mA/div, 0.1A TO 1A

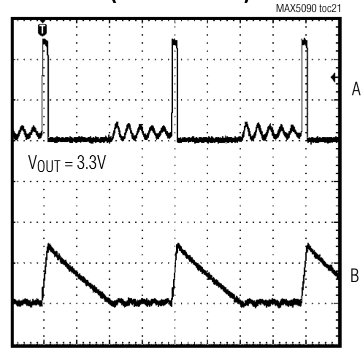
LX WAVEFORMS (MAX5090AATE)



4µs/div

A: SWITCH VOLTAGE (LX PIN), 20mV/div (V_{IN} = 48V)
B: INDUCTOR CURRENT, 2A/div (I_0 = 2A)

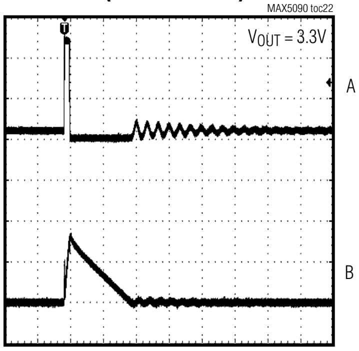
LX WAVEFORMS (MAX5090AATE)



4µs/div

A: SWITCH VOLTAGE, 20V/div (V_{IN} = 48V)
B: INDUCTOR CURRENT, 200mA/div (I_0 = 75mA)

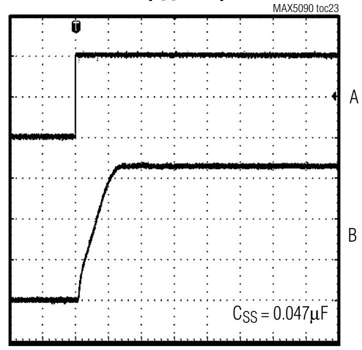
LX WAVEFORM (MAX5090AATE)



4µs/div

A: SWITCH VOLTAGE, 20V/div (V_{IN} = 48V)
B: INDUCTOR CURRENT, 200mA/div (I_{OUT} = 0)

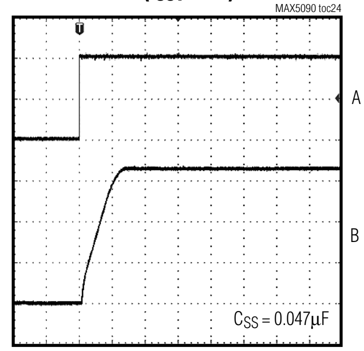
STARTUP WAVEFORM (I_{OUT} = 0)



4ms/div

A: $V_{ON/\overline{OFF}}$, 2V/div
B: V_{OUT}, 1V/div

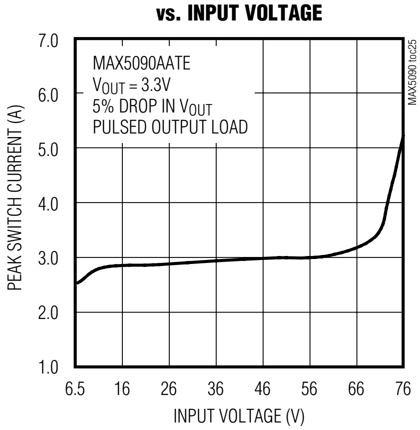
STARTUP WAVEFORM (I_{OUT} = 2A)



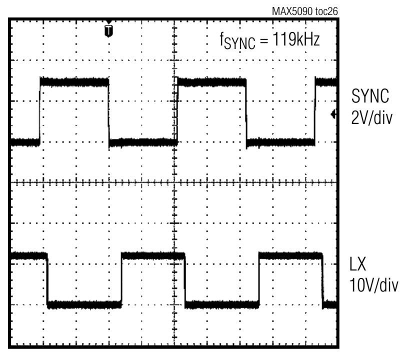
4ms/div

A: $V_{ON/\overline{OFF}}$, 2V/div
B: V_{OUT}, 1V/div

PEAK SWITCH CURRENT vs. INPUT VOLTAGE

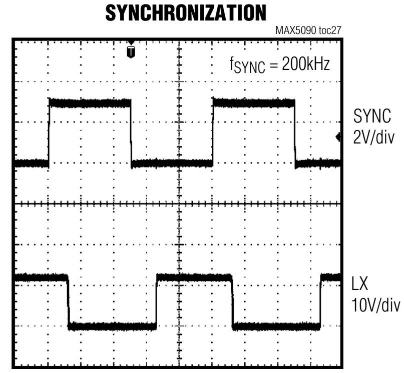


SYNCHRONIZATION



2µs/div

SYNCHRONIZATION



1µs/div

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Pin Description

PIN	NAME	FUNCTION
1, 2	LX	Source Connection of Internal High-Side Switch
3	BST	Boost Capacitor Connection. Connect a 0.22µF ceramic capacitor from BST to LX.
4	V_{IN}	Input Voltage. Bypass V_{IN} to SGND with a low-ESR capacitor as close to the device as possible.
5	VD	Internal Regulator Output. Bypass VD to PGND with a 3.3µF/10V or greater ceramic capacitor.
6	SYNC	Synchronization Input. Connect SYNC to an external clock for synchronization. Connect to SGND to select the internal 127kHz switching frequency.
7	SS	Soft-Start Capacitor Connection. Connect an external capacitor from SS to SGND to adjust the soft-start time.
8	FB	Output Sense Feedback Connection. For fixed output voltage (MAX5090A/MAX5090B), connect FB to V_{OUT}. For adjustable output voltage (MAX5090C), use an external resistive voltage-divider to set V_{OUT}. V_{FB} regulating set point is 1.228V.
9	ON/$\overline{\text{OFF}}$	Shutdown Control Input. Pull ON/$\overline{\text{OFF}}$ low to put the device in shutdown mode. Drive ON/$\overline{\text{OFF}}$ high for normal operation. Connect ON/$\overline{\text{OFF}}$ to V_{IN} with short leads for always-on operation.
10	SGND	Signal Ground. SGND must be connected to PGND for proper operation.
11, 15, 16	N.C.	No Connection. Not internally connected.
12	PGND	Power Ground
13, 14	DRAIN	Internal High-Side Switch Drain Connection
—	EP	Exposed Pad. Solder EP to SGND plane to aid in heat dissipation. Do not use as the only electrical ground connection.

Detailed Description

The MAX5090 step-down DC-DC converter operates from a 6.5V to 76V input voltage range. A unique voltage-mode control scheme with voltage feed-forward and an internal switching DMOS FET provides high efficiency over a wide input voltage range. This pulse-width-modulated converter operates at a fixed 127kHz switching frequency or can be synchronized with an external system clock frequency. The device also features automatic pulse-skipping mode to provide high efficiency at light loads. Under no load, the MAX5090 consumes only 310µA, and in shutdown mode, consumes only 20µA. The MAX5090 also features undervoltage-lockout, hiccup-mode output short-circuit protection and thermal shutdown.

ON/$\overline{\text{OFF}}$/Undervoltage Lockout (UVLO)

Use the ON/$\overline{\text{OFF}}$ function to program the external UVLO threshold at the input. Connect a resistive voltage-divider from V_{IN} to SGND with the center node to ON/$\overline{\text{OFF}}$, as shown in Figure 1. Calculate the threshold value by using the following formula:

$$V_{UVLO(TH)} = \left(1 + \frac{R1}{R2}\right) \times 1.38$$

Set the external $V_{UVLO(TH)}$ to greater than 6.45V. The maximum recommended value for R2 is less than 1MΩ.

ON/$\overline{\text{OFF}}$ is a logic input and can be safely driven to the full V_{IN} range. Connect ON/$\overline{\text{OFF}}$ to V_{IN} for automatic startup. Drive ON/$\overline{\text{OFF}}$ to ground to shut down the MAX5090. Shutdown forces the internal power MOSFET off, turns off all internal circuitry, and reduces the V_{IN} supply current to 20µA (typ). The ON/$\overline{\text{OFF}}$ rising threshold is 1.546V (max). Before any operation begins, the voltage at ON/$\overline{\text{OFF}}$ must exceed 1.546V. The ON/$\overline{\text{OFF}}$ input has 100mV hysteresis.

If the external UVLO threshold setting divider is not used, an internal undervoltage-lockout feature monitors the supply voltage at V_{IN} and allows the operation to start when V_{IN} rises above 6.45V (max). The internal UVLO rising threshold is set at 6.17V with 0.5V hysteresis. The V_{IN} and $V_{ON/\overline{OFF}}$ voltages must be above 6.5V and 1.546V, respectively, for proper operation.

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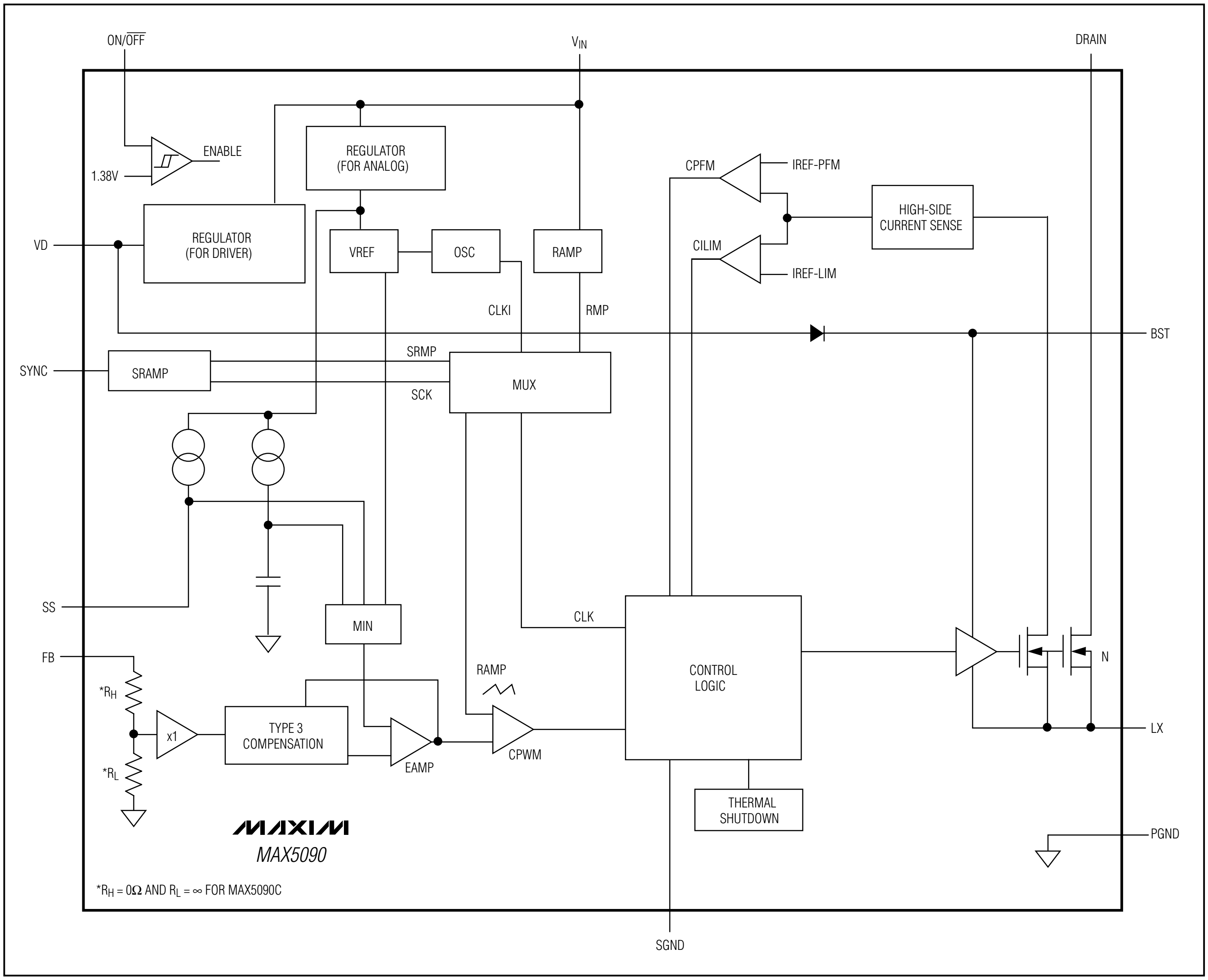
Simplified Functional Diagram



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Boost High-Side Gate Drive (BST)

Connect a flying bootstrap capacitor between LX and BST to provide the gate-drive voltage to the high-side n-channel DMOS switch. The capacitor is alternately charged from the internally regulated output-voltage VD and placed across the high-side DMOS driver. Use a 0.22µF, 16V ceramic capacitor located as close to the device as possible.

On startup, an internal low-side switch connects LX to ground and charges the BST capacitor to (VD - V_{DIODE}). Once the BST capacitor is charged, the internal low-side switch is turned off and the BST capacitor voltage provides the necessary enhancement voltage to turn on the high-side switch.

Synchronization (SYNC)

SYNC controls the oscillator frequency. Connect SYNC to SGND to select 127kHz operation. Use the SYNC input to synchronize to an external clock. SYNC has a guaranteed frequency range of 119kHz to 200kHz when using an external clock.

When SYNC is connected to SGND, the internal clock is used to generate a ramp with the amplitude in proportion to V_{IN} and the period corresponding to the internal clock frequency to modulate the duty cycle of the high-side switch.

If an external clock (SYNC clock) is applied at SYNC for four cycles, the MAX5090 selects the SYNC clock. The MAX5090 generates a ramp (SYNC ramp) with the amplitude in proportion to V_{IN} and the period corresponding to the SYNC clock frequency. The MAX5090 initially blanks the SYNC ramp for 375µs (typ) to allow the ramp to reach its target amplitude (proportion to the V_{IN} supply). After the SYNC blanking time, the SYNC ramp and the SYNC clock switch to the PWM controller and replace the internal ramp and the internal clock, respectively. If the SYNC clock is removed for three internal clock cycles, the internal clock and the internal ramp switch back to the PWM controller.

The minimum pulse-width requirement for the external clock is 350ns, and if the requirement is not met, the MAX5090 could ignore the clock as a noisy bounce.

Soft-Start (SS)

The MAX5090 provides the flexibility to externally program a suitable soft-start time for a given application. Connect an external capacitor from SS to SGND to use the external soft-start. Soft-start gradually ramps up the reference voltage seen by the error amplifier to control the output's rate of rise and reduce the input surge current during startup. For soft-start time longer than 700µs, use the following equation to calculate the soft-start capacitor (C_{SS}) required for the soft-start time (t_{SS}):

$$C_{SS} = \frac{10 \times 10^{-6} \times t_{SS}}{1.46}$$

where t_{SS} > 700µs and C_{SS} is in Farads.

The MAX5090 also provides an internal soft-start (700µs, typ) with a current source to charge an internal capacitor to rise up to the bandgap reference voltage. The internal soft-start voltage will eventually be pulled up to 3.4V. The internal soft-start reference also feeds to the error amplifier. The error amplifier takes the lowest voltage among SS, the internal soft-start voltage, and the bandgap reference voltage as the input reference for V_{OUT}.

Soft-start occurs when power is first applied and when the device exits shutdown. The MAX5090 also goes through soft-start when coming out of thermal-overload protection. During a soft-start, if the voltage at SS (V_{SS}) is charged up to 1.46V in less than 700µs, the MAX5090 takes its default internal soft-start (700µs) to ramp up as its reference. After the SS and the internal soft-start ramp up over the bandgap reference, the error amplifier takes the bandgap reference.

Thermal-Overload Protection

The MAX5090 features integrated thermal-overload protection. Thermal-overload protection limits power dissipation in the device, and protects the device from a thermal overstress. When the die temperature exceeds +175°C, an internal thermal sensor signals the shutdown logic, turning off the internal power MOSFET, resetting the internal soft-start and allowing the IC to cool. The thermal sensor turns the internal power MOSFET back on after the IC's die temperature cools down to +155°C, resulting in a pulsed output under continuous thermal-overload conditions.

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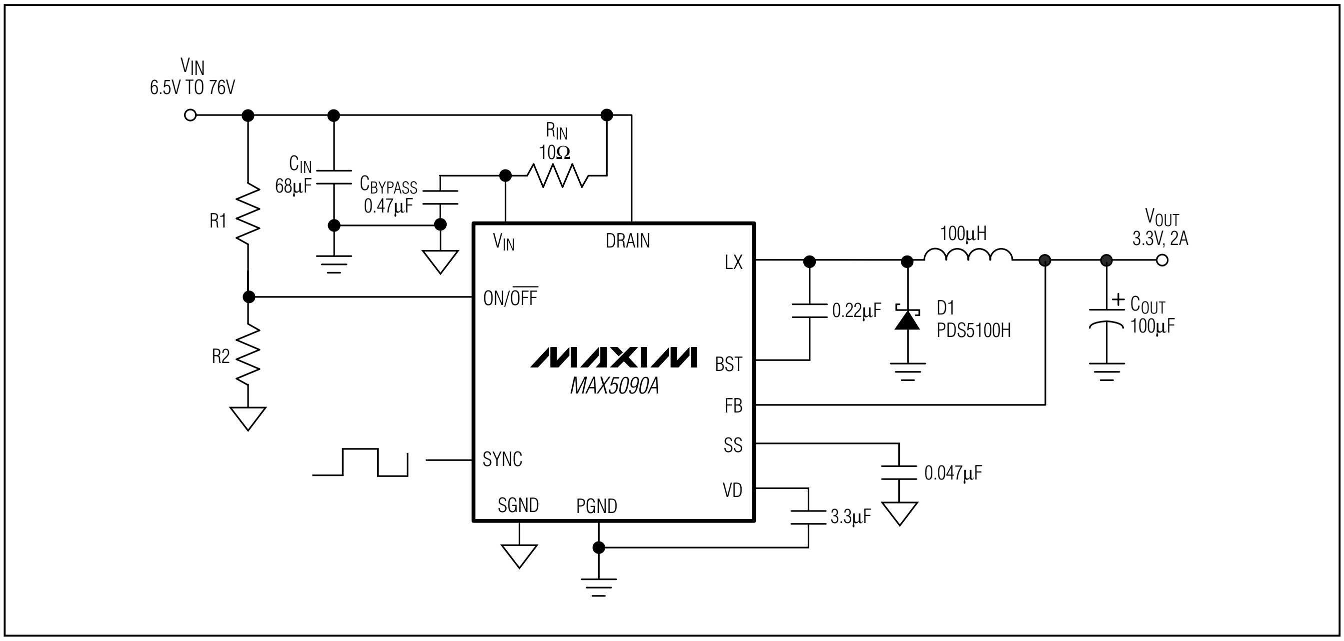

Figure 1. Fixed Output-Voltage Configuration

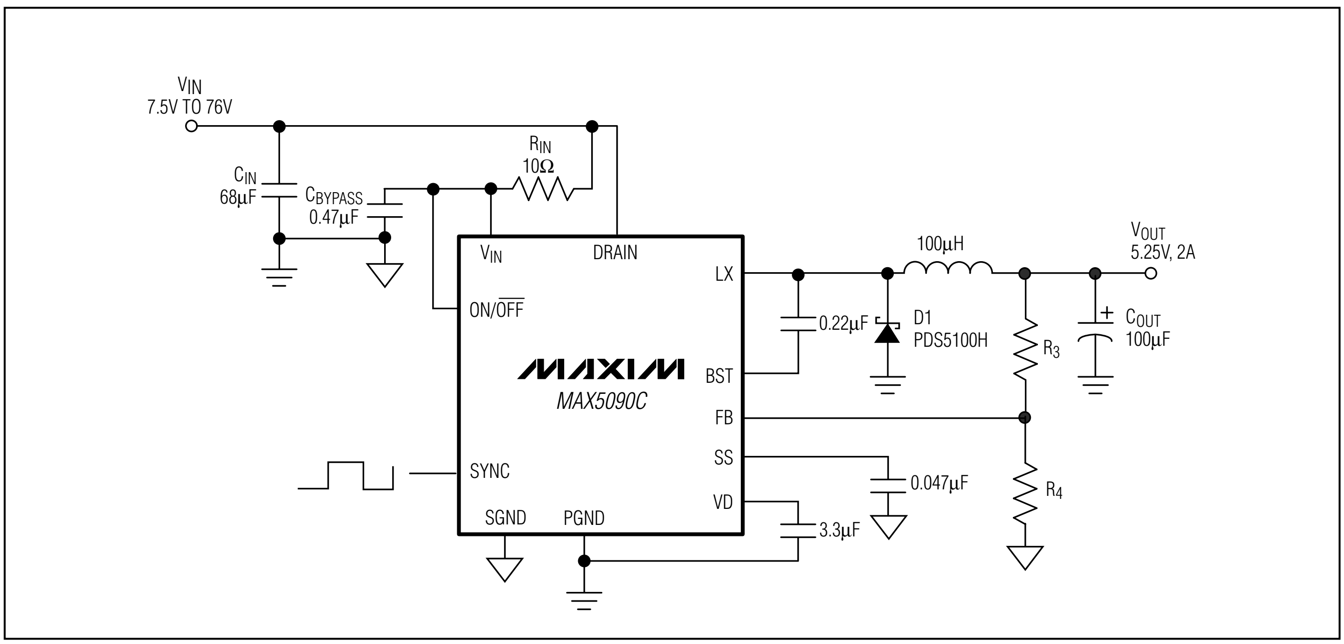

Figure 2. Adjustable Output-Voltage Configuration

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Thermal-overload protection is intended to protect the MAX5090 in the event of a fault condition. For normal circuit operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Setting the Output Voltage

The MAX5090A/MAX5090B have preset output voltages of 3.3V and 5.0V, respectively. Connect FB to V_{OUT} for the preset output voltage (Figure 1).

The MAX5090C offers an adjustable output voltage. Set the output voltage with a resistive divider connected from the circuit's output to ground (Figure 2). Connect the center node of the divider to FB. Choose R4 less than 15kΩ, then calculate R3 as follows:

$$R3 = \frac{(V_{OUT} - 1.228)}{1.228} \times R4$$

The MAX5090 features internal compensation for optimum closed-loop bandwidth and phase margin. Because of the internal compensation, the output must be sensed immediately after the primary LC.

Inductor Selection

The MAX5090 is a fixed-frequency converter with fixed internal frequency compensation. The internal fixed compensation assumes a 100µH inductor and 100µF output capacitor with 50mΩ ESR. It relies on the location of the double LC pole and the ESR zero frequency for proper closed-loop bandwidth and the phase margin at the closed-loop unity-gain frequency. See Table 2 for proper component values. Usually, the choice of an inductor is guided by the voltage difference between V_{IN} and V_{OUT}, the required output current and the operating frequency of the circuit. However, use the recommended inductors in Table 2 to ensure stable operation with optimum bandwidth.

Use an inductor with a maximum saturation current rating greater than or equal to the maximum peak current limit (5A). Use inductors with low DC resistance for a higher efficiency converter.

Selecting a Rectifier

The MAX5090 requires an external Schottky rectifier as a freewheeling diode. Connect this rectifier close to the device using short leads and short PC board traces. The rectifier diode must fully conduct the inductor current when the power FET is off to have a full rectifier function. Choose a rectifier with a continuous current rating greater than the highest expected output current. Use a rectifier with a voltage rating greater than the maximum expected input voltage, V_{IN}. Use a low forward-voltage Schottky rectifier for proper operation and high efficiency. Avoid higher than necessary reverse-voltage Schottky rectifiers that have higher forward-voltage drops. Use a Schottky rectifier with forward-voltage drop (V_F) less than 0.55V and 0.45V at +25°C and +125°C, respectively, and at maximum load current to avoid forward biasing of the internal parasitic body diode (LX to ground). See Figure 3 for forward-voltage drop vs. temperature of the internal body diode of the MAX5090. Internal parasitic body-diode conduction may cause improper operation, excessive junction temperature rise, and thermal shutdown. Use Table 1 to choose the proper rectifier at different input voltages and output current.

Table 1. Diode Selection

V_{IN} (V)	DIODE PART NUMBER	MANUFACTURER
6.5 to 36	B340LB	Diodes Inc.
	RB051L-40	Central Semiconductor
	MBRS340T3	ON Semiconductor
6.5 to 56	MBRM560	Diodes Inc.
	RB095B-60	Central Semiconductor
	MBRD360T4	ON Semiconductor
6.5 to 76	50SQ80	IR
	PDS5100H	Diodes Inc.

Input Bypass Capacitor

The discontinuous input current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflecting back to the source dictate the capacitance requirement. The MAX5090 high switching frequency allows the use of smaller value input capacitors.

The input ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR aluminum electrolytic capacitors with high-ripple current capability at the input. Assuming that the contribution from the ESR and capacitor discharge is equal to 90% and 10%, respectively, calculate the input capacitance and the ESR required for a specified ripple using the following equations:

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$$ESR_{IN} = \frac{\Delta V_{ESR}}{\left(I_{OUT} + \frac{\Delta I_L}{2}\right)}$$

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

I_{OUT} is the maximum output current of the converter and f_{SW} is the oscillator switching frequency (127kHz). For example, at V_{IN} = 48V, V_{OUT} = 3.3V, the ESR and input capacitance are calculated for the input peak-to-peak ripple of 100mV or less, yielding an ESR and capacitance value of 40mΩ and 100µF, respectively.

Low-ESR ceramic multilayer chip capacitors are recommended for size-optimized application. For ceramic capacitors assume the contribution from ESR and capacitor discharge is equal to 10% and 90%, respectively.

The input capacitor must handle the RMS ripple current without significant rise in the temperature. The maximum capacitor RMS current occurs at approximately 50% duty cycle. Ensure that the ripple specification of the input capacitor exceeds the worst-case capacitor RMS ripple current. Use the following equations to calculate the input capacitor RMS current:

$$I_{CRMS} = \sqrt{I_{PRMS}^2 - I_{AVGin}^2}$$

where:

$$I_{PRMS} = \sqrt{(I_{PK}^2 + I_{DC}^2 + I_{PK} \times I_{DC}) \times \frac{D}{3}}$$

$$I_{AVGin} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

$$I_{PK} = I_{OUT} + \frac{\Delta I_L}{2}$$

$$I_{DC} = I_{OUT} - \frac{\Delta I_L}{2}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

I_{PRMS} is the input switch RMS current, I_{AVGin} is the input average current, and η is the converter efficiency.

The ESR of the aluminum electrolytic capacitor increases significantly at cold temperatures. Use a 1µF or greater value ceramic capacitor in parallel with the aluminum electrolytic input capacitor, especially for input voltages below 8V.

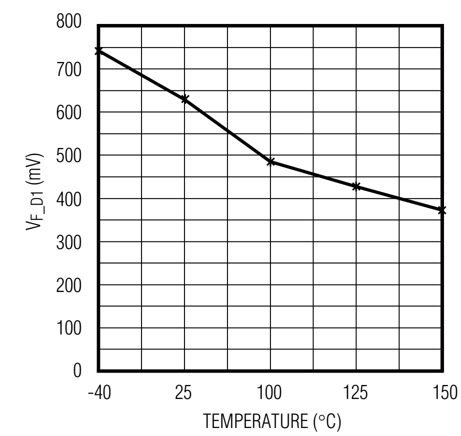

Figure 3. Forward-Voltage Drop vs. Temperature of the Internal Body Diode of MAX5090

Output Filter Capacitor

The output capacitor C_{OUT} forms double pole with the inductor and a zero with its ESR. The MAX5090's internal fixed compensation is designed for a 100µF capacitor, and the ESR must be from 20mΩ to 100mΩ. The use of an aluminum or tantalum electrolytic capacitor is recommended. See Table 2 to choose an output capacitor for stable operation.

The output ripple is comprised of ΔV_{OQ} (caused by the capacitor discharge), and ΔV_{OESR} (caused by the ESR of the capacitor). Use low-ESR tantalum or aluminum electrolytic capacitors at the output. Use the following equations to calculate the contribution of output capacitance and its ESR on the peak-to-peak output ripple voltage:

$$\Delta V_{OESR} = \Delta I_L \times ESR$$

$$\Delta V_{OQ} \approx \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The MAX5090 has a programmable soft-start time (t_{SS}). The output rise time is directly proportional to the output capacitor, output voltage, and the load. The output rise time also depends on the inductor value and the current-limit threshold. It is important to keep the output rise time at startup the same as the soft-start time (t_{SS}) to avoid output overshoot. Large output capacitors take longer than the programmed soft-start time (t_{SS}) and cause error-amplifier saturation. This results in output overshoot. Use greater than 2ms soft-start time for a 100µF output capacitor.

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In a dynamic load application, the allowable deviation of the output voltage during the fast transient load dictates the output capacitance value and the ESR. The output capacitors supply the step-load current until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter. The resistive drop across the capacitor ESR and capacitor discharge cause a voltage droop during a step-load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient load and ripple/noise performance. Use the following equations to calculate the deviation of output voltage due to the ESR and capacitance value of the output capacitor:

$$\Delta V_{OESR} = I_{STEP} \times ESR_{OUT}$$

$$\Delta V_{OQ} = \frac{I_{STEP} \times t_{RESPONSE}}{C_{OUT}}$$

where I_{STEP} is the load step and $t_{RESPONSE}$ is the response time of the controller. Controller response time is approximately one-third of the reciprocal of the closed-loop unity-gain bandwidth, 20kHz typically.

Board Layout Guidelines

1) Minimize ground noise by connecting the anode of the Schottky rectifier, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a large PGND plane.
2) Minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise. In particular, place the Schottky rectifier diode right next to the device. Also, place the BST and VD bypass capacitors very close to the device.
3) Connect the exposed pad of the IC to the SGND plane. Do not make a direct connection between the exposed pad plane and SGND (pin 7) under the IC. Connect the exposed pad and pin 7 to the SGND plane separately. Connect the ground connection of the feedback resistive divider, ON/$\overline{\text{OFF}}$ threshold resistive divider, and the soft-start capacitor to the SGND plane. Connect the SGND plane and PGND plane at one point near the input bypass capacitor at V_{IN}.
4) Use large SGND plane as a heatsink for the MAX5090. Use large PGND and LX planes as heatsinks for the rectifier diode and the inductor.

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Application Circuit

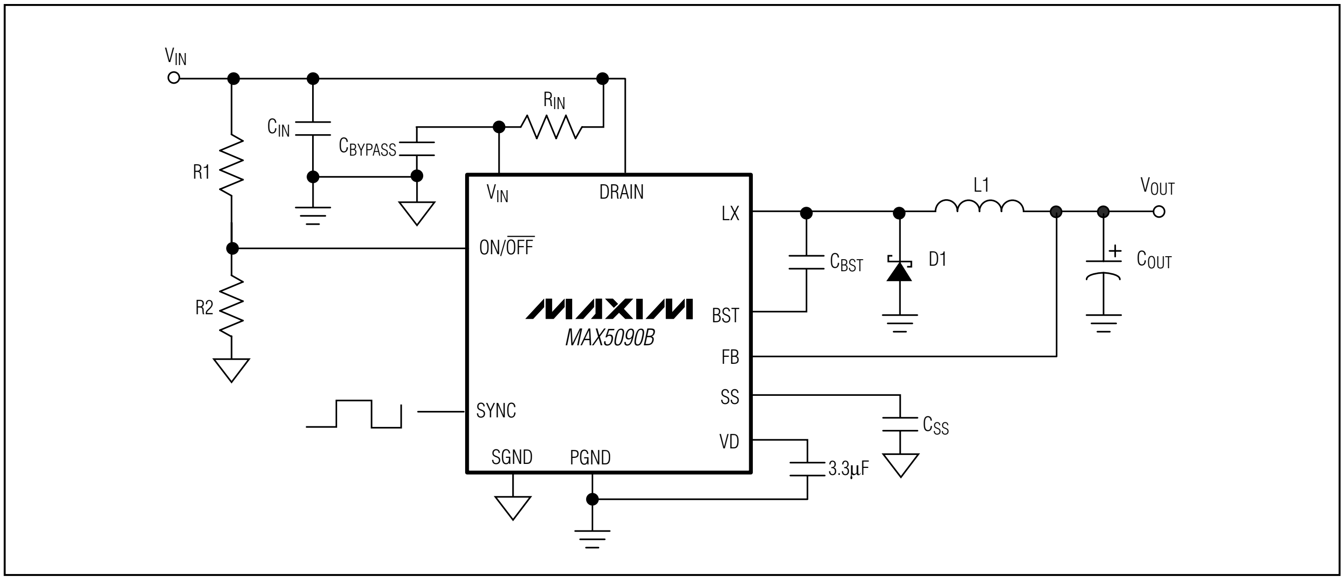

Figure 4. Fixed Output Voltage

Table 2. Typical External Components Selection (Circuit of Figure 4)

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	EXTERNAL COMPONENTS
6.5 to 76	3.3	2	MAX5090AATE C_{IN} = 2 x 68µF/100V EEVFK2A680Q, Panasonic C_{BYPASS} = 0.47µF/100V, GRM21BR72A474KA, Murata C_{OUT} = 220µF/6.3V 6SVP220MX, Sanyo C_{BST} = 0.22µF/16V, GRM188R71C224K, Murata R1 = 0Ω R2 = Open R_{IN} = 10Ω, ±1% (0603) D1 = PDS5100H, Diodes Inc. L1 = 47µH, DO5022P-473
7.5 to 76	5	2	MAX5090BATE C_{IN} = 2 x 68µF/100V EEVFK2A680Q, Panasonic C_{BYPASS} = 0.47µF/100V, GRM21BR72A474KA, Murata C_{OUT} = 100µF/6.3V 6SVP100M, Sanyo C_{BST} = 0.22µF/16V, GRM188R71C224K, Murata R1 = 0Ω R2 = Open R_{IN} = 10Ω, ±1% (0603) D1 = PDS5100H, Diodes Inc. L1 = 47µH, DO5022P-473

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Table 2. Typical External Components Selection (Circuit of Figure 4) (continued)

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	EXTERNAL COMPONENTS
6.5 to 40	3.3	2	MAX5090AATE C_{IN} = 330µF/50V EEVFK1H331Q, Panasonic C_{BYPASS} = 0.47µF/50V, GRM21BR71H474KA, Murata C_{OUT} = 100µF/6.3V 6SVP100M, Sanyo C_{BST} = 0.22µF/16V, GRM188R71C224K, Murata R1 = 0Ω R2 = Open R_{IN} = 10Ω, ±1% (0603) D1 = B360, Diodes Inc. L1 = 100µH, DO5022P-104
7.5 to 40	5	2	MAX5090BATE C_{IN} = 330µF/50V EEVFK1H331Q, Panasonic C_{BYPASS} = 0.47µF/50V, GRM21BR71H474KA, Murata C_{OUT} = 100µF/6.3V 6SVP100M, Sanyo C_{BST} = 0.22µF/16V, GRM188R71C224K, Murata R1 = 0Ω R2 = Open R_{IN} = 10Ω, ±1% (0603) D1 = B360, Diodes Inc. L1 = 100µH, DO5022P-104
15 to 40	11	2	MAX5090CATE (V_{OUT} programmed to 11V) C_{IN} = 330µF/50V EEVFK1H331Q, Panasonic C_{BYPASS} = 0.47µF/50V, GRM21BR71H474KA, Murata C_{OUT} = 100µF/16V 16SVP100M, Sanyo C_{BST} = 0.22µF/16V, GRM188R71C224K, Murata R1 = 910kΩ R2 = 100kΩ R3 = 88.2kΩ, ±1% (0603) R4 = 10kΩ, ±1% (0603) R_{IN} = 10Ω, ±1% (0603) D1 = B360, Diodes Inc. L1 = 100µH, DO5022P-104

Table 3. Component Suppliers

SUPPLIER	WEBSITE
AVX	www.avxcorp.com
Coilcraft	www.coilcraft.com
Diodes Incorporated	www.diodes.com
Panasonic	www.panasonic.com
Sanyo	www.sanyo.com
TDK	www.component.tdk.com
Vishay	www.vishay.com

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2A, 76V, High-Efficiency MAXPower Step-Down DC-DC Converters

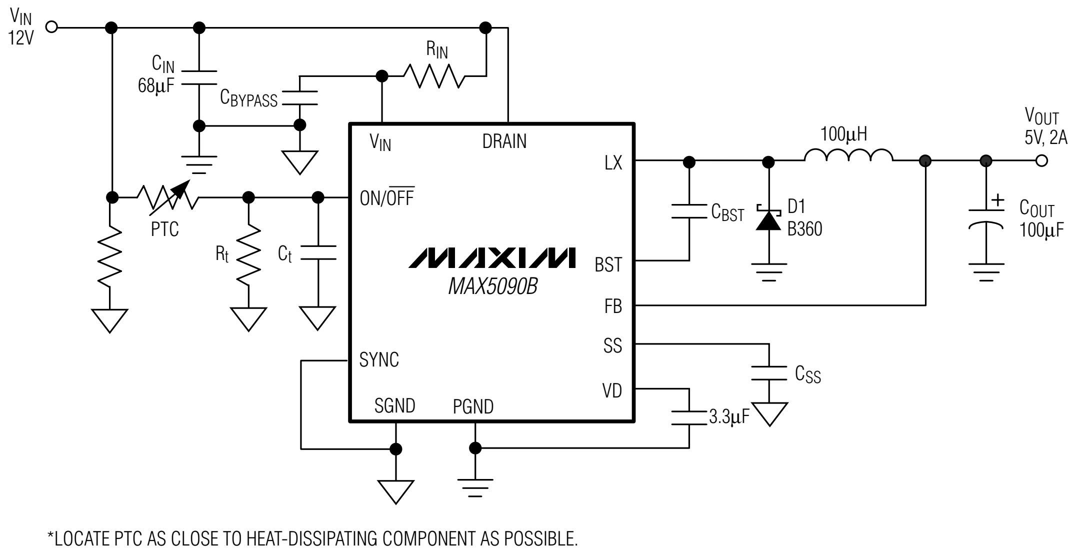

Figure 5. Load-Temperature Monitoring with ON/OFF (Requires Accurate V_{IN})

Chip Information

PROCESS: BCD

TRANSISTOR COUNT: 7893

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE*	OUTPUT VOLTAGE (V)
MAX5090CATE+	-40°C to +125°C	16 TQFN-EP**	Adj
MAX5090CATE	-40°C to +125°C	16 TQFN-EP**	Adj

**The package code is T1655-3.*
***EP = Exposed pad.*
+Denotes lead-free package.

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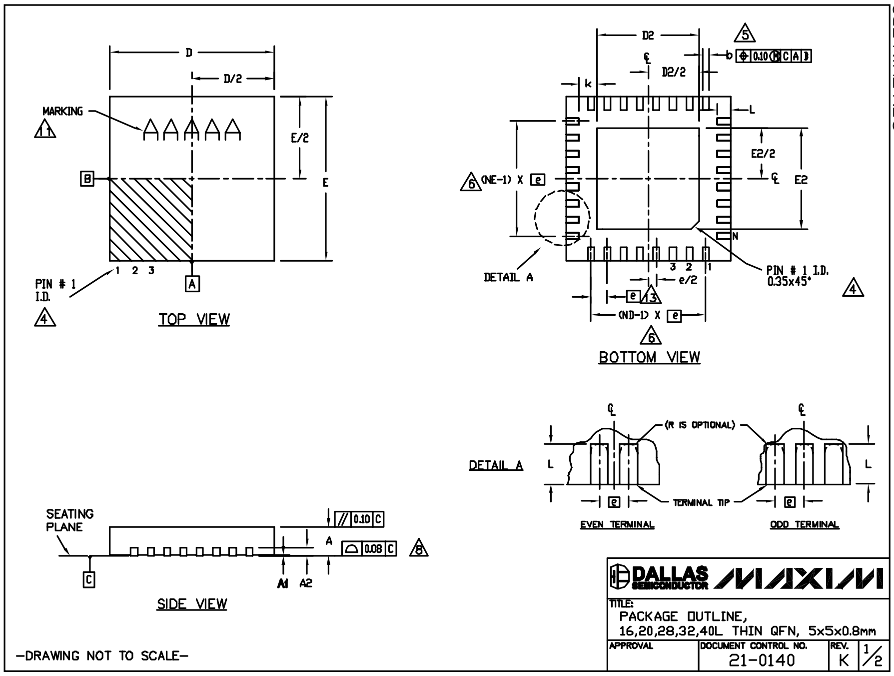
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055M-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.8mm

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