Agilent HSDL-3209
IrDA® Data Compliant Low Power 115.2 kbit/s Infrared Transceiver

Description

The HSDL-3209 is an ultra-small low cost infrared transceiver module that provides the interface between logic and infrared (IR) signals for through air, serial, half-duplex IR data link. It is designed to interface to input/output logic circuits as low as 1.5V. The module is compliant to IrDA Physical Layer Specifications version 1.4 Low Power from 9.6 kbit/s to 115.2 kbit/s with extended link distance and it is IEC 825-Class 1 eye safe.

The HSDL-3209 can be shutdown completely to achieve very low power consumption. In the shutdown mode, the PIN diode will be inactive and thus producing very little photocurrent even under very bright ambient light. Such features are ideal for battery operated handheld products.

Functional Block Diagram

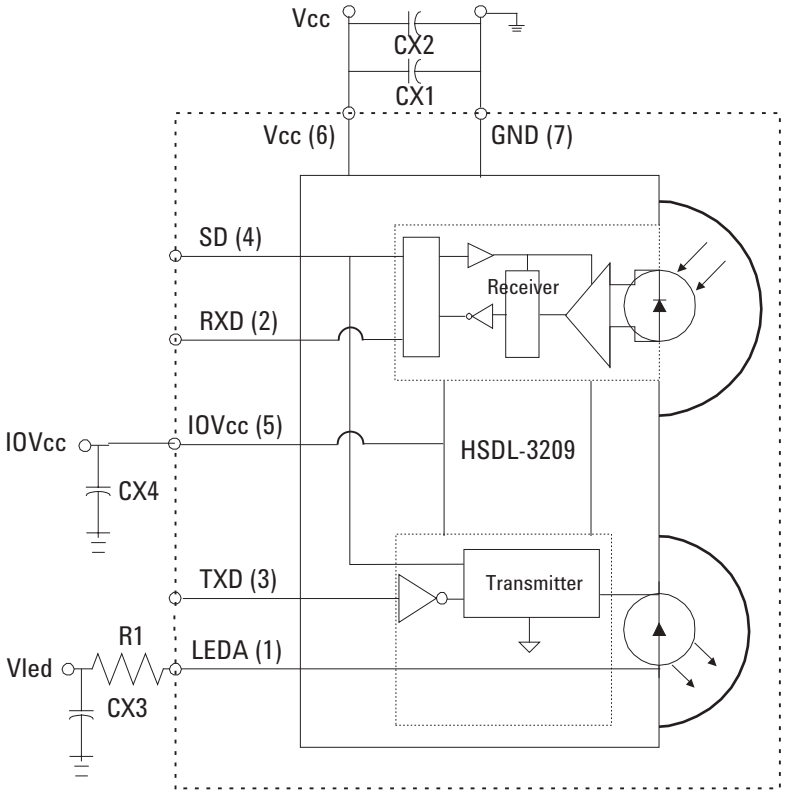


Figure 1. Functional Block Diagram

Features

- **Fully Compliant to IrDA 1.4 Low Power Specification from 9.6 kbit/s to 115.2 kbit/s**
- **Miniature Package**
  - **Height : 1.60 mm**
  - **Width : 7.00 mm**
  - **Depth : 2.80 mm**
- **Guaranteed Temperature Performance, -25 to +70 °C**
  - **Critical parameters are guaranteed over temperature & supply voltage**
- **Low Power Consumption**
  - **Complete shutdown of TXD, RXD, and PIN diode**
- **Vcc Supply 2.4 to 3.6 Volts**
- **Interface to Input/Output Logic Circuits as Low as 1.5V**
- **LED Stuck-High Protection**
- **Designed to Accommodate Light Loss with Cosmetic Windows**
- **IEC 825-Class 1 Eye Safe**

Applications

- **Mobile Telecom**
  - **Mobile Phones**
  - **Pagers**
  - **Smart Phone**
- **Data Communication**
  - **PDAs**
  - **Portable Printers**
- **Digital Imaging**
  - **Digital Cameras**
  - **Photo-Imaging Printers**
- **Electronic Wallet**

Agilent Technologies

Order Information

Part Number	Packaging Type	Package	Quantity
HSDL-3209-021	Tape and Reel	Front View	2500

I/O Pins Configuration Table

Pin	Symbol	Description	I/O Type	Function
1	LED A	LED Anode	Input	Tied through external resistor, R1, to VLED from 2.4V to 4.5V. Please refer to Table 1 for VLED versus Series Resistor, R1.
2	RXD	Receive Data	Output, Active Low	This pin is capable of driving a standard CMOS or TTL load. No external pull-up or pull down resistor is required. It is in tri-state mode when the transceiver is in shutdown mode.
3	TXD	Transmit Data	Input, Active High	This pin is used to transmit serial data when SD pin is low. If held high longer than ~ 50µs, the LED will be turned off.
4	SD	Shutdown	Input, Active High	The transceiver is in shutdown mode if this pin is high
5	IOVcc	Input/Output ASIC Vcc	Input/Output Active High	Connect to ASIC logic controller Vcc Voltage as low as 1.5V.
6	Vcc	Supply Voltage	Supply Voltage	Regulated, 2.4 to 3.6 Volts.
7	GND	Ground	Ground	Connect to system ground.

Recommended Application Circuit Components

Component	Recommended Value	Note
R1	15Ω±5%, 0.0625 Watt for 2.4 ≤ Vled ≤ 2.7V 27Ω±5%, 0.0625 Watt for 2.7 < Vled ≤ 3.6V 36Ω±5%, 0.0625 Watt for 3.6 < Vled ≤ 4.5V	
CX1, CX4	0.47 µF ± 20%, X7R Ceramic	1
CX2, CX3	6.8 µF ± 20%, X7R Ceramic or Tantalum	1

Notes:
1. CX1, CX2, CX3 and CX4 must be placed within 0.7 cm of the HSDL-3209 to obtain optimum noise immunity.

CAUTIONS: The CMOS inherent to the design of this component increases the component's susceptibility to damage from the electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD

Absolute Maximum Ratings

For implementations where case to ambient thermal resistance is ≤ 50°C/W.

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+100	°C	
Operating Temperature	T_A	-25	85	°C	
LED Anode Voltage	V_{LEDA}	0	6.5	V	
Supply Voltage	V_{CC}	0	6.5	V	
Input/Output Voltage	IO_{VCC}	0	V_{CC}	V	
Input Voltage : SD	$V_{I(SD)}$	0	IOV_{CC}	V	
Input Voltage : TXD	$V_{I(TXD)}$	0	IOV_{CC}	V	
DC LED Transmit Current	I_{LED} (DC)		50	mA	
Peak LED Transmit Current	I_{LED} (PK)		250	mA	2

Notes:
2. ≤ 20% duty cycle, ≤ 90 ms pulse width.

Recommended Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Temperature		T_A	-25		70	°C	
Supply Voltage		V_{CC}	2.4		3.6	V	
Input/Output Voltage		IOV_{CC}	1.5		VCC	V	
Logic Input Voltage for TXD/SD	Logic High	V_{IH}	IOVcc-0.2		IOVcc	V	The minimum input logic voltage should not be lower than 1.5V
	Logic Low	V_{IL}	0		0.4	V	
Receiver Input Irradiance	Logic High	EI_H	0.0081		500	mW/cm^2	For in-band signals ≤ 115.2kbit/s [3]
	Logic Low	EI_L			1.0	$\mu W/cm^2$	For in-band signals [3]
LED (Logic High) Current Pulse Amplitude		I_{LEDA}		50		mA	
Receiver Data Rate			9.6		115.2	kbit/s	
Ambient Light	See IrDA Serial Infrared Physical Layer Link Specification, Appendix A for ambient levels						

Notes:
3. An in-band optical signal is a pulse/sequence where the peak wavelength, λp, is defined as 850 ≤ λp ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification v1.4.

Electrical & Optical Specifications

Specifications (Min. & Max. values) hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range. All typical values (Typ.) are at 25°C with Vcc set to 3.0V and IOVcc set to 1.8V unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Receiver							
Viewing Angle		$2\theta_{1/2}$	30			°	
Peak Sensitivity Wavelength		λp		880		nm	
RXD Output Voltage	Logic High	V_{OH}	IOVcc-0.2		IOVcc	V	I_{OH} = -200 µA, EI ≤ 1.0 µW/cm2
	Logic Low	V_{OL}	0		0.4	V	I_{OL} = 200 µA, EI ≥ 8.1 µW/cm2
RXD Pulse Width (SIR) [4]		t_{PW} (SIR)	1		4.0	µs	$\theta_{1/2} \leq 15°$, CL =9 pF
RXD Rise and Fall Times		t_r, t_f		60		ns	CL =9 pF
Receiver Latency Time [5]		t_L		50		µs	
Receiver Wake Up Time [6]		t_W		100		µs	
Transmitter							
Radiant Intensity		IE_H	4	14		mW/sr	I_{LEDA}= 50 mA, $\theta_{1/2} \leq 15°$, $V_{TXD} \geq V_{IH}$ T_A=25 °C, IOVcc = 1.8V
Viewing Angle		$2\theta_{1/2}$	30		60	°	
Peak Wavelength		λp		875		nm	
Spectral Line Half Width		$\Delta\lambda 1/2$		35		nm	
TXD Input Current	High	I_H		0.02	10	µA	$V_I \geq V_{IH}$
	Low	I_L	-10	-0.02	10	µA	$0 \leq V_I \leq V_{IL}$
LED Current	On	I_{VLED}		50		mA	V_I(TXD) ≥ V_{IH}
	Shutdown	I_{VLED}			200	nA	$V_{I(SD)} \geq V_{IH}$
Optical Pulse Width (SIR)		t_{PW} (SIR)	1.4	1.6	1.8	µs	t_{PW} (TXD) = 1.6 µs at 115.2 kbit/s
Maximum Optical PW [7]		t_{PW}(max.)			100	µs	
TXD Rise and fall Time (Optical)		tr, tf			600	ns	tpw(TXD) = 1.6 µs
LED Anode On State Voltage		$V_{ON(LEDA)}$		1.55	1.8	V	I_{LEDA}=50mA, $V_{I(TXD)} \geq V_{IH}$
Transceiver							
Supply Current	Shutdown [8]	I_{CC1}			1	µA	$V_{SD} \geq V_{IH}$, T_A=25°C
	Idle	I_{CC2}		100		µA	$V_{I(TXD)} \leq V_{IL}$, EI = 0

Notes:

4. For in-band signals from 9.6kbit/s to 115.2 kbit/s, where $9\mu W/cm^2 \leq EI \leq 500mW/cm^2$.
5. Latency time is defined as the time from the last TxD light output pulse until the receiver has recovered full sensitivity
6. Receiver wake up time is measured from Vcc power on or SD pin high to low transition to a valid RXD output.
7. The maximum optical PW is the maximum time the LED remains on when the TXD is constantly high. This is to prevent long turn on time of the LED for eye safety protection.
8. For V_{cc} > 3V and IOV_{cc} < 1.8V, I_{CC1} can exceed 15uA.

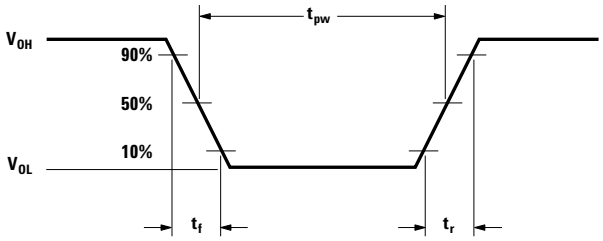


Figure 2. RXD output waveform.

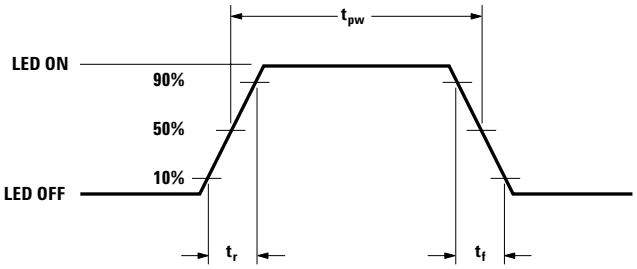


Figure 3. LED optical waveform.

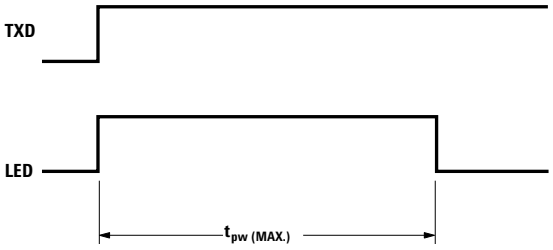


Figure 4. TXD "stuck on" protection waveform.

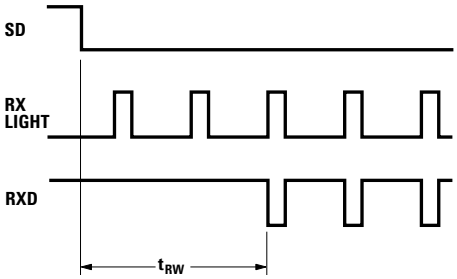


Figure 5. Receiver wakeup time waveform.

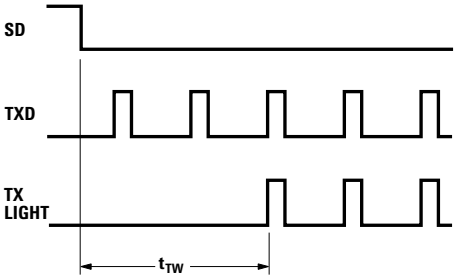


Figure 6. TXD wakeup time waveform.

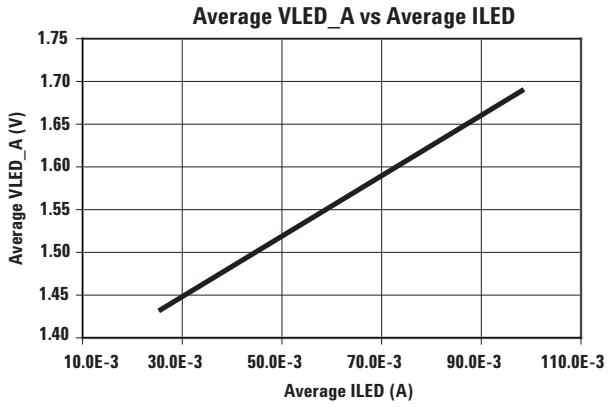


Figure 7. V_{LED} vs. I_{LED}

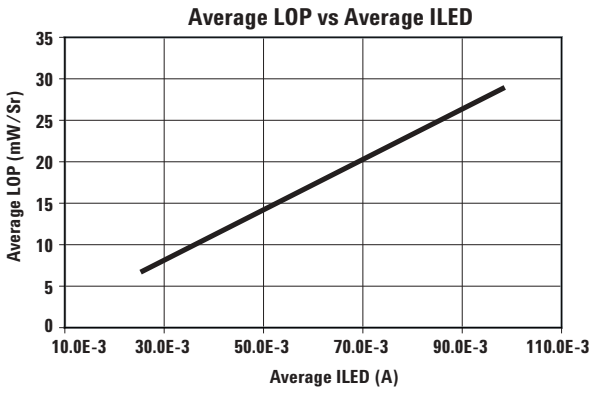
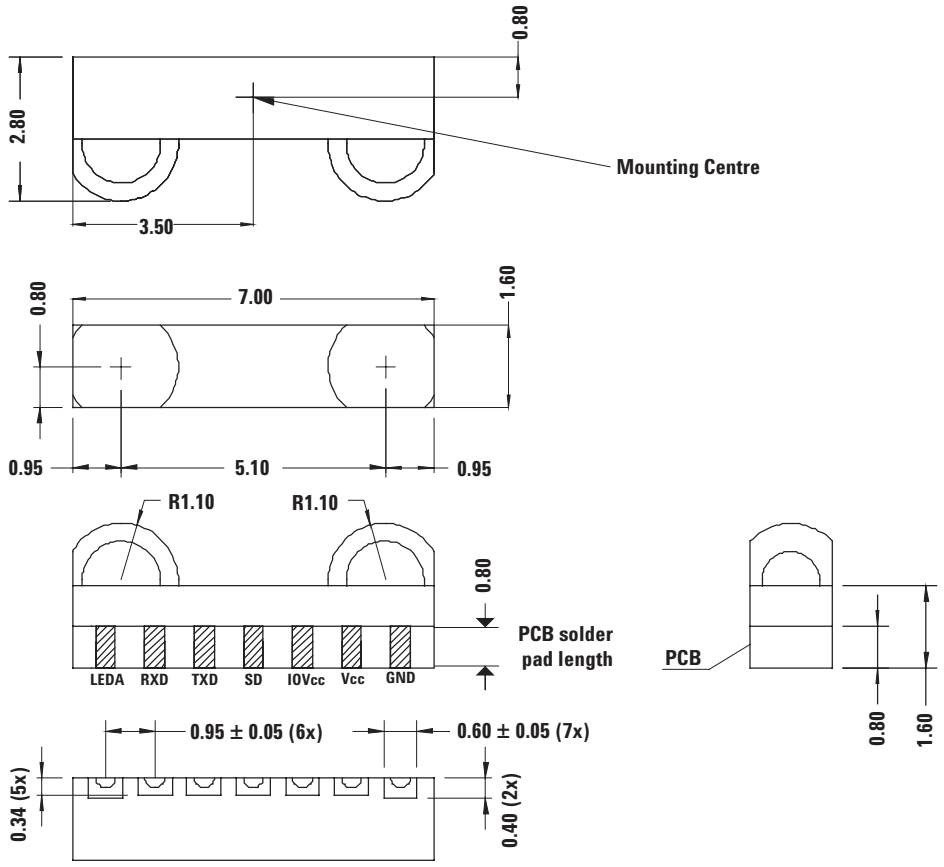


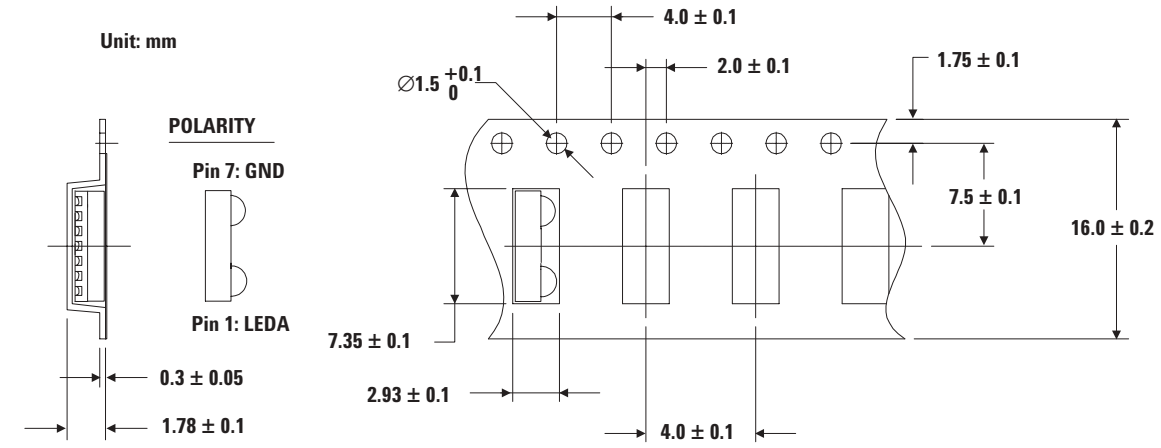
Figure 8. V_{LOP} vs. I_{LED}

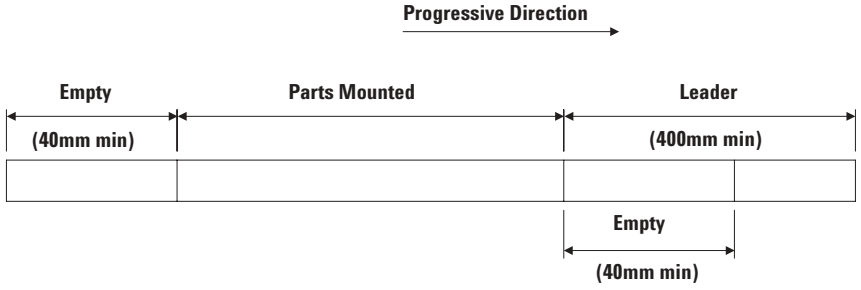
HSDL-3209 Package Outline with Mechanical Dimensions



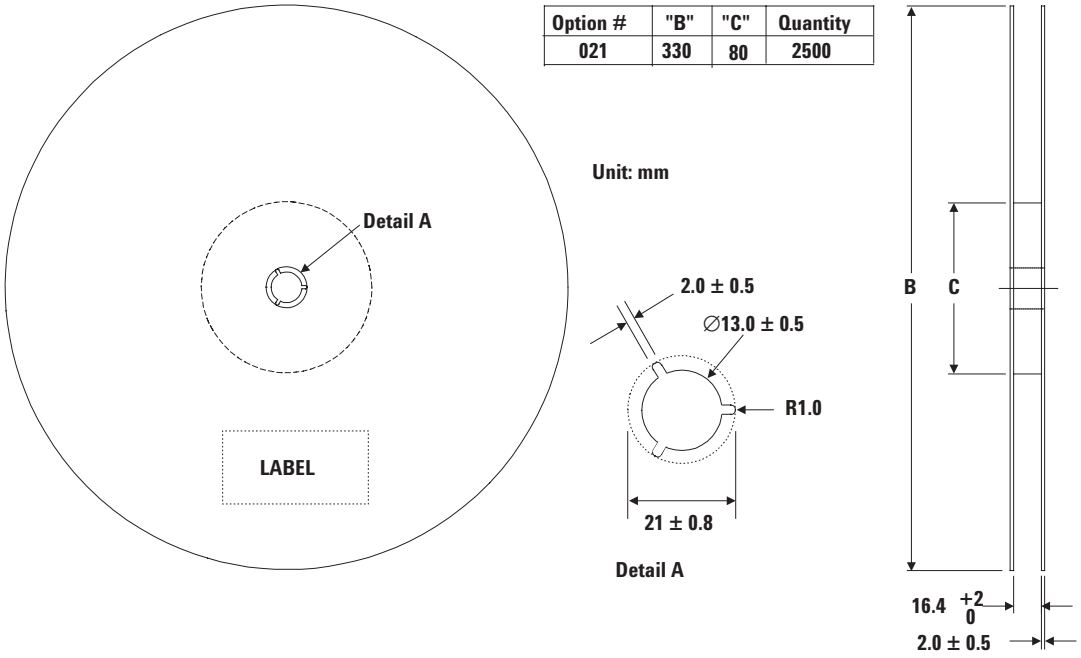
Notes :
1. ALL DIMENSIONS IN MILLIMETERS (mm).
2. DIMENSION TOLERANCE IS 0.2mm UNLESS OTHERWISE SPECIFIED.

HSDL-3209 Tape and Reel Dimensions



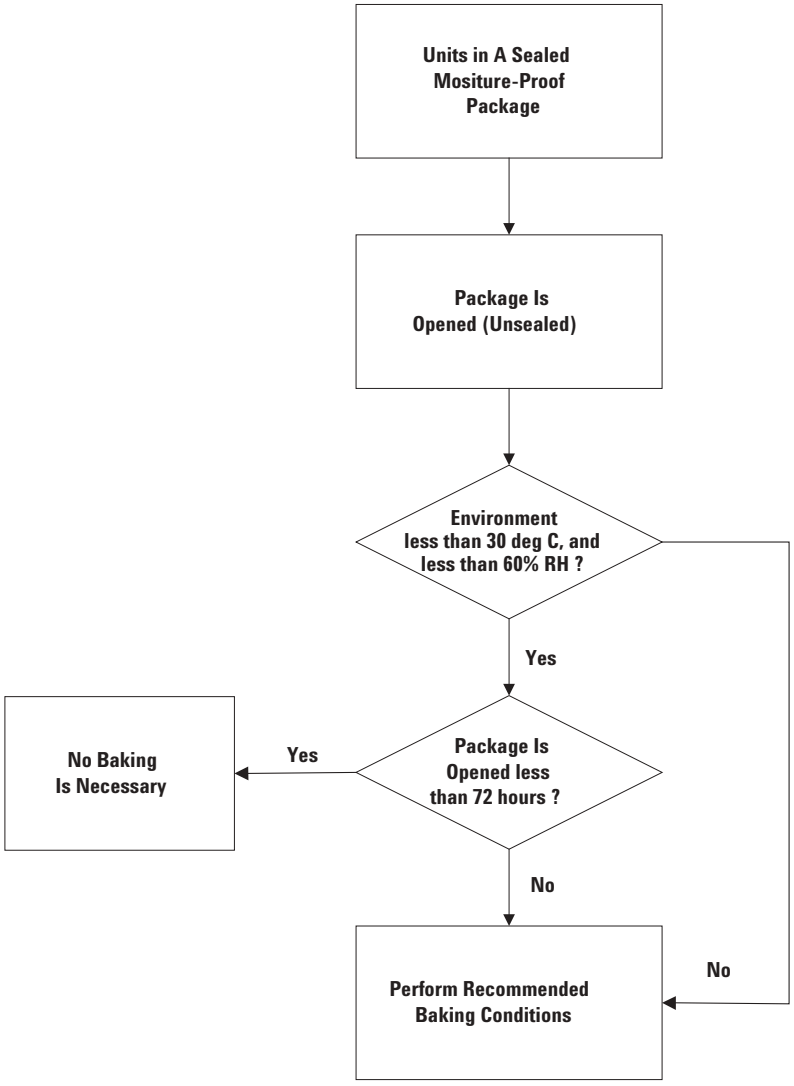


Option #	"B"	"C"	Quantity
021	330	80	2500



Moisture Proof Packaging

All HSDL-3209 options are shipped in moisture proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC Level 4.



Baking Conditions:

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Baking should only be done once.

Package	Temperature	Time
In Reel	60°C	≥ 48 hours
In Bulk	100°C	≥ 4 hours
	125°C	≥ 2 hours
	150°C	≥ 1 hours

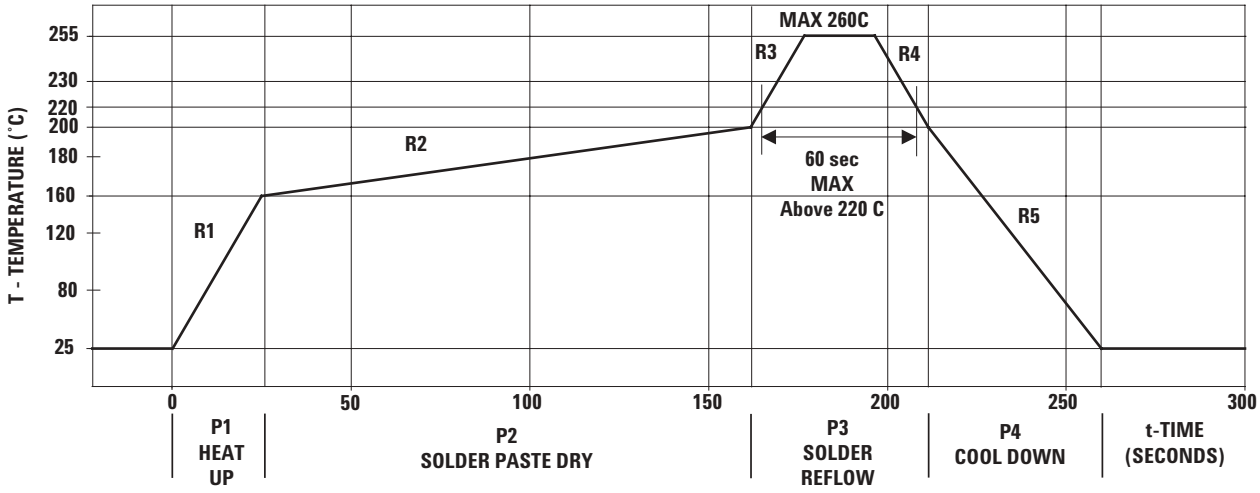
Recommended Storage Conditions:

Time from unsealing to soldering:

After removal from the bag, the parts should be soldered within 72 hours if stored at the recommended storage conditions. If times longer than 72 hours are needed, the parts must be stored in a dry box.

Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Recommended Reflow Profile



Process Zone	Symbol	DT	Maximum ΔT/Δtime
Heat Up	P1, R1	25°C to 160°C	4°C/s
Solder Paste Dry	P2, R2	160°C to 200°C	0.5°C/s
Solder Reflow	P3, R3 P3, R4	200°C to 255°C (260°C at 10 seconds max) 255°C to 200°C	4°C/s -6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different DT/Dtime temperature change rates. The DT/Dtime rates are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In process zone P1, the PC board and HSDL-3209 castellation pins are heated to a temperature of 160°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 4°C per second to allow for even heating of both the PC board and HSDL-3209 castellations.

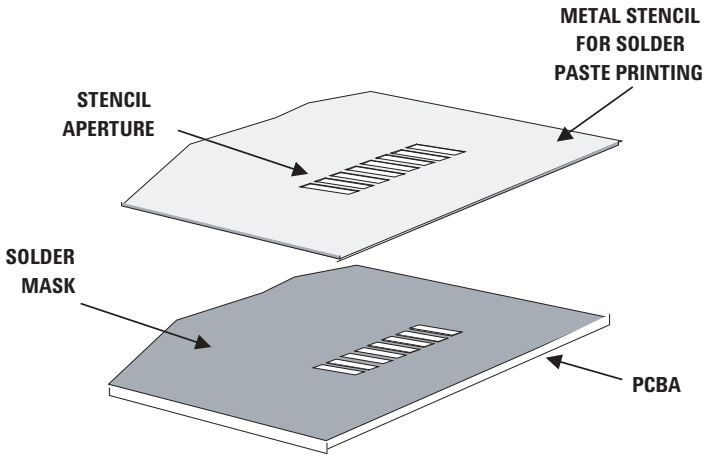
Process zone P2 should be of sufficient time duration (60 to 120 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 200°C (392°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 255°C (491°F) for optimum results. The dwell time above the liquidus point of solder should be between 20 and 60 seconds. It usually takes about 20 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 60 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 200°C (392°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and HSDL-3209 castellations to change dimensions evenly, putting minimal stresses on the HSDL-3209 transceiver.

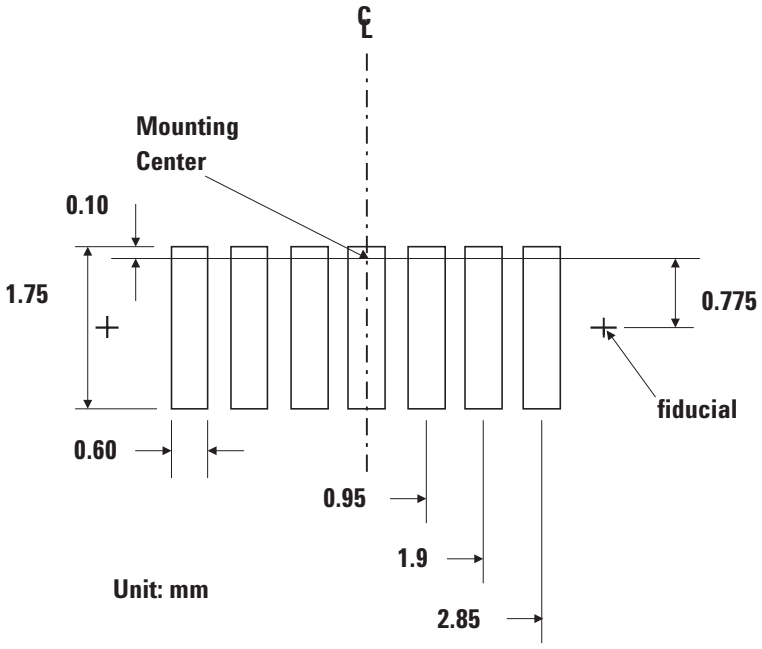
Appendix A: SMT Assembly Application Note

1.0 Solder Pad, Mask and Metal Stencil Aperture



Stencil and PCBA

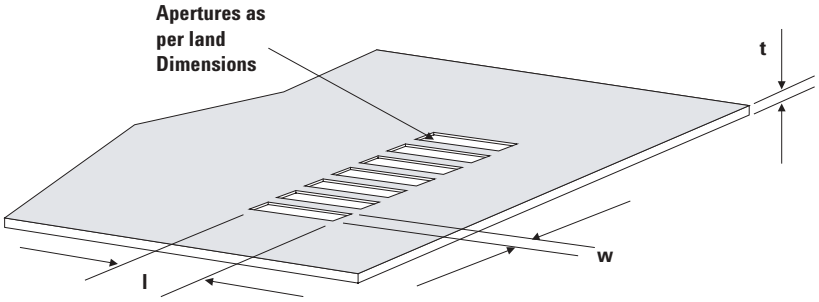
1.1 Recommended Land Pattern



1.2 Recommended Metal Solder Stencil Aperture

It is recommended that only a 0.152 mm (0.006 inches) or a 0.127 mm (0.005 inches) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. See the table below the drawing for combinations of metal stencil aperture and metal stencil thickness that should be used.

Aperture opening for shield pad is 2.7 mm x 1.25 mm as per land pattern.

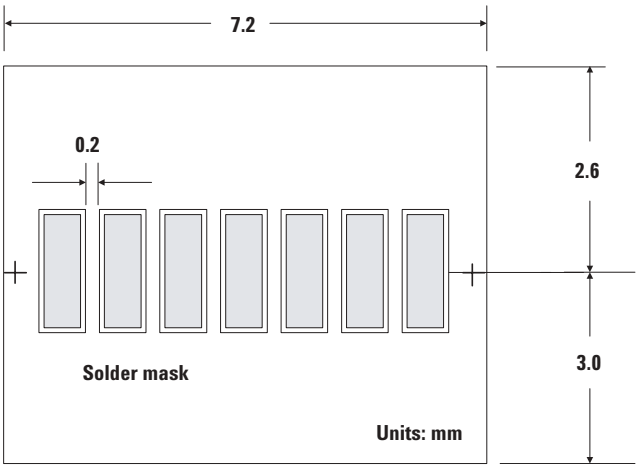


Stencil Thickness, t (mm)	Aperture size (mm)	
	Length, l (mm)	Width, w (mm)
0.152 mm	2.60 ± 0.05	0.55 ± 0.05
0.127 mm	3.00 ± 0.05	0.55 ± 0.05

1.3 Adjacent Land Keepout and Solder Mask Areas

Adjacent land keep-out is the maximum space occupied by the unit relative to the land pattern. There should be no other SMD components within this area. The minimum solder resist strip width required to avoid solder bridging adjacent pads is 0.2 mm. It is recommended that two fiducial crosses be place at midlength of the pads for unit alignment.

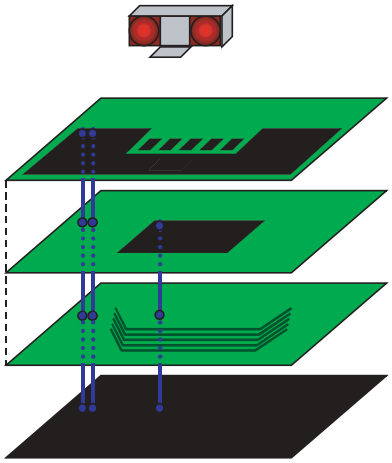
Note: Wet/Liquid Photo-Imageable solder resist/mask is recommended.



Appendix B: PCB Layout Suggestion

The HSDL 3209 is a shieldless part and hence does not contain a shield trace unlike the other transceivers. The following PCB layout guidelines should be followed to obtain a good PSRR and EM immunity resulting in good electrical performance. Things to note:

1. The ground plane should be continuous under the part.
2. VLED can be connected to either unfiltered or unregulated power supply. If VLED and Vcc share the same power supply, CX3 need not be used and the connections for CX1 and CX2 should be before the current limiting resistor R1. CX1 is generally a ceramic capacitor of low inductance providing a wide frequency response while CX2 and CX3 are tantalum capacitors of big volume and fast frequency response. The use of a tantalum capacitor is more critical on the VLED line, which carries a high current. CX4 is an optional ceramic capacitor, similar to CX1, for the IOVcc line.
3. Preferably a multi-layered board should be used to provide sufficient ground plane. Use the layer underneath and near the transceiver module as Vcc, and sandwich that layer between ground connected board layers. Refer to the diagram below for an example of a 4 layer board,



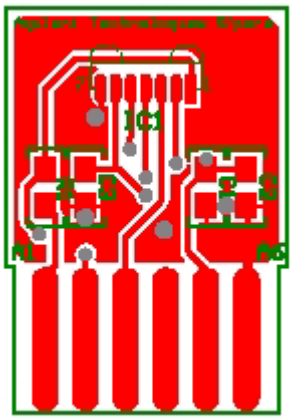
Top layer
Connect the metal shield & module ground pin to bottom ground layer

Layer 2
Critical ground plane zone. Do not connect directly to the module ground pin

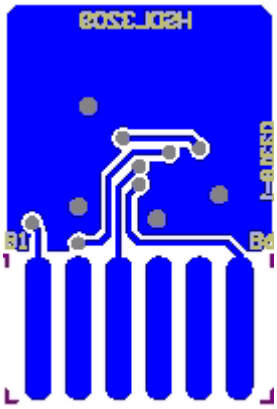
Layer 3
Keep data bus away from critical ground plane zone

Bottom layer
(GND)

The area underneath the module at the second layer, and 3cm in all direction around the module is defined as the critical ground plane zone. The ground plane should be maximized in this zone. Refer to application note AN1114 or the Agilent IrDA Data Link Design Guide for details. The layout below is based on a 2-layer PCB.



Top View



Bottom View

Appendix C: General Application Guide for the HSDL-3209

Description The HSDL-3209, a low-cost and ultra-small form factor infrared transceiver, is designed to address the mobile computing market such as PDAs, as well as small embedded mobile products such as digital cameras and cellular phones. It is fully compliant to IrDA 1.4 low power specification from 9.6 kb/s to 115.2 kb/s, and supports HP-SIR and TV Remotes modes. The design of the HSDL-3209 also includes the following unique features:

- Low passive component count.
- Shutdown mode for low power consumption requirement.

Selection of Resistor R1 Resistor R1 should be selected to provide the appropriate peak pulse LED current over different ranges of Vcc as shown on page 2 under "Recommended Application Circuit Components".

Interface to Recommended I/O chips The HSDL-3209's TXD data input is buffered to allow for CMOS drive levels. No peaking circuit or capacitor is required. Data rate from 9.6 kb/s up to 115.2 kb/s is available at the RXD pin.

Figure 10 shows how the IrDA port fits into a mobile phone and PDA platform.

The link distance testing was done using typical HSDL-3209 units with SMC's FDC37C669 and FDC37N769 Super I/O controllers. An IrDA link distance of up to 50 cm was demonstrated.

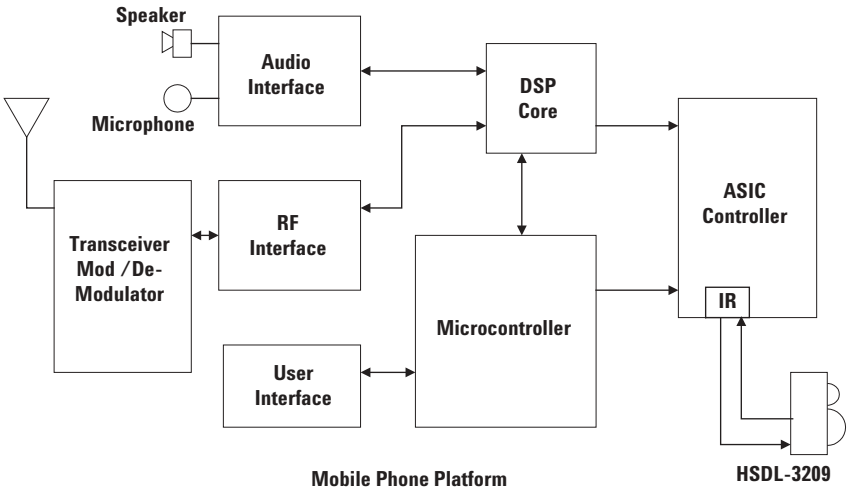


Figure 9. Mobile phone platform

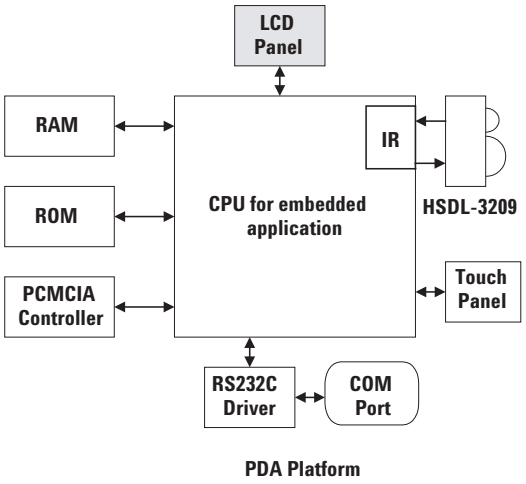


Figure 10. PDA platform

Appendix D: Window Designs for HSDL-3209

Optical Port Dimensions for HSDL-3209

To ensure IrDA compliance, some constraints on the height and width of the window exist. The minimum dimensions ensure that the IrDA cone angles are met without vignetting. The maximum dimensions minimize the effects of stray light. The minimum size corresponds to a cone angle of 30° and the maximum size corresponds to a cone angle of 60°.

In the figure above, X is the width of the window, Y is the height of the window and Z is the distance from the HSDL-3208 to the back of the window. The distance from the center of the LED lens to the center of the photodiode lens, K, is 5.1mm. The equations for computing the window dimensions are as follows:

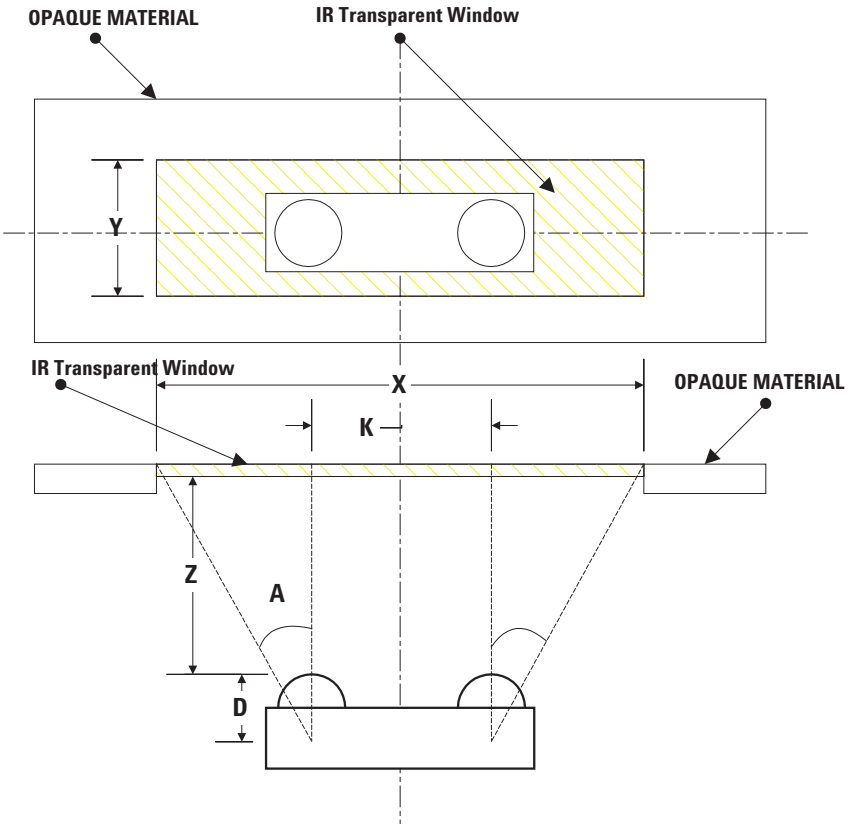
X = K + 2*(Z+D)*tanA

Y = 2*(Z+D)*tanA

The above equations assume that the thickness of the window is negligible compared to the distance of the module from the back of the window (Z). If they are comparable, Z' replaces Z in the above equation. Z' is defined as

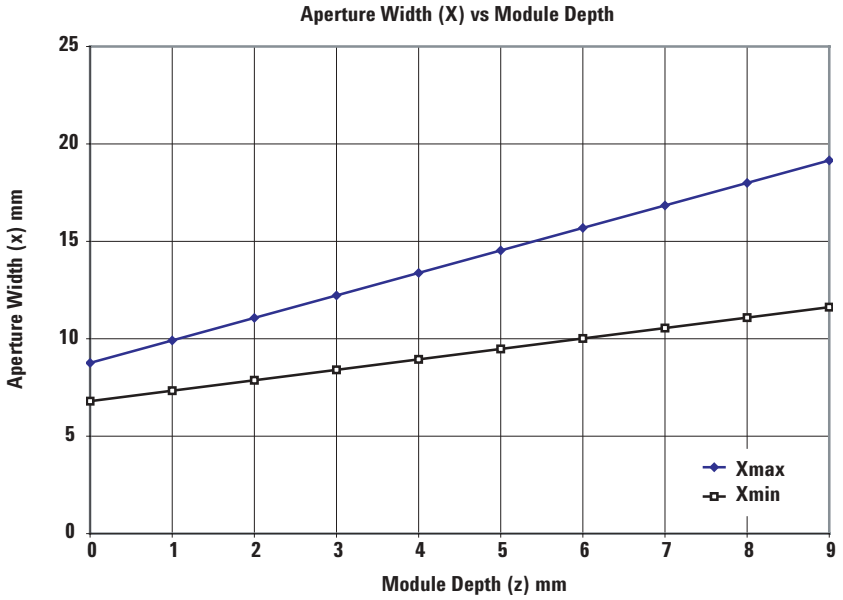
Z'=Z+t/n

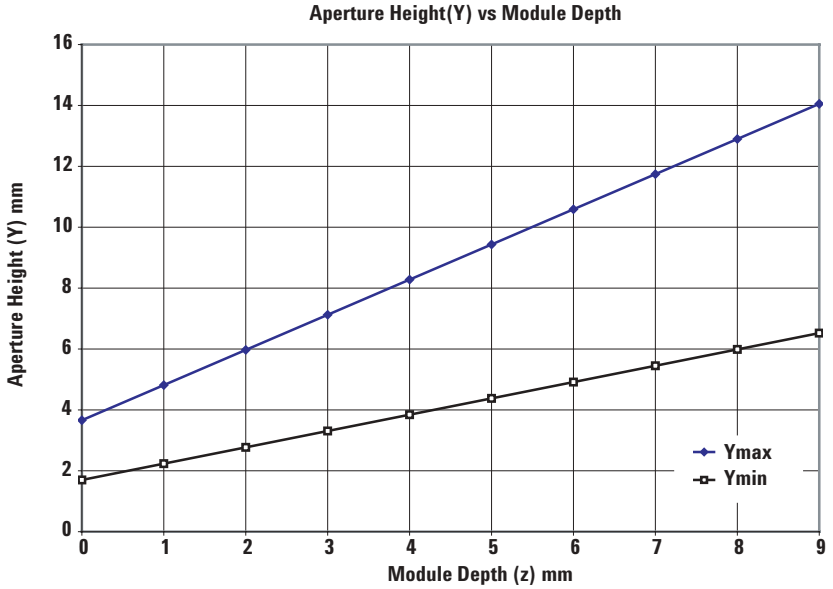
where 't' is the thickness of the window and 'n' is the refractive index of the window material.



The depth of the LED image inside the HSDL-3208, D, is 3.17mm. 'A' is the required half angle for viewing. For IrDA compliance, the minimum is 15° and the maximum is 30°. Assuming the thickness of the window to be negligible, the equations result in the following tables and graphs:

Module Depth (z) mm	Aperture Width (x, mm)		Aperture height (y, mm)	
	Max	min	Max	Min
0	8.76	6.80	3.66	1.70
1	9.92	7.33	4.82	2.33
2	11.07	7.87	5.97	2.77
3	12.22	8.41	7.12	3.31
4	13.38	8.94	8.28	3.84
5	14.53	9.48	9.43	4.38
6	15.69	10.01	10.59	4.91
7	16.84	10.55	11.74	5.45
8	18.00	11.09	12.90	5.99
9	19.15	11.62	14.05	6.52





Window Material

Almost any plastic material will work as a window material. Polycarbonate is recommended. The surface finish of the plastic should be smooth, without any texture. An IR filter dye may be used in the window to make it look black to the eye, but the total optical loss of the window should be 10% or less for best optical performance. Light loss should be measured at 875 nm.

The recommended plastic materials for use as a cosmetic window are available from General Electric Plastics.

Recommended Plastic Materials:

Material #	Light Transmission	Haze	Refractive Index
Lexan 141	88%	1%	1.586
Lexan 920A	85%	1%	1.586
Lexan 940A	85%	1%	1.586

Note: 920A and 940A are more flame retardant than 141.
Recommended Dye: Violet #21051 (IR transmissant above 625 nm)

Shape of the Window

From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode.

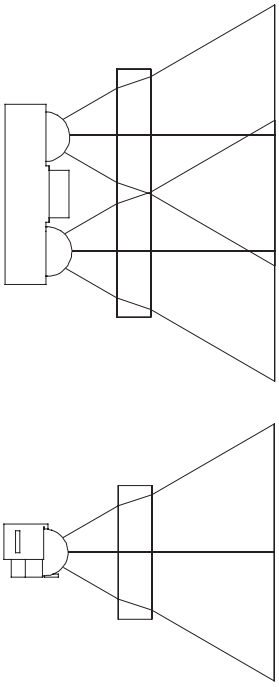
If the window must be curved for mechanical or industrial design reasons, place the same curve on the back side of the window that has an identical radius as the front side.

While this will not completely eliminate the lens effect of the front curved surface, it will significantly reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve.

The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back surface of the window is 3 mm.

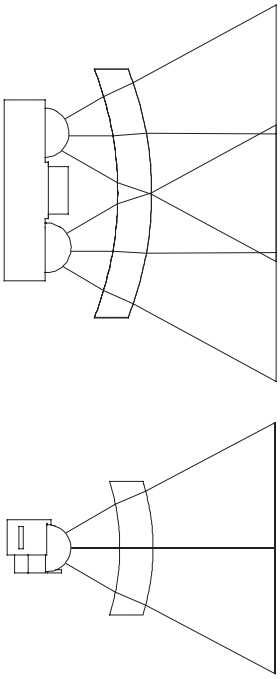
Flat Window

(First choice)



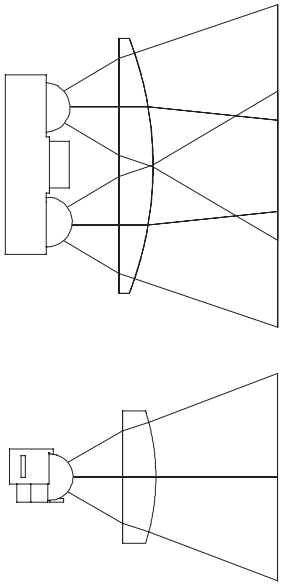
Curved Front and Back

(Second choice)



Curved Front, Flat Back

(Do not use)



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