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Z86295

HDD MICROCONTROLLER WITH ENHANCED DSP SERVO CONTROL

FEATURES

Part	RAM (Kbyte)	Speed (MHz)
Z86295	256	40

*General Purpose

- ROMless
- 100-Pin VQFP
- 0°C to 70°C Temperature Range
- 4.5 to 5.5 Volt Operation Range
- 10-Bit Digital-to-Analog Converter (DAC)
- Programmable Servo Timer
- Z8® Microcontroller
- 16-Bit Digital Signal Processor (DSP)
- Six-Channel, 10-Bit Analog-to-Digital Converter (ADC)

GENERAL DESCRIPTION

The Z86295 microcontroller with enhanced DSP servo control provides system-level integration that enhances a variety of end-user applications. In addition to the industry-standard Z8 MCU, the Z86295 features an enhanced 16-bit DSP, a servo control timing generator, a six-channel 10-bit Analog-to-Digital Converter (ADC), and a 10-bit Digital-to-Analog Converter (DAC).

The DSP provides the necessary calculations for servo control. The Z86295 allows arithmetic operations such as multiplication, addition, subtraction, and a multiply-accumulate of two 16-bit operands. Instruction execution is typically a one-cycle pipeline that is usually performed in one clock cycle.

A mailbox feature provides an efficient communication link between the Z8 and the DSP. When the mailbox register is written to, an interrupt signal is sent to the other processor.

The servo timing processor handles the generation of burst and sector timing, spindle speed control, and detection of servo timing marks. It is fully programmable from the Z8, and can interrupt the Z8 or the DSP. Additionally, selected registers are available to the DSP for servo control.

The built-in 10-bit half-flash ADC and 10-bit DAC eliminates the requirement for additional system level components.

The Z86295 supports numerous power management modes including STOP, HALT, or low power-down of selected blocks. The Z86295 can be used to power-down external components such as the Read channel.

Note: All Signals with an overline, "‾", are active Low. For example: B/$\overline{W}$, in which WORD is active Low; or $\overline{B}$/W, in which BYTE is active Low.

GENERAL DESCRIPTION (Continued)

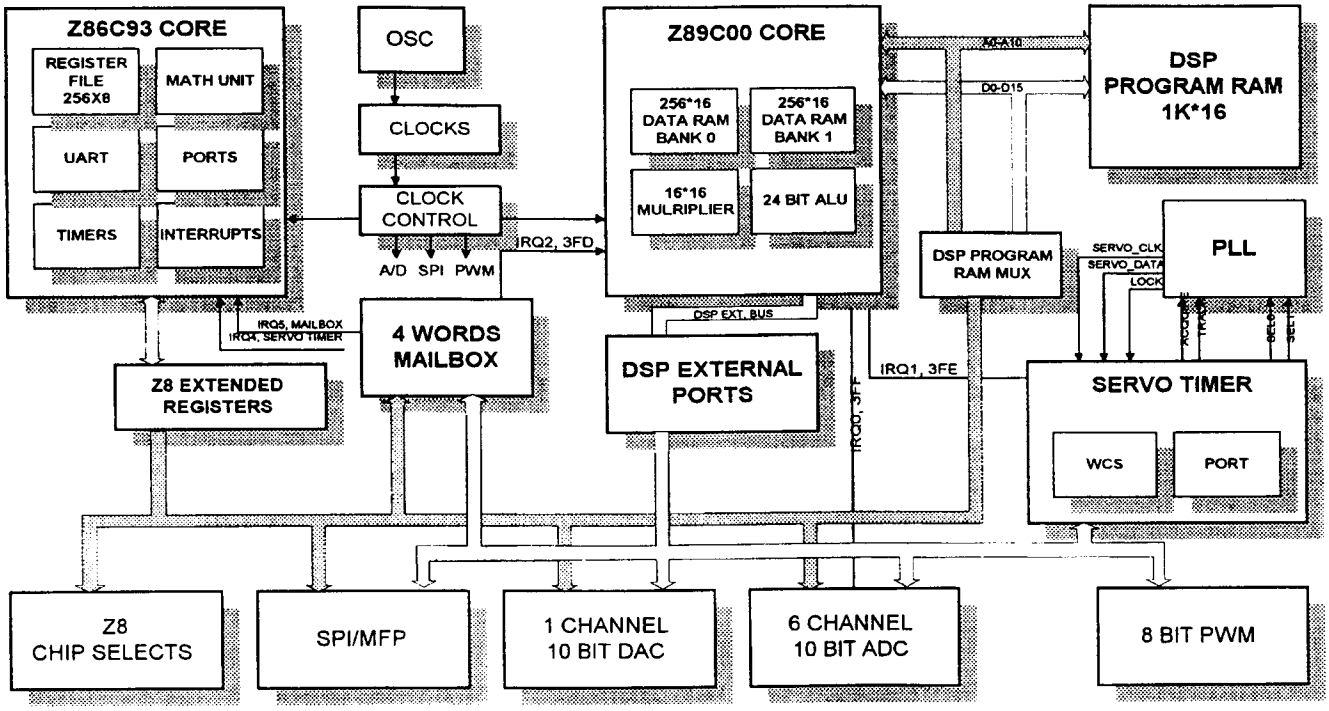

Figure 1. Z86295 Functional Block Diagram

PIN DESCRIPTION

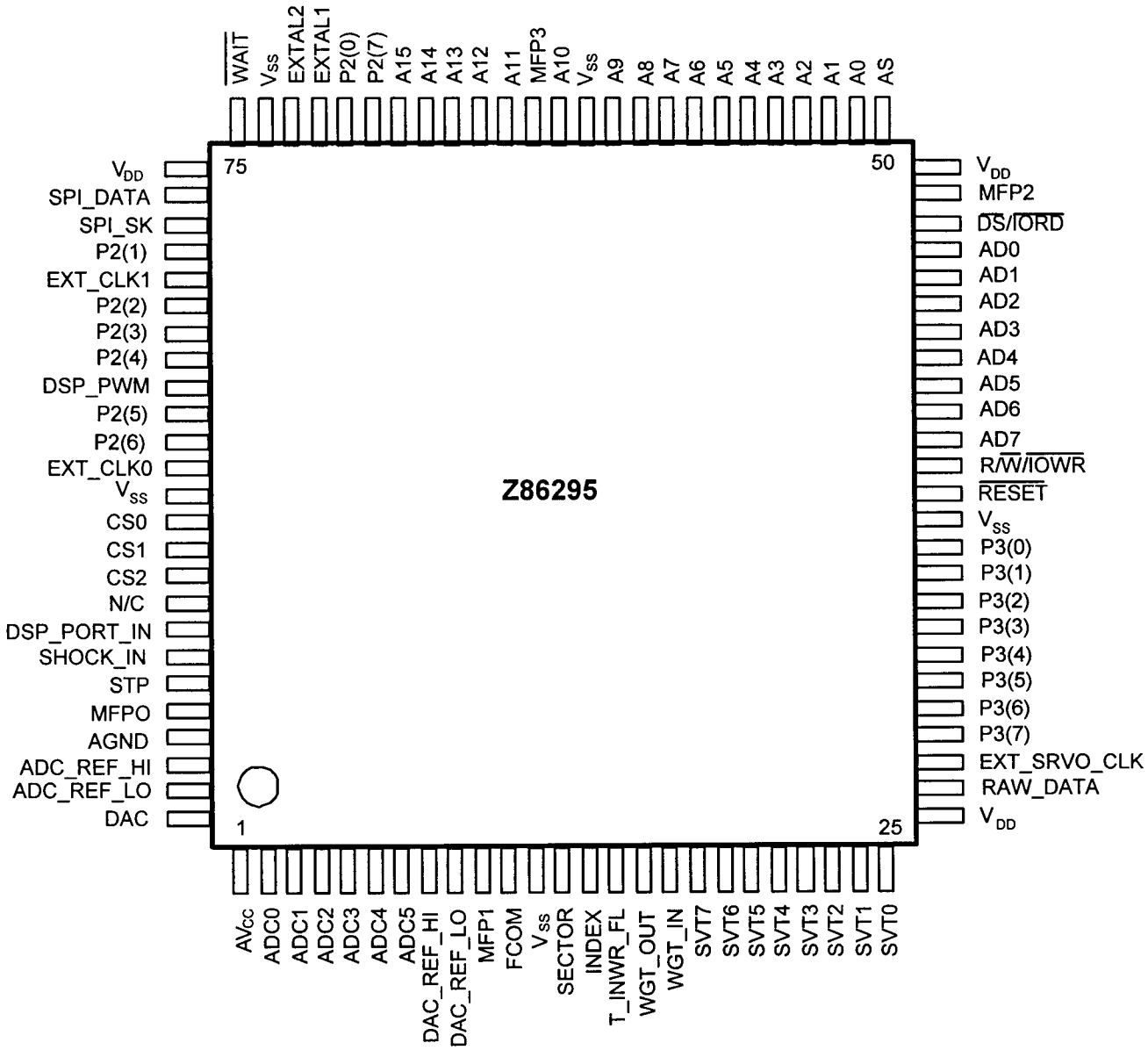

Figure 2. Z86295 100-Lead VQFP Pin Assignments

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Min	Max	Unit
V_{DD}	Supply Voltage[2]	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	°C
TA	Oper Ambient Temp	0	70	°C

Notes:
1. Voltages on all pins with respect to GND.
2. See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics indicated in the following pages apply for standard test conditions (see Figure 3).

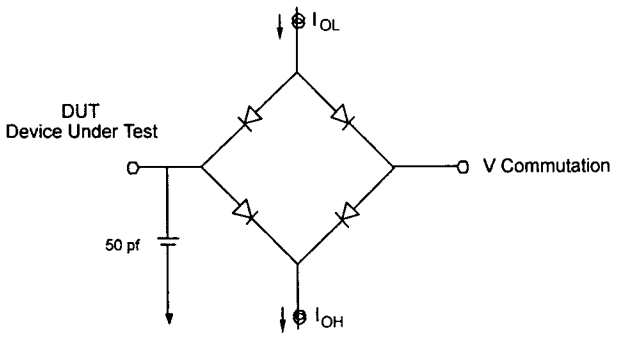

Figure 3. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Sym	Parameter	Min	Max	Units
V_{IH}	Input High Voltage P0/P1/P2	2.00		V
V_{IH}	Input High Voltage P3	2.2		V
V_{IL}	Input Low Voltage		0.80	V
V_{OH}	@ I_{OH} = −2.0 mA	2.40		V
V_{OH}	@ I_{OH} = −100 µA	V_{CC}−100 mV		V
V_{OL}	@ I_{OL} = +5.0 mA		0.40	V
I_{IL}	Input Leakage	−2	+2	µA
I_{OL}	Output Leakage	−2	+2	µA
V_{CH}	Clock Input High Voltage	3.80		V
V_{CL}	Clock Input Low Voltage		0.80	V
V_{RH}	Reset Input High Voltage	3.80		V
V_{RL}	Reset Input Low Voltage		0.80	V
I_{CC}	V_{CC} Supply Current		180	mA @ 40 MHz
I_{CC1}	V_{CC} Supply Current HALT Mode		80	mA @ 40 MHz
I_{CC2}	Reset Input Current		−180	µA
I_{IR}	V_{CC} Supply Current STOP/Pause Mode		5	mA
I_{ALL}	Auto Latch Low Current	−16	16	µA

AC CHARACTERISTICS[1]

40-MHz External I/O or Memory Read/Write;
V_{CC} = 5.0V ± 10%, 0°C–70°C

			40 MHz[2]		
No	**Sym**	**Parameter**	**Min**	**Max**	**Units**
1	TdA(AS)	Address Valid To $\overline{AS}$ Rise Delay	15		ns
2	TdAS(A)	$\overline{AS}$ Rise To Address Hold Time	15		ns
3	TdAS(DI)	$\overline{AS}$ Rise Data In Required Valid Delay		70	ns
4	TwAS	$\overline{AS}$ Low Width	15		ns
5	TdAZ(DSR)	Address Float To $\overline{DS}$ Fall (Read)	0		ns
6	TwDSR	$\overline{DS}$ (Read) Low Width	60		ns
7	TwDSW	$\overline{DS}$ (Write) Low Width	35		ns
8	TdDSR(DI)	$\overline{DS}$ Fall (Read) To Data Required Valid Delay		40	ns
9	ThDSR(DI)	$\overline{DS}$ Rise (Read) to Data In Hold Time	0		ns
10	TdDS(A)	$\overline{DS}$ Rise To Address Active Delay	20		ns
11	TdDS(AS)	$\overline{DS}$ Rise To $\overline{AS}$ Delay	12		ns
12	TdR/W(AS)	R/W To Valid $\overline{AS}$ Rise Delay	10		ns
13	TdDS(R/W)	$\overline{DS}$ Rise To R/W Not Valid Delay	10		ns
14	TdDO(DSW)	Data Out To $\overline{DS}$ Fall (Write) Delay	10		ns
15	ThDSW(DO)	$\overline{DS}$ Rise (Write) To Data Out Hold Time	10		ns
16	TdA(DI)	Address Valid To Data Required Valid Delay		80	ns
17	TdAS(DSR)	$\overline{AS}$ Rise To $\overline{DS}$ Fall (Read) Delay	15		ns
19	TdDM(AS)	$\overline{DM}$ Valid To $\overline{AS}$ Rise Delay	10		ns
20	TdDS(DM)	$\overline{DS}$ Rise To $\overline{DM}$ Valid Delay	10		ns
21	ThDS(A)	$\overline{DS}$ Rise To Address Valid Hold Time	10		ns
22	TdXT(SCR)	XTAL Falling to SCLK Rising		35	ns
23	TdXT(SCF)	XTAL Falling to SCLK Falling		35	ns
24	TdXT(DSRF)	XTAL Falling to $\overline{DS}$ Read Falling		45	ns
25	TdXT(DSRR)	XTAL Falling to $\overline{DS}$ Read Rising		30	ns
26	TdXT(DSWF)	XTAL Falling to $\overline{DS}$ Write Falling		30	ns
27	TdXT(DSWF)	XTAL Falling to $\overline{DS}$ Write Rising		30	ns
28	TsW(XT)	Wait Setup Time	5		ns
29	ThW(XT)	Wait Hold Time	15		ns
30	TwW	Wait Width (One Wait Time)	20		ns

Notes:
1. When using extended memory timing, add 2 TpC. Timing numbers provided are for minimum TpC.
2. Preliminary engineering value, to be characterized.

Timing Diagrams

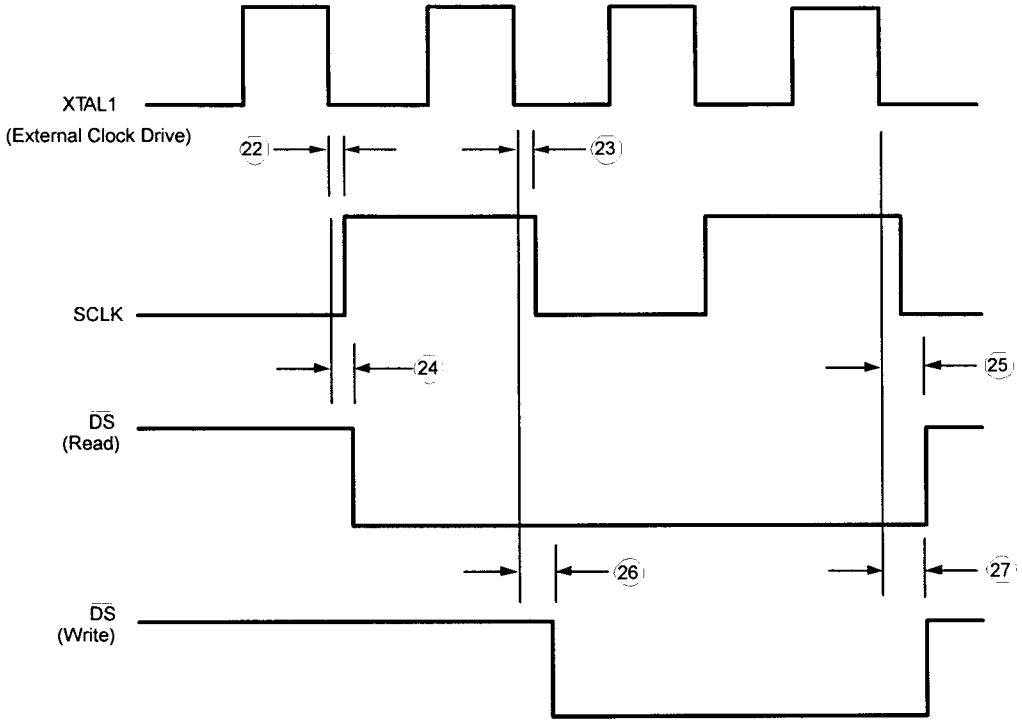

Figure 4. XTAL/SCLK to DSR and DSW Timing

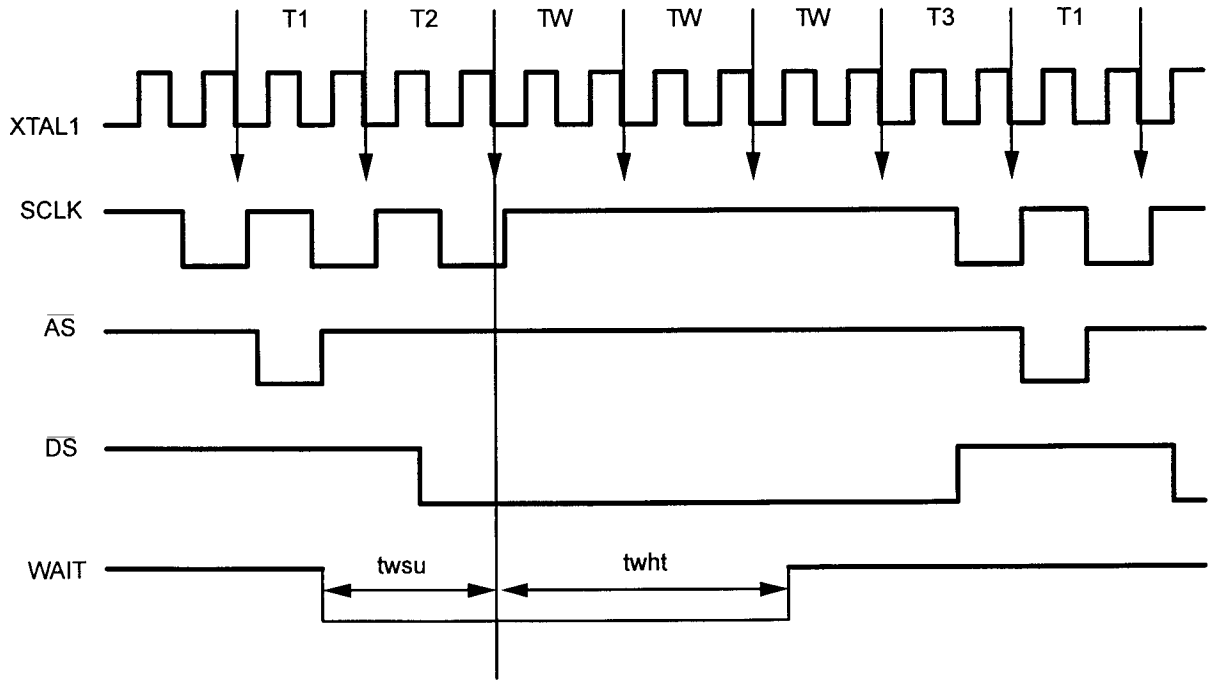

Figure 5. XTAL/SCLK to WAIT Timing

AC CHARACTERISTICS1 (Continued)

Read/Write Timing Diagrams

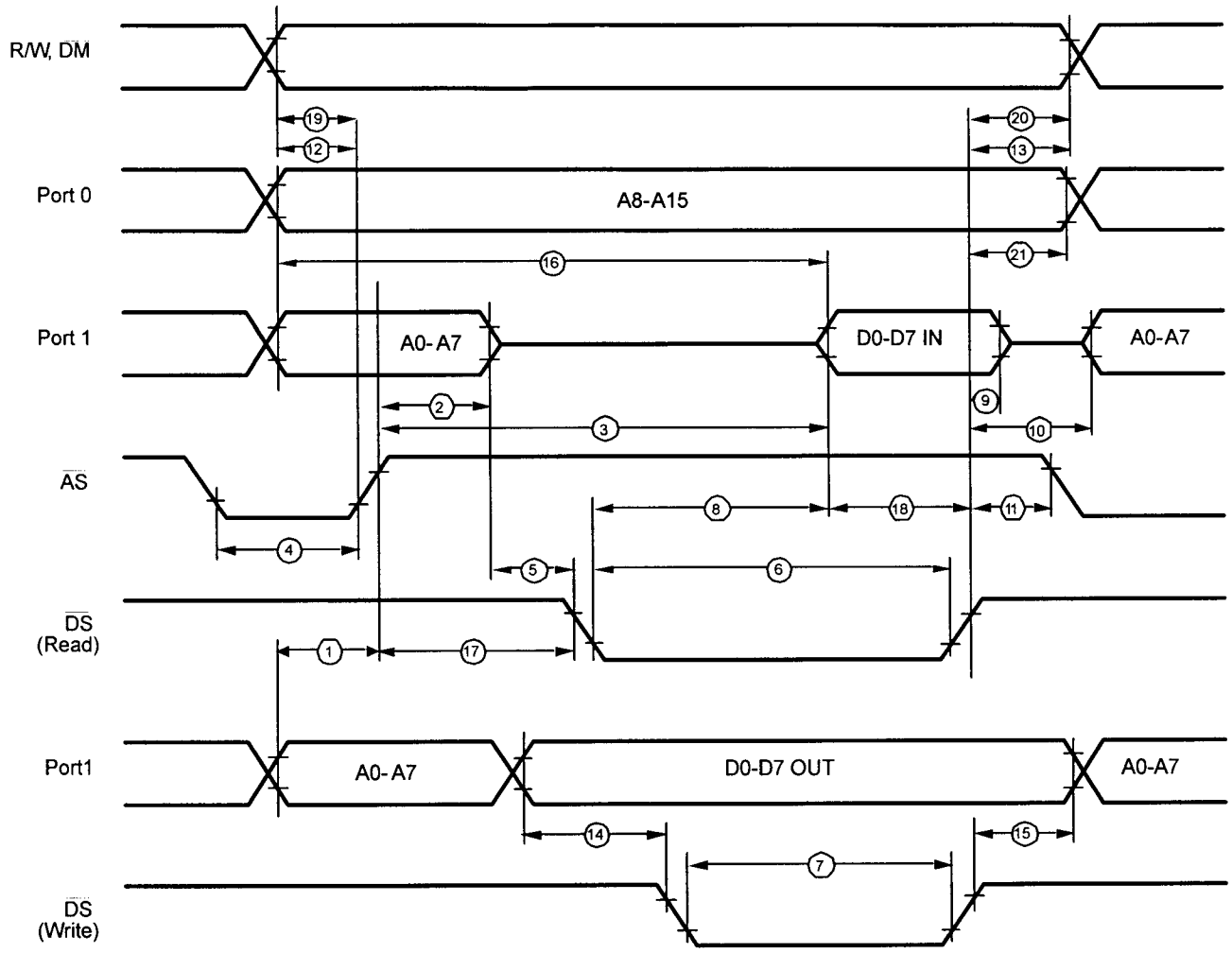

Figure 6. XTAL/SCLK to DSR and DSW Timing

Handshake Timing Diagrams

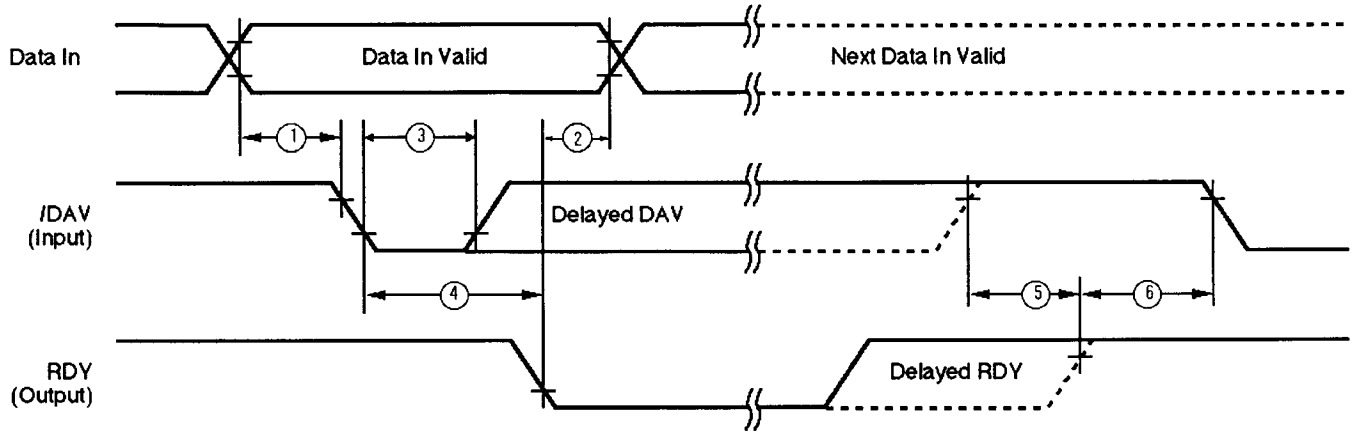

Figure 7. Input Handshake Timing

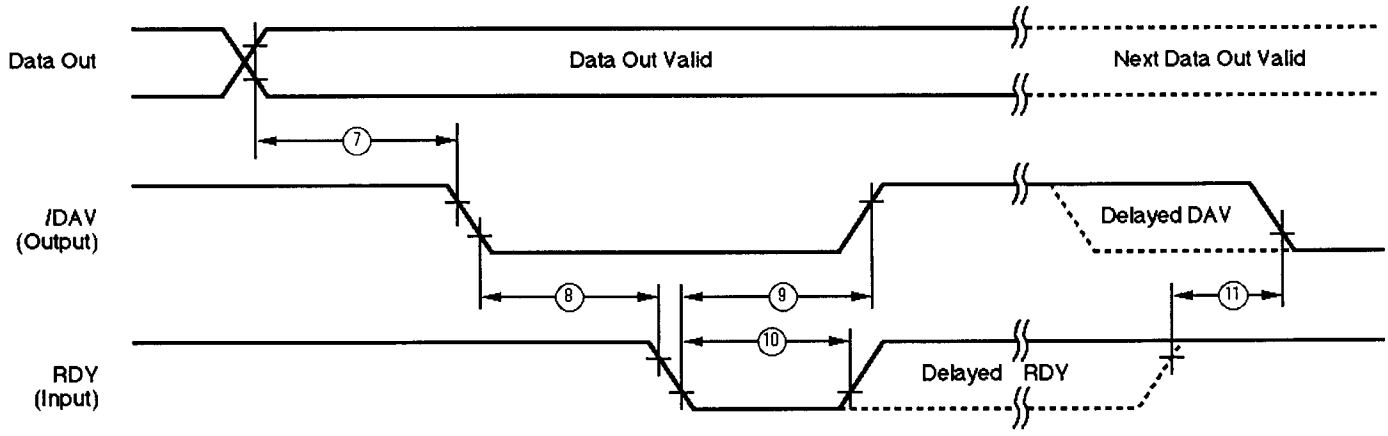

Figure 8. Output Handshake Timing

AC CHARACTERISTICS1 (Continued)

Handshake Timing V_{CC} = 5.0V ± 10%

			TA = 0°C to +70°C		
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Units**
1	TsDI(DAV)	Data In Setup Time to /DAV	0	ns	
2	ThDI(DAV)	RDY to Data In Hold	0	ns	
3	TwDAV	$\overline{DAV}$ Width	40	ns	
4	TdDAVIf	$\overline{DAV}$ to RDY Delay		70	ns
5	TdDAVIr	DAV Rise to RDY Wait		40	ns
6	TdRDYOr	RDY Rise to DAV Delay	0		ns
7	TdDO(DAV)	Data Out to DAV Delay	TpC	ns	
8	TdDAVOf	$\overline{DAV}$ to RDY Delay	0		ns
9	TdRDYIf	RDY to $\overline{DAV}$ Rise Delay	70		ns
10	TwRDY	RDY Width	40	ns	
11	TdRDYIr	RDY Rise to DAV Wait	40	ns	

Note:
TpC = Input Clock Period

Additional Timing
V_{CC} = 5.0V ± 10%

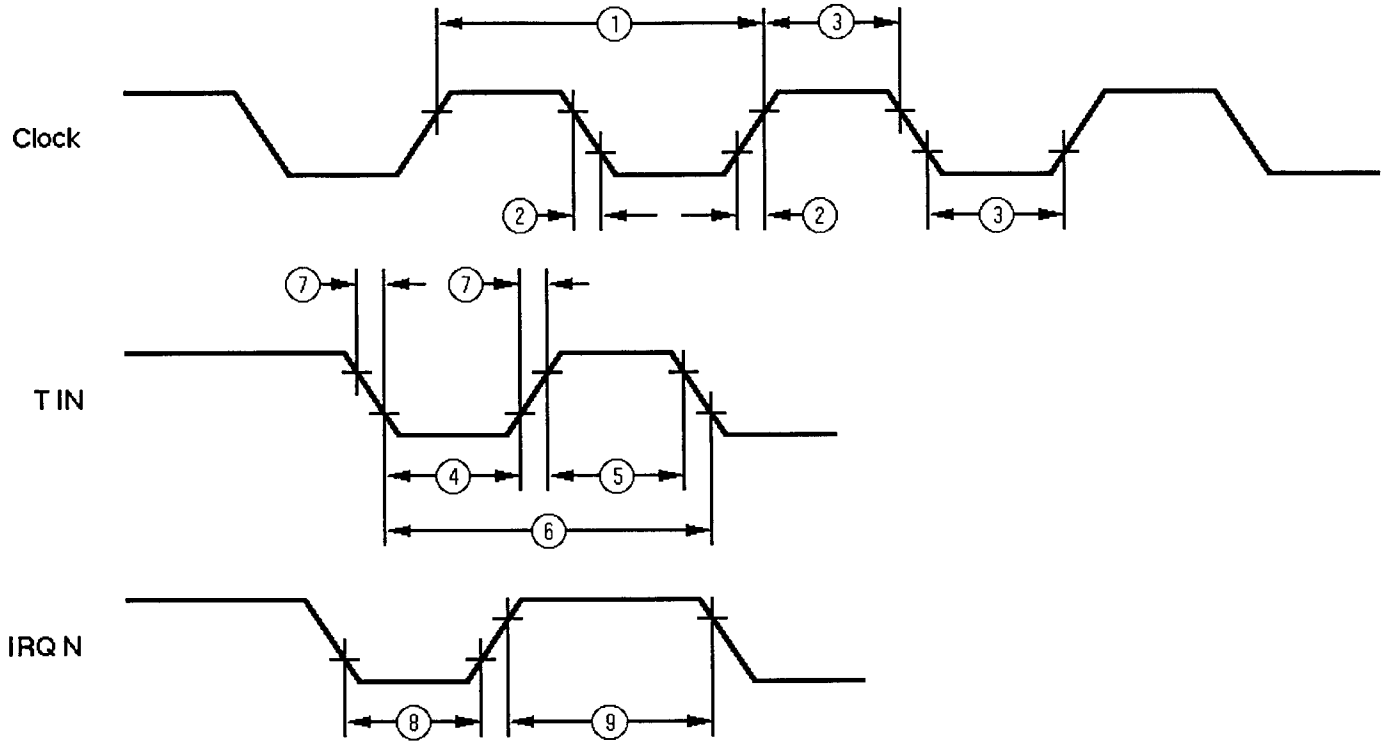

Figure 9. Additional Timing

			T_A = 0°C to +70°C 40 MHz		
No	**Symbol**	**Parameter**	**Min**	**Max**	**Units**
1	TpC	Input Clock Period	25		ns
2	TrC,TfC	Clock Input Rise and Fall		5	ns
3	TwC	Input Clock Width	10		ns
4	TwTinL	Timer Input Low Width	75		ns
5	TwTinH	Timer Input High Width	3 TpC		
6	TpTin	Timer Input Period	8 TpC		
7	TrTin,TfTin	Timer Input Rise and Fall	100	ns	
8a	TwIL	Interrupt Request Input Low	70	ns	
8b	TwIL	Interrupt Request Input Low	5 TpC		
9	TwIH	Interrupt Request Input High	3 TpC		

AC CHARACTERISTICS1 (Continued)

Table 1. A/D Converter Electrical Characteristics*
V_{CC} = 5.0V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		10		Bits
Integral nonlinearity		0.5	1	LSB
Differential nonlinearity		0.5	1	LSB
Zero Error at 25°C			150	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		35	75	mW
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			2	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	ANGND		AV_{CC}–2.5	Volts
VA_{HI}–VA_{LO}	2.5		AV_{CC}	Volts

Note:
*Voltage: 4.5V–5.5V; Temp: 0°C–70°C

Table 2. D/A Converter Electrical Characteristics
V_{CC} = 5.0V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		10		Bits
Integral nonlinearity		0.25	1	LSB
Differential nonlinearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0	µsec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		0.25	0.5	LSB
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		10		mW
Ref Input resistance	2K	4K	10K	Ohms
VD_{HI} range at 3 volts	2.6		3.5	Volts
Output noise voltage		50		μV_{PP}
VD_{LO} range at 5 volts	0.5		1.7	Volts
VD_{HI}–VD_{LO}, at 5 volts	0.9		3.0	Volts
Capacitive output load, CL			30	pF
Resistive output load, RL	20K			Ohms
Output slew rate	1.0	3.0		V/µsec

Note:
*Voltage: 4.5V–5.5V; Temp: 0°C–70°C

Development Projects:

Customer is cautioned that while reasonable efforts will be employed to meet performance objectives and milestone dates, development is subject to unanticipated problems and delays.

No production release is authorized or committed until the Customer and ZiLOG have agreed upon a Customer Procurement Specification for this project.

Low Margin:

Customer is advised that this product does not meet ZiLOG's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on ZiLOG liability stated on the front and back of the acknowledgement, ZiLOG makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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