

## Z8614

# KEYBOARD CONTROLLER ( $KBC^{TM}$ ) NMOS $Z8^{\otimes}$ 8-BIT MCU

#### **DESCRIPTION**

The Z8614 Keyboard Controller (KBC $^{\text{\tiny TM}}$ ) introduces a new level of sophistication to single-chip architecture. The Z8614 is a member of the Z8 single-chip microcontroller family with 4 Kbytes of ROM.

The Z8614 KBC is housed in 40-lead DIP and 44-lead PLCC packages, and is manufactured in NMOS technology. Zilog's microcontroller offers fast execution, efficient use of memory, sophisticated interrupt, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The KBC architecture is characterized by a flexible I/O scheme, an efficient register, I/O, and a number of ancillary features that are useful in keyboard applications.

The device applications demand powerful I/O capabilities. The KBC fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports, each port consists of eight lines, and are configurable under software control to provide timing, status signals, and serial or parallel I/O ports.

The Z8614 offers low EMI emission achieved by means of

several modifications in the output drivers and clock circuitry of the device.

There are two basic address spaces available to support this wide range of configurations: Program Memory and 124 General-Purpose Registers.

The KBC offers two on-chip counter/timers with a large number of user selectable modes. This unburdens the program from coping with real-time problems such as counting/timing.

#### Notes:

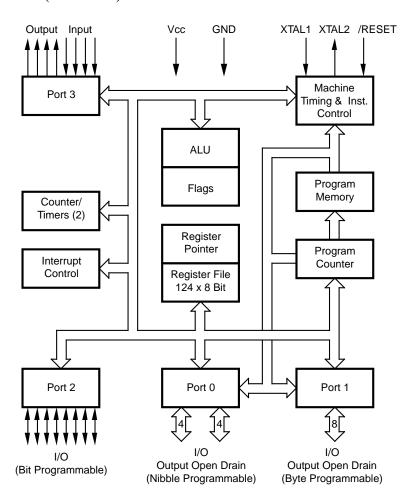
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

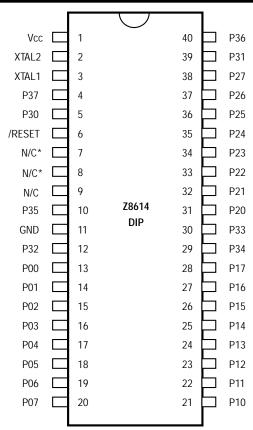
Connection	Circuit	Device		
Power Ground	V <sub>cc</sub> GND	$egin{array}{c} egin{array}{c} egin{array}{c} V_{DD} \ V_{SS} \end{array}$		

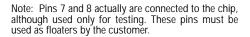
DC 4038-03 (11-2-93)

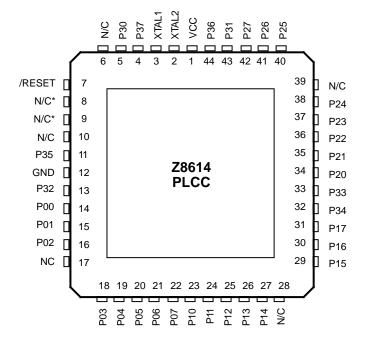
## **GENERAL DESCRIPTION** (Continued)



**Functional Block Diagram** 







Note: Pins 8 and 9 actually are connected to the chip, although used only for testing. These pins must be used as floaters by the customer.

#### 44-Lead PLCC Pin Configuration

#### **40-Lead DIP Pin Configuration**



### DC CHARACTERISTICS

 $V_{CC} = 4.75 \text{ V to } 5.25 \text{V} @ 0^{\circ}\text{C to } +70^{\circ}\text{C}$ 

Symbol	Parameter	Min	Max	Тур*	Unit	Condition
$V_{CH}$	Clock Input High Voltage	3.8	$V_{cc}$		V	Driven by External Clock Generator
V <sub>CL</sub>	Clock Input Low Voltage	-0.3	0.8		V	Driven by External Clock Generator
V <sub>IH</sub>	Input High Voltage	2.0	$V_{\rm cc}$		V	•
$V_{IL}^{II}$	Input Low Voltage	-0.3	0.8		V	
V <sub>RH</sub>	Reset Input High Voltage	3.8	V <sub>CC</sub>		V	
$V_{_{ m RL}}$	Reset Input Low Voltage	-0.3	0.8		V	
$V_{OH}$	Output High Voltage	2.0			V	$I_{OH} = -250 \mu\text{A} \text{ (Port 2 only)}$
<b>0.1</b>	Output High Voltage	2.4			V	$I_{OH}^{OH} = -250 \mu\text{A} \text{ (Port 3 only)}$
V <sub>OL</sub>	Output Low Voltage		0.8		V	$I_{OI} = +4.0 \text{ mA}$ (see Note 1 below)
$I_{IL}$	Input Leakage	-10	10		μΑ	$V_{IN} = 0V, 5.25V$
I <sub>OL</sub>	Output Leakage	-10	10		μΑ	$V_{IN} = 0V, 5.25V$
$\overline{\mathrm{I}_{_{\mathrm{IR}}}}$	Reset Input Current		-50		μΑ	$V_{IN} = 0V, 5.25V$
I <sub>CC</sub>	V <sub>CC</sub> Supply Current		150	135	mA	

#### Note:

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<sup>\*</sup> Typical @ 25°C

<sup>1.</sup> A combined total of six I/O pins from Ports 2 and 3 may be used to sink 10 mA at 0.8  $\rm V_{oL}$ (max three pins per port). These may be used for LEDs or as general purpose outputs requiring high sink current.