Structure Silicon monolithic integrated circuit

Product Name Home Electronics and Security Devices IC

Type **BU6554GVW**

Feature Built-in JPEG Codec, 3M pixels Camera Module Interface, QVGA LCD controller interface, and SD Card Interface

• Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage 1 (IO1)	VDDIO1	-0.3～+3.5	V
Supply voltage 2 (IO2)	VDDIO2	-0.3～+3.5	V
Supply voltage 3 (CORE)	VDD	-0.3～+1.9	V
Power dissipation	PD	380*1, 1000*2	mW
Input voltage 1	VIN1	-0.3～VDDIO1+0.3	V
Input voltage 2	VIN2	-0.3～VDDIO2+0.3	V
Storage temperature range	Tstg	-25～+125	°C

*1 IC only. If exceeding 25°C, 3.8mW should be reduced at the rating 1°C.

*2 When packaging a glass epoxy board of 70*70*1.6mm. If exceeding 25°C, 10.0 mW should be reduced at the rating 1°C.

* Anti radiation design is not provided.

* Operation is not guaranteed.

• Operating conditions (Ta=-20°C～+85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply voltage 1 (IO1)	VDDIO1	1.70	1.80	3.00	V
Supply voltage 2 (IO2)	VDDIO2	2.70	2.85	3.00	V
Supply voltage 3 (CORE)	VDD	1.45	1.50	1.55	V
Input "H" voltage 1	VIH1	VDDIO × 0.8	-	VDDIO+0.3	V
Input "L" voltage 1	VIL1	-0.3	-	VDDIO × 0.2	V
Input "H" voltage 2	VIH2	VDDIO × 0.85	-	VDDIO+0.3	V
Input "L" voltage 2	VIL2	-0.3	-	VDDIO × 0.15	V
Input voltage range	VIN-VDDIO1,2	-0.3	-	VDDIO+0.3	V

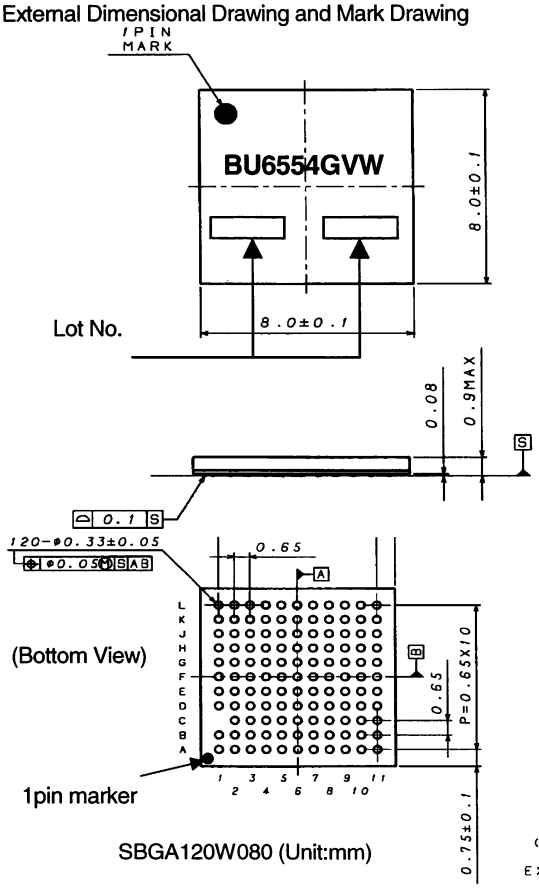
* Supply power in the order of VDD -> VDDIO1 -> VDDIO2.

Status of this document
The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

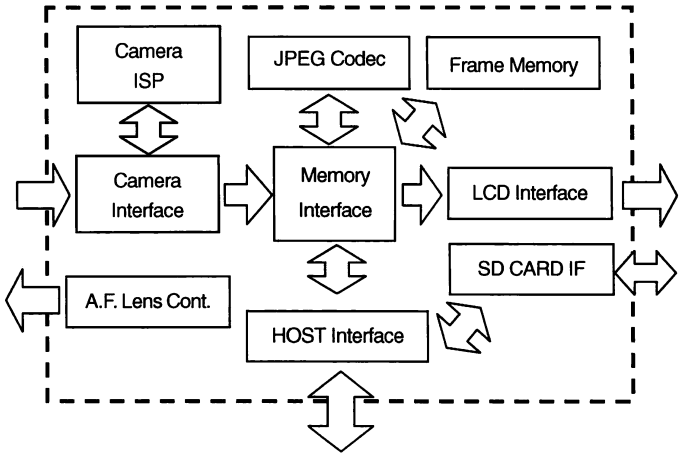
• Electric Characteristics (Unless otherwise specified, VDD=1.50V, VDDIO=2.85V, GND=0.0V, Ta=25°C, F_{IN} =12.0MHz, and F_{SSYS} =48.0MHz.)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Input frequency	F_{IN}	10.0	-	24.0	MHz	XIN(Duty48%～52%)
Internal operating frequency	F_{SSYS}	-	-	48.0	MHz	Internal SCLK frequency
Internal PLL input frequency	F_{PIN}	2.5	-	7.5	MHz	Internal PLL input frequency
Internal PLL output frequency	F_{POUT}	100	-	200	MHz	Internal PLL output frequency
Standby current	IDDst	-	-	150	μA	At suspend mode setting
Input "H" current 1	IIH1	-10	-	10	μA	VIH=VDDIO
Input "H" current 2	IIH2	25	50	100	μA	Pull-Down terminal, VIH=VDDIO
Input "H" current 3	IIH3	-10	-	10	μA	Pull-Up terminal, VIH=VDDIO
Input "L" current 1	IIL1	-10	-	10	μA	VIL=GND
Input "L" current 2	IIL2	-10	-	10	μA	Pull-Down terminal, VIL=GND
Input "L" current 3	IIL3	-160	-80	-25	μA	Pull-Up terminal, VIL=GND
Input "H" voltage 1	VIH1	VDDIO ×0.8	-	VDDIO +0.3	V	Normal input (including input mode of I/O terminal)
Input "L" voltage 1	VIL1	-0.3	-	VDDIO ×0.2	V	Normal input (including input mode of I/O terminal)
Input "H" voltage 2	VIH2	VDDIO ×0.85	-	VDDIO +0.3	V	Hysteresis input (RESETB, CSB, SD_CSB, WRB, RDB, XIN)
Input "L" voltage 2	VIL2	-0.3	-	VDDIO ×0.15	V	Hysteresis input (RESETB, CSB, SD_CSB, WRB, RDB, XIN)
Output "H" voltage 1	VOH1	VDDIO -0.4	-	VDDIO	V	IOH1=-1.0mA(DC) (Including output mode of I/O terminal)
Output "L" voltage 1	VOL1	0.0	-	0.4	V	IOL1=1.0mA(DC) (Including output mode of I/O terminal)
Output "H" voltage 2	VOH2	VDDIO -0.4	-	VDDIO	V	IOH2=-1.0mA(DC)、XOUT terminal
Output "L" voltage 2	VOL2	0.0	-	0.4	V	IOL2=1.0mA(DC)、XOUT terminal

• External Dimensional Drawing and Mark Drawing



• Block Diagram



• Ball No. and Pin Name

Ball No.	Pin Name
G3	A1
G2	A2
L5	CAMCKI
L2	CAMCKO
J3	CAMD0
K4	CAMD1
L3	CAMD2
F6	CAMD3
G6	CAMD4
J4	CAMD5
L4	CAMD6
K5	CAMD7
H6	CAMD8
J5	CAMD9
K2	CAMHS
H5	CAMVS
K6	CAM_CNT0
F7	CAM_CNT1
G7	CAM_CNT2
L6	CAM_CNT3
H7	CAM_CNT4
K7	CAM_CNT5
J6	CAM_CNT6
L7	CAM_CNT7
H1	CSB
G4	SD_CSB
G1	D0
F3	D1
F4	D2
F5	D3
F1	D4
E5	D5
E1	D6
E2	D7
D3	D8
D1	D9
D2	D10
D3	D11
C2	D12
B1	D13

Ball No.	Pin Name
B2	D14
C3	D15
F10	PHA/PWM/KEY0
E7	PHB/KEY1
A9	PHC/GIO2/KEY2
G11	PHD/VD/GIO6
H4	INT
G9	LCDA0
F11	LCDCS1B
G10	LCDCS2B
F9	LCDD0
D11	LCDD1
E10	LCDD2
C11	LCDD3
D10	LCDD4
C10	LCDD5
B11	LCDD6/SCL
E9	LCDD7/SI
D8	LCDD8
C8	LCDD9
A8	LCDD10
B8	LCDD11
A7	LCDD12
D7	LCDD13
C7	LCDD14
A6	LCDD15
B7	LCDD16
B6	LCDD17
D9	LCDRDB
C9	LCDWRB
J10	LEDCNT/GIO1
C6	PWM0/GIO0
H9	PWM1/GIO3
H10	PWM2/GIO4
H11	PWM3/GIO5
J1	RDB
A5	RESETB
K1	SDA
G5	SDC
D6	SDCLK

Ball No.	Pin Name
E6	SDCMD
A4	SDDAT0
B5	SDDAT1
B3	SDDAT2
C5	SDDAT3
D5	SDCD
A3	SDWP
L8	TE_PCLK
K8	TE_PIXCLK
J7	TE_VSYNC
L9	TE_HSYNC
L10	TED0/SGIO0
H8	TED1/SGIO1
K9	TED2/SGIO2
K10	TED3/SGIO3
K11	TED4/SGIO4
J8	TED5/SGIO5
J9	TED6/SGIO6
J11	TED7/SGIO7
A10	TEST
H3	WRB
D4	XIN
C4	XOUT
F2	VDD
K3	
E11	
B9	
J2	VDDIO1
B4	
H2	VDDIO2
G8	
B10	
E4	GND
F8	
E8	
A2	
A1	N.C.
L1	
L11	
A11	

• Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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