○ Structure Silicon monolithic integrated circuit

○ Product Name Video Encoder IC with Fog Reduction/AIE for security camera

○ Type **BU6521KV**

○ Function
- Format of video output is compatible with NTSC/PAL composite video format (CVBS).
- Built-in Fog Reduction function, dynamic range correction, edge-emphasizing filter and gamma filter.
- Input/output data format is compatible with ITU-R BT.656 and YCbCr=4:2:2 with synchronization signal.
- Compatible with NTSC(27MHz, 28.63636MHz and 19.06993MHz)/ PAL(27MHz, 28.375MHz, 35.46895MHz and 18.9375MHz).
- Registers can be set up with a 2-line serial interface.
- Registers can be automatically set up by reading from external EEPROM ,when after resetting or changing mode.

○ Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Applied power source voltage1	VDDIO	-0.3～+4.2	V
Applied power source voltage2	VDDI2C	-0.3～+4.2	V
Applied power source voltage3	AVDD	-0.3～+4.2	V
Applied power source voltage4	VDD	-0.3～+2.1	V
Input voltage	VIN	-0.3～IO_LVL+0.3 *1	V
Storage temperature range	Tstg	-40～+125	℃
Power dissipation	PD	400 *2, 900 *3	mW

*1 IO_LVL is a generic name of VDDIO, VDDI2C, and AVDD.
*2 IC only. In the case exceeding 25ºC, 4.0mW should be reduced at the rating 1ºC.
*3 When packaging a glass epoxy board of 70x70x1.6mm. If exceeding 25ºC, 9.0mW should be reduced at the rating 1ºC.
* Has not been designed to withstand radiation.
* Operation is not guaranteed at absolute maximum ratings.

○ Operating conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Applied power source voltage1 (IO)	VDDIO	2.70	3.30	3.60	V
Applied power source voltage2 (IO)	VDDI2C	2.70	3.30	3.60	V
Applied power source voltage3 (DAC)	AVDD	2.70	3.30	3.60	V
Applied power source voltage4 (CORE)	VDD	1.40	1.50	1.60	V
Input voltage range	VIN	0.00	-	IO_LVL *1	V
Operating temperature range	Topr	-40	-	85	℃

*1 IO_LVL is a generic name of VDDIO, VDDI2C and AVDD.

* Please supply power source in order of VDD→IO_LVL

○ Electric Characteristics (Unless otherwise specified VDD=1.50V, VDDIO=3.3V, VDDI2C=3.3V, AVDD=3.3V, GND=0.0V, Ta=25℃, f_{IN}=35.5MHz)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Input frequency	f_{IN}	2	-	35.5	MHz	CAMCKI(DUTY45%～55%)
Operational consumption current(CORE)	IDD1	-	40	62	mA	35.5MHz operational setting *1
Static consumption current (CORE)	IDDst	-	-	50	uA	At sleep mode setting, input terminal = GND setting
Input "H" current 1	IIH	-10	-	10	uA	VIH=IO_LVL
Input "H" current 2	IIL	-10	-	10	uA	VIL=GND
Pull-down current	IPD	25	50	100	uA	VIH=IO_LVL
Input "L" current 1	VIH1	IO_LVL x0.8	-	IO_LVL +0.3	V	Normal input (Including input mode of I/O terminal)
Input "L" current 2	VIL1	-0.3	-	IO_LVL x0.2	V	Normal input (Including input mode of I/O terminal)
Input "H" voltage 1	VIH2	IO_LVL x0.85	-	IO_LVL +0.3	V	Hysteresis input (RESETB, CAMCKI, AUTO, MODE0, MODE1)
Input "L" voltage 1	VIL2	-0.3	-	IO_LVL x0.15	V	Hysteresis input (RESETB, CAMCKI, AUTO, MODE0, MODE1)
Input "H" voltage 2	VOH	IO_LVL -0.4	-	IO_LVL	V	IOH=-1.0mA(DC) (including output mode of I/O terminal)
Input "L" voltage 2	VOL	0.0	-	0.4	V	IOL=1.0mA(DC) (including output mode of I/O terminal)
Operational consumption Current (DAC)	IDD2	-	38	56	mA	R_L=37.5Ω、R_{IREF}=2.4kΩ
Static consumption current (DAC)	IDDst2	-	-	5	uA	input terminal=GND and DAC power down mode setting
Integral Non-linearity	INL	-	±4.0	±8.0	LSB	R_L=37.5Ω, R_{IREF}=2.4kΩ, DAC resolution=10bit
Differential Non-linearity	DNL	-	±1.0	±2.0	LSB	R_L=37.5Ω, R_{IREF}=2.4kΩ, DAC resolution=10bit
Output Voltage (full scale)	VFS	1.1	1.25	1.4	V	R_L=37.5Ω, R_{IREF}=2.4kΩ, DAC resolution=10bit

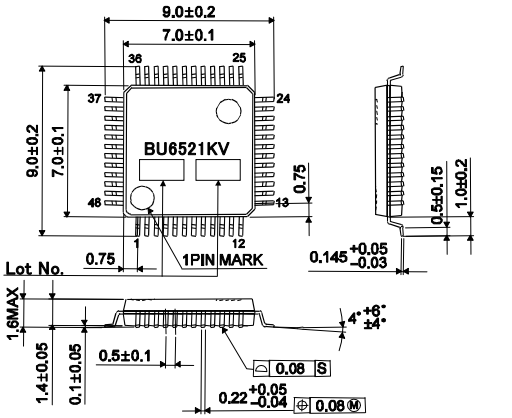
*1 Operational consumption current(CORE) at color-bar image input in Fog-Reduction enable, AIE enable and Digital output disable settings.

* IO_LVL is a generic name of VDDIO, VDDI2C and AVDD.

○ Pin Function Descriptions

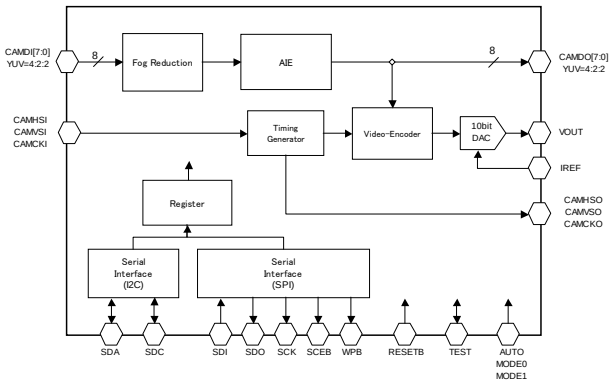
PIN No.	PIN Name	Description	PIN No.	PIN Name	Description
1	SDI	SPI-bus data input	25	CAMHSO	Horizontal timing output
2	CAMDI7	Data input bit 7	26	CAMVSO	Vertical timing output
3	CAMDI6	Data input bit 6	27	CAMCKO	Clock output
4	CAMDI5	Data input bit 5	28	GND	Common GROUND
5	CAMDI4	Data input bit 4	29	VDD	CORE power source
6	GND	Common GROUND	30	AUTO	Auto register setting enable signal
7	VDD	CORE power source	31	MODE0	Auto register setting mode select bit 0
8	CAMDI3	Data input bit 3	32	MODE1	Auto register setting mode select bit 1
9	CAMDI2	Data input bit 2	33	VOUT	Analog composite output
10	CAMDI1	Data input bit 1	34	AVSS	Analog GROUND for DAC
11	CAMDI0	Data input bit 0	35	IREF	Reference voltage for DAC
12	CAMHSI	Horizontal timing input	36	AVDD	Analog power source for DAC
13	CAMVSI	Vertical timing input	37	GND	Common GROUND
14	CAMCKI	Clock input	38	VDDI2C	Digital IO power source (For 2-line serial interface input/output)
15	GND	Common GROUND	39	SDA	2-line serial interface data input/output
16	VDDIO	Digital IO power source	40	SDC	2-line serial interface clock input
17	CAMDO0	Data output bit 0	41	RESETB	System reset signal
18	CAMDO1	Data output bit 1	42	TEST	Test mode terminal (Connect to GND)
19	CAMDO2	Data output bit 2	43	GND	Common GROUND
20	CAMDO3	Data output bit 3	44	VDDIO	Digital IO power source
21	CAMDO4	Data output bit 4	45	WPB	Write protect signal to EEPROM
22	CAMDO5	Data output bit 5	46	SCEB	Chip select signal to EEPROM
23	CAMDO6	Data output bit 6	47	SCK	SPI-bus clock
24	CAMDO7	Data output bit 7	48	SDO	SPI-bus data output

○ External Dimensional Drawing and Mark Drawing



VQFP48C

○ Block Diagram



○ Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Recommended Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) Rush current
For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

Notes

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