For Security camera and load Mobile display
AIE Adaptive Image Enhancer Series

TV encoder built in Adaptive Image Enhancer

BU6520KV

●Description

BU6520KV is TV encoder IC with AIE (image treating technology by ROHM's hardware) image correction.

●Features

1) Input/output data format — ITU-R BT.656-4 or YCbCr with synchronization signal
   Data format YCbCr 8bit
   Data range is full range or based on ITU-R BT.601
   Pixel clock
   NTSC 27MHz and 28.63636MHz
   PAL 27MHz, 28.375MHz and 35.46895MHz
2) Video output data format — NTSC/PAL SD-TV composite video output (CVBS)
3) Image Correction — Build-in dynamic range correction with Adaptive Image Enhancer (AIE)
   Build-in edge-emphasizing filter and gamma filter
4) Built-in DAC — 10bit DAC 1ch (output load R=75Ω)
5) Built-in slave function for 2-line serial interface
   The registers in BU6520KV from the outside can be set
6) Built-in master function for SPI BUS
   The registers setting value can be stored in external EEPROM
   When reset is released or the mode is changed, the setting of the registers in BU6520KV can be automatically set
7) Voltage source(Typical) — Compatible with 4 power sources(VDD=1.50V, VDDIO=3.30V, VDDI^{2}C=3.30V, AVDD=3.30V)
8) Package — 48pin VQFP Package (VQFP48C)

●Application

Security camera, Intercom with camera, Drive recorder, and Web camera etc.

●Lineup

Parameter	Power source voltage	Input interface	Control interface	Output Interface	TV Encoder	Temperature range of operating	Package
BU6520KV	1.4-1.6V(V_{DD}Core) 2.7-3.6V(V_{DD}I/o,AV_{DD})	8bit YUV=4:2:2 parallel ・CCIR601 ・CCIR656	I^{2}C/ Seral EEPROM Interface	8bit YUV=4:2:2 parallel ・CCIR601 ・CCIR656	NTSC PAL Composite output	-40℃～+85℃	VQFP48C

I^{2}C BUS is a registered trademark of Philips

Jan. 2008

●Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Applied power source voltage 1	VDDIO1	-0.3～+4.2	V
Applied power source voltage 2	VDDI^{2}C	-0.3～+4.2	V
Applied power source voltage 3	AVDD	-0.3～+4.2	V
Applied power source voltage 4	VDD	-0.3～+2.1	V
Input voltage	VIN	-0.3～IO_LVL+0.3*1	V
Storage temperature range	Tstg	-40～+125	℃
Power dissipation	PD	400*2	mW

*1 : IO_LVL is a generic name of VDDIO, VDDI^{2}C, and AVDD.

*2 : IC only.In the case exceeding 25ºC, 4.0mW should be reduced at the rating 1ºC.

●Recommended operating range

Parameter	Symbol	Rating	Unit
Applied power source voltage 1 (IO)	VDDIO	2.70～3.60(Typ:3.3V)	V
Applied power source voltage 2 (IO)	VDDI^{2}C	2.70～3.60(Typ:3.3V)	V
Applied power source voltage 3 (DAC)	AVDD	2.70～3.60(Typ:3.3V)	V
Applied power source voltage 4 (CORE)	VDD	1.40～1.60(Typ:1.5V)	V
Input voltage range	VIN	0～IO_LVL*1	V
Operating temperature range	Topr	-40～+85	℃

*Please supply power source in order of VDD→(VDDIO,VDDI^{2}C,AVDD)

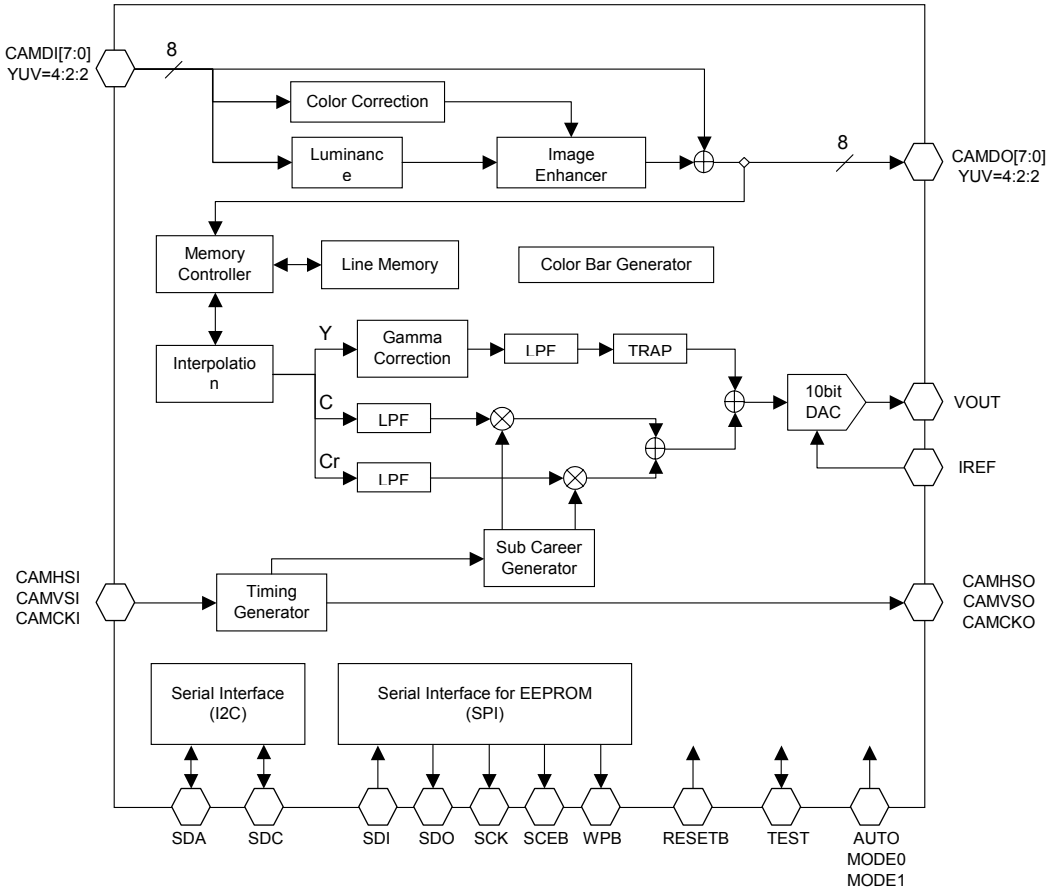
●Electric characteristics

(Unless otherwise specified VDD=1.50V, VDDIO=VDDI^{2}C=3.3V, AVDD=3.3V, GND=0.0V, Ta=25 ºC, f_{in}=35.5MHz)

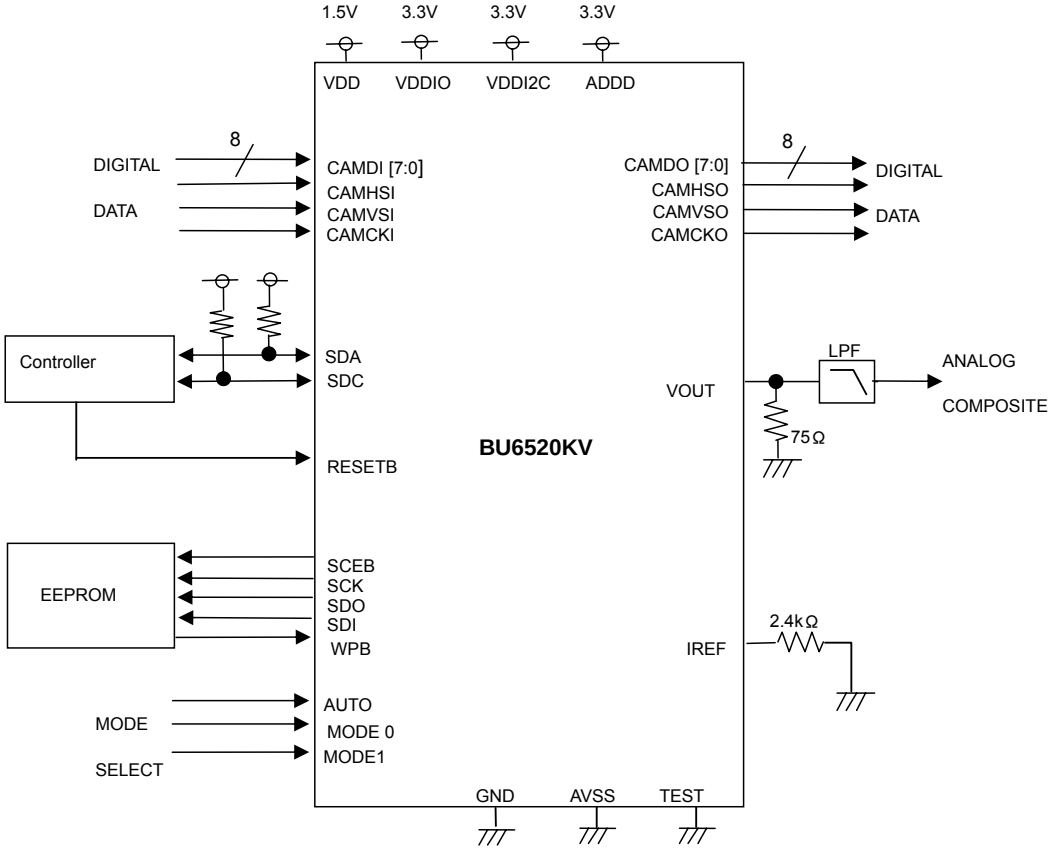
Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Input frequency	F_{IN}	2	-	35.5	MHz	CAMCKI(DUTY45%～55%)
Operational current	IDD1	-	57	-	mA	In the enhance mode (35.5 MHz) (Total value of current of VDD, VDDIO, and VDDI^{2}C)
Static current	IDDst1	-	-	50	uA	In the sleep mode, input pin: GND
Input "H" current 1	IIH	-10	-	10	uA	VIH=IO_LVL
Input "H" current 2	IIL	-10	-	10	uA	VIL=GND
Pull-down current	IPD	25	50	100	uA	VIH=IO_LVL
Input "L" current 1	VIH1	IO_LVL x0.8	-	IO_LVL +0.3	V	Normal input (Including input mode of I/O terminal)
Input "L" current 2	VIL1	-0.3	-	IO_LVL x0.2	V	Normal input (Including input mode of I/O terminal)
Input "H" voltage 1	VIH2	IO_LVL x0.85	-	IO_LVL +0.3	V	Hysteresis input (RESETB, CAMCKI, AUTO, MODE0, MODE1)
Input "L" voltage 1	VIL2	-0.3	-	IO_LVL x0.15	V	Hysteresis input (RESETB, CAMCKI, AUTO, MODE0, MODE1)
Input "H" voltage 2	VOH	IO_LVL -0.4	-	IO_LVL	V	IOH=-1.0mA(DC) (including output mode of I/O terminal)
Input "L" voltage 2	VOL	0.0	-	0.4	V	IOL=1.0mA(DC) (including output mode of I/O terminal)
Resolution (DAC)	RES	-	-	10	Bits	
Operational Current (DAC)	IDD2	-	38	-	mA	R_L=37.5Ω、R_{IREF}=2.4kΩ (Only the current value of AVDD)
Static consumption current (DAC)	IDDst2	-	-	5	uA	Input terminal =GND setting
Integral Non-linearity	INL	-	±4.0	±8.0	LSB	R_L=37.5Ω、R_{IREF}=2.4kΩ
Differential Non-linearity	DNL	-	±1.0	±2.0	LSB	R_L=37.5Ω、R_{IREF}=2.4kΩ
Voltage of Full scale	VFS	1.1	1.25	1.4	V	R_L=37.5Ω、R_{IREF}=2.4kΩ

* IO_LVL is a generic name of VDDIO, VDDI^{2}C, and AVDD.

●Block Diagram



● Recommended Application Circuit



●Terminal functions

PIN No.	PIN Name	In/Out	Active Level	Init	Function explanation	Power Source System	I/O type
1	SDI	In	DATA	-	SPI BUS data input	1	A
2	CAMDI7	In	DATA	-	Data input bit 7	1	C
3	CAMDI6	In	DATA	-	Data input bit 6	1	C
4	CAMDI5	In	DATA	-	Data input bit 5	1	C
5	CAMDI4	In	DATA	-	Data input bit 4	1	C
6	GND	-	GND	-	Common GROUND	1,2,4	-
7	VDD	-	PWR	-	CORE P power source	4	-
8	CAMDI3	In	DATA	-	Data input bit 3	1	C
9	CAMDI2	In	DATA	-	Data input bit 2	1	C
10	CAMDI1	In	DATA	-	Data input bit 1	1	C
11	CAMDI0	In	DATA	-	Data input bit 0	1	C
12	CAMHSI	In	*	-	Horizontal timing input	1	C
13	CAMVSI	In	*	-	Vertical timing input	1	C
14	CAMCKI	In	CLK	-	Clock input	1	E
15	GND	-	GND	-	Common GROUND	1,2,4	-
16	VDDIO	-	PWR	-	Digital IO power source	1	-
17	CAMDO0	Out	DATA	Low	Data output bit 0	1	F
18	CAMDO1	Out	DATA	Low	Data output bit 1	1	F
19	CAMDO2	Out	DATA	Low	Data output bit 2	1	F
20	CAMDO3	Out	DATA	Low	Data output bit 3	1	F
21	CAMDO4	Out	DATA	Low	Data output bit 4	1	F
22	CAMDO5	Out	DATA	Low	Data output bit 5	1	F
23	CAMDO6	Out	DATA	Low	Data output bit 6	1	F
24	CAMDO7	Out	DATA	Low	Data output bit 7	1	F

* "∗" in the Active Level column indicates that it may be changed during set-up of the register.
* Init indicates pin status when released from reset.
* In the power system column, "1" stands for VDDIO, "2" stands for VDDI^{2}C, "3" stands for AVDD, "4" stands for VDD.

PIN No.	PIN Name	In/Out	Active Level	Init	Function explanation	Power Source System	I/O type
25	CAMHSO	Out	*	Low	Horizontal timing output	1	F
26	CAMVSO	Out	*	Low	Vertical timing output	1	F
27	CAMCKO	Out	CLK	Low	Clock output	1	F
28	GND	-	GND	-	Common GROUND	1,2,4	-
29	VDD	-	PWR	-	CORE power source	4	-
30	AUTO	In	High	PD *1	Auto register setting enable signal	1	D
31	MODE0	In	DATA	PD *1	Auto register setting mode select bit 0	1	D
32	MODE1	In	DATA	PD *1	Auto register setting mode select bit 1	1	D
33	VOUT	Out	Analog	-	Analog composite output	3	H
34	AVSS	-	GND	-	Analog GROUND for DAC	3	-
35	IREF	Out	Analog	-	Reference voltage for DAC	3	I
36	AVDD	-	PWR	-	Analog power source for DAC	3	-
37	GND	-	GND	-	Common GROUND	1,2,4	-
38	VDDI^{2}C	-	PWR	-	Digital IO power source (For 2-line serial interface input/output)	2	-
39	SDA	In/Out	DATA	In	2-line serial interface data input/output	2	G
40	SDC	In/Out	CLK	In	2-line serial interface clock input	2	G
41	RESETB	In	Low	-	System reset signal	1	B
42	TEST	In	High	PD *1	Test mode terminal (Connect to GND)	1	D
43	GND	-	GND	-	Common GROUND	1,2,4	-
44	VDDIO	-	PWR	-	Digital IO power source	1	-
45	WPB	Out	Low	Low	Write protect signal to EEPROM	1	F
46	SCEB	Out	Low	High	Chip select signal to EEPROM	1	F
47	SCK	Out	CLK	Low	SPI BUS clock	1	F
48	SDO	Out	DATA	Low	SPI BUS data output	1	F

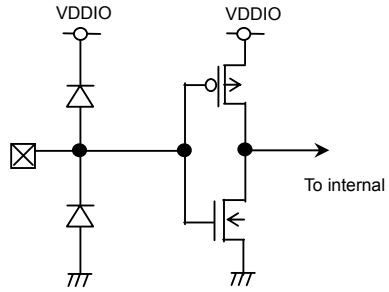
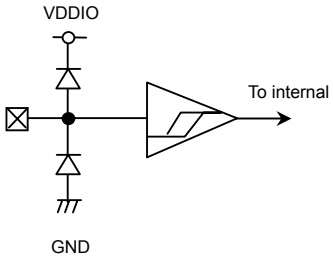
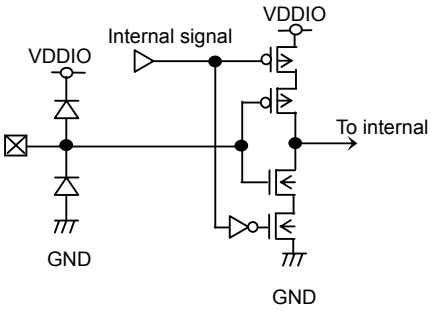
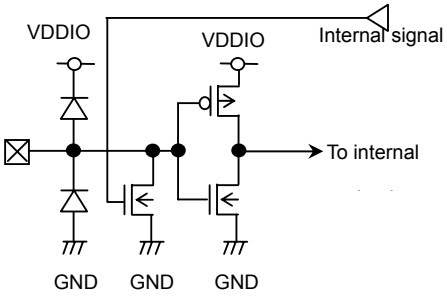
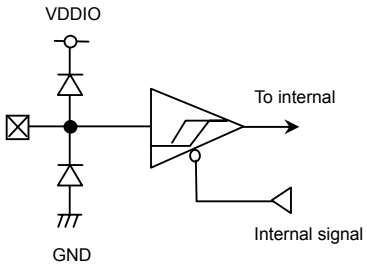
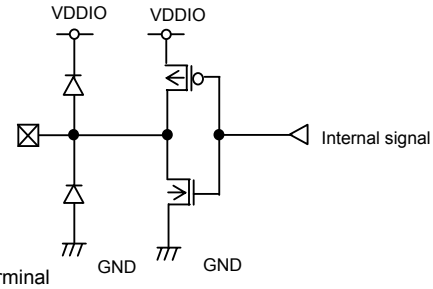
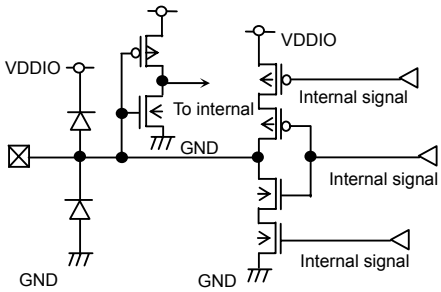
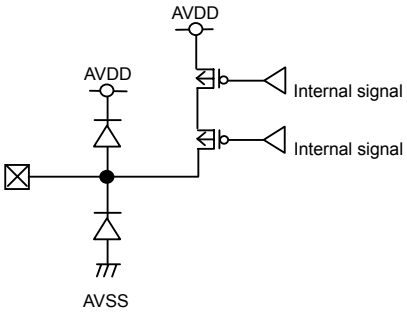
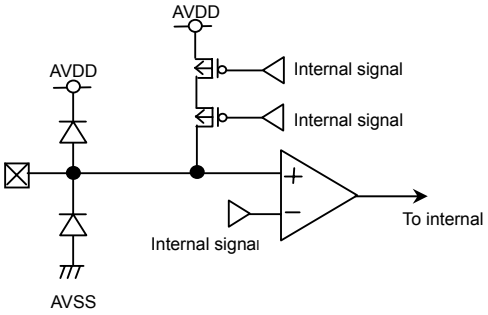
* "*" in the Active Level column indicates that it may be changed during set-up of the register.

* Init column indicates pin status when released from reset.

* In the power system column, "1" stands for VDDIO, "2" stands for VDDI^{2}C, "3" stands for AVDD, "4" stands for VDD.

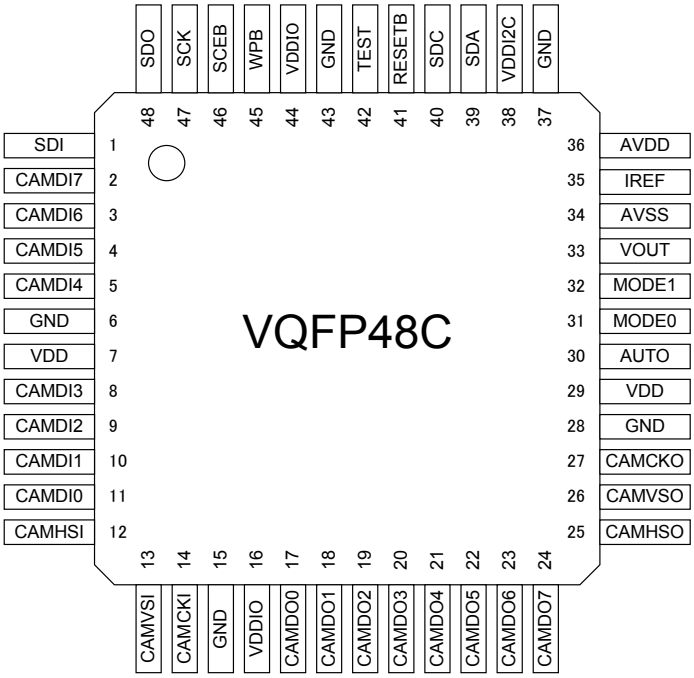
*1 : Pull-down status.

●Equivalent Circuit Structures of input / output pins

Type	Equivalent circuit configuration	Type	Equivalent circuit configuration
A	 Input terminal	B	 Input terminal with schmitt
C	 Input terminal with suspend	D	 Input terminal with pull down
E	 Input terminal with schmitt and suspend	F	 Output terminal
G	 Input/Output terminal	H	 VOUT
I	 IREF		

●Terminal Layout

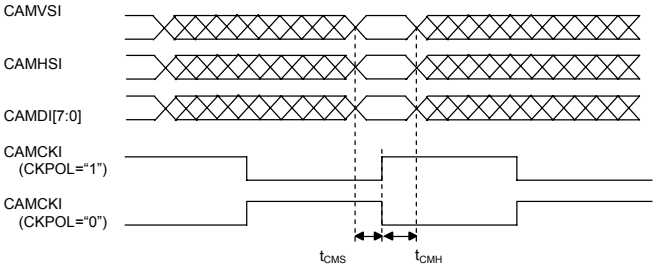
(Bottom View)



●Timing Chart

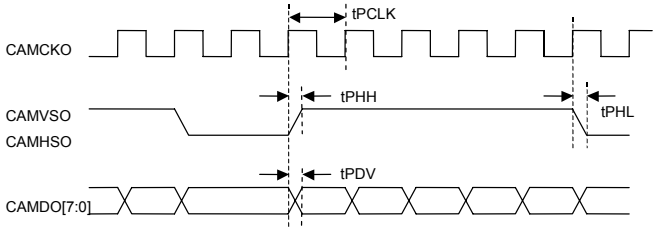
1. Date input / output interface

Data input interface timing



Symbol	Description	MIN	TYP	MAX	Unit
t_{CAMCKI}	Clock Cycle	27.8	-	-	ns
d_{CAMCKI}	Clock Duty	45	50	55	%
t_{CMS}	CAMCKI Rise / Fall Camera set-up Time	8	-	-	ns
t_{CMH}	CAMCKI Rise / Fall Camera Hold Time	6	-	-	ns

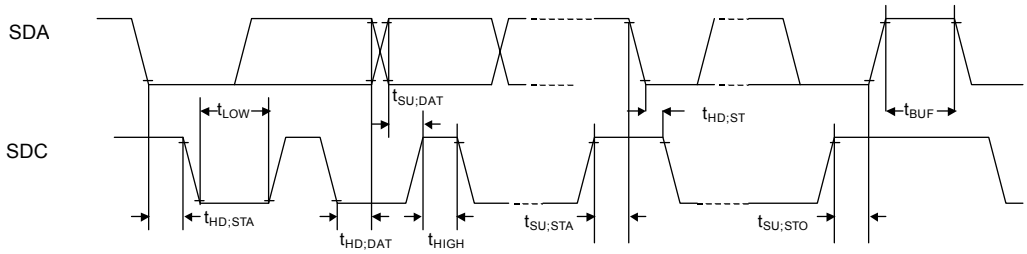
Data output interface timing



Symbol	Description	MIN	TYP	MAX	Unit
t_{PCLK}	Clock Cycle	27.8	-	-	ns
d_{PCLK}	Clock Duty	40	50	60	%
t_{PDV}	Decision of CAMDO from CAMCKO	-	-	7	ns
t_{PHL} t_{PHH}	Decision of CAMVSO or CAMHSO from CAMCKO	-	-	7	ns

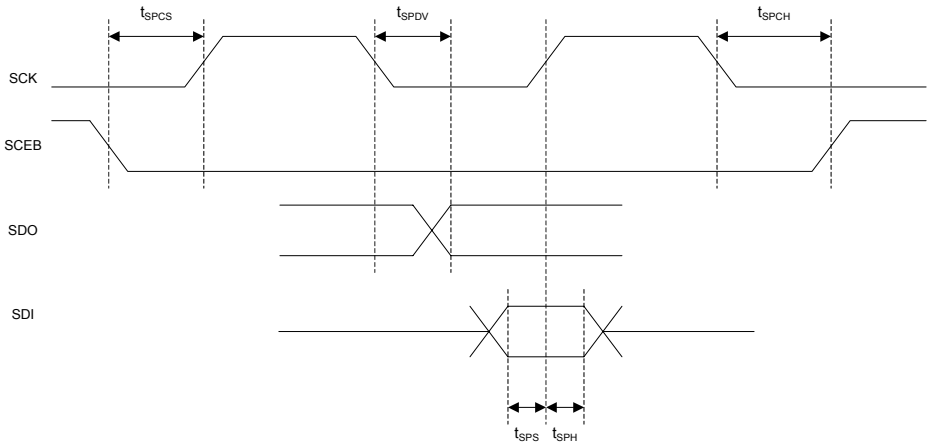
2. I^2C BUS interface

I^2C BUS interface timing



Symbol	Parameter	MIN.	TYP.	MAX.	Unit
fSCL	SDC Clock Frequency	0	-	400	kHz
tHD;STA	Hold-time(repetition)『START』conditions The first clock pulse is generated after this period.	0.6	-	-	us
fLOW	The "L" period of SDC clock	1.3	-	-	us
tHIGH	The "H" period of SDC clock	0.6	-	-	us
tSU;STA	Setup time of repetitive 『START』conditions	0.6	-	-	us
tHD;DAT	Data hold time	0			us
tSU;DAT	Data setup time	100	-	-	ns
tSU;STO	Setup time of the 『STOP』conditions	0.6	-	-	us

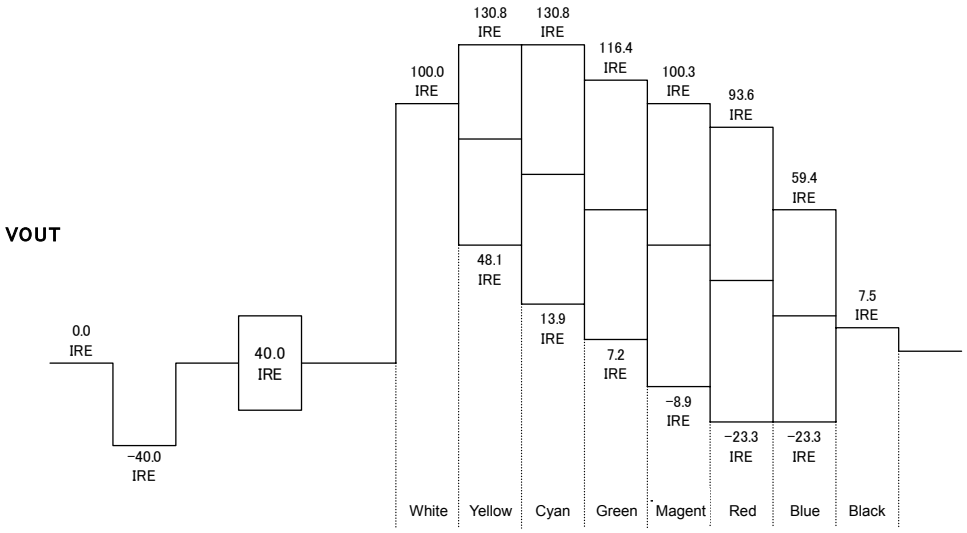
SPI BUS interface timing



Symbol	Description	MIN	TYP	MAX	Unit
t_{SPCLK}	Clock Cycle	2	736	8192	t_{CAMCKI}
d_{SPCLK}	Clock Duty	45	50	55	%
t_{SPCS}	SCK Rise SCEB set-up Time	4	738-1105	1102	t_{CAMCKI}
t_{SPCH}	SCK Fall after SCEB Rise Time	2	751	8319	t_{CAMCKI}
t_{SPDV}	Decision of SDO from SCK Fall	-	-	28	ns
t_{SPS}	SCK Rise SDI set-up Time	-	-	28	ns
t_{SPH}	SCK Rise SDI Hold Time	-	-	28	ns

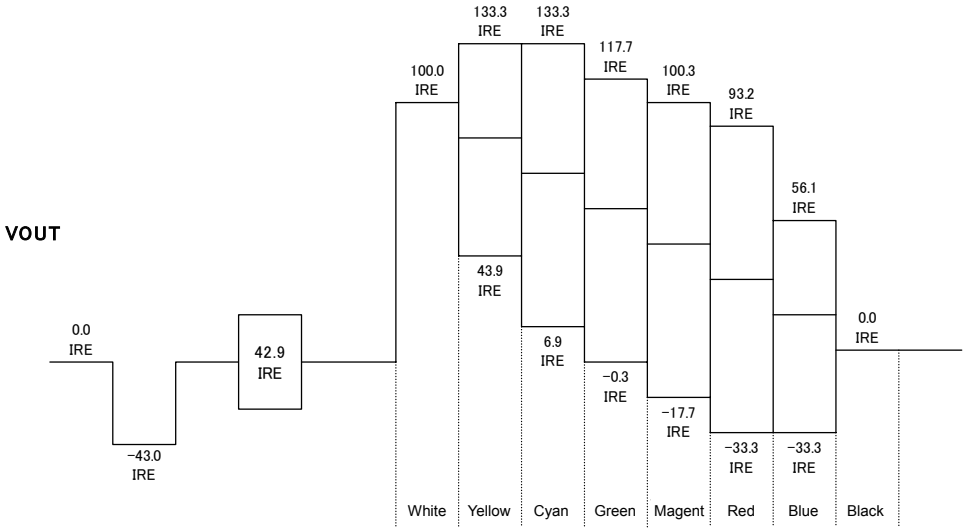
When the automatic reading function with the AUTO pin is used, it becomes timing of SCEB to SCK as above.
It is possible to access from the register of BU6520KV to interface.In that case, SCEB is controlled by the register.
After the value is set to the register, the SCEB pin is changed into the logic set at once.

3. Output waveform in NTSC



(Note)
(*1) The white level and the black level can be changed by the setting.

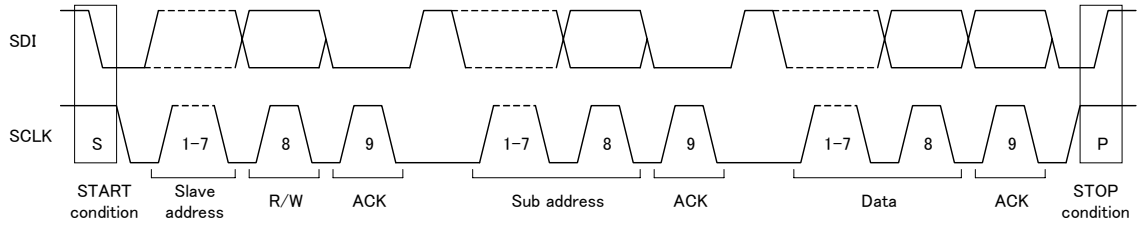
4. Output waveform in PAL



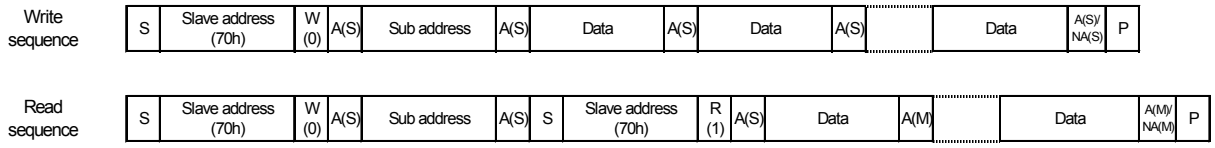
(Note)
(*1) The white level and the black level can be changed by the setting.

5. I²C BUS Format

Slave address is 70h.
The subaddress increment automatically when continuously accessing(read / write) it 2 times or more.

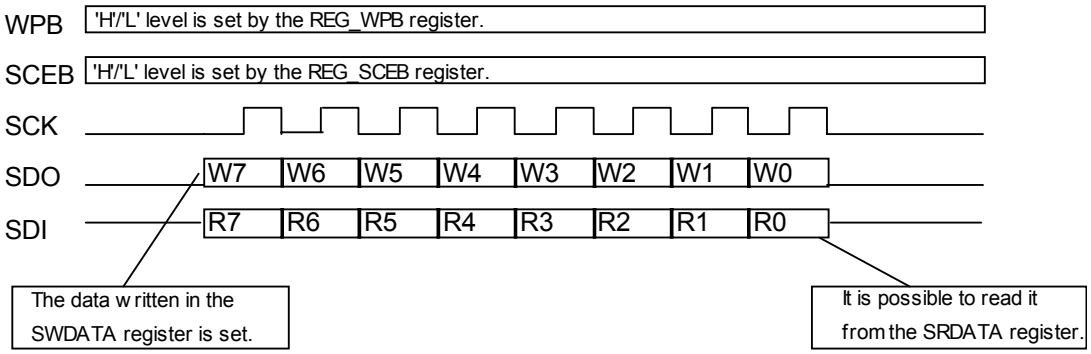


Data transmission part



S = START condition
P = STOP condition
A(S) = acknowledge by slave
A(M) = acknowledge by master
NA(S) = not acknowledge by slave
NA(M) = not acknowledge by master

6. SPI BUS Format



* REG_WPB, REG_SCEB, SWDATA, and SRDATA in figure are the register names, and the each function is as follows.

REG_WPB : Set WPB Terminal logic. Register value output direct.
REG_SCEB : Set SCEB Terminal logic. Register value output direct
SWDATA[7:0] : Write data to EEPROM. It is transfer MSB first.
SRDATA[7:0] : Read data from EEPROM. Convert MSB first.

The SCK clock frequency is as follows.

$$\text{SCK frequency} = \text{CAMCKI frequency} \div 2^{(\text{SPIPREDIV}+1)} \div (\text{SPIDIV}+1)$$

Register range : SPIPREDIV = 0～7. SPIDIV = 0～31
When CAMCKI is 27MHz, SCK becomes 3.3kHz from 13.5MHz.

●Cautions on use

(1)Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2)Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3)Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4)Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5)GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6)Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7)Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8)Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9)Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10)Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11)External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

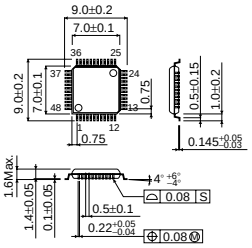
●Order Model Name Selection

B U	6 5 2 0	K V	—	E 2
ROHM model name	Product number	Package type KV:VQFP48C		Taping model name E2: Embossed reel tape

●Tape and Reel information

VQFP48C

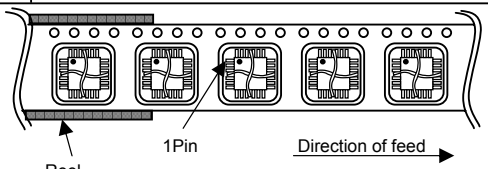
<Dimension>



(Unit:mm)

〈 Packing information 〉

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

Excellence in Electronics

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