Structure Silicon monolithic integrated circuit

Product Name Application control IC for Home Electronics and Security Devices

Type **BU6569GVW**

Feature Built-in JPEG Codec, Camera Module Interface, and LCD controller interface, USB/NAND Flash/SDC/MMC/TV-Encoder interface, MIDI/MP3/AAC/HE-AAC Decoder, ADPCM Codec, Audio serial interfase, DAC, PLL

• Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage 1 (IO)	VDDIO1	-0.3～+4.2	V
Supply voltage 2 (IO)	VDDIO2	-0.3～+4.2	V
Supply voltage 3 (USB)	VDDIO3	-0.3～+4.2	V
Supply voltage 4 (PLL)	VDDIO4	-0.3～+4.2	V
Supply voltage 5 (DAC)	AVDD	-0.3～+4.2	V
Supply voltage 6 (CORE)	VDD	-0.3～+2.1	V
Power dissipation	PD	380*1, 1000*2	mW
Input voltage	VIN	-0.3～VDDIO+0.3	V
Storage temperature range	Tstg	-40～+150	℃

*1 IC only. If exceeding 25℃, 3.8mW should be reduced at the rating 1℃.

*2 When packaging a glass epoxy board of 70*70*1.6mm. If exceeding 25℃, 10.0 mW should be reduced at the rating 1℃.

* Anti radiation design is not provided.

* Operation is not guaranteed.

• Operating conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply voltage 1 (IO)	VDDIO1	1.70	1.80	3.60	V
Supply voltage 2 (IO)	VDDIO2	2.70	3.30	3.60	V
Supply voltage 3 (USB)	VDDIO3	3.15	3.30	3.45	V
Supply voltage 4 (PLL)	VDDIO4	2.70	3.30	3.60	V
Supply voltage 5 (DAC)	AVDD	2.70	3.30	3.60	V
Supply voltage 6 (CORE)	VDD	1.45	1.50	1.55	V
Input voltage range	VIN-VDDIO	-0.3	-	VDDIO+0.3	V
Operation temperature range	Topr	-30	-	85	℃

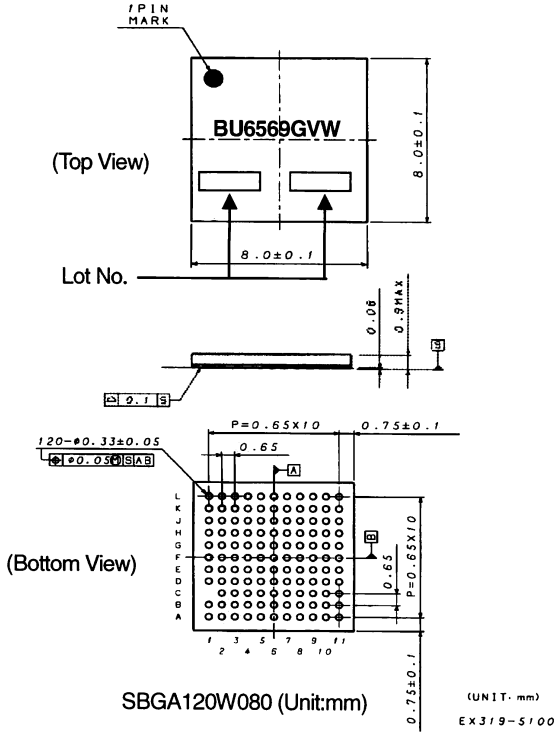
* Supply power in the order of VDD -> VDDIO (VDDIO1->VDDIO2->VDDIO4->AVDD->VDDIO3).

Status of this document
The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

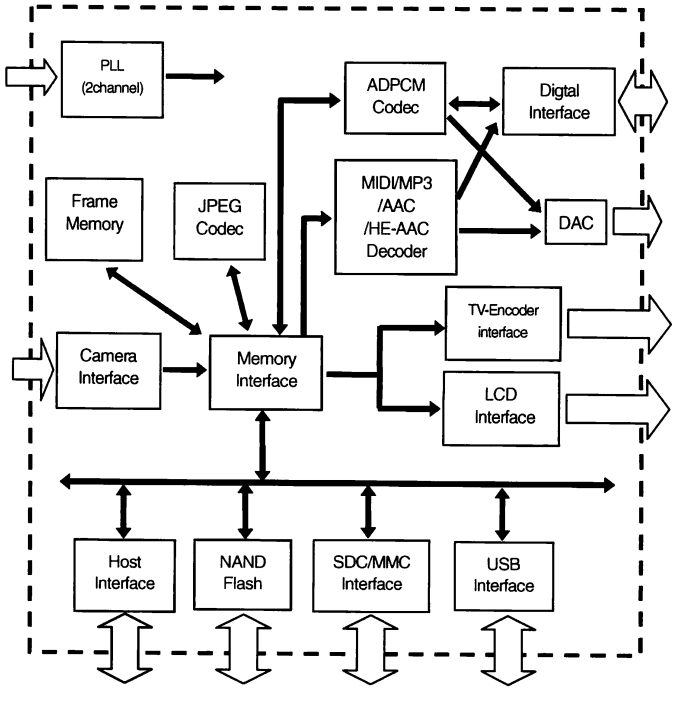
• Electric Characteristics (Unless otherwise specified, VDD=1.50V, VDDIO1,2,3,4,AVDD=3.30V, GND=0V, Ta=25℃, fXIN1=12.0MHz, fXIN2=12.0MHz, fAUDIO=74.0MHz, fIMAGE=52MHz)

Parameter	Symbol	Specification			Unit	Conditions
		MIN	TYP	MAX		
Input frequency 1	fXIN1	2.688	-	26.0	MHz	XIN1 (Duty 50±10%), at PLL ON
Input frequency 2	fXIN2	10.0	-	30.0	MHz	XIN2 (Duty 50±10%), at PLL ON
Internal clock frequency 1	fIMAGE	-	-	52.0	MHz	At PLL ON
Internal clock frequency 2	fAUDIO	-	-	74.0	MHz	At PLL ON
Static consumption current	IDDst	-	-	150	μA	At suspend mode setting
Input "H" current 1	IIH1	-10	-	10	μA	VIH=VDDIO1,2,3,4
Input "H" current 2	IIH2	25	50	100	μA	Pull-down terminal, VIH=VDDIO2
Input "H" current 3	IIH3	-10	-	10	μA	Pull-up terminal, VIH=VDDIO2
Input "L" current 1	IIL1	-10	-	10	μA	VIL=GND
Input "L" current 2	IIL2	-10	-	10	μA	Pull-down terminal, VIL=GND
Input "L" current 3	IIL3	-160	-80	-25	μA	Pull-up terminal, VIL=GND
Input "H" voltage1	VIH1	VDDIO*0.8	-	VDDIO+0.3	V	Normal type input
Input "L" voltage 1	VIL1	-0.3	-	VDDIO*0.2	V	Normal type input
Input "H" voltage 2	VIH2	VDDIO*0.85	-	VDDIO+0.3	V	Hysteresis input
Input "L" voltage 2	VIL2	-0.3	-	VDDIO*0.15	V	VDDIO1(CSB,WRB,RDB), VDDIO4(XIN1,XIN2)
Input "H" voltage3	VIH3	2.0	-	-	V	USB_DP,USB_DM
Input "L" voltage 3	VIL3	-	-	0.8	V	Single-ended input voltage level
Differential input sensitivity	VDI	0.2	-	-	V	ABS(VUSB_DP-VUSB_DM)
Differential common mode range	VCM	0.8	-	2.5	V	Include VDI range
Output "H" voltage 1	VOH1	VDDIO-0.4	-	VDDIO	V	IOH1=-1.0mA(DC), Normal type output (Including output mode of I/O terminal)
Output "L" voltage 1	VOL1	0.0	-	0.4	V	IOL1=1.0mA(DC), Normal type output (Including output mode of I/O terminal)
Output "H" voltage 2	VOH2	VDDIO-0.4	-	VDDIO	V	IOH2=-2.0mA(DC), CAMCKO
Output "L" voltage 2	VOL2	0.0	-	0.4	V	IOL2=2.0mA(DC), CAMCKO
Output "H" voltage 3	VOH3	VDDIO-0.4	-	VDDIO	V	IOH3=-4.0mA(DC), SD_CLK
Output "L" voltage 3	VOL3	0.0	-	0.4	V	IOL3=4.0mA(DC), SD_CLK
Output "H" voltage 4	VOH4	2.8	-	VDDIO	V	IOH4=-2.53mA(DC), USB_DP,USB_DM
Output "L" voltage 4	VOL4	0.0	-	0.3	V	IOL4=2.53mA(DC), USB_DP,USB_DM
VREF PIN voltage	VVREF	0.475*AVDD	0.5*AVDD	0.525*AVDD	V	IOUT=0A(no load),VREF
Analog output voltage range	VAOUT	0.47*AVDD	0.5*AVDD	0.53*AVDD	V	IOUT=0A(no load). In Silence
Output load for analog output	RAOUT	10	-	-	KOhm	R_OUT,L_OUT,MONO_OUT

• External Dimensional Drawing and Mark Drawing



• Block Diagram



• Land No. and Pin Name

REV. A

Land No.	Pin Name
B3	A1
B5	A2
E5	ADVB
F10	CAMCKI
E11	CAMCKO
E10	CAMD0
C11	CAMD1
D10	CAMD2
C10	CAMD3
B11	CAMD4
E9	CAMD5
E8	CAMD6
B10	CAMD7
F9	CAMHS
G11	CAMRST
G9	CAMVS
E4	CSB
E1	D0
E2	D1
D4	D10
C4	D11
B4	D12
A3	D13
D5	D14
C5	D15
E3	D2
D1	D3
D3	D4
C2	D5
B1	D6
B2	D7
C3	D8
A2	D9
G4	DACMCK
H4	DCLK
G3	DIGCK
H1	DIGDIN
H3	DIGDOUT
G2	DIGLR
L5	FL_CEB

Land No.	Pin Name
K6	FL_RB
J1	FSYNC
F5	INT
K1	L_OUT
K7	LCDA0
F7	LCDCS1B
G7	LCDCS2B
L7	LCDD0
F8	LCDD1
G8	LCDD2
L8	LCDD3
K8	LCDD4
J7	LCDD5
L9	LCDD6
L10	LCDD7
H8	LCDD8
K9	LCDD9
K10	LCDD10
K11	LCDD11
J8	LCDD12
J9	LCDD13
J11	LCDD14
J10	LCDD15
H9	LCDD16
H10	LCDD17
H7	LCDRDB
L6	LCDWRB
F3	LED0
K2	MONO_OUT
J2	PCMDIN
A5	PLL_FILTER
G5	R_OUT
F1	RDB
F4	RESETB
L4	SD_CLK
K5	SD_CMD
J5	SD_DAT0
F11	SDA
G10	SDC
C9	TE_HSYNC

Land No.	Pin Name
B9	TE_PIXCLK
D9	TE_VSYNC
A9	TED0
D8	TED1
C8	TED2
A8	TED3
B8	TED4
A7	TED5
E7	TED6
D7	TED7
J6	TEST
K4	USB_DM
L3	USB_DP
F6	USB_RDY
G1	VIB0
H5	VREF
F2	WRB
B7	XIN1
C6	XIN2
B6	XOUT1
D6	XOUT2
L2	AVDD
D2	VDD
H6	
D11	
H2	VDDIO1
A4	
J4	VDDIO2
H11	
A10	
J3	VDDIO3
A6	VDDIO4
L1	AVSS
K3	
A1	GND
G6	
L11	
A11	
C7	
E6	VSS4

• Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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