MOTOROLA

Advanced Information

Advanced Digital Video Encoder

Y/Cb/Cr Output Support
HCMOS Technology

MC44722A
MC44723A

FT SUFFIX
48 QFP
(0.8mm Pitch)

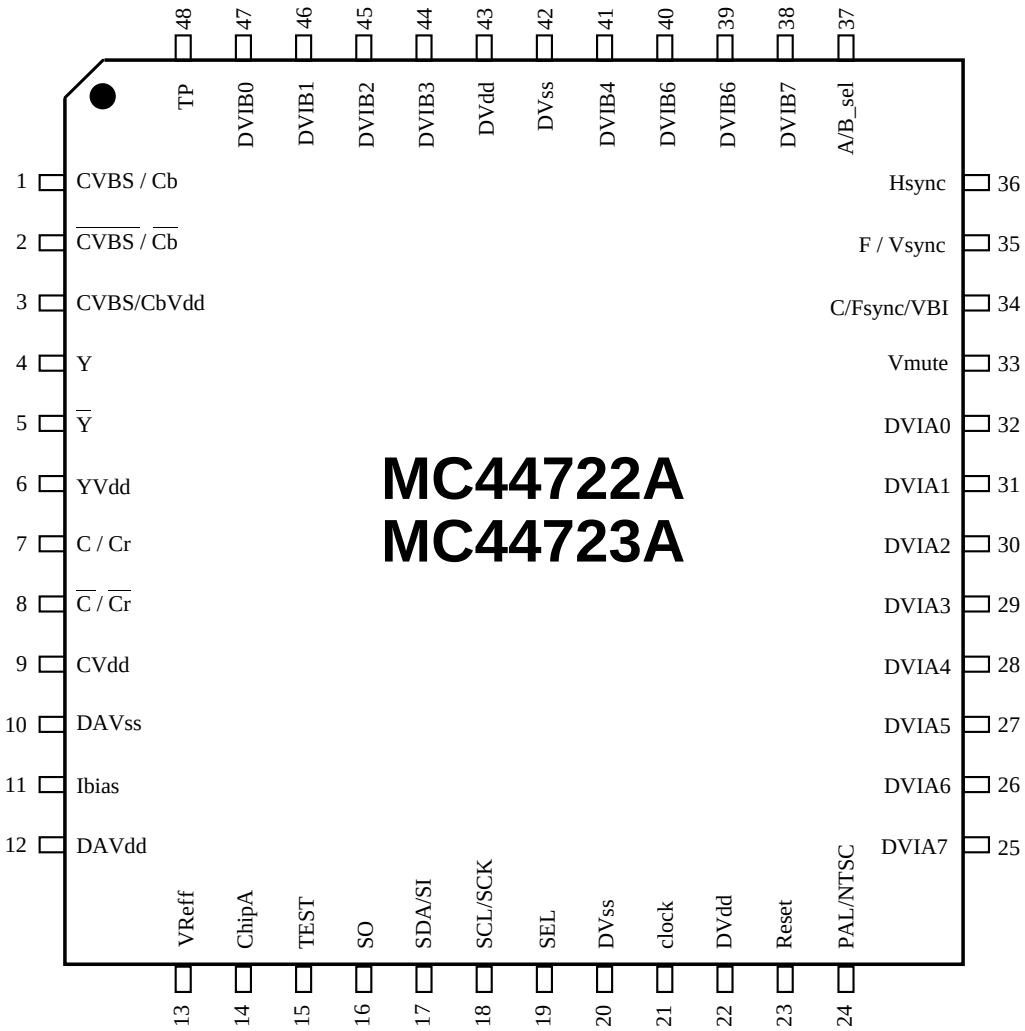
VFU SUFFIX
48 VQFP
(0.5mm Pitch)

The MC44722A and MC44723A are advanced Digital Video Encoders (DVE). They convert ITU-601/656 standard 4:2:2 Bit-Paralellel data into analog composite video, S-Video or analog component signals Y/Cb/Cr in PAL and NTSC formats. They accept the multiplexed two 8-bit or 16-bit ((CB,Y,CR)Y) signals from digital sources such as MPEG decoders and can act as a sync generator master or as a sync slave. All video processing is done digitally and requires no external adjustment.

Specifically designed for digital satellite, digital cable decoders, multimedia terminals and DVD players.

- World Wide Operation (PAL-BDGHI, PAL-N,PAL-M, NTSC-M)
- SMPTE 170M / ITU - R 624 composite video output
- Programmable Color Sub-carrier Frequencies
- Analog standard timing for Horizontal, Vertical, Frame and Composite Sync Outputs
- Sync Extraction From Digital Input Data (SAV, EAV)
- Sync Polarity and Horizontal / Vertical Phase Control
- Master or Slave Sync (H/Vsync, H/Fsync, ITU-R656 Slave) Operation
- Interlaced or Non-Interlaced Support
- 625/50 or 525/60 ITU-601/656 two 8-bit or 16-bit ((CB,Y,CR)Y) Digital Input
- Luma 2X / Chroma 4X Output interpolating Filter
- Dual Digital A / B selectable inputs
- External VBI Information Data Input (Teletext Information Data)
- Selectable One set of Signal within (CVBS/Y/C) or (Y/Cb/Cr)
- Selectable Analog Component Output (Beta Cam or MII Component Interface Level)
- Three Analog Outputs Through 10-bit DACs
- Easily programmed via Serial Bus (I2C or 4-Wired SPI Bus)
- 2 Hardware selectable I2C Chip Addresses
- Closed-Caption, CGMS and WSS Information data Insertion
- MACROVISION ver. 7.01 Anti-Copy Signal Insertion(MC44722A Only)
- On Chip Color - bar Generator
- 5V Tolerante Input
- +3.3V Power Supply or +3.3V(Digital)/+5V(Analog) Power Supply
- Pin Compatible with MC44722/3

[Pin Assignment]

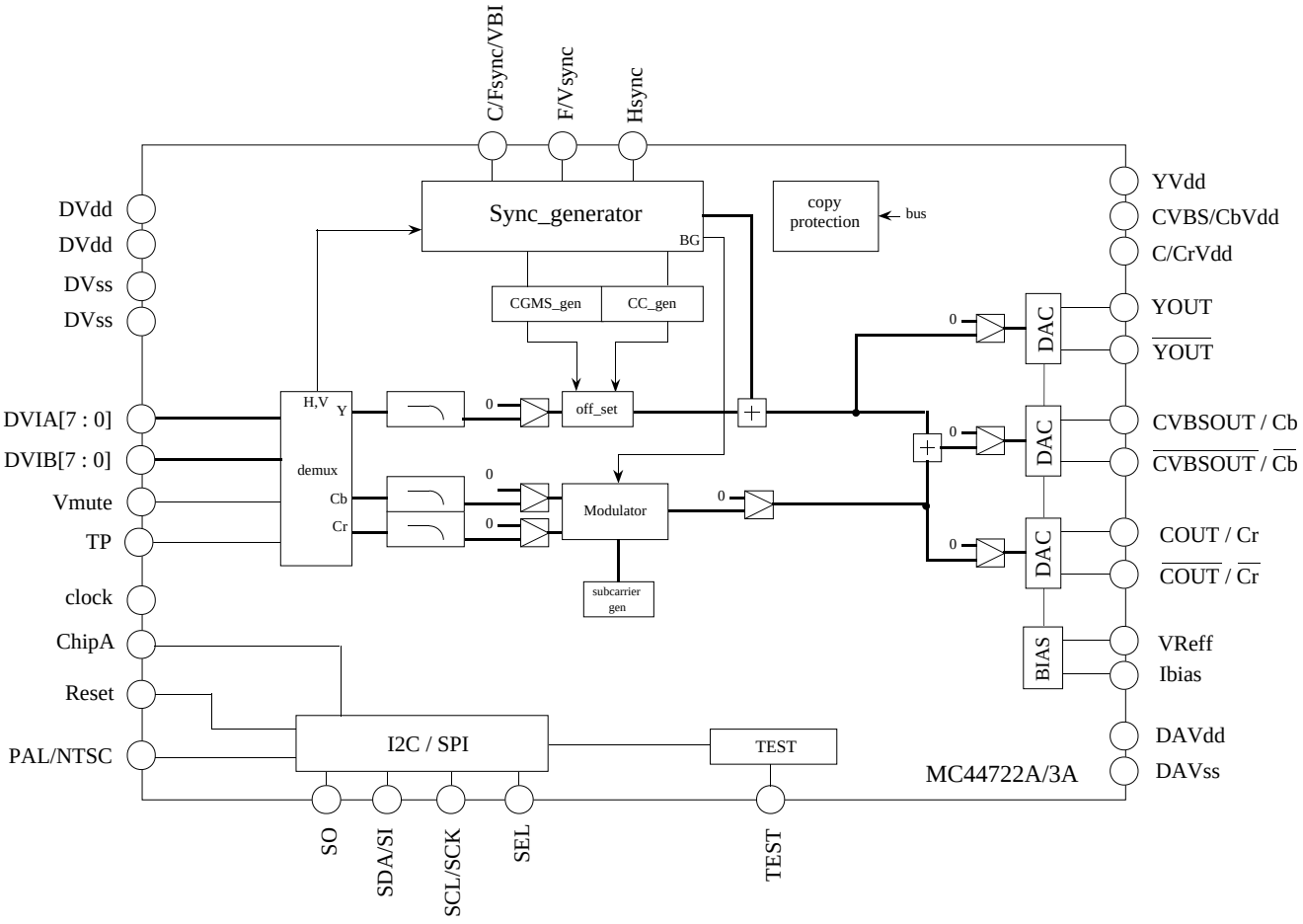


[Pin Descriptions]

PIN	NAME	I/O	DESCRIPTIONS
1	CVBS / Cb	O	Analog composite video signal output or Cb signal output current drive(positive)
2	$\overline{\text{CVBS}}$ /$\overline{\text{Cb}}$	O	Analog composite video signal output or Cb signal output current drive(negative)
3	CVBS/CbVdd		Power Supply for CVBS / Cb DAC circuit
4	Y	O	Analog luminance signal output current drive(positive)
5	$\overline{\text{Y}}$	O	Analog luminance signal output current drive(negative)
6	YVdd		Power Supply for Y DAC circuit
7	C/Cr	O	Analog chrominance signal output or Cr signal output current drive(positive)
8	$\overline{\text{C}}$/$\overline{\text{Cr}}$	O	Analog chrominance signal output or Cr signal output current drive(negative)
9	C/CrVdd		Power Supply for C / Cr DAC circuit
10	DAVss		Ground for DAC circuit
11	Ibias	O	Reference current for the 3 DACs
12	DAVdd		Power Supply for DAC circuit
13	VReff		Reference full scale voltage for the 3 DACs
14	ChipA		I2C chip address select { 0 : 42(hex)/43(hex) 1 : 1C(hex)/1D(hex) }
15	TEST	I	TEST pin(Ground)
16	SO	z(O)	If SPI mode, serial data output / If I2C mode, connect to Ground
17	SDA/SI	I/O(I)	Serial data input, Open drain output / If SPI mode, serial data input
18	SCL/SCK	I	Serial clock
19	SEL	(I)	Connect to Ground / If SPI mode, this pin is chip select
20	DVss		Ground for Digital circuit
21	CLOCK	I	27MHz clock input
22	DVdd		Power Supply for Digital circuit
23	Reset	I	Reset signal, active LOW
24	PAL/NTSC	I	NTSC/PAL select . This pin active only Reset time. (NTSC : Low PAL : High)
25~32	DVIA7~0	I	8-bit Multiplexed Y/Cr/Cb 4:2:2 data(ITU Rec656) input(DVIA) or Multiplexed Y data
			(ITU- Rec656/601) input in 16-bit input mode (DVIA7 : MSB)
33	Vmute	I	Video mute on Reset (0 : nomal, 1 : mute), or TEST data input
34	C/Fsync/VBI	I/O	Csync/Frame sync output or external VBI information input
35	F/Vsync	I/O	Frame sync or Vertical sync input/output
36	Hsync	I/O	Horizontal sync input/output
37	A/B_sel	I/O	Switch control for 8-bit X 2 Multiplexed Y/Cr/Cb 4:2:2 data(ITU- Rec656) input
			(DVIA) or (DVIB) , or test data I/O
38~41	DVIB8~5	I/O	8-bit Multiplexed 4:2:2 data(ITU- Rec656/601) input(2), or Multiplexed Cr/Cb data
			(ITU- Rec656/601) input in 16-bit input mode (MSB: DVIB8), or Test data input/output
42	DVss		Ground for Digital circuit
43	DVdd		Power Supply for Digital circuit
44~47	DVIB4~1	I/O	8-bit Multiplexed 4:2:2 data(ITU- Rec656/601) input(DVIB), or Multiplexed Cr/Cb
			data(ITU- Rec656/601) input in 16-bit input mode (LSB:DVIB1), or Test data I/O
48	TP	I/O	for test (should be ground)

Note : Power Supply Group Digital ---> 22-pin, 43-pin,
Analog ---> 3-pin, 6-pin, 9-pin, 12-pin

[Block Diagram]



I2C/SPI chip-address 42/43(hex)
1C/1D(hex)

[Function Descriptions]

Clock

27.0MHz. This signal on the clock pin needs to be active and stable for 5 cycles before the reset pin is de-asserted.

Reset Procedure

RESET is a level sensitive input pin. Driving the RESET pin low causes a DVE reset. The 27Mhz DVE clock signal must be active before RESET is released. De-asserting reset will latch the status of the PAL/ NTSC, Vmute and SEL pins.

The PAL/NTSC pin determines the default values for the DVE control registers. The default register values have been chosen so that standard PAL or NTSC video will appear at the DAC outputs immediately when a valid input digital video data stream is present and Vmute is Low at reset.
The Vmute pin controls the "out of reset" operation of the Analog output signals. When "1" at reset, the video output is muted - output signal is "black - sync". When "0" at reset, the video output is from the input video data. This control can be used to mute the disable noise signals from a MPEG decoder at reset until a clear and stable picture is available.
The value on the SEL pins determine the default serial communication mode. If Low, the DVE use I2C bus operation. If High, the DVE use 4-wired SPI operation.

After reset, the VBI signals (Closed-Caption, CGMS and WSS) are disabled.

(see page --- for sub-address register descriptions.)

Fig 1 : DVIA/DVIB Data Input Timing

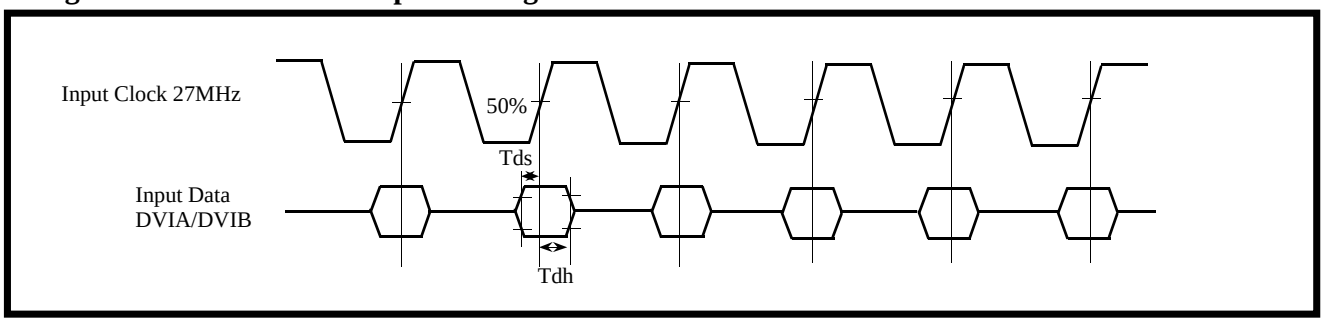
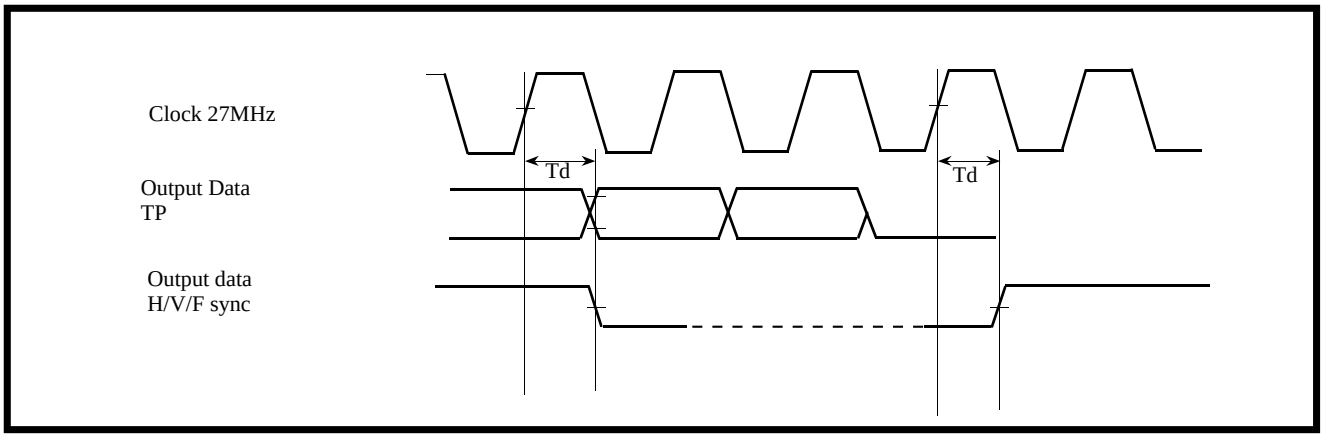


Fig 2 : Sync Data Output Timing



Input Data Format

The input digital video is in accord with the ITU-R Rec.656 and SMPTE 125M standards. It is two 8-bit or 16-bit multiplexed 4:2:2 ((CB,Y,CR)Y) data stream. Samples are latched on the rising edge of the clock signal. Data is input on pins **DVIA[7 : 0]** and **DVIB[7 : 0]**
(see figures 3 and 4 for sub-address register descriptions.)

Video Timing / Sync Generator

The DVE outputs PAL-B,D,G,H,I, PAL-N, PAL-M or NTSC-M standard video signals.
The DVE sync generator can be operated in two sync modes, master or slave.
In master mode, the DVE generates all the correct Horizontal and Vertical or Frame sync signals internally, and outputs the Csync signal through the C/Fsync/VBI pin(C/Fsync).
In slave mode, the DVE derives the sync signals from the Bit-Parallel input data stream Start Active Video (SAV) and End Active Video (EAV) data packet information. Sync signals are output on the Hsync and F/Vsync or C/Fsync/VBI pins and can be programmed for positive or negative polarity. The phase of Hsync can also be controlled.
Also, the DVE allows more two slave modes. One is H/Vsync slave, and the another is H/Fsync slave mode.
Vertical Blanking corresponds to the following lines.

625/50 624-22 311-335 ITU-R line numbering
525/60 1-19 264-282 SMPTE line numbering

(see figures 3,4,5,6,7,8,9,10, and 11 for sub-address register descriptions.)

Fig 3 : Digital Input Timing(525/60 system) in Master Mode 70(hex){[1:0]=01}

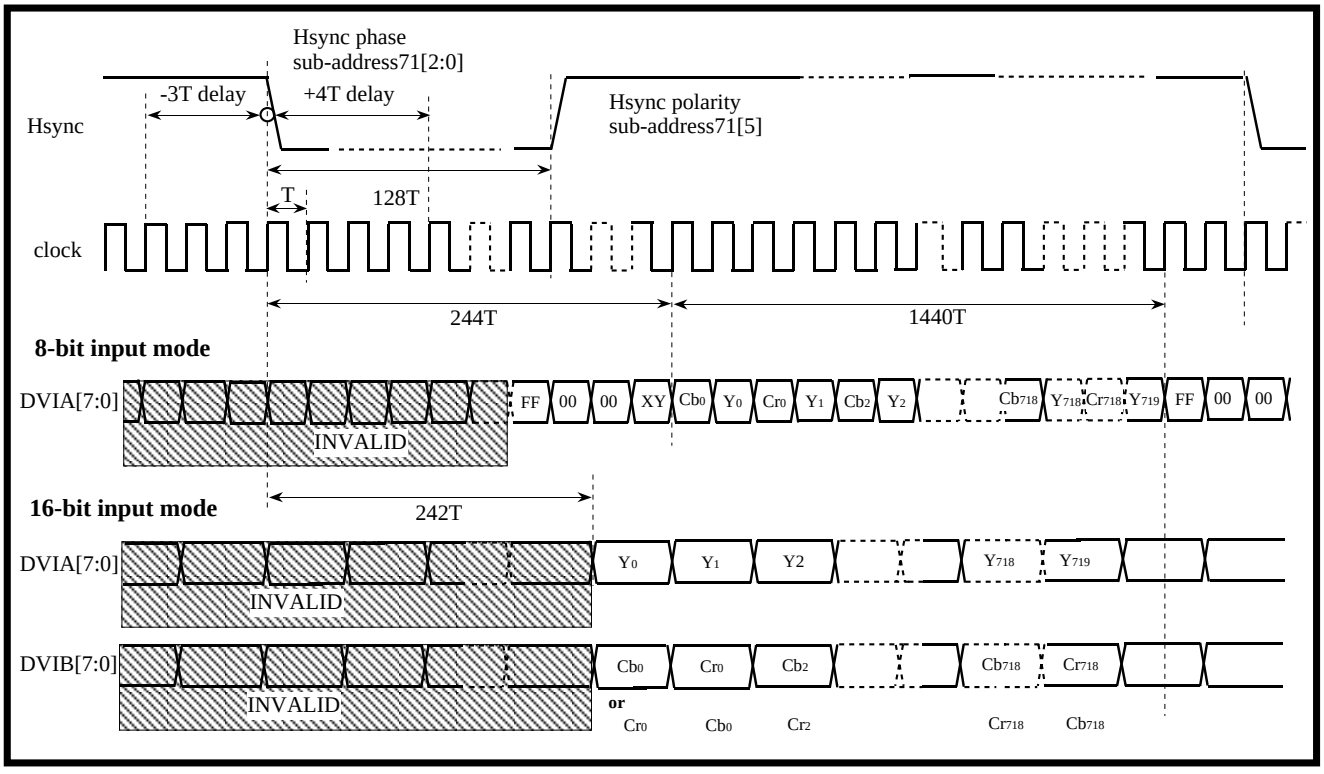


Fig 4 : Digital Input Timing(625/50 system) in Master Mode 70(hex){[1:0]=01}

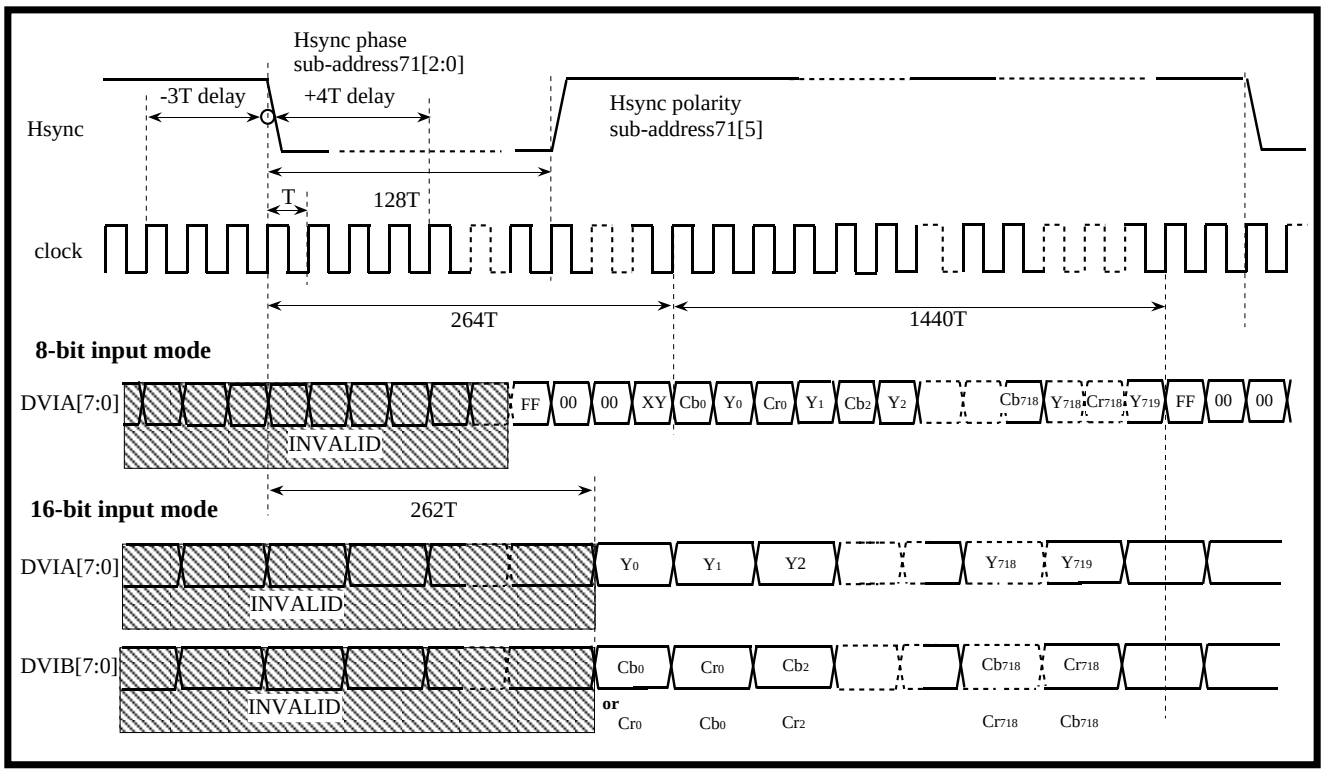


Fig 5 : Sync Timing::525/60 Interlaced System in Master Mode sub-address71[7] =0

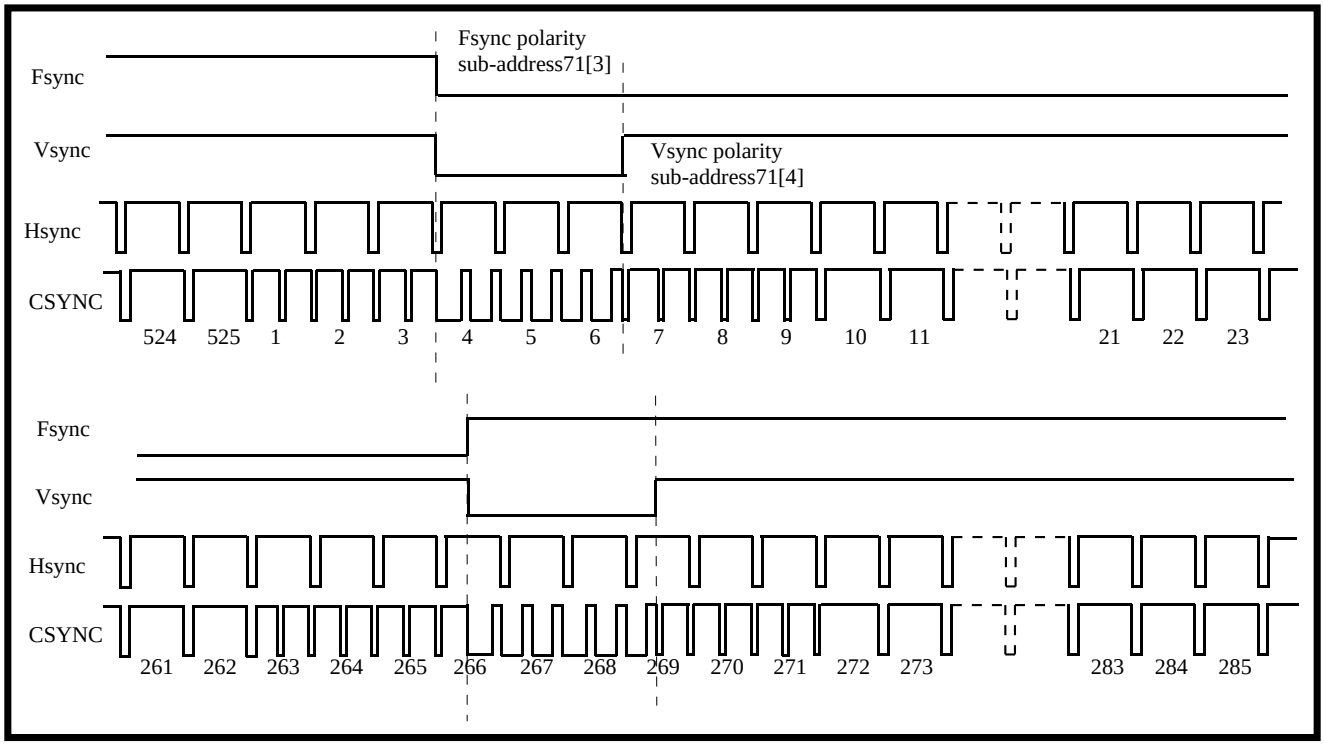


Fig 6 : Sync Timing::625/50 Interlaced System in Master Mode sub-address71[7] =0

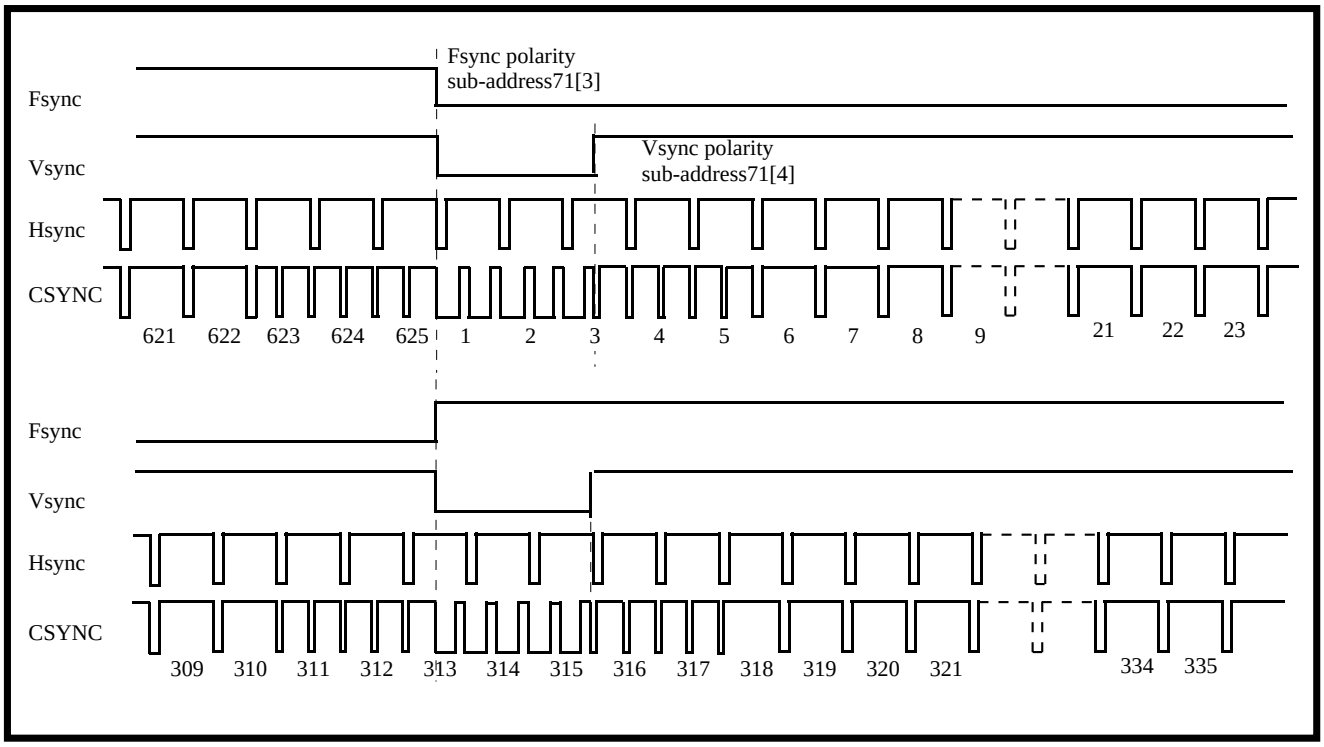


Fig 7 : Sync Timing::525/60 Non-interlaced System in Master Mode sub-address71[7] =1

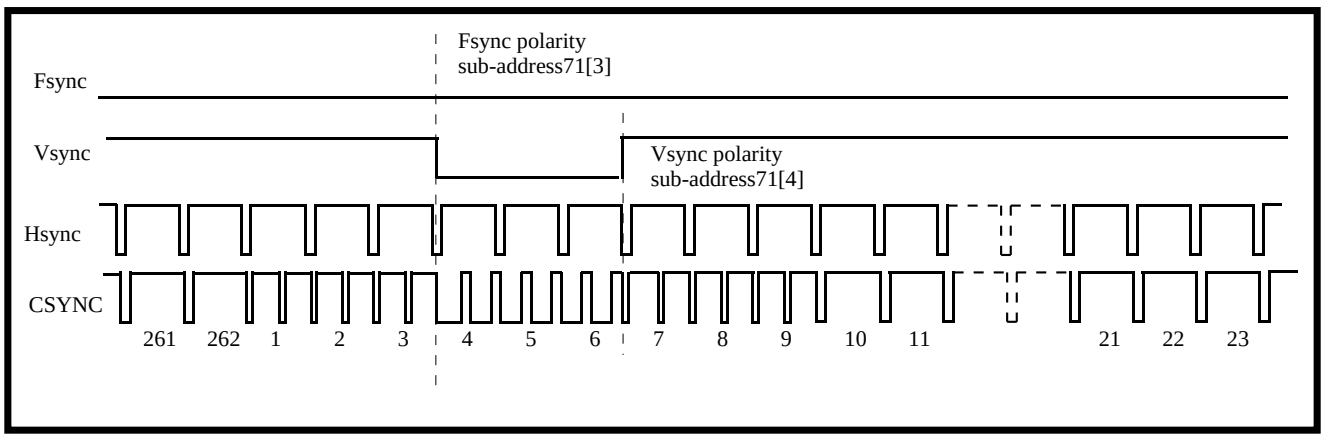


Fig 8 : Sync Timing::625/50 Non-interlaced System in Master Mode sub-address71[7] =1

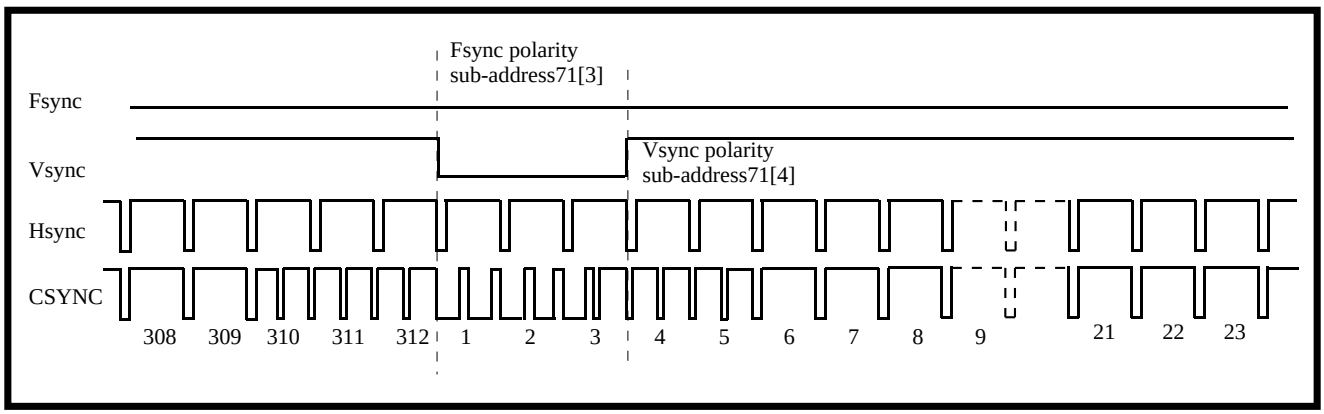


Fig 9 : Analog Sync Timing::Rise and fall

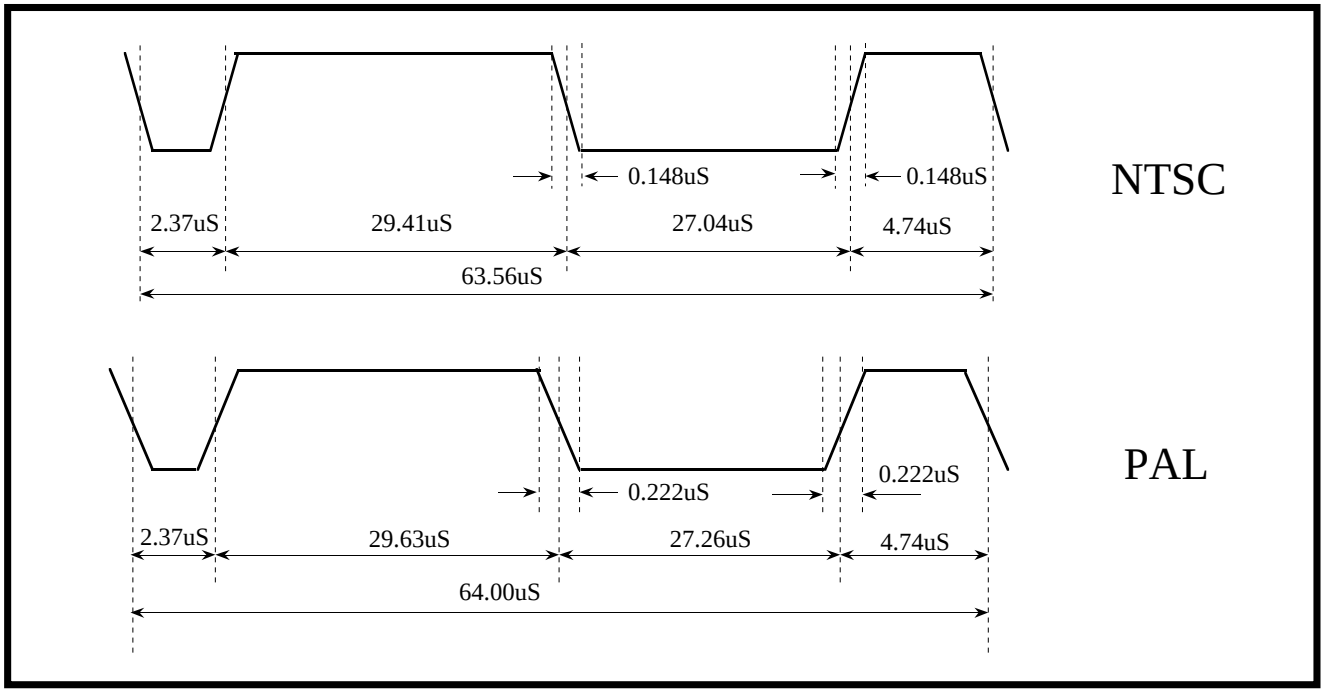


Fig 10 : Sync Timing::525/60 Interlaced System in Slave Mode sub-address71[1:0] =10, 11

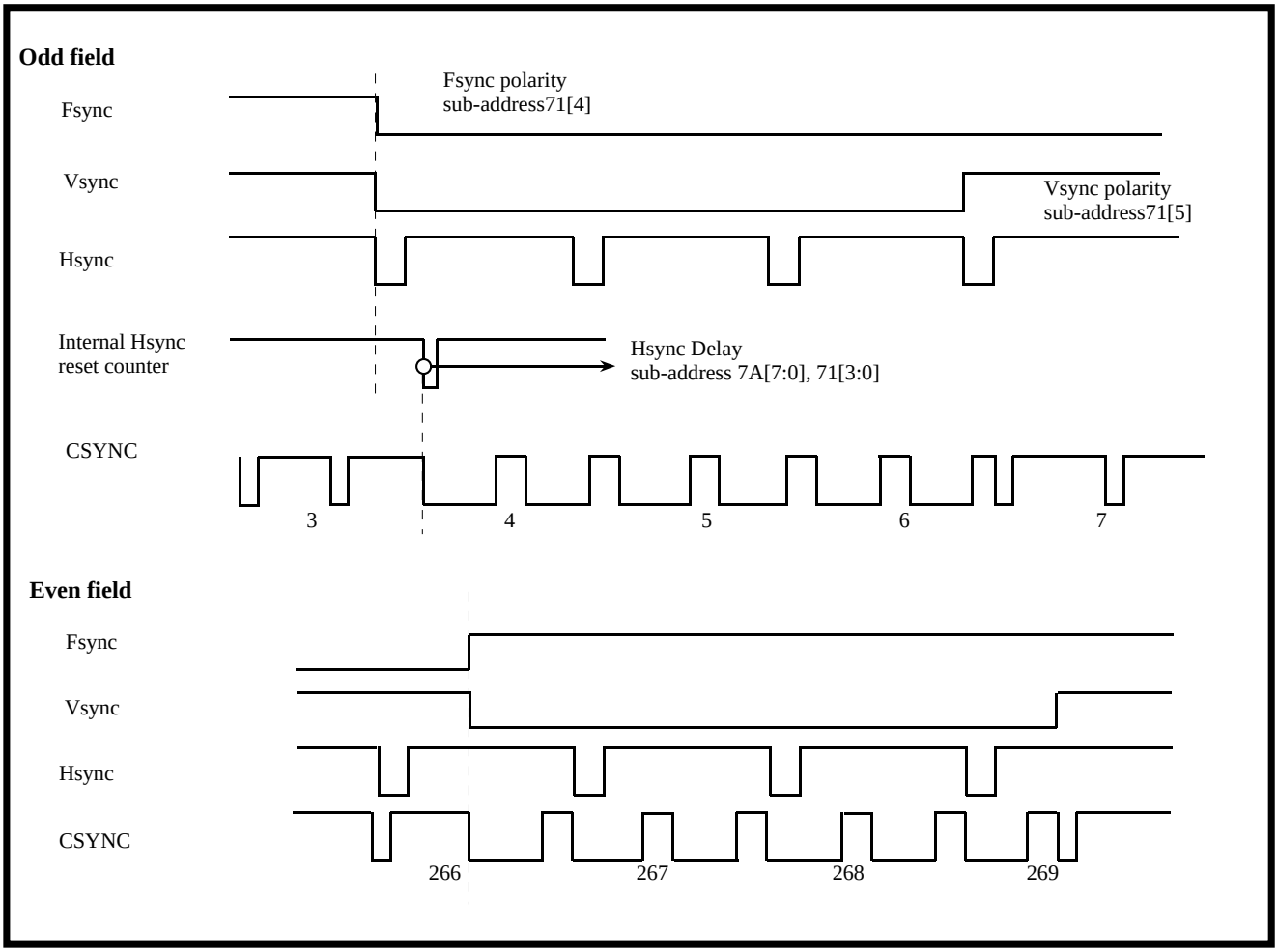
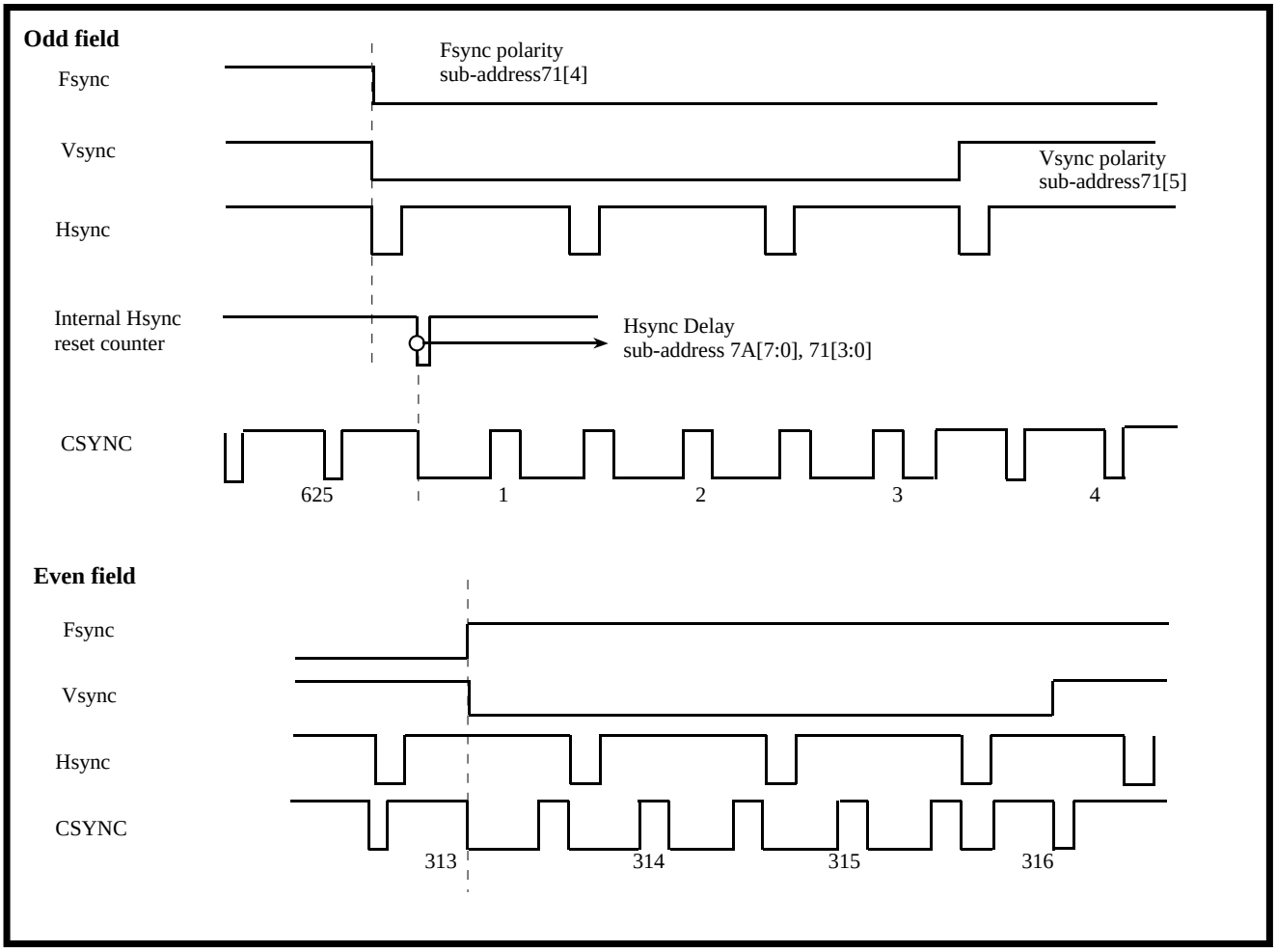


Fig 11 : Sync Timing::625/50 Interlaced System in Slave Mode sub-address71[1:0] =10, 11



Chroma / Luma Encoding

The DVE de-multiplexes the 4:2:2 digital video data stream.

The de-multiplexed Y or Luma samples are interpolated at the clock rate. Offset compensation is then added, next any VBI signals consisting of Closed-Caption, CGMS and WSS are added to the appropriate lines, then finally composite sync pulses are added to the Luma signal.(see figure 14.)

De-multiplexed component color CB and CR samples are interpolated at the clock rate.

The Luma and Chroma Interpolation filter compensate for the sin(x)/x attenuation to on chip D/A converter and simplify the output filter and allows more accurate encoding. A set of 3 different filters is available for each Luma and Chroma filtering. And user can select within these filters to fit a wide variety of applications. (see figure 12 and 13, and sub-address resister 6F)

The DVE generates the necessary subcarrier color frequency for PAL or NTSC encoding from the 27Mhz system clock. This color subcarrier is then modulated by the base band component color CB and CR signals to create the video Chroma signal. (see figure 15.)

A 7.5 IRE pedestal is added for the 60Hz field rate. This can be added for the 50Hz field rate through serial bus control. (see sub-address register descriptions)

Fig. 12 Luma Filtering Including DAC Attenuation

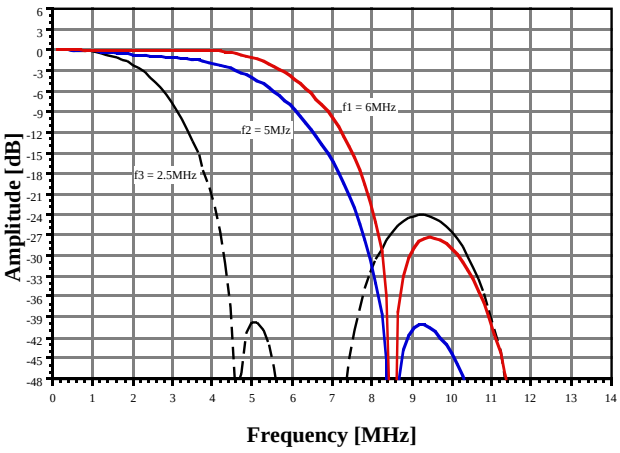
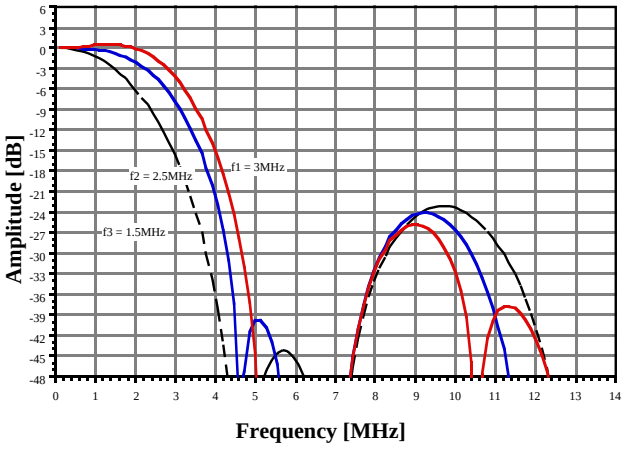


Fig. 13 Chroma Filtering



"CVBS and S-VIDEO" or "YCbCr" Outputs

The internal digital video signals drive 10-bit D/A converters. Converter outputs are bidirectional current sources where the current is proportional to the digital data with reference to the IBIAS reference current. The pins CVBS/Cb, Y and C/Cr are the respective composite, Luma and Chroma or Y/Cb/Cr signal current source pins. Each of the DACs can drive **75ohm** load resister.

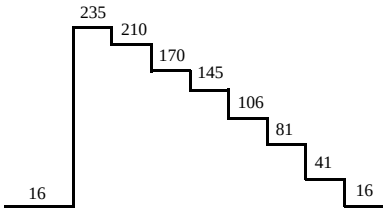
User can select 1 sets of signals from the above 2 signal sets (CVBS/Y/C or Y/Cb/Cr).
(see "Application Diagram" and "sub-address register descriptions".)

In Y/Cr/Cb analog component output mode, user can select one of the component interface level , Beta Cam or M2 format (see sub-address register 6E).

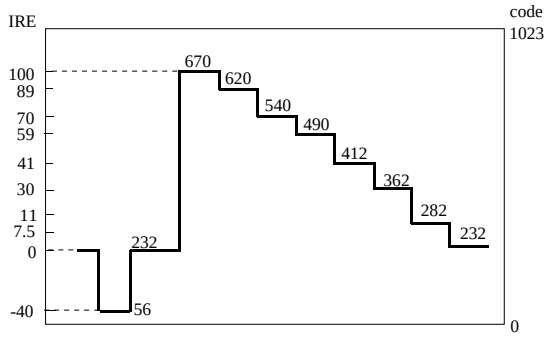
Bias Current Gain

DACs can be switched off through serial bus control to reduce power consumption. Both outputs of unused DACs should be connected to ground through a resister to avoid charge buildup.

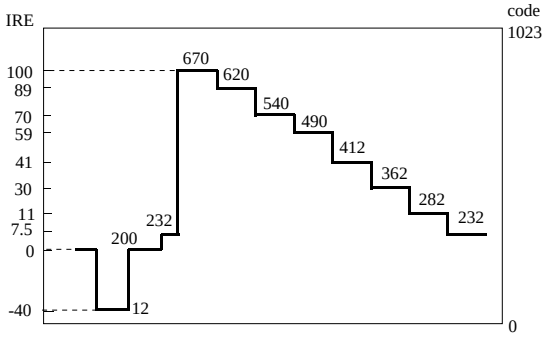
Fig 14 : Luminance Output Range



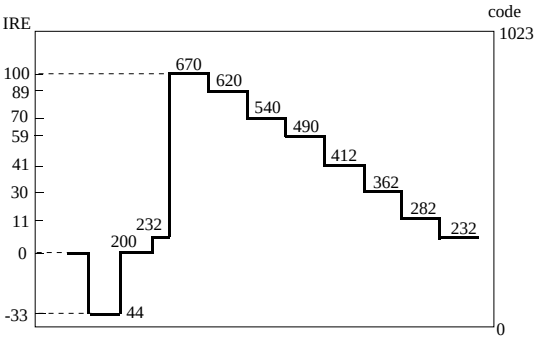
Digital Y input code(16~235)
525/60 and 625/50 system
100%amplitude,100%saturation color bar



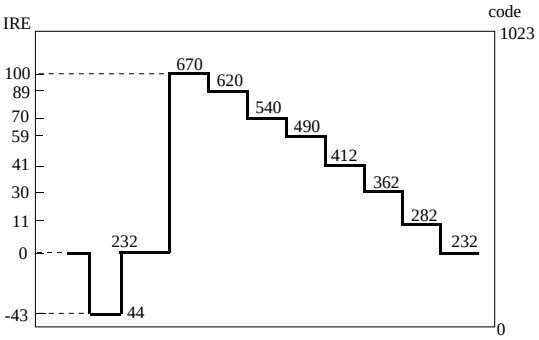
Analog Y output level(525/60 system)
100%amplitude,100%saturation color bar
=> 7.5IRE Setup Off



Analog Y output level(525/60 system)
100%amplitude,100%saturation color bar
=> 7.5IRE Setup On

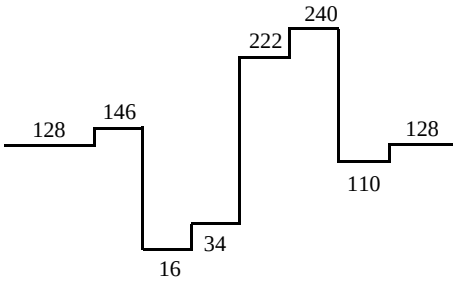


Analog Y output level(625/50 system)
100%amplitude,100%saturation color bar
=> 7.5IRE Setup On

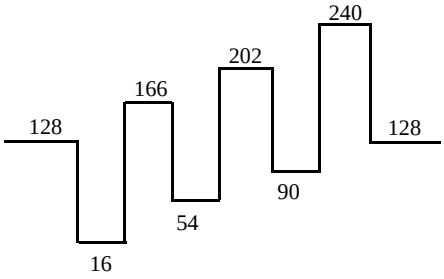


Analog Y output level(625/50 system)
100%amplitude,100%saturation color bar
=> 7.5IRE Setup Off

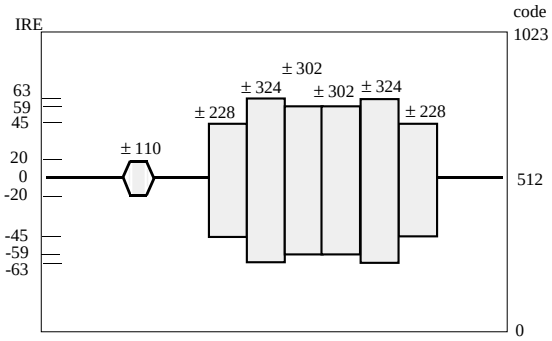
Fig 15 : Chrominance Output Range



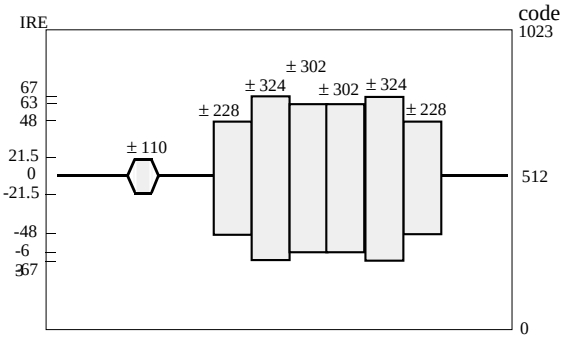
Digital Cr-input code(16~240)
525/60 and 625/50 system
100%amplitude,100%saturation color bar



Digital Cb-input code(16~240)
525/60 and 625/50 system
100%amplitude,100%saturation color bar

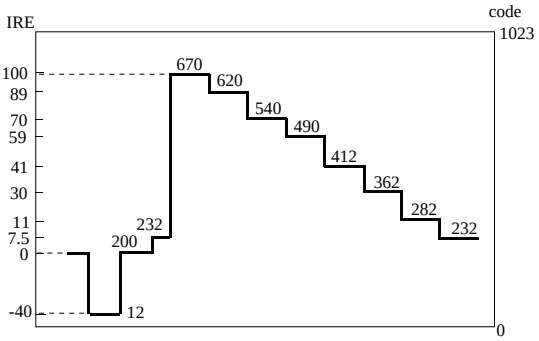


Analog C output level(525/60 system)
100%amplitude,100%saturation color bar
=> 7.5IRE Setup Off/On

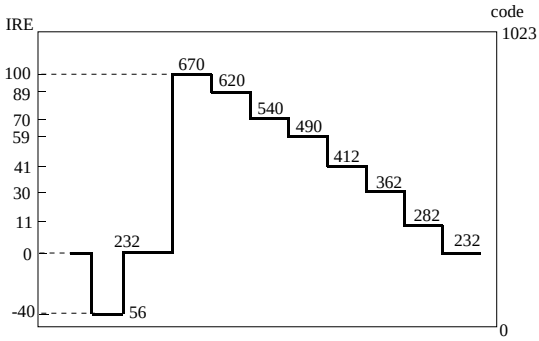


Analog C output level(625/50 system)
100%amplitude,100%saturation color bar
=> 7.5IRE Setup On/Off

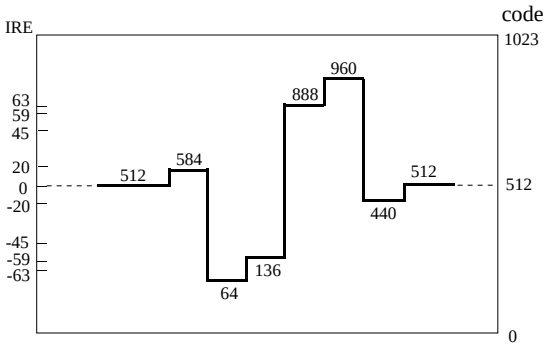
Fig 16 : Y/Cb/Cr Output Range (Beta Cam Component Interface Level)



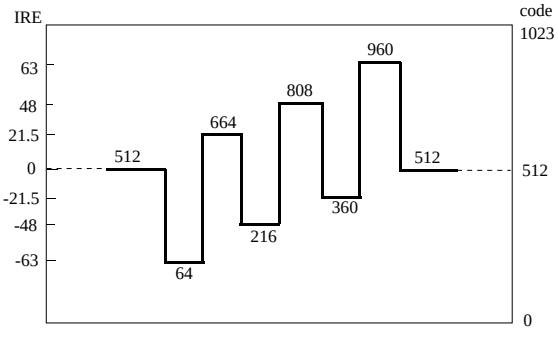
Analog Y output level
100%amplitude,100%saturation color bar
=> 7.5IRE Setup On



Analog Y output level
100%amplitude,100%saturation color bar
=> 7.5IRE Setup Off

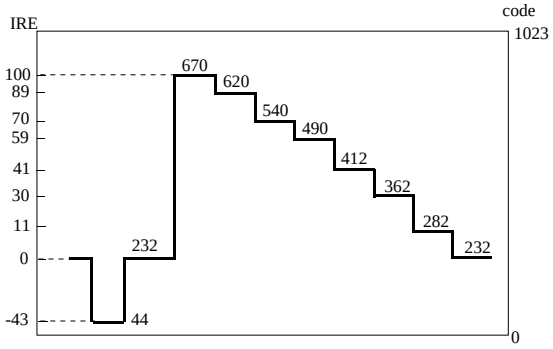


Digital Cr-input code
100%amplitude,100%saturation color bar
=> 7.5IRE Setup On/Off

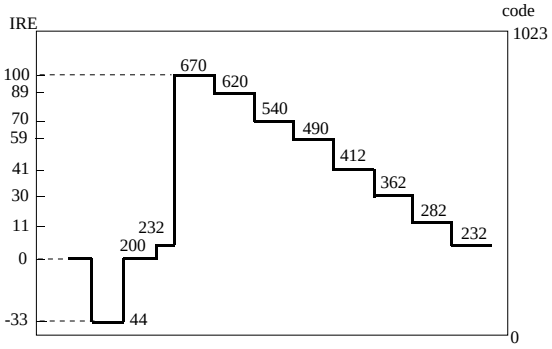


Digital Cb-input code
100%amplitude,100%saturation color bar
=> 7.5IRE Setup On/Off

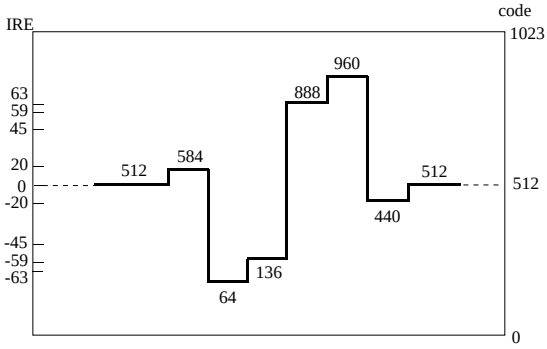
Fig 17 : Y/Cb/Cr Output Range (M2 Component Interface Level)



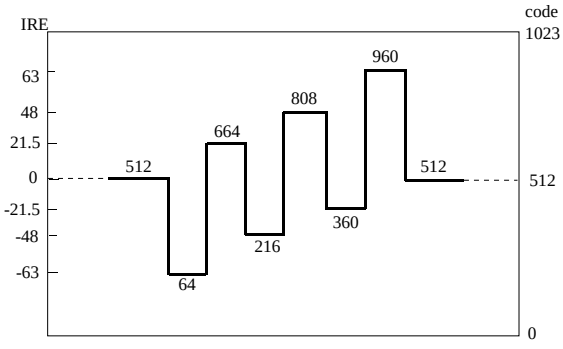
Analog Y output level
100%amplitude,100%saturation color bar
=> 7.5IRE Setup Off



Analog Y output level
100%amplitude,100%saturation color bar
=> 7.5IRE Setup On



Digital Cr-input code
100%amplitude,100%saturation color bar
=> 7.5IRE Setup On/Off



Digital Cb-input code
100%amplitude,100%saturation color bar
=> 7.5IRE Setup On/Off

Copy Generation Management System (CGMS) Encoding

CGMS signals can be encoded by the DVE onto output video line 20 (525 / 60 for Japan).
CGMS identification signals also identify and control the TV screen presentation mode - wide screen, letter box and or normal -16:9 or 4:3.
Data is Double-Buffered and is latched at the start of Field 1.

CRC code is generated by controling $88 [0] CGMS_parity bit automatically.

(see figures 24 for sub-address register descriptions.)

Wide Screen Signaling (WSS) Encoding

WSS signals can be encoded by the DVE onto output video line 23 (625 / 50 for Europe).
WSS identification signals also identify and control the TV screen presentation mode - wide screen, letter box and or normal -16:9 or 4:3.
Data is Double-Buffered and is latched at the start of Field 1.

Odd parity code is generated by controling $88 [1] WSS_parity bit automatically.

(see figures 25 for sub-address register descriptions.)

Closed-Caption Encoding

Closed-Captioned or Extended Data Service signals can be encoded by the DVE onto output video line 21/284 (NTSC) and line 22/335 (PAL). The CC data is input through the serial bus interface. Two 8-bit byte data pairs are encoded for each field. There are four registers for holding the data - two bytes per field. The serial data is 7bit US-ASCII MSB first, proceeded by an odd parity bit. Total 8-bits. (P-7-6-5-4-3-2-1-0)

The DVE automatically generates the required clock run in and start bit for CC encoding. (see figure 16.) When Closed-Captioning is enabled, the system micro processor (uP) should update the CC data once each frame. This DVE will automatically NULL characters when there is no CC data to encoder after the CC data has been processed by setting the $87[5] register.

It is recommended to write CC data only to the inactive frame. Field1 and Field2 data are double-buffered by the Frame sync falling edge of previous Frame, updating Frame 2 data during Frame1 display and Frame1 data during Frame2 display.

When the $87[4] register is set, the DVE will generate the parity bit automatically.

(see figures 26 and 27 for sub-address register descriptions.)

Serial Control Bus

Control of the DVE device is accomplished through the **I2C-Bus** or 4-wired **SPI** serial bus.
In I2C mode, pins **SDA** and **SCL** are the respective data and clock signals. Device address can be 42(hex)/43(hex) or 1C(hex)/1D(hex) . Slave address is chosen at reset by the state of the ChipA pin signal { 0 : 42(hex)/43(hex), 1 : 1C(hex)/1D(hex) }
Sub-address register read and write operations are documented in the following figures 22a - 22b.

In SPI mode, pins SO, SI, SCK and SEL are the respective data input, output, serial clock and chip select signals. Register read and write operations are documented in the following figures 23a - 23b

MACROVISION™ Copy Protection

When enabled, the Luma and Chroma signals are modified according to the MACROVISION ™ copy protection process for Pay Per View (PPV) and DVD applications revision **7.01** dated Sep 6th , 1996.

Enabling and control is through the serial control bus.

No MC44722A parts will be sent to the customer until the customer provides MOTOROLA with written confirmation of a license, non-disclosure or a waiver from MACROVISION ™.

The MC44723A device is available without MACROVISION ™ encoding.

Fig 18-a : I2C-BUS Interface Write operation Timing

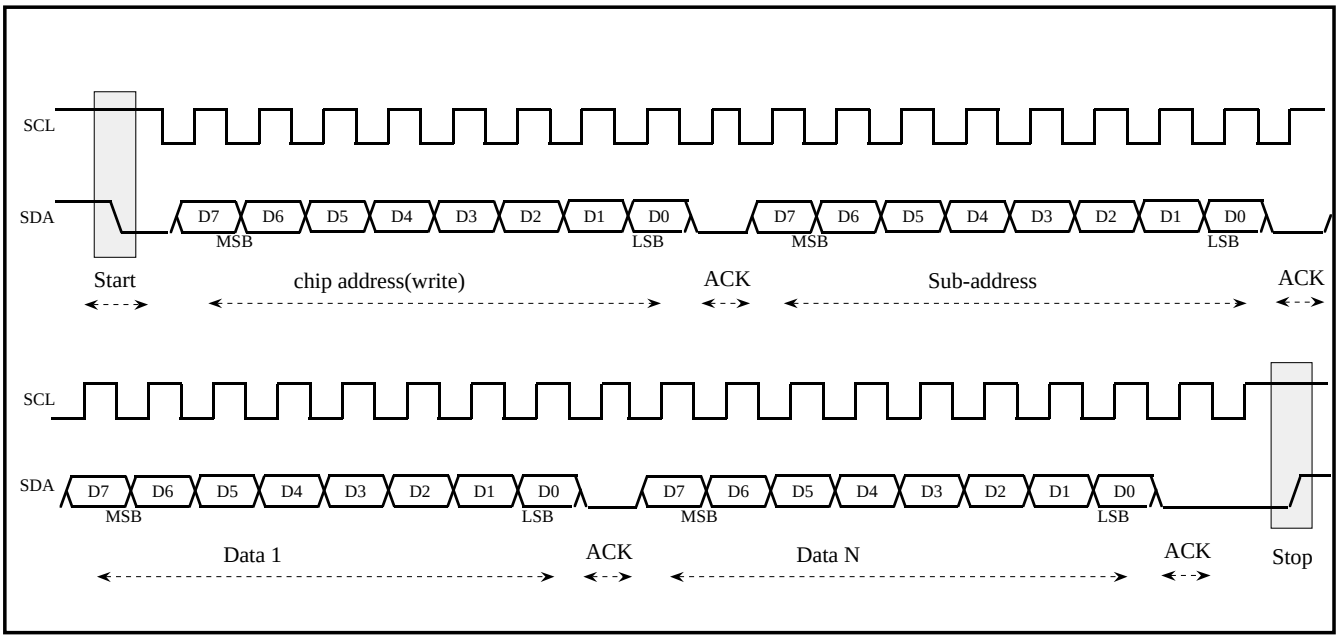


Fig 18-b : I2C-BUS Interface Read operation Timing

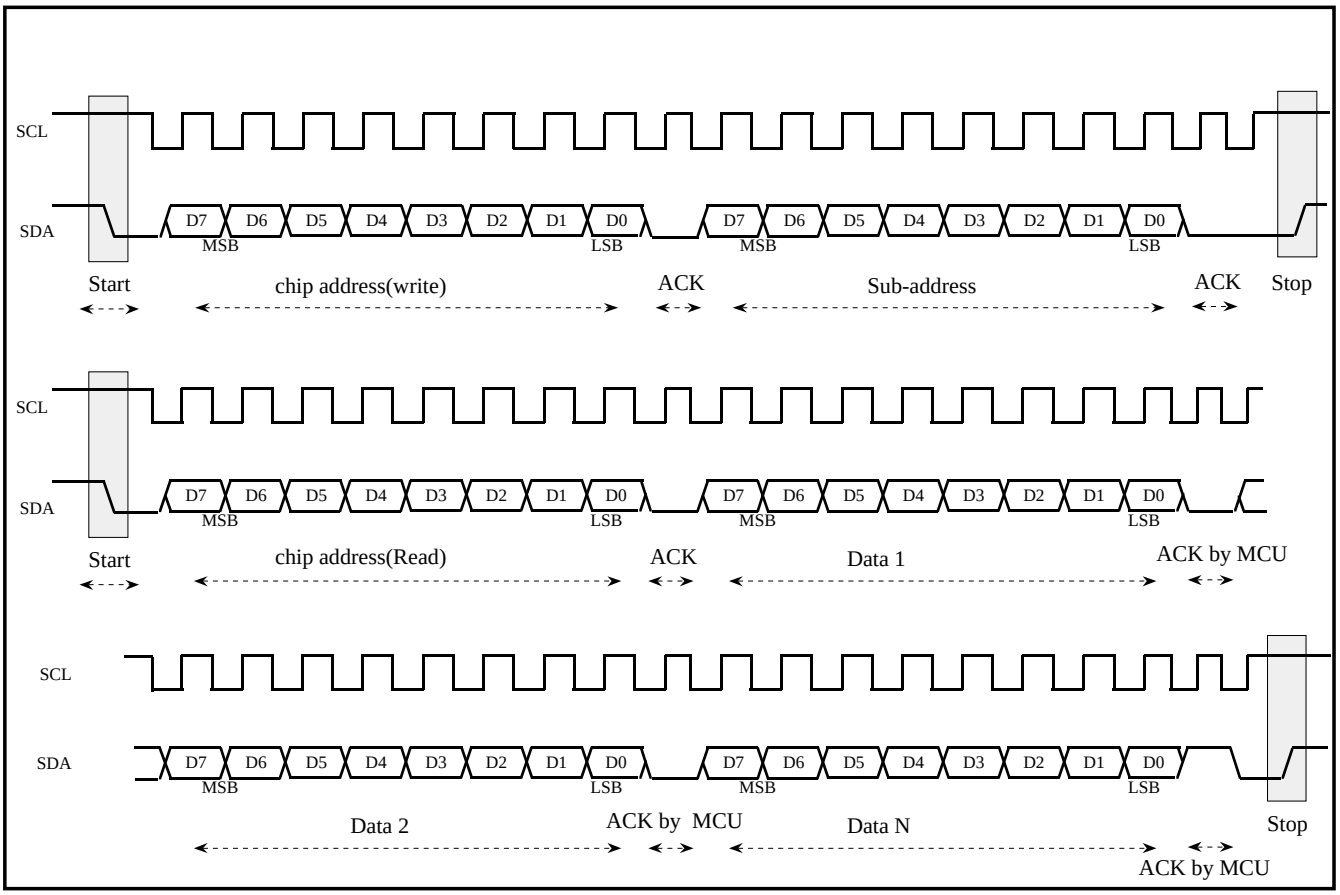


Fig 19-a : SPI-BUS Interface Write operation Timing

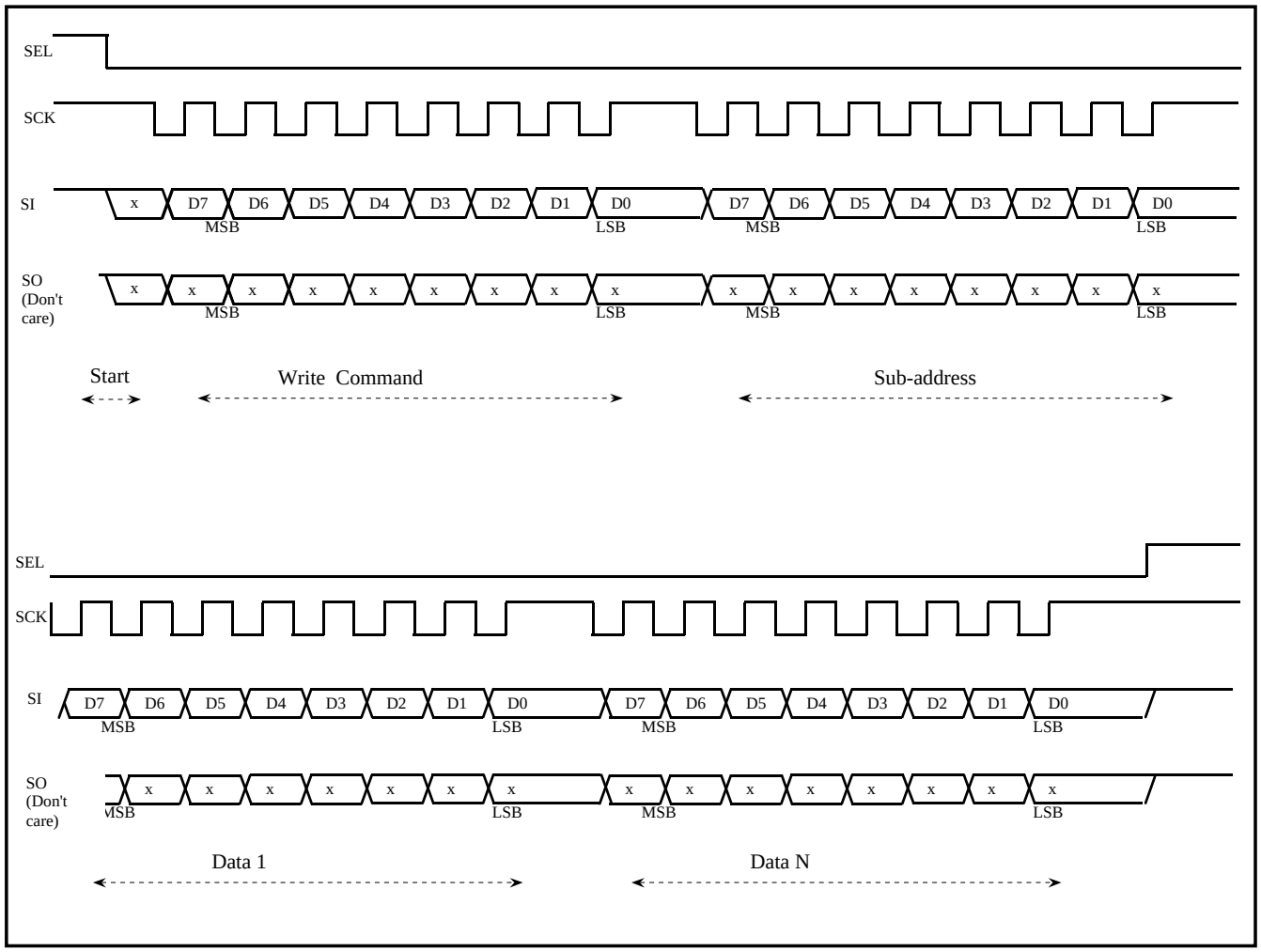
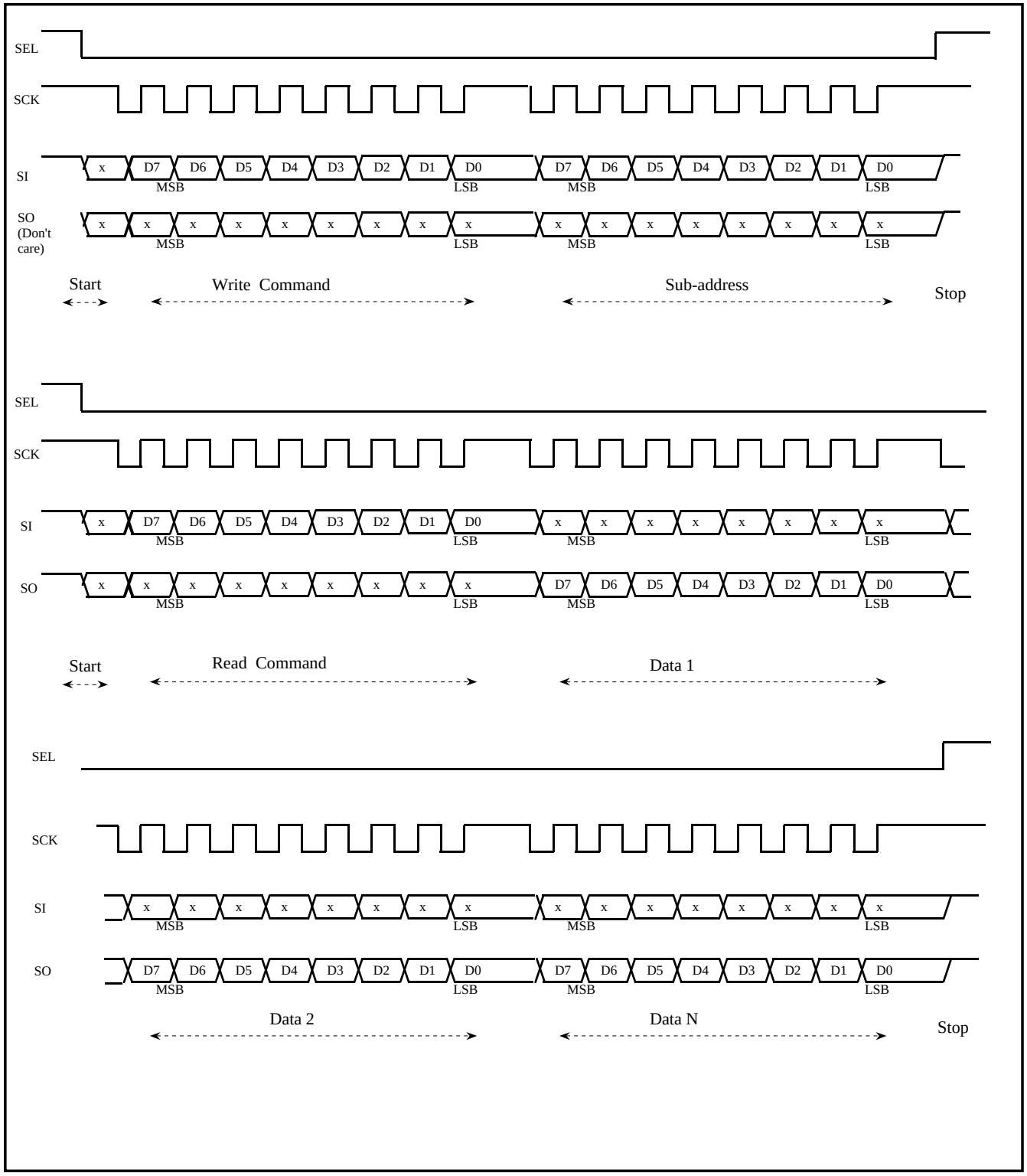


Fig 19-b : SPI-BUS Interface Read operation Timing



[Specifications]

Maximum Ratings

DC Supply Voltage	Vdd	-0.5 ~ +7.0	V	Other
Input Voltage, All Inputs	Vin	-1.5 ~ Vdd+1.5	V	-1.5 ~ Vdd+1.95V at Vdd=3.3V
Output Voltage, All Outputs	Vout	-0.5 ~ Vdd+1.5	V	
DC Output Current, per Pin	Iout	25	mA	
Power Dissipation	Pd	750	mW	
Storage Temperature	Tstg	-65 ~ +150	°C	

Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit	Other
Power Supply Voltage(Analog Blocks) DAVDD	AVDD	3.1 4.75	3.3 5.0	3.5 5.25	V	
Power Supply Voltage(Digital Blocks) DVDD	DVDD	3.1	3.3	3.5	V	
Supply Current(Analog Blocks)	AIcc	-	70	-	mA	Vref = 1.0V,
Supply Current(Digital Blocks)	DIcc	-	50	-	mA	Iref = 1.8KΩ, Rl = 180Ω
Operating Temperature	Ta	0	-	70	°C	

DAC Blocks Characteristics(Power Supply 3.3V,Ta=25℃)

Characteristics	Sym.	Min	Typ	Max	Unit	Other
Resolution	-	-	-	10	Bit	
Integral Non-Linearity	INL	-	-	± 2.0	LSB	Vref = 1.0V, Ibias = 1.8kΩ, Rl = 180Ω
Differential Non-Linearity	DNL	-	-	± 1.0	LSB	Vref = 1.0V, Ibias = 1.8kΩ, Rl = 180Ω
Analog Output Voltage	Vyo	0.85	1.00*	1.15	Vp-p	Vref = 1.0V, Ibias = 1.8kΩ, Rl = 180Ω
Full Scale Output Voltage	Vyfs	0.85	1.00**	1.15	V	Vref = 1.0V, Ibias = 1.8kΩ, Rl = 180Ω
Zero Scale Output Voltage	Vyzs	-	0.0***	0.1	V	Vref = 1.0V, Ibias = 1.8kΩ, Rl = 180Ω
External Load Resistance	RL	75	-	-	Ω	

* : code 000(hex) ~code max.
** : code max.
*** : code 000(hex)

DAC Blocks Characteristics(Power Supply 5.0V,Ta=25℃)

Characteristics	Sym.	Min	Typ	Max	Unit	Other
Resolution	-	-	-	10	Bit	
Integral Non-Linearity	INL	-	-	± 2.0	LSB	Vref = 1.5V, Ibias = 1.8kΩ, Rl = 180Ω
Differential Non-Linearity	DNL	-	-	± 1.0	LSB	Vref = 1.5V, Ibias = 1.8kΩ, Rl = 180Ω
Analog Output Voltage	Vyo	1.35	1.5*	1.65	Vp-p	Vref = 1.5V, Ibias = 1.8kΩ, Rl = 180Ω
Full Scale Output Voltage	Vyfs	1.35	1.5**	1.65	V	Vref = 1.5V, Ibias = 1.8kΩ, Rl = 180Ω
Zero Scale Output Voltage	Vyzs	-	0.0***	0.1	V	Vref = 1.5V, Ibias = 1.8kΩ, Rl = 180Ω
External Load Resistance	RL	75	-	-	Ω	

* : code 000(hex) ~code max.
** : code max.
*** : code 000(hex)

Note : D/A Converter Output Full Scale Voltage

Vyts (V) = (Vref / Iref) * K * R load (K = 10 : DAC Current Gain)
(code 3ff(fex))

Power Dissipation

Pd = [(Vref/Iref * 10 * 3ch) + 10mA (Bais Current)] * 3.3V (or 5V)

[Specifications]

Clock Blocks Characteristics

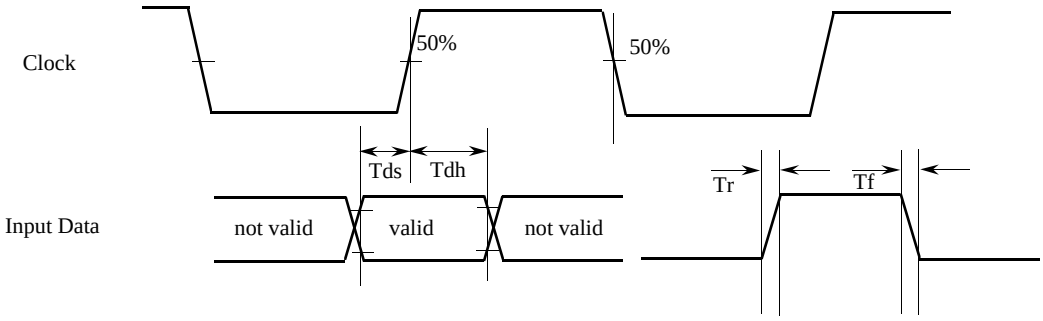
Characteristic	Symbol	Min	Typ	Max	Unit
Clock Rate	fc	-	27.0	-	MHz
Clock Duty Cycle	Dty	45	50	55	%

Digital Blocks Electrical Characteristics(Power Supply 3.3V,Ta=25℃ ± 3℃)

Characteristics		Symbol	Min	Typ	Max	Unit
Input Voltage	HIGH	ViH	2.0	-	5.25	V
	LOW	ViL	-	-	0.8	V
Output Voltage	HIGH	VoH	2.4	-	-	V
(2.0mA)	LOW	VoL	-	-	0.4	V
Input Leakage Current		Iin	-	±2.5	-	µA
Hi-Z Leakage Current		Ioz	-	±20	-	µA
Input Capacitance		Cin	-	-	20	pF
Load Capacitance		C_L	-	-	20	pF
Data Setup Time		Tds	4	-	-	nS
Data Hold Time		Tdh	5	-	-	nS
Input Rise Time		Tr	-	-	5	nS
Input Fall Time		Tf	-	-	5	nS
Data delay		Td	-	-	27	nS

I2C/SPI-BUS Blocks Characteristics(Power Supply 3.3V,Ta=25℃ ± 3 ℃)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Voltage LOW	V_{ILM}	-	-	0.8	V
Input Voltage High	V_{IHM}	2.3	-	5.25	V
Input Current	V_{IM}	-	-	± 10	µA
SDA Output Voltage (I_{OM}=3mA)	V_{OM}	-	-	0.4	V
Output Current (during acknowledge)	I_{OM}	3	-	-	mA
SPI Maxmum Clock Rate	fspi	-	-	3	MHz



[I2C-BUS Slave Address 42(hex)/43(hex) or 1C(hex)/1D(hex)]

<I2C-Bus Format>

WRITE MODE

S	Slave Address	A	Sub Address	A	DATA 0	A	--------	DATA N	A	P

42(hex) or 1C(hex)

if more than 1byte DATA is transmitted,
then auto-increment of the Sub Address is performed

S	Start condition
Slave Address	42(hex) or 1C(hex)
A	Acknowledge, generated by the slave
Sub Address	Sub address byte
DATA 0	First data byte
DATA N	continued data byte(Sub Address is auto increment)
P	Stop condition

READ MODE

S	Slave Address	A	Sub Address N	A	P

← Slave receiver

42(hex) or 1C(hex)

then

S	Slave Address	A	DATA N	AM	DATA N + 1	AM	------	AM	P

← Slave transmitter

43(hex) or 1D(hex)

S	Start condition
Slave Address	Slave receiver is act transmitter is ad
A	Acknowledge, generated by the slave
Sub Address N	Sub Address byte
DATA N	DATA byte of Register N
DATA N + 1	DATA byte of Register N + 1 (address auto-increment)
AM	Acknowledge, generated by the micro controller
P	Stop condition (When Last AM must be '1')

[SPI-BUS]

<SPI-Bus Format>

WRITE MODE

S	Write Command	Sub Address	DATA 0	--------	DATA N	P

42(hex) or 1C(hex)

if more than 1byte DATA is transmitted,
then auto-increment of the Sub Address is performed

S	Chip select on (Hi to Lo)
Write Command	42(hex) or 1C(hex)
Sub Address	Sub address byte
DATA 0	First data byte
DATA N	continued data byte(Sub Address is auto increment)
P	Chip select off (Lo to Hi)

READ MODE

S	Write Command	Sub Address N	P

← Slave receiver

42(hex) or 1C(hex)

then

S	Read Command	DATA N	DATA N + 1	---------	P

← Slave transmitter

43(hex) or 1D(hex)

S	Chip select on (Hi to Lo)
Sub Address N	Sub Address byte set
Read Command	43(hex) or 1D(hex)
DATA N	DATA byte of Register N
DATA N + 1	DATA byte of Register N + 1 (address auto-increment)
P	Chip select off (Lo to Hi)

[Register Mapping and Description]

Sub-address 6E : Y/CbCr mode setup (write)

	MSB							LSB
Register 6E	-	-	-	-	CbCr mode	Y mode	M2/Beta[1]	M2/Beta[0]

default : 0000_0000(bin)

M2/Beta : Y select M2 type, BetaCam type
- 00 : BetaCam (default)*
- 01 : M2 (7.5IRE setup)*
- 10 : BetaCam (7.5IRE setup)*
- 11 : M2*

Note * : These bit can related w/ sub address $72 [4] setup bit.

Y mode : Separate switch
- 0 : **Y**/CbCr's **Y** is same as **Y**/C/CVBS's **Y** (default)
- 1 : **Y**/CbCr's **Y** is the BetaCam or M2 **Y** signal

CbCr gain : Cb/Cr gain
- 0 : normal operation (default)
- 1 : 1/2 gain (disable code divided by 2)

Sub-address 6F : Interpolation Filter Switch (write)

	MSB							LSB
Register 6F	-	Y Fil mode1	Cb/Cr/U/V Fil mode1	Cb Fil mode0	Cr Fil mode0	U Fil mode0	V Fil mode0	Y Fil mode0

default : 0000_0000(bin)

Y Fil mode 0 : Luma Filter switch
- 0 : wide 6MHz (default)
- 1 : narrow 2.5Mhz

V Fil, U Fil mode0 : Chroma Filter switch
- 0 : wide 3.0MHz(default)
- 1 : narrow 1.5MHz

Cr Fil, Cb Fil mode 0 : Cr/Cb Filter switch
- 0 : wide 3.0MHz(default)
- 1 : narrow 1.5MHz

Cr /Cb Fil mode 1 : wide Filter switch
- 0 : wide0 3.0MHz(default)
- 1 : wide1 2.5MHz

Y Fil mode 1 : wide Filter switch
- 0 : wide0 6.0MHz(default)
- 1 : wide1 5MHz

Sub-address 70 : Variable I/O Switch (write/read)

	MSB							LSB
Register 70	bs-off	self-SW	color bar select	VBLK SW	C/Fsync SW	F/Vsync SW	M/S mode1	M/S mode0

default : 0000_0001(bin)

bs - off : color burst control switch On/Off
- 0 : color burst ON (default)
- 1 : color burst OFF

self - SW : internal self H/V counter reset switch On / Off
- 0 : self counter reset OFF (default)
- 1 : self counter reset ON

Note : this mode is ONLY valid at when 70h[1: 0] is "10(bin)" or "11(bin)".

color bar select : color bar select

	Luma	Chroma
0 : color bar	100%	75%
1 : color bar	100%	100%

VBLK SW : Vertical Blanking Mask Enable switch On-Off
- 0 : reject VBI information data in vertical blanking period (default)
- 1 : through VBI information data in vertical blanking period

C/Fsync SW : Composite sync/Frame sync output switch
- 0 : Frame sync output (default)
- 1 : composite sync output

F/Vsync SW : Frame sync /Vertical sync output switch
- 0 : Vertical sync output (default)
- 1 : Frame sync output

M/S sync mode1 : Master or Slave sync mode
M/S sync mode0
- 00 : 601 H/V master mode
- 01 : 656 slave mode(no H/Vsync output) (default)
- 10 : Fsync/Hsync slave mode
- 11 : Vsync/Hsync slave mode

Sub-address 71 : Sync control (write/read)

	MSB							LSB
Register 71	non-inter	VBI SW	h-polarity	v-polarity	f-polarity	h- delay2	h-delay1	h-delay0

default : 0000_0100(bin)

non-inter : non-interlaced mode select
- 0 : interlace mode (default)
- 1 : non-interlace mode

VBI SW : vertical blanking information signal input control switch on 34 pin
- 0 : VBI input Off (default)
- 1 : VBI input On

h-polarity : polarity of Hsync
- 0 : negative (default)
- 1 : positive

v-polarity : polarity of Vsync
- 0 : negative (default)
- 1 : positive

f-polarity : polarity of Fsync
- 0 : field1 (odd) = low level (default)
- 1 : field1 (odd) = high level

h-delay2, h-delay1, h-delay0 : delay on Hsync with reference to DVIA/DVIB data in Master mode
- 000: + 4 clock delay
- 001: + 3 clock delay
- 010: + 2 clock delay
- 011: + 1 clock delay
- 100: + 0 clock delay
- 101: - 1 clock delay
- 110: - 2 clock delay
- 111: - 3 clock delay

Note : this h-delay can be also related with 7A[7:0] register and can delay totally +2023 clock delay in H/V or H/Fsync slave mode.

Sub-address 72 : PAL/NTSC setup (write / read)

	MSB							LSB
Register 72	phase-set	TEST	C/Fsync/VBI I/O SW	color bar	setup75	625/525	PAL/ NTSC2	PAL/ NTSC1

default : 0000_1000(bin) NTSC (If "PAL/NTSC" pin is LOW level)
0000_0101(bin) PAL

phase-set : color sub-carrier phase synchronization
0 : free running (default)
1 : 1 phase reset/8 field and 1 phase reset/4 frame

TEST : for test, should be "0"

C/Fsync/VBI I/O SW : Input/Output switch on 34 pin (C/Fsync/VBI pin)
0 : VBI input(default)
1 : Csync or Frame sync output

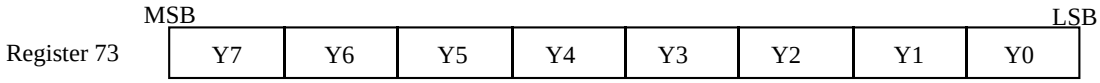
color bar : internal color bar generator control
0 : normal operation (default)
1 : color bar generator On
(need to set color bar mode on sub-address 70[5].)

setup75 : Setup level for Luminance
0 : setup level for luminance = 0IRE
1 : setup level for luminance = 7.5IRE

625/525 : control line mode
0 : 525 lines / 60 Hz mode
1 : 625 lines / 50 Hz mode

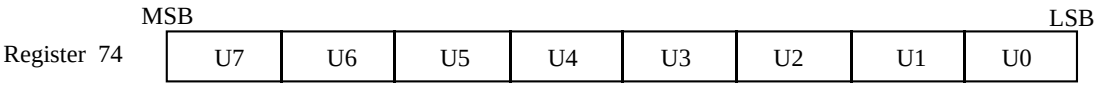
PAL/NTSC2
PAL/NTSC1 : subcarrier control
00 : NTSC(M)
01 : PAL (BDGHI)
10 : PAL (M)
11 : PAL (N)

Sub-address 73: Vertical Blanking Information Luma (Y) Level (write only)



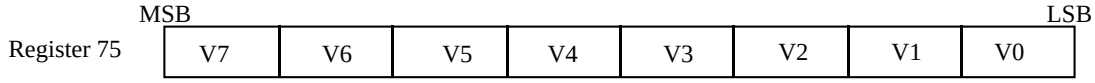
default : 1000_0000(bin)

Sub-address 74: Burst Chroma (U) Level (write only)



default : 77(dec) (NTSC)
89(dec) (PAL)

Sub-address 75: Burst Chroma (V) Level (write only)



default : 128(dec) (NTSC)
155(dec) (PAL)

Sub-address 76 : DAC set 1 signal control (write only)

	MSB							LSB
Register 76	Cr	Cb	Luma	dac 1pin	dac 7pin	dac 4pin	dac set 1 mode[1]	dac set 1 mode[0]

default : 0000_0000(bin)

Cr : Cr/Cb signal control (Data path enable)
Cb
0 : Cr, Cb On (default)
1 : chrominance Off

Luma : Luminance control (Data path enable)
0 : luminance On (default)
1 : luminance Off

dac 1pin : D/A converter (1) output On-Off control
dac 4pin
dac 7pin
0 : CVBS/Cb DAC, C/Cr DAC, Y DAC output On (default)
1 : CVBS/Cb DAC, C/Cr DAC, Y DAC output Off

dac set 1 mode : 1~9-pin's D/A converter output signal control
10 : Y/Cr/Cb output On
00 : Y/C/CVBS output On

Sub-address 77 : reserved

	MSB							LSB
Register 77	-	-	-	-	-	-	-	-

Sub-address 78~79 : Sub-carrier phase control (write only)

	MSB							LSB
Register 78	sc-ph9	sc-ph8	sc-ph7	sc-ph6	sc-ph5	sc-ph4	sc-ph3	sc-ph2

default : 0000_0000(bin)

	MSB							LSB
Register 79	-	-	-	-	-	-	sc-ph1	sc-ph0

default : 0000_0000(bin)

sc-ph9 : sub-carrier phase control
sc-ph8 00_0000_0000 : sub-carrier phase 0 degree (default)
sc-ph7 to
sc-ph6 11_1111_1111 : sub-carrier phase 359 degree
sc-ph5
sc-ph4
sc-ph3
sc-ph2
sc-ph1
sc-ph0

Sub-address 7A : Hsync delay control (write only)

	MSB							LSB
Register 7A	H-delay10	H-delay9	H-delay8	H-delay7	H-delay6	H-delay5	H-delay4	H-delay3

default : 0000_0000(bin)

h-delay10 : delay on Hsync with reference to DVIA/DVIB data
h-delay9 0000_0000_000 : Hsync delay 0 delay
h-delay8 to
h-delay7 1111_1111_000 : Hsync delay +255 delay
h-delay6
h-delay5
h-delay4
h-delay3

Note : this h-delay can be also related with 71[3:0] register and can delay totally +2023 delay(1111_1111_111) in H/V or H/Fsync slave mode.

Sub-address 7B : Digital Video Input Select Control (write only)

	MSB							LSB
Register 7B	-	-	Cr_tmg[1]	Cr_tmg[0]	Cb_tmg[1]	Cb_tmg[0]	Y_tmg	16-bit input mode

default : 0000_0000(bin)

Cr_tmg : Cr clock timing delay in 16-bit Digital Input Mode
00 : Cr clock delay 0 clock (default)
01 : Cr clock delay +1 clock
10 : Cr clock delay +2 clock
11 : Cr clock delay +3 clock (See fig 3,4)

Cb_tmg : Cb clock timing delay in 16-bit Digital Input Mode
00 : Cb clock delay 0 clock (default)
01 : Cb clock delay +1 clock
10 : Cb clock delay +2 clock
11 : Cb clock delay +3 clock (See fig 3,4)

Y_tmg : Y clock timing delay in 16-bit Digital Input Mode
0 : Y clock delay 0 clock (default)
1 : Y clock delay +1 clock

16-bit input mode : 16-bit YY / CbCr Digital Video Input mode
0 : 8-bit Multiplexed CbYCrY Digital Video Input mode (default)
1 : 16-bit YY / CbCr Digital Video Input mode

Sub-address 7C : signal control 3(write only)

	MSB							LSB
Register 7C	Ysync	-	-	-	-	-	CbCr bf	Chroma bf

default : 0000_0000(bin)

Y sync : Y sync Signal On/Off (Y/Cb/Cr mode only)
0 : Y sync On (default)
1 : Y sync Off

CbCr bf : CbCr burst On/Off
0 : Cb/Cr bf data Off
1 : Cb/Cr bf data On

Chroma bf : Chroma burst On/Off
0 : Chroma bf data On
1 : Chroma bf data off

Sub-address 7D~7E : Vsync delay control (write only)

	MSB							LSB
Register 7D	V-delay7	V-delay6	V-delay5	V-delay4	V-delay3	V-delay2	V-delay1	V-delay0

default : 0000_0000(bin)

	MSB							LSB
Register 7E	-	-	-	-	-	-	V-delay9	V-delay8

default : 0000_0000(bin)

V-delay9 : delay on Vsync with reference to DVIA/DVIB data in slave mode
V-delay8 0000_0000_00 : Vsync delay 0 delay
V-delay7 to
V-delay6 1111_1111_11 : Hsync delay +1023 delay
V-delay5
V-delay4
V-delay3
V-delay2
V-delay1
V-delay0

Sub-address 80~82: CGMS characters for Field1(Line20)/Field2(Line283) (write only) NTSC only

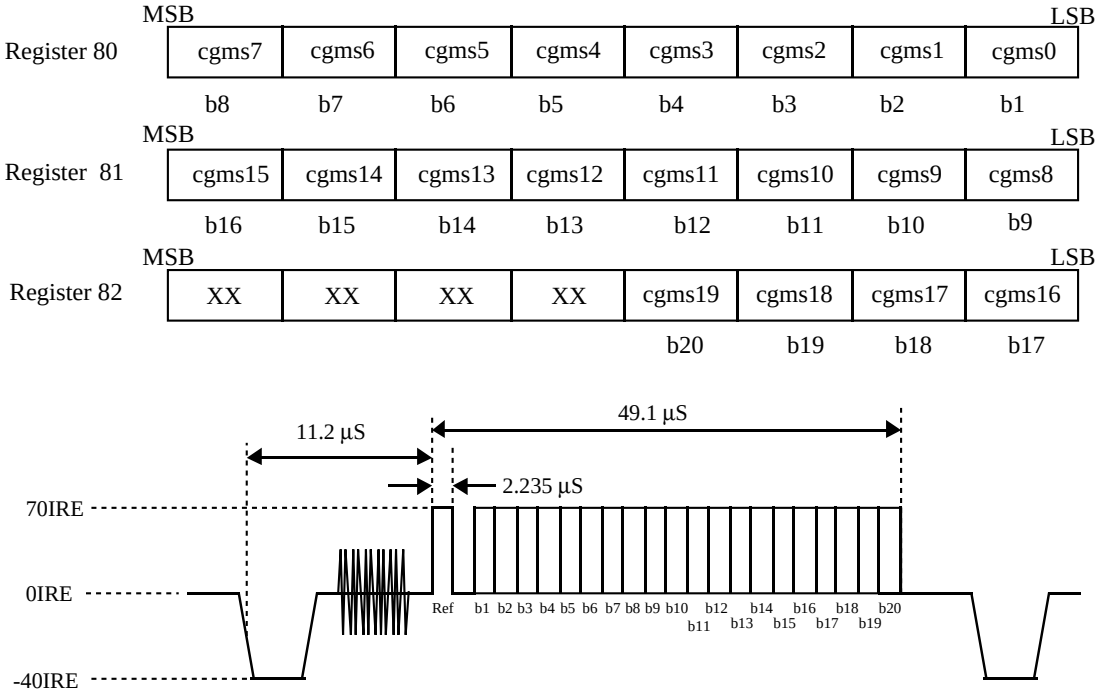


Fig 20 : CGMS wave form

Sub-address 80~81: WSS characters for Line23 (write only) PAL only

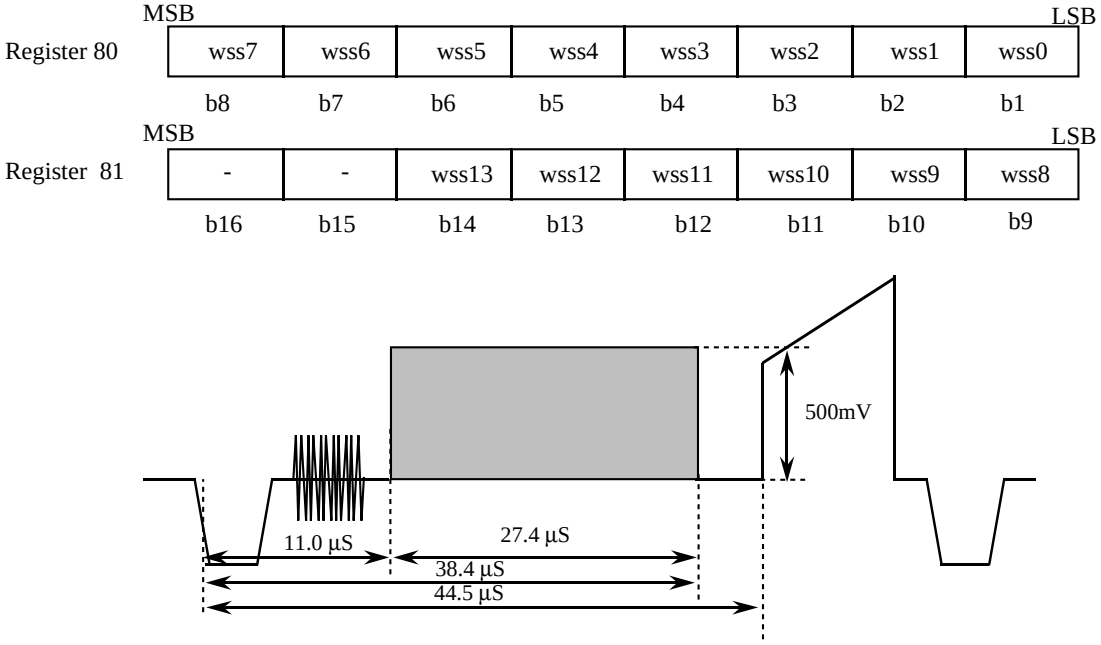


Fig 21 : WSS wave form

Sub-address 83~84 :closed caption characters/extended data for Field1(Line21) (write)

First byte to Encode

	MSB							LSB
Register 83	ccp118	ccb117	ccb116	ccb115	ccb114	ccb113	ccb112	ccb111
	parity	b7	b6	b5	b4	b3	b2	b1

Second byte to Encode

	MSB							LSB
Register 84	ccp128	ccb127	ccb126	ccb125	ccb124	ccb123	ccb122	ccb121
	parity	b7	b6	b5	b4	b3	b2	b1

Sub-address 85~86 :closed cation character/extended data for Field2(Line284)

First byte to Encode

	MSB							LSB
Register 85	ccp218	ccb217	ccb216	ccb215	ccb214	ccb213	ccb212	ccb211
	parity	b7	b6	b5	b4	b3	b2	b1

Second byte to Encode

	MSB							LSB
Register 86	ccp228	ccb227	ccb226	ccb225	ccb224	ccb223	ccb222	ccb221
	parity	b7	b6	b5	b4	b3	b2	b1

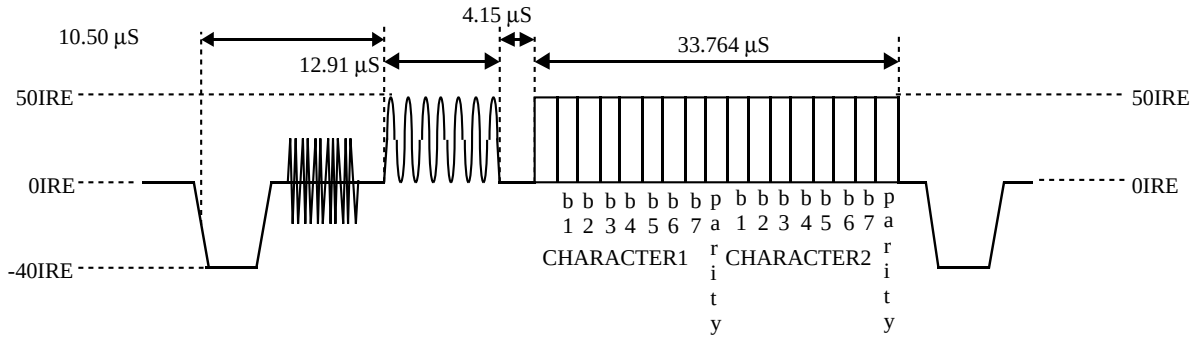


Fig 22 : Closed caption wave form

Note : This Closed Caption wafeform is defined by when the register $72 [3] = "1" is set

sub-address 80, 81, 82, 83, 84, 85 and 86 (previous frame data)
are double-buffered by Frame sync falling edge

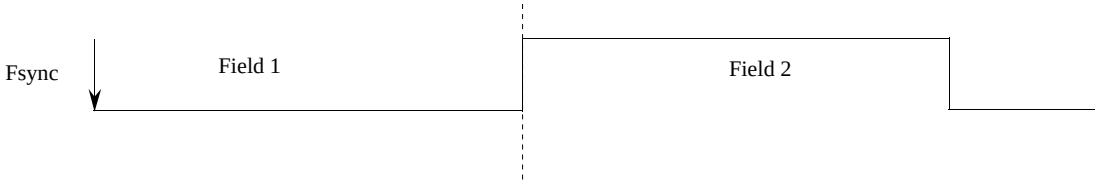


Fig 23 : VBI data update timing

Sub-address 87 :Closed caption / CGMS / WSS

	MSB							LSB
Register 87	CC2_flag	CC1_flag	CC_null	CC_parity	WSS	CGMS	CC2	CC1

default 00h

CC2_flag : Closed Caption Status Flag for field2/field1 (Read only)
CC1_flag 0 : Automatically set to " 1 " when 2-byte Closed Caption data are written, and then cleared to "0" when the data is send to doubled buffer
1 : Do NOT work " 1 " to these bits. " 0 " is correct.

CC_null : Automatically set the null code when the data is send to doubled buffer
0 : Keep the current CC data in the resister.
1 : Automatically set the null code in the CC data resister

CC_parity: CC Parity Generation On-Off
0 : Use parity bit in data. (default)
1 : Automatically generate parity bit.

WSS : WSS information data insertion On-Off
0 : WSS information data insertion Off
1 : WSS information data insertion On

CGMS : CGMS information data insertion On-Off
0 : CGMS information data insertion Off
1 : CGMS information data insertion On

CC2 : closed caption/extended data for field2 encoding On-Off
0 : closed caption/extended data for field2 encoding Off
1 : closed caption/extended data for field2 encoding On

CC1 : closed caption/extended data for field1 encoding
0 : closed caption/extended data for field1 encoding Off
1 : closed caption/extended data for field1 encoding On

Sub-address 88 :CGMS/WSS Parity Generation On-Off

	MSB							LSB
Register 88	-	-	-	-	-	-	WSS_parity	CGMS_parity

default 00h

WSS_parity
CGMS_parity :WSS/CGMS Parity Generation On-Off
0 : Use parity bit in data. (default)
1 : Automatically generate parity bit.

I2C-BUS Slave Receiver Sub-address map

6Eh[7:4]	n.a.
6Eh[3]	Cb/Cr gain control
6Eh[2]	Y mode switch
6Eh[1:0]	M2/Beta Cam select
6F[7]	n.a.
6F[6:0]	Interpolation filter switch
70h:[7]	burst control (default 0:on)
[6]	self counter reset switch (default 0:off)
[5]	color bar select (default 0:Luma 100% Chroma 75%)
[4]	vertical blanking switch(default 0:off)
[3]	34 pin output mode select (Csync:1, Flame sync:0)
[2]	F/Vsync select(default 0:Vsync)
[1:0]	Master/Slave mode select(default 01:656_slave)
71h:[7]	interlaced / non-interlaced (default 0:interlaced)
[6]	VBI input control on 34 pin (default 0:off)
[5]	horizontal sync polarity (default 0)
[4]	vertical sync polarity (default 0)
[3]	frame sync polarity (default 0)
[2:0]	hsync delay control (default 100:0 clock delay) (In slave mode can use with 7A[7:0])
72h:[7]	sub-carrier phase synchronization(default 0)
[6]	Test mode (default 0:off)
[5]	34 pin I/O switch(default 1:cysnc output)
[4]	color bar generate(default 0:off)
[3]	setup level control(default 1:7.5IRE)
[2]	625lines50Hz/525Lines60Hz (default set PAL/NTSC pin)
[1:0]	PAL/NTSC (default set PAL/NTSC pin) 00:NTSC/M 01:PAL/BDGHI (10:PAL/M) (11:PAL/N)
73h[7:0]	VBI Luma level register(default 80h)
74h[7:0]	Burst U_register(default 77d:ntsc/89d:PAL)
75h[7:0]	Burst V_register(default 128d:ntsc/155d:PAL)
76h[7]	Cr on/off (default 0:on)
[6]	Cb on/off (default 0:on)
[5]	Luma on/off(default 0:on) (default 0: on)
[4:2]	1pin dac/4pin dac/7pin dac on/off(default 0: on)
[1:0]	D/A converter output signal control (default 00 : CBVS/Y/C output)
77h[7:0]	reserved
78h[7:0]	sub-carrier phase control(default 00h)
79h[1:0]	sub-carrier phase control(default 00)
79h[7:2]	n.a.
7A[7:0]	hsync-delay control (In slave mode, is valid with 71h[2:0] register)
7B[7:6]	n.a..
[5:2]	Cr/Cb clock timing delay in 16-bit digital input mode (default 00: clock delay 0)
[1]	Y clock timing delay in 16-bit digital input mode (default 0: clock delay 0)
[0]	16-bit multiplexed CbYCrY digital video input mode (default 0: 8-bit YCrCb digital video input mode)
7C[7]	Ysync signal On/Off(YCrCb mode only)(default 0: On)
[6:1]	n.a.
[0]	Chroma burst On/Off(default 0: On)
7D[7:0]	delay on Vsync with reference to DVIA/DVIB data in slave mode
7E[7:2]	n.a.
[1:0]	delay on Vsync with reference to DVIA/DVIB data in slave mode
80~82h	CGMS characters for field1(line20)/field2(line283)
80~81h	WSS characters for field1(line23)
83h[7:0]	CC character1(line21) (default 'h80)
84h[7:0]	CC character2(line21) (default 'h80)
85h[7:0]	CC character1(line284) (default 'h80)
86h[7:0]	CC character2(line284) (default 'h80)
87h[7:6]	Closed Caption Status Flag for field2
[5]	Automatic set to null code(Closed Caption data)
[4]	Automatic generate CC parity bit (default 0: off)
[3]	WSS information data insertion on/off (default 0: off)
[2]	CGMS on/off (default 0: off)
[1]	CC closed caption/extended data for field2 encoding (default 0: off)
[0]	CC closed caption/extended data for field1 encoding (default 0: off)
88h[7:2]	reserved
[1]	WSS_parity Generation On-Off
[0]	CGMS_parity Generation On-Off

<<<<<<<< I2C-BUS Format >>>>>>

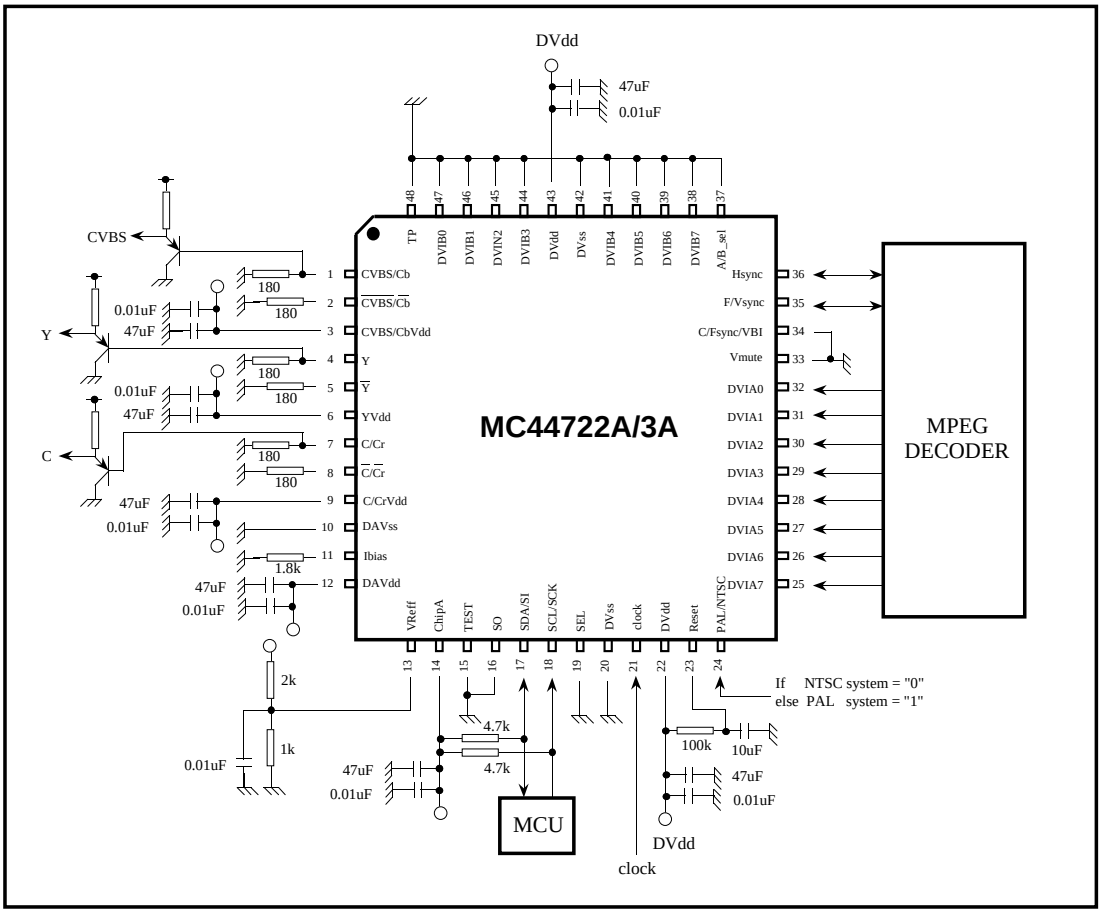
** WRITE MODE **
S | Slave_address(W) | A | Sub_address | A | Data0 | A | ... | DataN | A | P

S	Start condition
Slave_address	42(hex) or 1C(hex)
A	Acknowledge generated by DVE
Sub_address	Sub_address register
Data0	First data
DataN	Continued data(address is auto incremented)
P	Stop condition

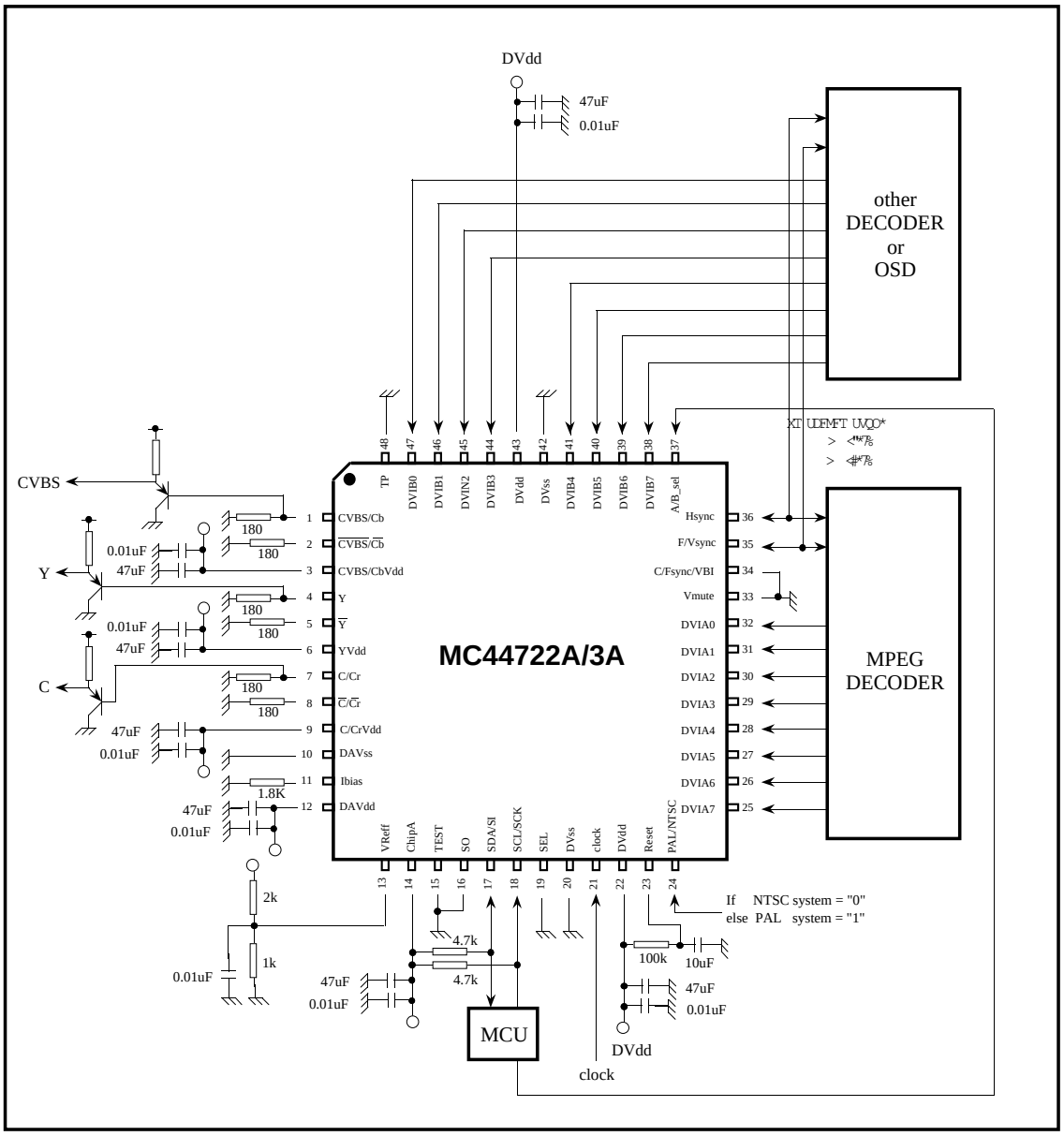
<<<<<<<< SPI-Bus Format >>>>>>
** WRITE MODE **
S | Write Command | Sub_address | Data0 | ... | DataN | P

S	Chip select on (High to Low)
Write Command	43(hex) or 1D(hex)
Sub_address	Sub_address byte
Data0	First data
DataN	Continued data byte(address is auto incremented)
P	Chip select off (Low to High)

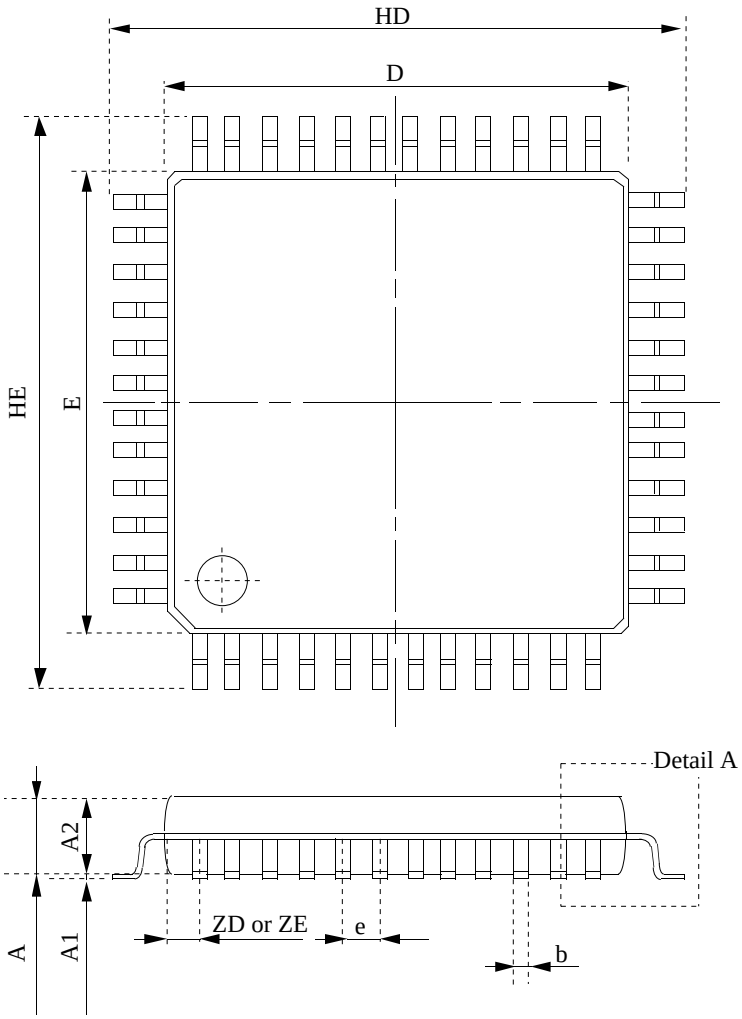
[Application Diagram 1]

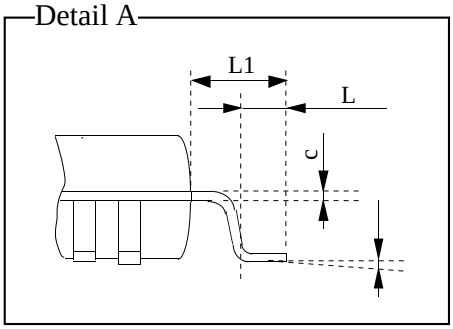


[Application Diagram 2]



48-pin QFP Package (0.8mm pitch)

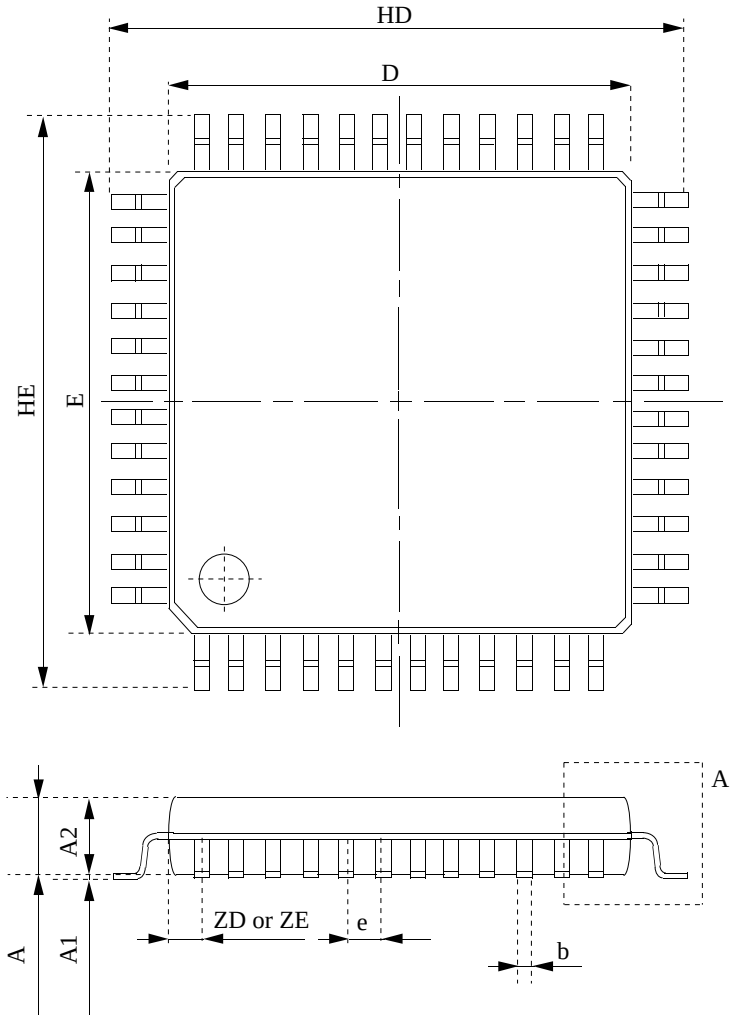


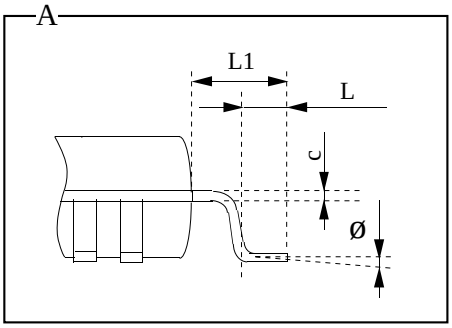


	min	max
A	-	1.70
A1	0.05	0.15
A2	1.40TYP	
b	0.3	0.45
c	0.10	0.20
D	11.90	12.10
E	11.90	12.10
e	0.80	
HD	13.80	14.20
HE	13.80	14.20
L	0.30	0.70
L1	0.80	1.20
	0	10
y	-	0.10
ZD	1.60	
ZE	1.60	

unit : mm

48-pin VQFP Package (0.5mm pitch)





	Min	Max
A	-	2.00
A1	0.00	0.25
A2	1.4TYP	
b	0.14	0.30
c	0.05	0.20
D	6.80	7.20
E	6.80	7.20
e	0.50	
HD	8.80	9.20
HE	8.80	9.20
L	0.30	0.70
L1	0.80	1.20
Ø	0	10
y	-	0.10
ZD	0.75	
ZE	0.75	

Unit mm