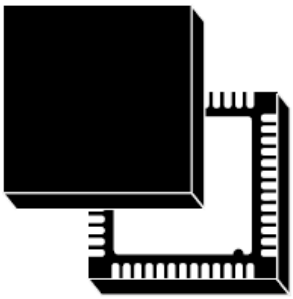
STA330

2.0 digital audio processor with FFX digital modulator and analog and digital inputs

Features

- Up to 96 dB dynamic range
- Sample rates from 8 kHz to 192 kHz
- FFX (digital modulation) class-D driver
- Digital supply voltage from 1.5 V to 3.6 V
- Analog supply voltage from 1.5 V to 3.6 V
- 18-bit audio processing and class-D FFX digital modulator
- 100-dB SNR analog to digital converter
- Digital volume control:
  - +36 dB to -105 dB in 0.5 dB steps
  - Software volume update
- Individual channel and master gain/attenuation
- Automatic invalid-input detect mute



VFQFPN52

- 2-channel serial input/output data interface
- Digitally controlled pop-free operation

Table 1. Device summary

Order code	Package	Packaging
STA330	VFQFPN52	Tube
STA33013TR	VFQFPN52	Tape and reel

Contents

1 Introduction

The STA330 is a digital stereo audio processor with analog and digital input. It includes an audio DSP and FFX, a ST proprietary high-efficiency class-D driver. In conjunction with a power device, the STA330 provides high-quality digital amplification.

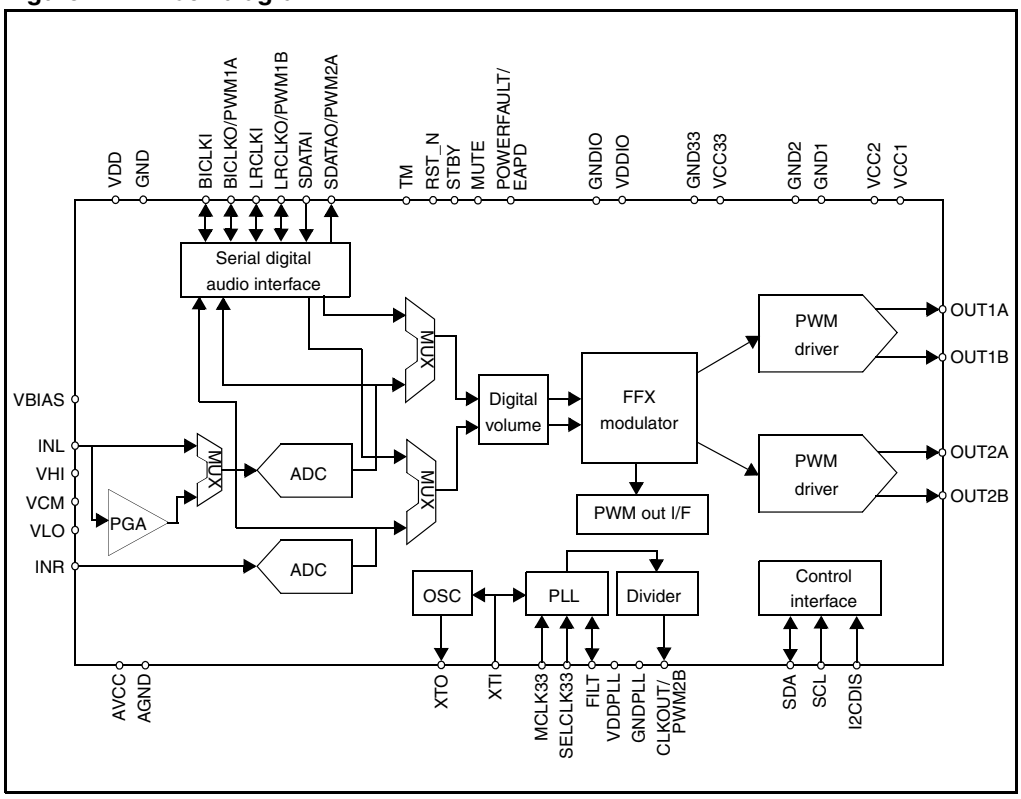
The STA330 contains an on-chip volume/gain control.

The PWM amplifier achieves greater than 90% efficiency for longer battery life for portable systems.

The STA330 I2CDIS pin disables the audio DSP functions to provide a direct conversion of the input signal into output power (the I^2C interface is disabled). This conversion is done without the microcontroller.

The STA330 is designed for low-power operation with extremely low-current consumption in standby mode. It is available in the package VFQFPN52, a very thin (1.2 mm thick) package that can be used for small portable applications.

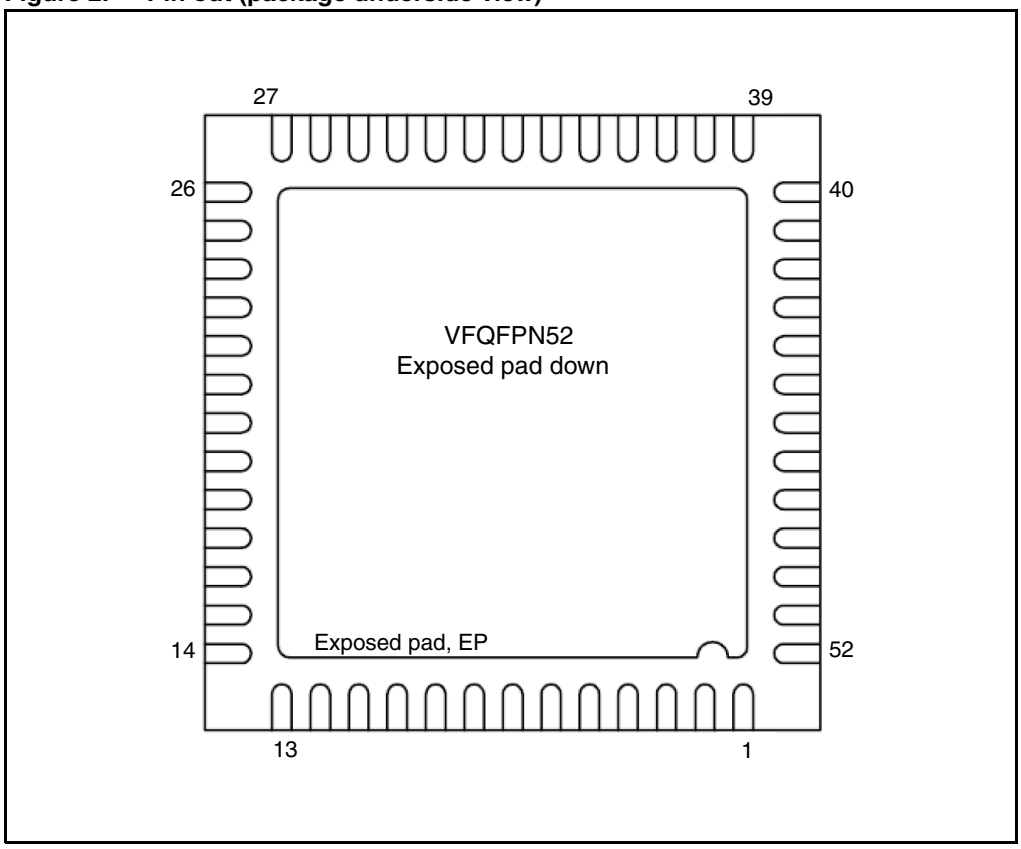
Figure 1. Block diagram



2 Connection diagrams and pin descriptions

2.1 Connection diagram

Figure 2. Pin out (package underside view)



2.2 Pin description

Table 2. Pin list

Pin #	Name	Type	Description
1	STBY	Digital input	Standby (active high)
2	INL	Analog input	ADC left channel line input or microphone input
3	INR	Analog input/output	ADC right channel line input
4	VBIAS	Analog input/output	ADC microphone bias voltage
5	AVDD	Supply	ADC analog supply
6	VHI	Analog input	ADC high reference voltage
7	VLO	Analog input	ADC low reference voltage
8	AGND	Ground	ADC analog ground
9	VCM	Analog input/output	ADC Common mode voltage
10	RST_N	Digital input	Reset (active low)
11	CLKOUT	Digital output	Buffered clock output
12	GND1	Ground	Digital ground
13	VDD1	Supply	Digital supply
14	MUTE	Digital input	Mute (active high)
15	VCC1A	Supply	Channel 1 PWM A power supply
16	OUT1A	PWM output	Channel 1 PWM A output
17	GND1A	Ground	Channel 1 PWM A power ground
18	GND1B	Ground	Channel 1 PWM B power ground
19	OUT1B	PWM output	Channel 1 PWM B output
20	VCC1B	Supply	Channel 1 PWM B power supply
21	VCC2B	Supply	Channel 2 PWM B power supply
22	OUT2B	PWM output	Channel 2 PWM B output
23	GND2B	Ground	Channel 2 PWM B power ground
24	GND2A	Ground	Channel 2 PWM A power ground
25	OUT2A	PWM output	Channel 2 PWM A output
26	VCC2A	Supply	Channel 2 PWM A power supply
27	GND33	Ground	Pre-driver ground
28	GNDIO1	Ground	I/O ring ground
29	VDDIO1	Supply	I/O ring supply
30	VCC33	Supply	Pre-driver supply

Table 2. Pin list (continued)

Pin #	Name	Type	Description
31	POWERFAULT/ EAPD	Digital output	Power fault signal (active high) / External audio power-down signal
32	TM	Digital input	Test mode (active high)
33	I2CDIS	Digital input	I^2C disable pin (active high)
34	SCL	Digital input	I^2C serial clock
35	SDA	Digital input/output	I^2C serial data
36	SELCLK33	Digital input	Master clock input selector: SELCLK33 = 1 -> MCLK33 selected SELCLK33 = 0 -> XTI selected
37	MCLK33	Digital input	Master clock input 3.3-V capable XTI: crystal input or master clock input 3.3-V capable
38	XTI	Digital input	Crystal input or master clock input
39	XTO	Digital output	Crystal output
40	FILT	Analog input/output	PLL loop filter terminal
41	GNDPLL	Ground	PLL analog ground
42	VDDPLL	Supply	PLL analog supply
43	GND2	Ground	Digital ground
44	VDD2	Supply	Digital supply
45	SDATAI	Digital input	Input serial audio interface data
46	SDATAO	Digital output	Output serial audio interface data
47	LRCLKI	Digital input/output	Input serial audio interface L/R-clock
48	LRCLKO	Digital input/output	Output serial audio interface L/R-clock (volume UP when I2CDIS=1)
49	GNDIO2	Ground	I/O ring ground
50	VDDIO2	Supply	I/O ring supply
51	BICLKI	Digital input/output	Input serial audio interface bit-clock
52	BICLKO	Digital input/output	Output serial audio interface bit-clock (volume DOWN when I2CDIS=1)
	EP	Ground	Exposed pad ground

3 Electrical specifications

3.1 Maximum and recommended operating conditions

Table 3 gives the maximum ratings and *Table 4* the recommended operating conditions.

Table 3. Absolute maximum ratings

Symbol	Description	Min	Max	Unit
VDD/VDD1/VDD2	Digital supply voltage	-0.5	+4.0	V
AVDD	ADC supply voltage	-0.5	+4.0	V
VDDPLL	PLL analog supply voltage	-0.5	+4.0	V
VCC1A/1B/2A/2B	Power stage supply voltage	-0.5	+4.0	V
VCC33	Pre-driver supply	-0.5	+4.0	V
VDDIO	Digital I/O supply	-0.5	+4.0	V
V_{DI}	Voltage range digital in	-0.5	VDDIO +0.3	V
V_{AI}	Voltage range analog in	-0.5	AVDD +0.3	V
V_o	Voltage on output pins	-0.5	VDDIO +0.3	V
T_{STG}	Storage temperature	-40	150	^{o}C
T_{AMB}	Ambient operating temperature	-20	85	^{o}C

Note: All grounds must be within 0.3 V of each other.

Table 4. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD/VDD1/VDD2	Digital supply voltage	1.55	1.8	3.6	V
AVDD	ADC supply voltage	1.8	3.3	3.6	V
VDDPLL	PLL analog supply voltage	1.55	1.8	3.6	V
VCC1A/1B/2A/2B	Power stage supply voltage	1.8	3.3	3.6	V
VCC33	Pre-driver supply voltage	1.8	3.3	3.6	V
GND1, GND2, GND33	Channel 1 and 2 power ground, pre-driver ground		0		V
T_{AMB}	Ambient operating temperature	0	25	70	^{o}C

3.2 Electrical characteristics

Table 5 lists the device electrical characteristics under the conditions nominal supply voltage (see *Table 4*), LRCLKI frequency (f_S) = 48 kHz, input frequency = 1 kHz, and R_{load} = 32 Ω, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
IstbyL	Logic power supply current at standby			1.3		µA
IddL	Logic power supply current at operating			15		mA
Tds	Low current dead time (static)			1		ns
Tdd	High current dead time (dynamic)			2.5		ns
Tr	Rise time			3		ns
Tf	Fall time			3		ns
DNR	Dynamic range A-weighted	Speaker mode		96		dB
SNR	Signal-to-noise ratio (A-weighted)	Speaker mode		92		dB
THDN	Total harmonic distortion	0 dBFS input, 8 Ω speaker		0.1		%
		-6 dBFS input, 8 Ω speaker		0.05		%
		0 dBFS input, 32 Ω headphone		0.1		%
		-6 dBFS input, 32 Ω headphone		0.05		%

3.3 Lock time

Table 6 gives the typical lock time of the PLL using the suggested loop filter *on page 18*, a 1.8-V supply and 30° C junction temperature.

Table 6. PLL lock time

Parameter	Value
Lock time	200 µs

3.4 ADC performance values

Table 7. Programmable gain performance

Parameter	Min	Typ	Max	Unit
Dynamic range, 1 kHz, 3.3-V supply				dB
Dynamic range, 1 kHz, 1.8-V supply				dB
Dynamic range, 1 kHz, 3.3-V supply A-weighted		92		dB
Dynamic range, 1 kHz, 1.8-V supply A-weighted		84		dB
SNDR 1 kHz, 3.3 V supply				dB
SNDR 1 kHz, 1.8 V supply				dB
SNDR 1 kHz, 3.3 V supply A-weighted		92		dB
SNDR 1 kHz, 1.8 V supply A-weighted		84		dB
THD 1 kHz, -1 dB input, 1.8-V supply		75		dB
THD 1 kHz, -1 dB input, 3.3-V supply		85		dB
Deviation from linear phase				°
Pass band				kHz
Pass band ripple				dB
Stop band				kHz
Stop band attenuation				dB
Group delay, 8 kHz				ms
Group delay, 48 kHz				ms
Cross talk, 1.8 V				dB
Cross talk, 3.3 V				dB

4 Applications

Figure 3 to *Figure 6* below show the circuit diagrams of a typical application with the STA510F.

Figure 3. STA330 codec block

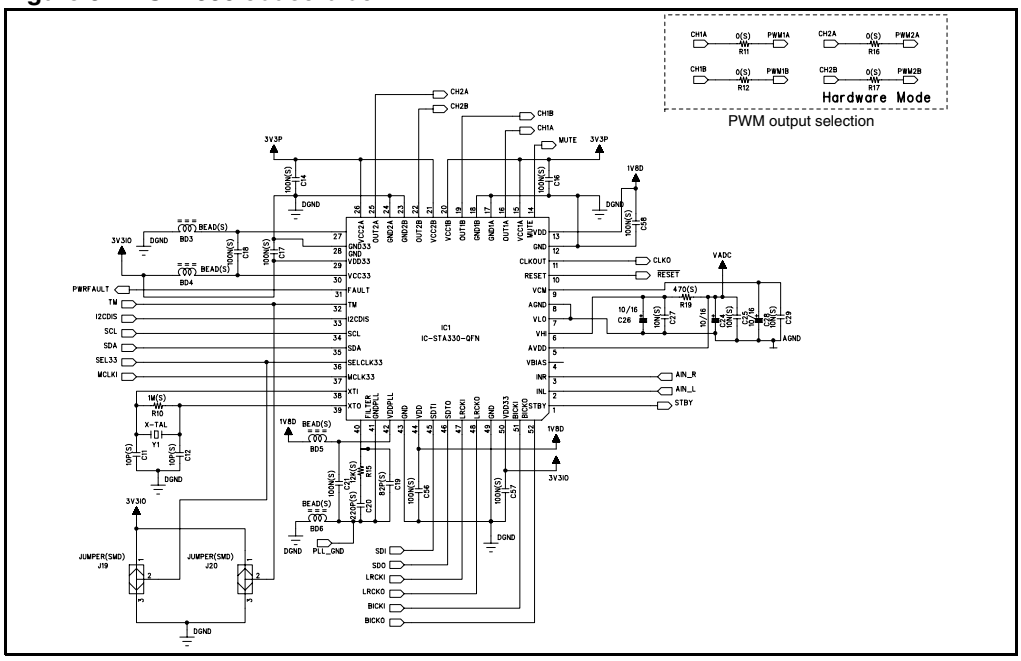
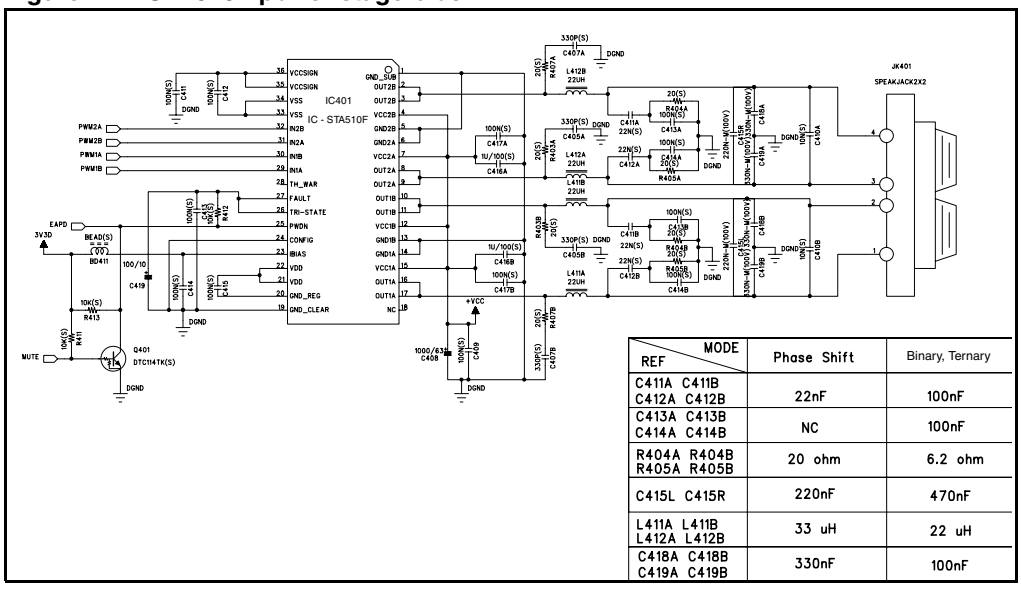


Figure 4. STA510F power stage block



MODE / REF	Phase Shift	Binary, Ternary
C411A C411B C412A C412B	22nF	100nF
C413A C413B C414A C414B	NC	100nF
R404A R404B R405A R405B	20 ohm	6.2 ohm
C415L C415R	220nF	470nF
L411A L411B L412A L412B	33 uH	22 uH
C418A C418B C419A C419B	330nF	100nF

Figure 5. Connector and power supply block

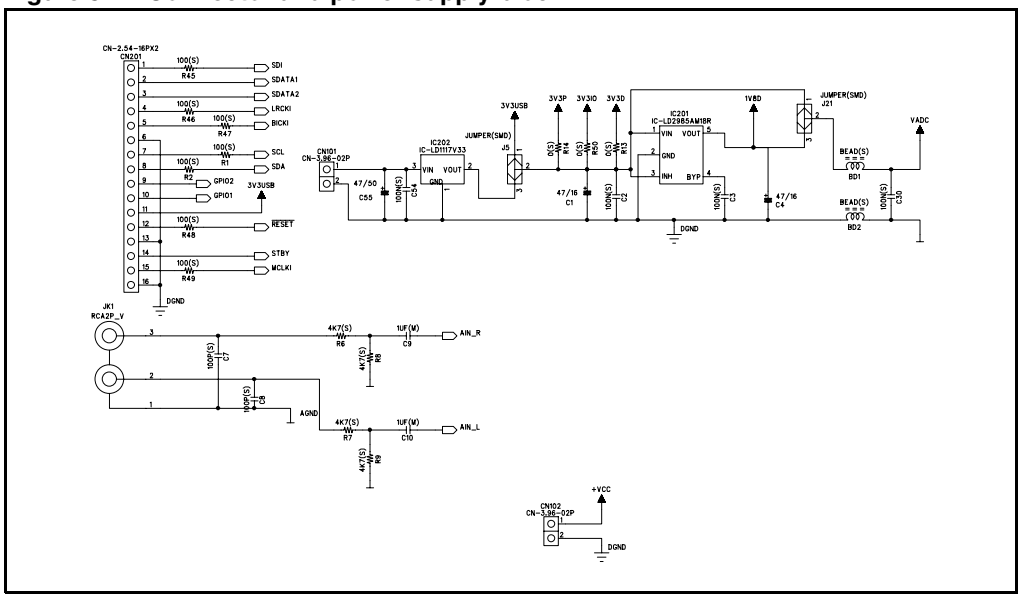
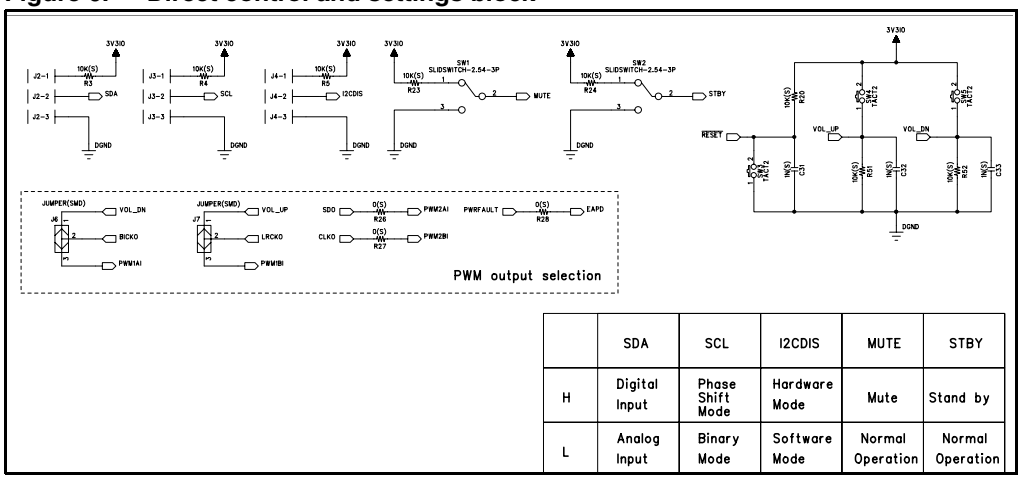


Figure 6. Direct control and settings block



	SDA	SCL	I2CDIS	MUTE	STBY
H	Digital Input	Phase Shift Mode	Hardware Mode	Mute	Stand by
L	Analog Input	Binary Mode	Software Mode	Normal Operation	Normal Operation

Table 8. Components for setting up application

Component	µController	µLess	Comments
R413	No	Yes	EAPD (µLess mode)
R28	Yes	No	POWERFAULT -> EAPD (µP mode)
R12	Yes	Yes	STA510F: PWM1B
R21	No	No	
R11	Yes	Yes	STA510F: PWM1A
R18	No	No	
R17	Yes	Yes	STA510F: PWM2B

Table 8. Components for setting up application (continued)

Component	µController	µLess	Comments
R25	No	No	
R16	Yes	Yes	STA510F: PWM2A
R22	No	No	
J7	2-3	1-2	Volume up (µLess mode)
J6	2-3	1-2	Volume down (µLess mode)
J5	2-3	2-3	3.3-V supply
J4	2-3 (L)	1-2 (H)	I2CDIS

5 Digital processing

The STA330 processor block is a digital block providing two channels of audio processing and channel-mapping capability.

5.1 Signal processing flow

I^2S or stereo ADC data can be selected. The I^2S frequency range is from 8 kHz to 192 kHz. ADC sampling frequency can be selected from 8 kHz to 48 kHz.

5.2 I^2C interface disabled

When pin I2CDIS = 1, the SDA, SCL, LRCLKO and BICLKO pins can be pulled high or low to change certain parameters of operation.

- SDA = 0: FFX input comes from ADC
  SDA = 1: FFX input comes from digital audio interface
- SCL = 0: binary output mode (binary soft start/stop enabled)
  SCL = 1: phase shift output mode
- LRCLKO = 0: no volume change
  LRCLKO = 1: volume up
- BICLKO = 0: no volume change
  BICLKO = 1: volume down

At power-up, the master volume is set to -60 dB. When holding pin LRCLKO = 1 and pin BICLKO = 1 simultaneously, the master volume is set to 0 dB. A high pulse on pin LRCLKO causes a master volume change of +0.5 dB and a high pulse on pin BICLKO causes a master volume change of -0.5 dB.

5.3 Volume control and gain

The volume control structure of the STA330 consists of individual volume registers for each channel and a master volume register that provides an offset to each channel's volume setting. The individual channel volumes are adjustable in 0.5 dB steps from +36 dB to -91.5 dB. As an example, if register LVOL = 0x00 or +36 dB and register MVOL = 0x18 or -12 dB, then the total gain for the left channel is +24 dB.

When the mute bit is set to 1, all channels are muted. The volume control provides a soft mute with the volume ramping down to mute in 4096 samples from the maximum volume setting at the internal processing rate (approximately 48 kHz).

Table 9. Master volume offset as a function of register MVOL

MVOL[7:0]	Volume offset from channel value
0x00	0 dB
0x01	-0.5 dB
0x02	-1dB
…	…
0x78	-60 dB
…	…
0xFE	-105 dB
0xFF	Hard master mute

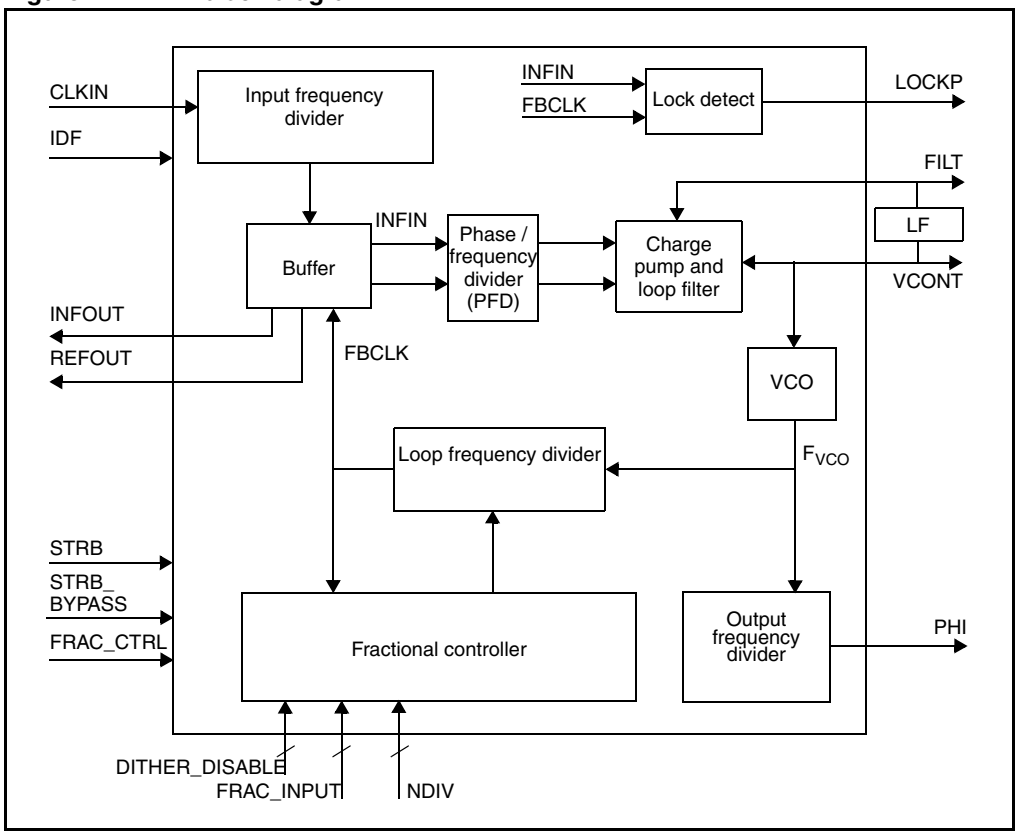
Table 10. Channel volume as a function of registers LVOL and RVOL

LVOL/RVOL[7:0]	Volume
0x00	+36 dB
0x01	+35.5 dB
0x02	+35 dB
…	…
0x47	+0.5 dB
0x48	0 dB
0x49	-0.5 dB
…	…
…	…
0xFF	-91.5 dB

6 PLL

Figure 7 shows the main components of the PLL.

Figure 7. PLL block diagram



6.1 Functional description

Phase/frequency detector

The phase/frequency detector (PFD) compares the phase difference between the corresponding rising edges of INFIN and FBCLK, (clock output from the loop frequency divider) by generating voltage pulses with widths proportional to the input phase error.

Charge pump and loop filter

This block converts the voltage pulses from the phase/frequency detector to current pulses which charge the loop filter and generate the control voltage for the voltage-controlled oscillator. The loop filter is placed external to the PLL on pin FILT.

Voltage controlled oscillator

The voltage controlled oscillator (VCO) is the oscillator inside the PLL. It produces a frequency output (F_{VCO}) proportional to the input control voltage.

Input frequency divider

This frequency divider divides the PLL input clock CLKIN by a factor called the input division factor (IDF) to generate the PFD input frequency INFIN.

Loop frequency divider

This frequency divider is present within the PLL for dividing F_{VCO} by a factor called the loop division factor (LDF). The output of this block is the FBCLK.

Output frequency divider

The PLL output PHI is generated by dividing the F_{VCO} by the output division factor (ODF). The divider that divides the F_{VCO} to generate the clock to the core is called the output frequency divider. In the STA330, the ODF is fixed to be divisible by 2 and cannot be configured.

Lock-detect circuit

The output of this block (the LOCKP signal) is asserted high when the PLL enters the state of COARSE LOCK in which the output frequency is within ±10% (approximately) of the desired frequency. The LOCKP signal is refreshed every 32 cycles of the INFIN. The generated value is based on the result of comparing the number of FBCLK cycles in a window of 14 INFIN cycles. The different cases generated after comparison are as follows.

- If LOCKP is already at 0, then in the next refresh cycle LOCKP goes to 1 if the number of FBCLK cycles in the 14-cycle INFIN window is 13, 14, or 15. Otherwise LOCKP stays at 0.
- If LOCKP is already at 1, then in the next refresh cycle LOCKP goes to 0 if the number of FBCLK cycles in the 25-cycle INFIN window is less than 11 or higher than 17, otherwise LOCKP stays at 1.
- If LOCKP is already at 1 and CLKIN is lost (no longer present on the input pin), LOCKP stays at 1. In this case, the PLL is unlocked.

PLL filter

Figure 8 shows the PLL filter scheme. Recommended values are R1 = 12.5 kΩ, C1 = 250 pF, and C2 = 82 pF.

Figure 8. PLL filter scheme

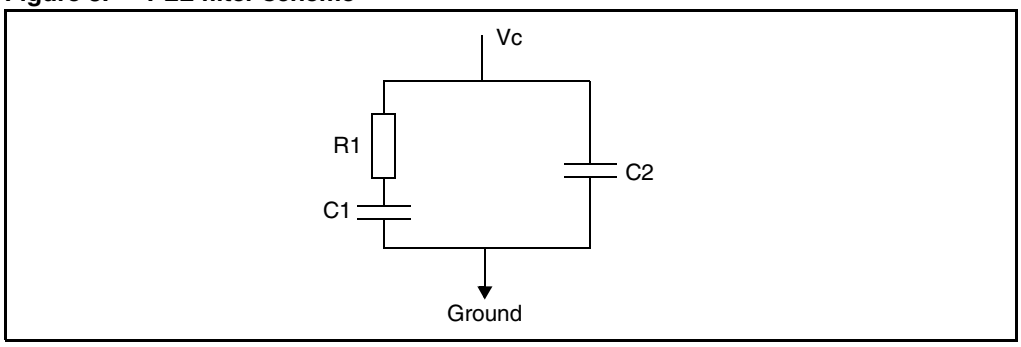


Table 6 on page 10 gives a typical lock time value for the PLL.

6.2 Configuration examples

The STA330 PLL can be configured in two ways:

- default startup configuration
- direct PLL programming

The default startup configuration reads the device defaults. With this configuration, it is not necessary to program the PLL dividers directly as some presets are used. In this mode, the oversampling ratio between pins XTI (or MCLK33) and LRCLKI is fixed to 256.

The direct PLL programming bypasses the automatic presets allowing direct programming of the PLL dividers.

The output PLL frequency can be determined as following:

Output division factor:

$ODF = 2$

Relation between input and output clock frequency:

$F_{INFIN} = F_{XTI} / IDF$

If register bit PLLCFG0.FRAC_CTRL = 1

$F_{VCO} = F_{INFIN} * (LDF + FRACT / 2^{16} + 1 / 2^{17})$

$F_{PHI} = F_{VCO} / ODF$

When register bit PLLCFG0.DITHER_DISABLE[1] = 1, the $1 / 2^{17}$ factor is not in the multiplication. It is recommended to keep register bit PLLCFG0.DITHER_DISABLE[1] = 0, otherwise there can be spurious signals in the output clock spectrum.

If register bit PLLCFG0.FRAC_CTRL = 0, then:

$F_{VCO} = F_{INFIN} * LDF$

$F_{PHI} = F_{VCO} / ODF$

In the above equations:

FRACT = Decimal equivalent of register bit PLLCFG1.FRAC_INPUT[15:0]

IDF = Input division factor (refer to previous formulas)

LDF = Loop division factor (refer to previous formulas)

ODF = Output division factor = 2

F_{INFIN} = INFIN frequency

F_{XTI} = XTI frequency

F_{VCO} = VCO frequency

F_{PHI} = Frequency of the PLL output clock

When selecting the value of IDF, LDF and FRACT make sure the following limits are maintained:

$2.048\ MHz < F_{XTI} < 49.152\ MHz$

$2.048\ MHz < F_{INFIN} < 16.384\ MHz$

$65.536\ MHz < F_{VCO} < 98.304\ MHz$

There are also some additional constraints on IDF and LDF. IDF should be greater than 0, LDF should be greater than 5 if FRAC_CTRL = 0 and greater than 8 if FRAC_CTRL = 1.

When automatic settings are not used, the PLL must be configured to generate an internal frequency of N * f_S, where f_S is the LRCLKI pin frequency. Values of N are given in *Table 11*.

Table 11. Oversampling table

f_S (kHz)	N	F_{PHI} (MHz)
8	4096	32.768
11.025	4096	45.1584
12	4096	49.152
16	2048	32.768
22.05	2048	45.1584
24	2048	49.152
32	1024	32.768
44.1	1024	45.1584
48	1024	49.152
64	512	32.768
88.2	512	45.1584
96	512	49.152
128	256	32.768
176.4	256	45.1584
192	256	49.152

In the following examples **floor** means rounded towards zero and **round** means rounded to nearest integer.

Example 1

F_{XTI} = 13 MHz

f_S = 44.1 kHz

IDF should be equal to 3 otherwise LDF become less than 8 (FRAC_CTRL must be 1):

LDF = floor(45.1584 / (13 / IDF)) = 10

FRACT = round([(45.1584 / (13 / IDF)) - floor(45.1584 / (13 / IDF))] * 2^{16}) = 27602

Using the above configuration, the system clock is 45.15841675 MHz, the approximate static error is 16 Hz (that is, 0.5 ppm).

Example 2

F_{XTI} = 19.2 MHz

f_S = 48 kHz

IDF should be equal to 4 otherwise LDF become less than 8 (FRAC_CTRL must be 1):

LDF = floor(49.152 / (19.2 / IDF)) = 10

FRACT = round([(49.152 / (19.2 / IDF)) - floor(49.152 / (19.2 / IDF))] * 2^{16}) = 15728

Using the above configuration, the system clock is 49.151953125 MHz, the approximate static error is 47 Hz (that is, 1 ppm).

7 Analog-digital converter (ADC)

7.1 Functional description

The STA330 analog input is provided through a low-power, low-voltage, stereo, audio-ADC front end designed for audio applications. It includes a programmable gain amplifier, anti-aliasing filter, a low-noise microphone biasing circuit, a third-order, MASH2-1, delta-sigma modulator, a digital decimating filter and a first-order DC-removal filter. This device is fabricated using a 0.18 µm CMOS process, where high-speed precision analog circuits are combined with high-density logic circuits.

The ADC works in a microphone-input (mic-in) mode and in a line-input mode.

If the line-input mode is selected, the ADC is configured in stereo and all conversion channels are active.

If the microphone-input mode is selected, the ADC is configured in mono. The mono channel is routed through the left conversion path, and the right conversion path is kept in power-down mode to minimize power consumption. A programmable gain amplifier (PGA) is available in mic-in mode, giving the possibility to amplify the signal from 0 to +42 dB in steps of 6 dB.

7.1.1 Digital anti-aliasing filter characteristics

The digital filter characteristics are shown in *Table 12*.

Table 12. Digital filter characteristics

Parameter	Typical
Pass band	0.4535 * f_S
Pass band ripple: Fs mode Fs_by_2 mode Fs_by_4 mode	 0.08 dB at 44.1 kHz 0.08 dB at 22.05 kHz 0.08 dB at 11.025 kHz
Stop band attenuation: Fs mode Fs_by_2 mode Fs_by_4 mode	 45 dB at 44.1 kHz 45 dB at 22.05 kHz 45 dB at 11.025 kHz
Group delay: Fs mode Fs_by_2 mode Fs_by_4 mode	 0.4 ms at 32 kHz 0.7 ms at 16 kHz 1.4 ms at 8 kHz

7.1.2 High-pass filter characteristics

Table 13. High-pass filter characteristics

Parameter	Typical
Frequency response: -3 dB -0.08 dB	 7 Hz 50 Hz
Phase deviation at 20 Hz	19.35°
Pass-band ripple	0.08 dB

7.1.3 Programmable gain amplifier

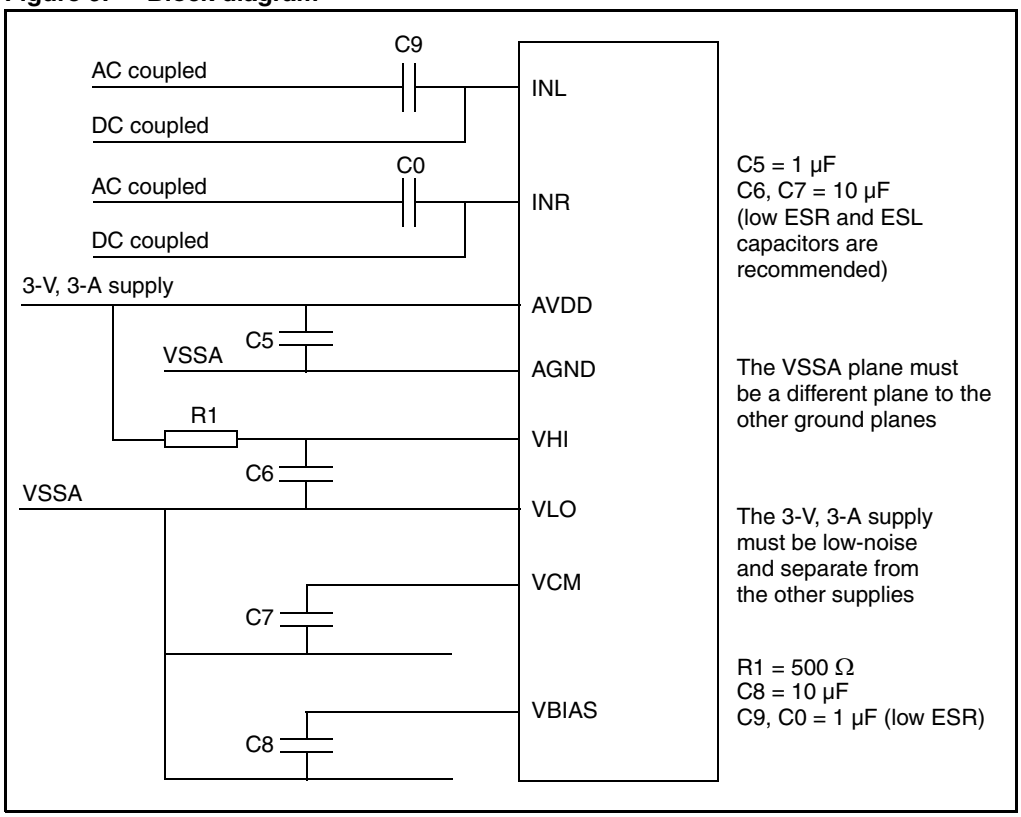
The programmable gain amplifier (PGA) is available in mic-in mode only. It is possible to amplify the input signal from 0 to 42 db in steps of 6 db. The setting is done through bits PGA of register *ADCCFG on page 47*.

See *Table 7 on page 10* for performance values.

7.2 Application scheme

Figure 9 shows the filter circuit.

Figure 9. Block diagram



7.3 Configuration examples

The ADC sampling frequency can be selected from three values:

- normal (from 32 kHz to 48 kHz)
- low (from 16 kHz to 24 kHz)
- very-low (from 8 kHz to 12 kHz).

The setting is done through bits ADC_FS_RANGE in register *MISC on page 48*. For all other settings, register *ADCCFG on page 47* is used.

8 Serial digital audio interface (SAI)

8.1 Specifications

The serial-to-parallel interface and the parallel-to-serial interface can have different sampling rates.

The following terms are used in this section:

- **BICLK active edge:** Pins SDATAI, SDATAO, LRCLKI, LRCLKO always change synchronously with BITCLK active edges. The active edge can be configured to a rising or falling edge via register programming.
- **BICLK strobe edge:** Pins SDATAI, SDATAO, LRCLKI, LRCLKO should be stable near BICLK strobe edges, the slave device is able to use strobe edges to latch serial data internally.

8.2 Master mode

In this mode pins BICLKI/BICLKO and pins LRCLKI/LRCLKO are configured as outputs.

Figure 10. Master mode

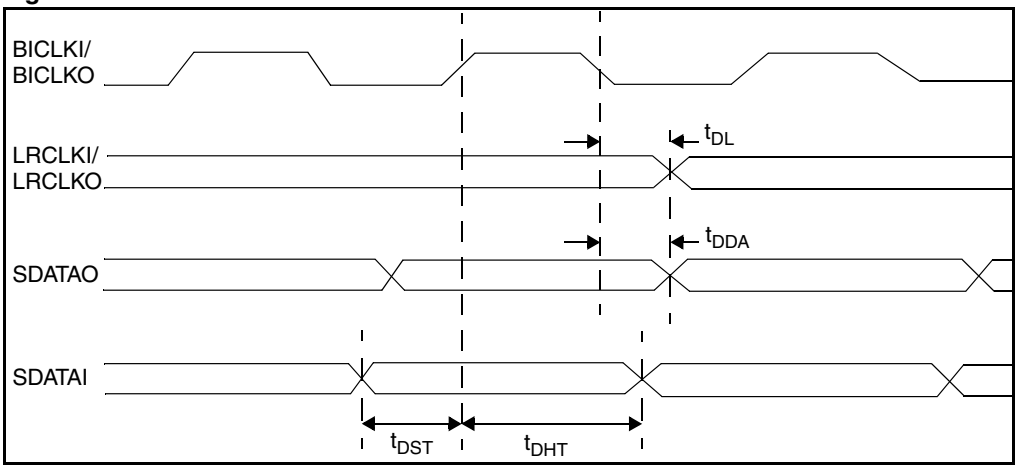


Table 14. Master mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{DL}	LRCLKI/LRCLKO propagation delay from BICLK active edge	0		10	ns
t_{DDA}	SDATAI propagation delay from BICLKI/O active edge	0		15	ns
t_{DST}	Sdatao setup time to BICLKI/O strobing edge	10			ns
t_{DHT}	Sdatao hold time from BICLKI/O strobing edge	10			ns

8.3 Slave mode

In this mode, pins BICLKI/O and pins LRCLKI/O are configured as inputs.

Figure 11. Slave mode

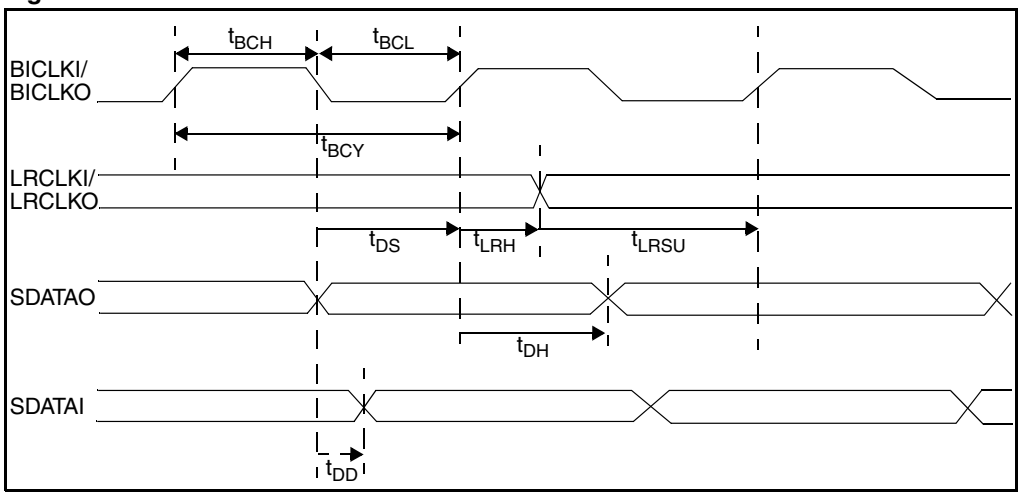


Table 15. Slave mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{BCY}	BICLK cycle time	50			ns
t_{BCH}	BICLK pulse width high	20			ns
t_{BCL}	BICLK pulse width low	20			ns
t_{LRSU}	LRCLKI/LRCLKO setup time to BICLK strobing edge	10			ns
t_{LRH}	LRCLKI/LRCLKO hold time to BICLK strobing edge	10			ns
t_{DS}	SDATAO setup time to BICLK strobing edge	10			ns
t_{DH}	SDATAO hold time to BICLK strobing edge	10			ns
t_{DD}	SDATAI propagation delay from BICLK active edge	0		10	ns

8.4 Serial formats

Different audio formats are supported in both master and slave modes. Clock and data configurations can be customized to match most of the serial audio protocols available on the market.

Data length can be customized for 8-, 16-, 24- and 32-bit.

Figure 12. Right justified

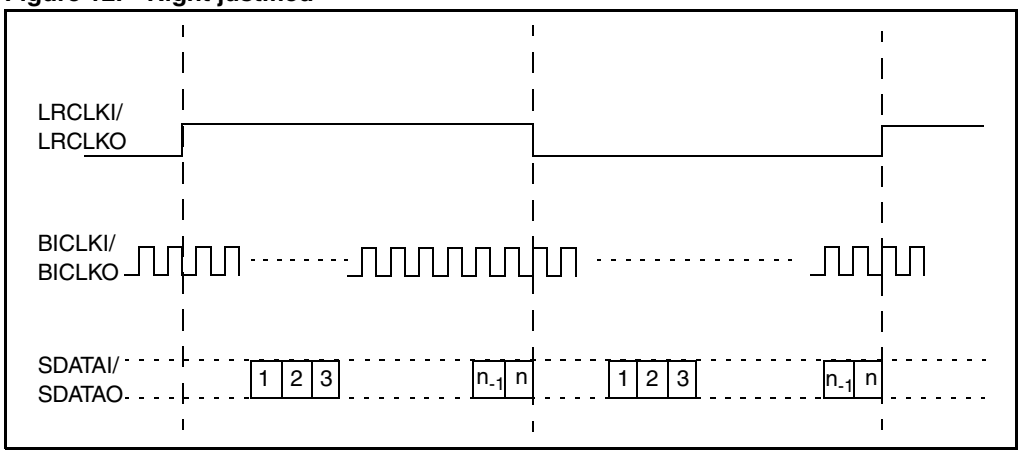
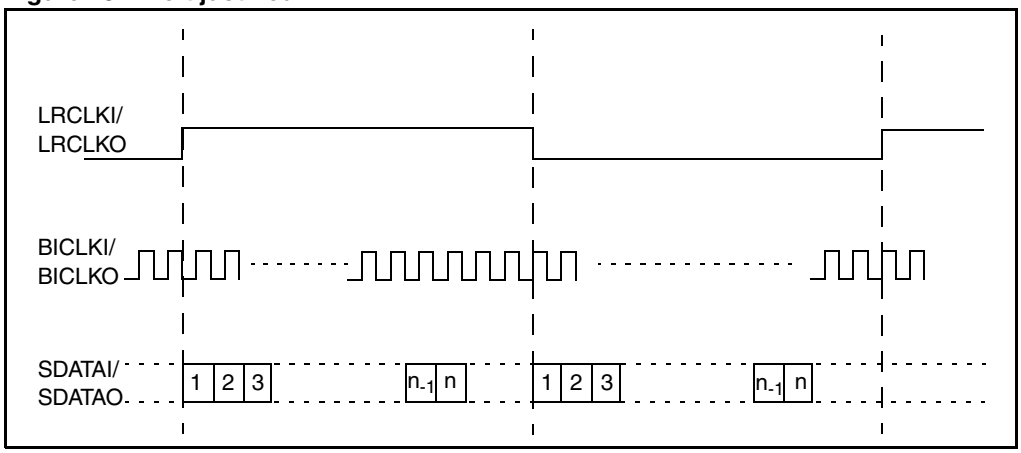
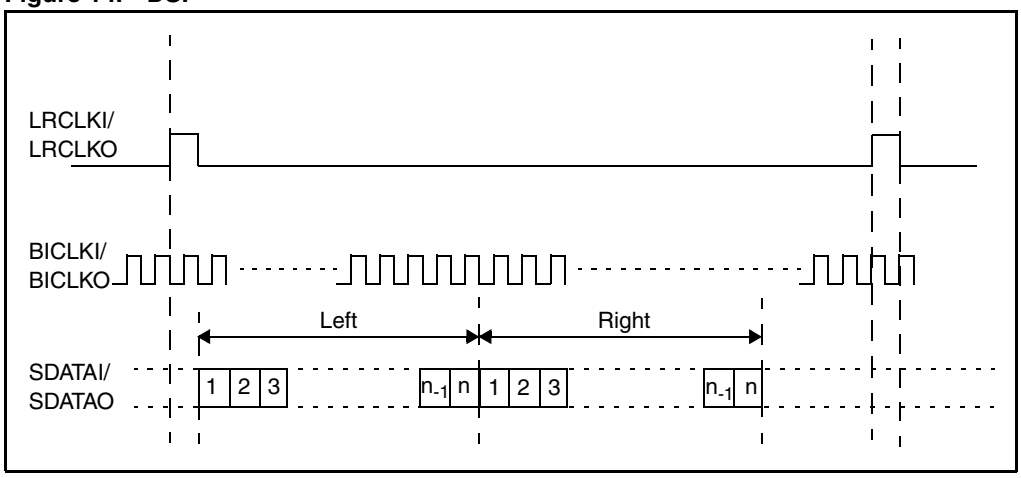


Figure 13. Left justified



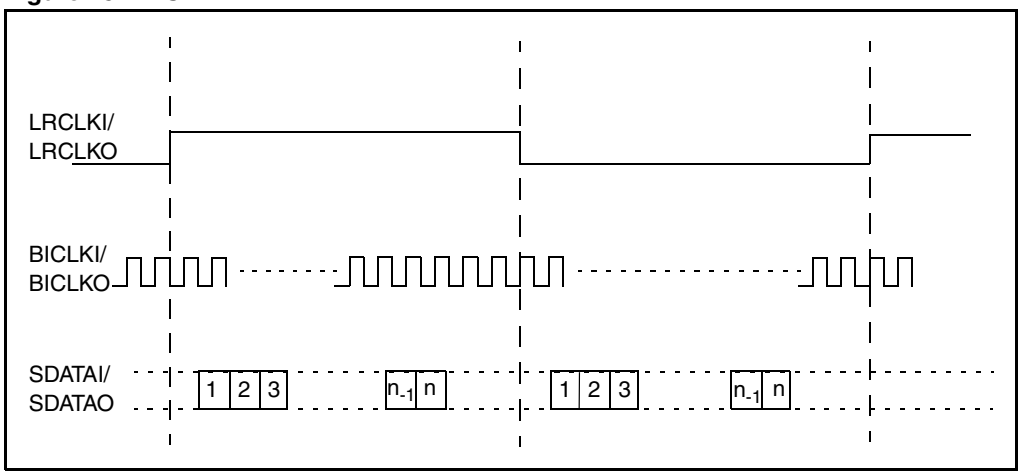
8.4.1 DSP

Figure 14. DSP



8.4.2 I^2S

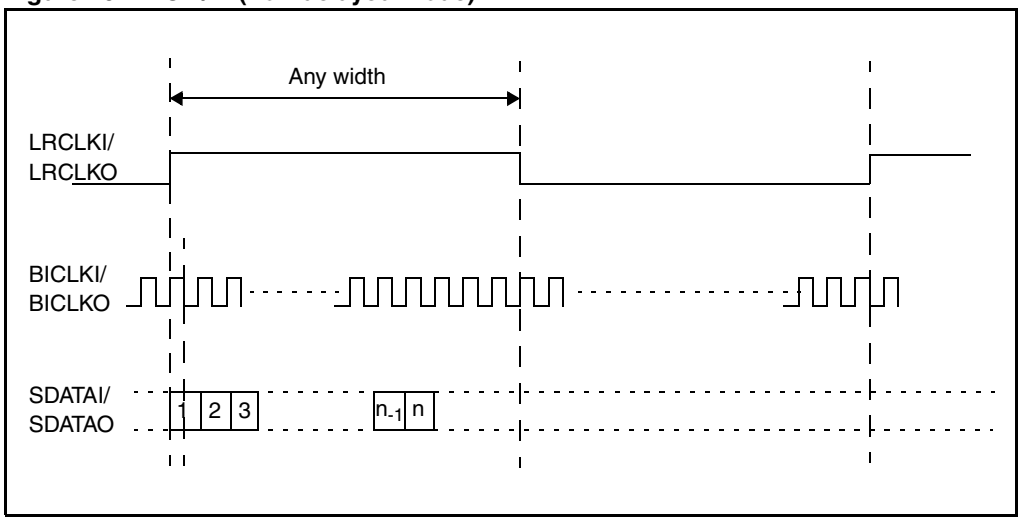
Figure 15. I^2S



8.4.3 PCM/IF (non-delayed mode)

- MSB first
- 16-bit data

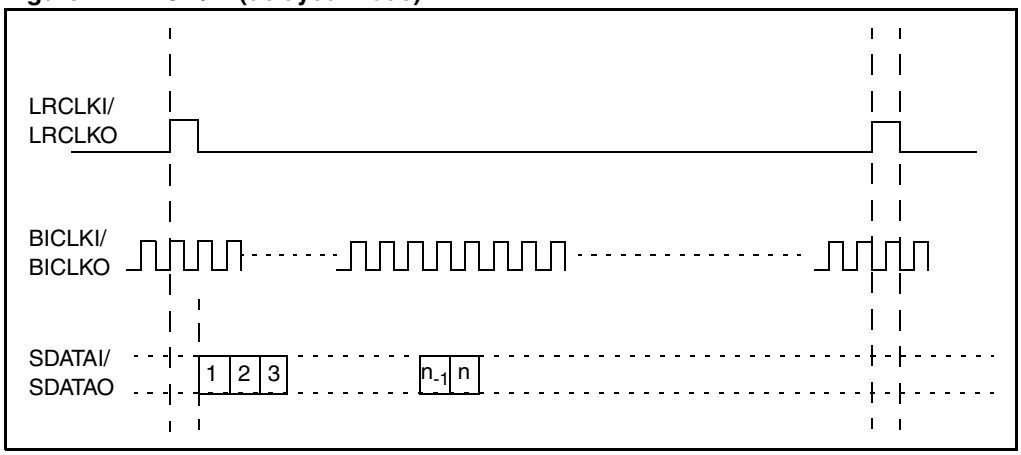
Figure 16. PCM/IF (non-delayed mode)



8.4.4 PCM/IF (delayed mode)

- MSB first
- 16-bit data

Figure 17. PCM/IF (delayed mode)



8.5 SAI pass-through

A configuration is available which allows the SAI input signal to be passed straight to the digital output. The STA330 is able to translate the incoming serial audio interface signal from SAI-in to a different output format on SAI-out. So the SAI pass-through enables devices to be cascaded, even devices with slightly different protocols.

The pass-through is set by programming register *PWMINT1 on page 49* with the value 0x00 and register *PWMINT2* with the value 0x01.

SAI-in protocol is set up with registers *S2PCFG0 on page 39* and *S2PCFG1* and SAI-out protocol with *P2SCFG0 on page 41* and *P2SCFG1*.

Input and output data sampling frequencies must be the same.

9 I²C interface

This section describes the communication protocol of the I²C interface.

9.1 Data transition and change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a start or stop condition.

9.2 Start condition

A start condition is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A start condition must precede any command for data transfer.

9.3 Stop condition

A stop condition is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A stop condition terminates communication between the STA330 and the master bus.

9.4 Data input

During data input, the STA330 samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

9.5 Device addressing

To start communication between the master and the STA330, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8 bits (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA330, the I²C interface has the device address 0x34.

The 8th bit (LSB) identifies read or write operation (R/W), this bit is set to 1 in read mode and 0 in write mode. After a start condition, the STA330 identifies on the bus the device address and if a match is found, it acknowledges the identification on SDA bus during the 9th bit time. The byte following the device identification byte is the internal space address.

9.6 Write operation

Following the start condition the master sends a device select code with the R/W bit set to 0. The STA330 acknowledges this and the writes to the byte of the internal address. After receiving the internal byte address, the STA330 responds with an acknowledgement.

9.6.1 Byte write

In the byte-write mode the master sends one data byte. This is acknowledged by the STA330. The master then terminates the transfer by generating a stop condition.

9.6.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generates a stop condition which terminates the transfer.

9.7 Read operation

9.7.1 Current address byte read

Following the start condition the master sends a device select code with the R/W bit set to 1. The STA330 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a stop condition.

9.7.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA330. The master acknowledges each data byte read and then generates a stop condition terminating the transfer.

9.7.3 Random address byte read

Following the start condition the master sends a device select code with the R/W bit set to 0. The STA330 acknowledges this and then the master writes the internal address byte. After receiving the internal byte address, the STA330 again responds with an acknowledgement. The master then initiates another start condition and sends the device select code with the R/W bit set to 1. The STA330 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a stop condition.

9.7.4 Random address multi-byte read

The multi-byte read modes could start from any internal address. Sequential data bytes are read from sequential addresses within the STA330. The master acknowledges each data byte read and then generates a stop condition terminating the transfer.

Figure 18. I²C write operations

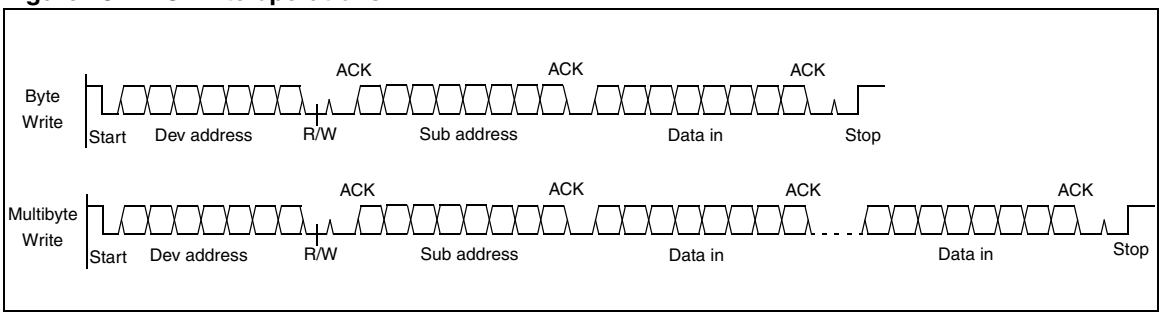
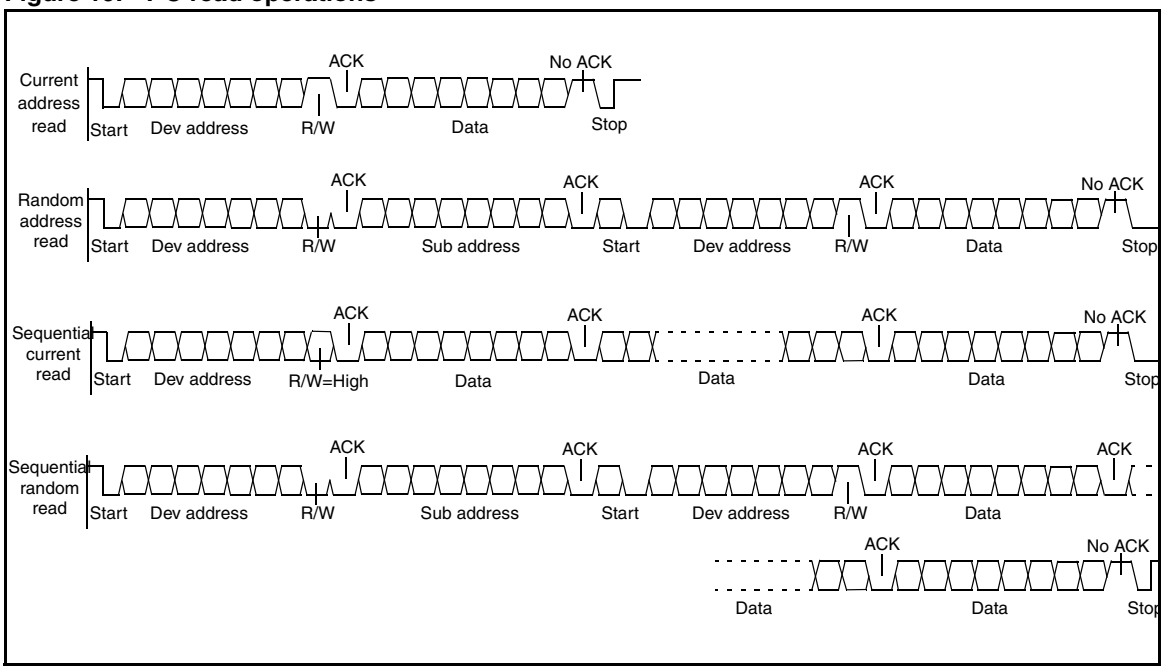


Figure 19. I²C read operations



10 Registers

10.1 Summary

Table 16. Register summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	FFXCFG0	MUTE	POW_STBY	SOFT_ VOL_ON	BIN_SOFT START	TIM_SOFT_VOL[3:0]			
0x01	FFXCFG1	L1_R2	MUTE_ON_ INVALID	PWM_MODE[1:0]		PWM_SHIFT[1:0]			
0x02	MVOL	SET_VOL_MASTER[7:0]							
0x03	LVOL	SET_VOL_LEFT[7:0]							
0x04	RVOL	SET_VOL_RIGHT[7:0]							
0x05	TTF0	TIM_TS_FAULT[15:8]							
0x06	TTF1	TIM_TS_FAULT[7:0]							
0x07	TTP0	TIM_TS_POWUP[15:8]							
0x08	TTP1	TIM_TS_POWUP[7:0]							
0x0A	S2PCFG0	BICLK_ STRB	LRCLK_ LEFT	SHARE_ BILR	MSB_FIRST	DATA_FORMAT[2:0]			MASTER_ MODE
0x0B	S2PCFG1	PDATA_LENGTH[1:0]		BICLK_OS[1:0]		MAP_L[1:0]		MAP_R[1:0]	
0x0C	P2SCFG0	BICLK_ STRB	LRCLK_ LEFT	SDATAO_ ACT	MSB_FIRST	DATA_FORMAT[2:0]			MASTER_ MODE
0x0D	P2SCFG1	PDATA_LENGTH[1:0]		BICLK_OS[1:0]		MAP_L[1:0]		MAP_R[1:0]	
0x14	PLLCFG0	PLL_DIRECT _PROG	FRAC_ CTRL	DITHER_DISABLE[1:0]		IDF[3:0]			
0x15	PLLCFG1	FRAC_INPUT[15:8]							
0x16	PLLCFG2	FRAC_INPUT[7:0]							
0x17	PLLCFG3	STRB	STRB _BYPASS	NDIV[5:0]					
0x18	PLLPFE	PLL_ BYP_ UNL	BICLK2PLL	PLL_ PWDN	PFE1A	PFE1B	PFE2A	PFE2B	RESET_ FAULT
0x19	PLLST	PLL_ UNLOCK	PLL_ PWD_STATE	PLL_ BYP_STATE					
0x1E	ADCCFG	PGA[2:0]			INSEL	STBY	BYPASS_ CALIB	CLKENBL	
0x1F	CKOCFG	CLKOUT_ DIS	CLKOUT_SEL[1:0]						
0x20	MISC	OSC_DIS	P2P_FS_RANGE[2:0]			ADC_FS_RANGE[1:0]		P2P_ IN_ ADC	CORE_ CLKENBL
0x21	PADST0	Reserved							
0x22	PADST1	Reserved							
0x23	FFXST						INVALID_ INP_FBK	MUTE_ INT_FBK	BINSS_FBK
0x28	BISTRUN	Reserved							
0x29	BISTST0	Reserved							

Table 16. Register summary (continued)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2A	BISTST1	Reserved							
0x2B	BISTST2	Reserved							
0x2D	PWMINT1	PWM_INT[15:8]							
0x2E	PWMINT2	PWM_INT[7:0]							
0x32	POWST	POWER DOWN	POW_ TRISTATE	POW_ FAULT1A	POW_ FAULT1B	POW_ FAULT2A	POW_ FAULT2B		

10.2 General registers

FFXCFG0 FFX configuration register 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MUTE	POW_STBY	SOFT_VOL_ON	BIN_ SOFTSTART	TIM_SOFT_VOL[3:0]			

Address: 0x00

Type: R/W

Buffer: No

Reset: 0x75

Description:

7 MUTE:
0: default 1: FFX output is zero

6 POW_STBY:
0: FFX bridge is in power-up mode
1: FFX bridge is in standby mode (default)

5 SOFT_VOL_ON:
0: smooth transition not active
1: smooth transition when changing volume control (default)

4 BIN_SOFTSTART:
Reserved (default is 1)

3:0 TIM_SOFT_VOL: volume control time step for any 0.5 dB volume change
Time is $2^{TIM\_SOFT\_VOL}$ * 20.83 µs
Default is 666.66 µs

FFXCFG1 Configuration register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L1_R2	MUTE_ON_ INVALID	PWM_MODE[1:0]		PWM_SHIFT[1:0]			

Address: 0x01

Type: R/W

Buffer: No

Reset: 0xF8

Description:

7 L1_R2: channel mapping:
0: right channel is mapped to output channel 1 and left channel is mapped to output channel 2
1: left channel is mapped to output channel 1 and right channel is mapped to output channel 2 (default)

6 MUTE_ON_ INVALID: mutes PWM outputs if invalid digital data is received:
0: outputs are not muted 1: outputs are muted (default)

5:4 PWM_MODE[1:0]:
00: binary (output B is opposite of output A)
01: binary headphones (output B is 50% duty cycle)
10: ternary
11: phase shift (default)

3:2 PWM_SHIFT[1:0]:
10: default
PWM period-shift between channels 1 and 2
Value is N * 90°
Default is 180°

1:0 Reserved (default is 0)

MVOL Master volume control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SET_VOL_MASTER[7:0]							

Address: 0x02

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 SET_VOL_MASTER[7:0]: master volume control:
From 0 dB to -127.5 dB in 0.5 dB steps

LVOL Left channel volume control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SET_VOL_LEFT[7:0]							

Address: 0x03

Type: R/W

Buffer: No

Reset: 0x48

Description:

7:0 SET_VOL_LEFT[7:0]: left channel volume control:
Left channel volume control (from +36 dB to -91.5 dB in 0.5 dB steps)
Default value (0x48) corresponds to 0 dB

RVOL Right channel volume control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SET_VOL_RIGHT[7:0]							

Address: 0x04

Type: R/W

Buffer: No

Reset: 0x48

Description:

7:0 SET_VOL_RIGHT[7:0]: right channel volume control:
Right channel volume control (from +36 dB to -91.5 dB in 0.5 dB steps)
Default value (0x48) corresponds to 0 dB

TTF0 Tri-state time-after-fault register 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIM_TS_FAULT[15:8]							

Address: 0x05

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 MSBs of TIM_TS_FAULT[15:0]:
See *TTF1 on page 37*.

TTF1 Tri-state time-after-fault register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIM_TS_FAULT(7:0)							

Address: 0x06

Type: R/W

Buffer: No

Reset: 0x02

Description:

7:0 LSBs of TIM_TS_FAULT[15:0]: time in which power is held in tri-state mode after a fault signal:
Time is TIM_TS_FAULT * 83.33 µs.
Default value (0x0002) corresponds to 166.66 µs tri-state time after fault

TTP0 Tri-state time-after-power-up register 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIM_TS_POWUP[15:8]							

Address: 0x07

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 MSBs of TIM_TS_POWUP[15:0]:
See register *TTP1*.

TTP1 Tri-state time-after-power-up register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIM_TS_POWUP[7:0]							

Address: 0x08

Type: R/W

Buffer: No

Reset: 0x02

Description:

7:0 LSBs of TIM_TS_POWUP[15:0]: time in which power is held in tri-state mode after a power-up signal:
Time is TIM_TS_POWUP * 83.33 µs
Default value(0x0002) corresponds to 166.66 µs tri-state time after power-up

S2PCFG0 Serial-to-parallel audio interface config register 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BICLK_STRB	LRCLK_LEFT	SHARE_BILR	MSB_FIRST	DATA_FORMAT[2:0]			MASTER_ MODE

Address: 0x0A

Type: R/W

Buffer: No

Reset: 0xD2

Description:

7 BICLK_STRB:
0: bit clock strobe edge is falling edge, bit clock active edge is rising edge
1: bit clock strobe edge is rising edge, bit clock active edge is falling edge (default)

6 LRCLK_LEFT:
0: left/right clock is low for left channel, high for right channel
1: left/right clock is high for left channel, low for right channel (default)

5 SHARE_BILR:
0: default
1: left/right clock and bit clock are shared between serial-parallel interface and parallel-to-serial interface, BICLKI and LRCLKI are used

4 MSB_FIRST:
0: LSB first 1: MSB first (default)

3:1 DATA_FORMAT[2:0]: serial interface protocol format:
000: left Justified 001: I^2S (default)
010: right justified 100: PCM no delay
101: PCM delay 111: DSP

0 MASTER_MODE:
0: default 1: serial interface is in master mode

S2PCFG1 Serial-to-parallel audio interface config register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDATA_LENGTH[1:0]		BICLK_OS[1:0]		MAP_L[1:0]		MAP_R[1:0]	

Address: 0x0B

Type: R/W

Buffer: No

Reset: 0x91

Description:

7:6 PDATA_LENGTH[1:0]: serial-to-parallel interface data length:
10: 24 bits (default)
Length is (N+1) * 8 bit

5:4 BICLK_OS[1:0]: bit clock oversampling:
01:64 * f_s (default)
Value is (N+1) * 32 * f_s (where f_s = sampling frequency)

3:2 MAP_L[1:0]: left data-mapping slot:
00: slot0 (default)
Value is nth slot

1:0 MAP_R[1:0]: right data-mapping slot:
01: slot1 (default)
Value is nth slot

P2SCFG0 Parallel-to-serial audio interface configuration register 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BICLK_ STRB	LRCLK_LEFT	SDATAO_ACT	MSB_FIRST	DATA_FORMAT[2:0]			MASTER_ MODE

Address: 0x0C

Type: R/W

Buffer: No

Reset: 0xD3

Description:

7 BICLK_STRB: defines the bit clock edges:
0: strobe is falling edge, active edge is rising
1: strobe is rising edge, active edge is falling (default)

6 LRCLK_LEFT: defines the channel for the LR clock:
0: clock is low for left channel, high for right channel
1: clock is high for left channel, low for right channel (default)

5 SDATAO_ ACT: sets the behavior of pin SDATAO:
0: output is tri-stated when no data is sent (default)
1: output is never in tri-state (it is 0 when no data is sent)

4 MSB_FIRST: data alignment in the protocol for SDATAI and SDATAO:
0: LSB is the first bit 1: MSB is the first bit (default)

3:1 DATA_FORMAT[2:0]: serial interface protocol format:
000: left justified 001: I^2S (default)
010: right justified 100: PCM no delay
101: PCM delay 110: Reserved
111: DSP

0 MASTER_ MODE: selects serial interface master/slave mode:
0: slave 1: master (default)

P2SCFG1 Parallel-to-serial audio interface config register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDATA_LENGTH[1:0]		BICLK_OS[1:0]		MAP_L[1:0]		MAP_R[1:0]	

Address: 0x0D

Type: R/W

Buffer: No

Reset: 0x91

Description:

7:6 PDATA_LENGTH[1:0]: serial-to-parallel interface data length:
10: 24 bits (default)
Length is (PDATA_LENGTH + 1) * 8 bit

5:4 BICLK_OS[1:0]: bit clock oversampling:
01: 64 * f_s (default)
Value is (BICLK_OS+1) * 32 * f_s

3:2 MAP_L[1:0]: left data-mapping slot:
00: slot0 (default)
Value is nth slot

1:0 MAP_R[1:0]: right channel data-mapping slot:
01: slot1 (default)
Value is nth slot

PLLCFG0 PLL configuration register 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL_DIRECT_PROG	FRAC_CTRL	DITHER_DISABLE[1:0]		IDF[3:0]			

Address: 0x14

Type: R/W

Buffer: No

Reset: 0x00

Description:

7 PLL_DIRECT_PROG: PLL programming:
0: default
1: PLL is programmed according to the PLLCFG register settings

6 FRAC_CTRL:
0: default
1: PLL fractional-frequency synthesis is enabled

5:4 DITHER_DISABLE[1:0]:
00: default
MSB = 1: disables rectangular PDF dither input to SDM
LSB = 1: disables triangular PDF dither input to SDM

3:0 IDF[3:0]: PLL input division factor:
0000: IDF = 1 (default) 0001: IDF = 1
0010: IDF = 2 …
1111: IDF = 15

PLLCFG1 PLL configuration register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FRAC_INPUT[15:8]							

Address: 0x15

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 FRAC_INPUT[15:8]: 16 bits are used to set the fractional part of PLL multiplication factor

PLLCFG2 PLL configuration register 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FRAC_INPUT[7:0]							

Address: 0x16

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 FRAC_INPUT[7:0]: 16 bits are used to set the fractional part of PLL multiplication factor

PLLCFG3 PLL configuration register 3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STRB	STRB_BYPASS	NDIV[5:0]					

Address: 0x17

Type: R/W

Buffer: No

Reset: 0x00

Description:

7 STRB: asynchronous strobe input to the fractional controller:
0: default

6 STRB_BYPASS: standby bypass:
0: STRB signal is not bypassed (default) 1: STRB signal is bypassed

5:0 NDIV[5:0]: PLL multiplication factor (integral part) named as loop division factor:
00 00XX: LDF = NA 00 0100: LDF = NA
00 0101: LDF = 5 ...
11 0111: LDF = 55 11 1XXX: LDF = NA

PLLPFE PLL/POP-free configuration register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL_BYP_UNL	BICLK2PLL	PLL_PWDN	PFE1A	PFE1B	PFE2A	PFE2B	RESET_FAULT

Address: 0x18

Type: R/W

Buffer: No

Reset: 0x00

Description:

7 PLL_BYP_UNL: PLL bypass:
0: PLL is not bypassed (default) 1: PLL is bypassed when not locked

6 BICLK2PLL:
0: default 1: BICLKI is input to PLL

5 PLL_PWDN:
0: default 1: PLL is put in power-down mode

4 PFE1A:
0: default
1: pop-free resistances are connected to output 1A

3 PFE1B:
0: default
1: pop-free resistances are connected to output 1B

2 PFE2A:
0: default
1: pop-free resistances are connected to output 2A

1 PFE2B:
0: default
1: pop-free resistances are connected to output 2B

0 RESET_FAULT:
0: default
1: fault signal in the I^2C register POWST is reset

PLLST PLL status register (RO)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL_UNLOCK	PLL_ PWD_ STATE	PLL_ BYP_ STATE					

Address: 0x19

Type: RO

Buffer: No

Reset: Undefined

Description:

7 PLL_UNLOCK: PLL unlock state:
0: PLL is not in unlock state 1: PLL is in unlock state

6 PLL_PWD_ STATE: PLL power-down state:
0: PLL is not in power-down state 1: PLL is in power-down state

5 PLL_BYP_STATE: PLL bypass state:
0: PLL is not in bypass state 1: PLL is in bypass state

4:0 Reserved

ADCCFG ADC configuration register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PGA[2:0]			INSEL	STBY	BYPASS_CALIB	CLKENBL	

Address: 0x1E

Type: RO

Buffer: No

Reset: Undefined

Description:

7:5 PGA[2:0]: gain selection bits for the ADC programmable gain amplifier:
000: default
Values are from 0 to 42 dB in 6 dB steps

4 INSEL:
0: line input selected (default)
1: microphone input selected (INL is the input)

3 STBY: ADC standby mode:
0: ADC in power-up mode (default) 1: ADC in standby mode

2 BYPASS_CALIB:
0: ADC DC-removal block not bypassed (default)
1: ADC DC-removal block bypassed

1 CLKENBL: Clock enable:
0: system clock not enabled
1: system clock available at ADC input (default)

0 Reserved

CKOCFG Clock-out configuration register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKOUT_DIS	CLKOUT_SEL[1:0]						

Address: 0x1F

Type: R/W

Buffer: No

Reset: Undefined

Description:

7 CLKOUT_DIS: CLKOUT PAD disabled
0: default 1: disabled

6:5 CLKOUT_SEL[1:0]:
00: default
The CLKOUT output frequency is the PLL output frequency divided by 2^{CLKOUT_SEL}.

4:0 Reserved

MISC Miscellaneous configuration register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSC_DIS	P2P_FS_RANGE[2:0]			ADC_FS_RANGE[1:0]		P2P_IN_ADC	CORE_ CLKENBL

Address: 0x20

Type: R/W

Buffer: No

Reset: 0x21

Description:

7 OSC_DIS: enable/disable crystal oscillator:
0: default 1: disabled

6:4 P2P_FS_RANGE[2:0]: FFX audio frequency range:
000: very low (f_s = 8 to 12 kHz)
001: low (f_s = 16 to 24 kHz)
010: normal (f_s = 32 to 48 kHz) (default)
011: high (f_s = 64 to 96 kHz)
1X: very high (f_s = 128 to 192 kHz)

3:2 ADC_FS_RANGE[2:0]: ADC audio frequency range:
00: normal (f_s = 32 to 48 kHz) (default)
01: low (f_s = 16 to 24 kHz)
1X: very low (f_s = 8 to 12 kHz)

1 P2P_IN_ADC: FFX input:
0: FFX input is from serial-to-parallel audio interface (default)
1: FFX input is from ADC

0 CORE_CLKENBL: availability of system clock:
0: FFX system clock disabled 1: FFX system clock enabled (default)

FFXST FFX status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					INVALID_ INP_ FBK	MUTE_INT_FBK	

Address: 0x23

Type: RO

Buffer: No

Reset: Undefined

Description:

7:3 Reserved

2 INVALID_INP_FBK: invalid input status:
1: invalid input sent to FFX

1 MUTE_INT_FBK: FFX mute status
1: FFX is in mute state

0 Reserved

PWMINT1 PWM driver configuration register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM_INT1[7:0]							

Address: 0x2D

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 PWM_INT1[7:0]: see *Section 8.5: SAI pass-through on page 29*

PWMINT2 PWM driver configuration register 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM_INT2[7:0]							

Address: 0x2E

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 PWM_INT2[7:0]: see *Section 8.5: SAI pass-through on page 29*

POWST Power bridge status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POW_ POWERDOWN	POW_ TRISTATE	POW_FAULT1A	POW_FAULT1B	POW_FAULT2A	POW_FAULT2B		

Address: 0x32

Type: RO

Buffer: No

Reset: Undefined

Description:

7 POW_POWERDOWN: power-down bridge:
0: not in power-down state 1: power-down state

6 POW_TRISTATE:
1: power bridge is in tri-state

5 POW_FAULT1A:
1: power bridge 1A is in fault state

4 POW_FAULT1B:
1: power bridge 1B is in fault state

3 POW_FAULT2A:
1: power bridge 2A is in fault state

2 POW_FAULT2B:
1: power bridge 2B is in fault state

1:0 Reserved

11 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These package have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 17 gives the package dimensions for the parameters shown in *Figure 20: VFQFPN52 outline* below.

Figure 20. VFQFPN52 outline

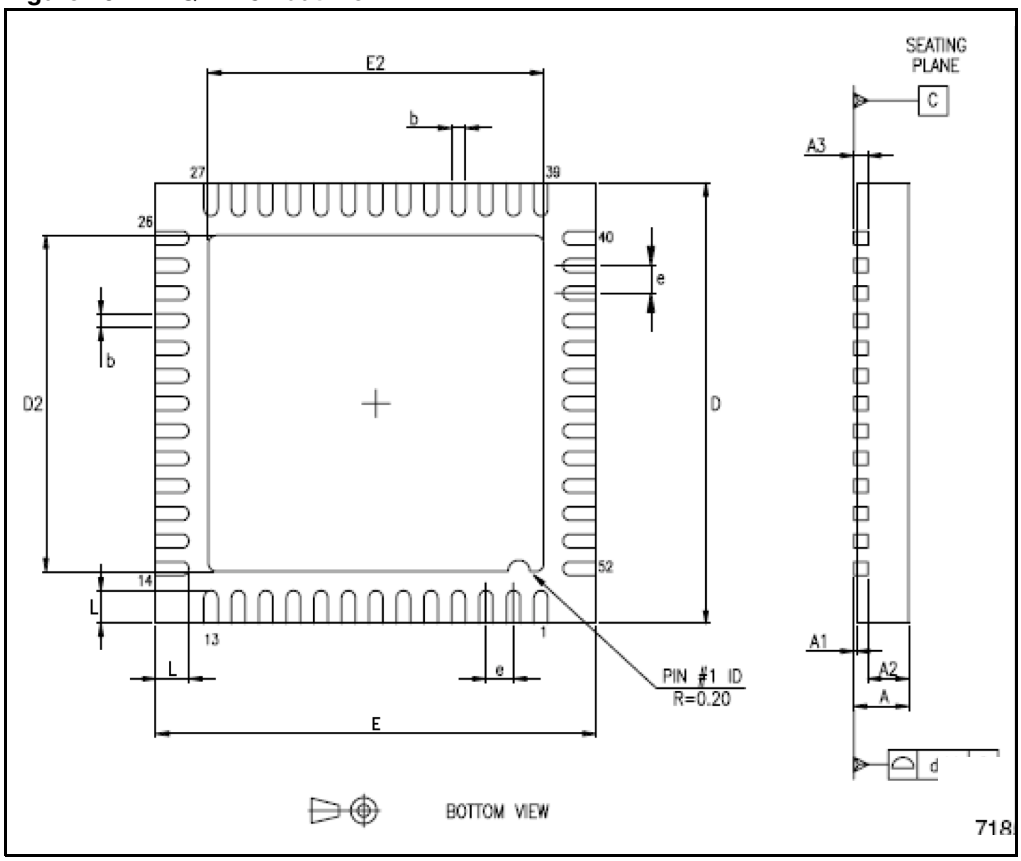


Table 17. VFQFPN52 dimensions

Reference	Dimensions in mm			Dimensions in inches		
	Min	Typical	Max	Min	Typical	Max
A	0.800	0.900	1.000	0.031	0.035	0.039
A1		0.020	0.050		0.001	0.002
A2		0.650	1.000		0.026	0.039
A3		0.250			0.010	
b	0.180	0.230	0.300	0.007	0.009	0.012
D	7.875	8.000	8.125	0.310	0.315	0.320
D2	2.750	5.700	6.250	0.108	0.224	0.246
E	7.875	8.000	8.125	0.310	0.315	0.320
E2	2.750	5.700	6.250	0.108	0.224	0.246
e	0.450	0.500	0.550	0.018	0.020	0.022
L	0.350	0.550	0.750	0.014	0.022	0.030
ddd			0.080			0.003

12 Trademarks and other acknowledgements

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13 Revision history

Table 18. Document revision history

Date	Revision	Changes
12-Dec-2007	1	Initial release

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