Freescale Semiconductor
Technical Data

MC13770/D
Rev. 2, 11/2003

MC13770

(Scale 2:1)
Package Information
Plastic Package
Case 1345
(QFN-12)

Ordering Information

Device	Device Marking	Package
MC13770FC	770	QFN-12

MC13770

Single Band LNA and Mixer FEIC

1 Introduction

The MC13770 is a single band front-end IC designed for wireless receiver applications. It contains a low noise LNA and a high linearity mixer. The LNA is integrated with a bypass switch to preserve input intercept performance. The device is fabricated using Freescale's Advanced RF BiCMOS process using the SiGe:C option and is packaged in a 12 pin Quad Flat Non-leaded package.

1.1 Features

- RF Input Frequency: 2100 to 2400 MHz
- LNA Gain = 15 dB (Typ)
- LNA Input 3rd Order Intercept Point (IIP3) = 0 dBm (Typ)
- LNA Noise Figure (NF) = 1.5 dB (Typ)
- Bypass Mode Included for Improved Intercept Point Performance
- Double Balanced Mixer
- Mixer Conversion Gain = 10 dB (Typ)
- Mixer Noise Figure (NF) = 8.0 dB (Typ)

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- Mixer Input 3rd Order Intercept Point (IIP3) = -3.0 dBm (Typ)
- Total Supply Current = 8.0 mA
  LNA = 3.0 mA
  Mixer = 5.0 mA

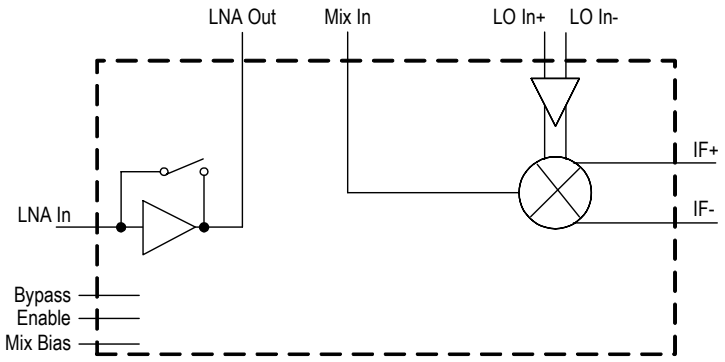

Figure 1. Simplified Block Diagram

2 Electrical Specifications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	3.6	V
Storage Temperature Range	T_{stg}	-65 to 150	°C
Operating Temperature Range	T_A	-40 to 85	°C

Note: Maximum Ratings and ESD

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤100 V and Machine Model (MM) ≤30 V. Additional ESD data available upon request.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage		2.7	2.75	3.0	Vdc
Logic Voltage (Enable and Bypass Pins)					V
Input High Voltage		0.85 V_{CC}	-	V_{CC}	
Input Low Voltage		0	-	0.15 V_{CC}	

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Table 3. Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Turn-on Time		-	100	-	ns
LNA High Gain Mode (Frequency = 2140 MHz, V_{CC} = 2.75 V, Bypass = 2.75 V, Enable = 2.75 V)					
LNA Gain		-	15	-	dB
LNA Noise Figure		-	1.5	-	dB
LNA Input IP3		-	0	-	dBm
LNA Supply Current	I_{DD}	-	3.0	-	mA
LNA Low Gain Mode (RF = 2140 MHz, V_{CC} = 2.75 V, Bypass = 0 V, Enable = 2.75 V)					
LNA Gain		-	-5.0	-	dB
LNA Noise Figure		-	5.0	-	dB
LNA Input IP3		-	20	-	dBm
LNA Supply Current	I_{DD}	-	10	-	μA
Mixer Mode (RF = 2140 MHz, LO = 2520 MHz, V_{CC} = 2.75 Vdc, Enable = 2.75 V)					
Conversion Gain		-	10	-	dB
SSB Noise Figure		-	8.0	-	dB
Input IP3		-	-3.0	-	dBm
Supply Current		-	5.0	-	mA
LO Drive Level		-	-10	-	dBm

Note: Tone spacing for IIP3 measurement is 5.0 MHz.

Table 4. Truth Table
(1 = 2.75 V, 0 = 0 V)

Enable	Bypass	Mode
0	0	Sleep
0	1	Undefined - do not use
1	0	Low Gain
1	1	High Gain

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3 Contact Description

Table 5. Contact Function Description

Pin	Symbol	Description
1	LNA Out	LNA Output
2	Bypass	LNA Bypass Control
3	Mix In	Mixer Input
4	Enable	Chip Enable
5	LO+	Local Oscillator Input +
6	LO-	Local Oscillator Input -
7	IF+	Differential IF Output +
8	IF-	Differential IF Output -
9	V_{CC}	Supply
10	LNA In	LNA Input
11	Gnd	Ground
12	Mix Bias	Mixer Bias Adjustment

4 Applications Information

Figure 2 shows the typical application circuit for 2110 to 2140 MHz band. The Mixer input is internally broadband matched. Two typical IF output match circuits are provided in Table 6 on page 5.

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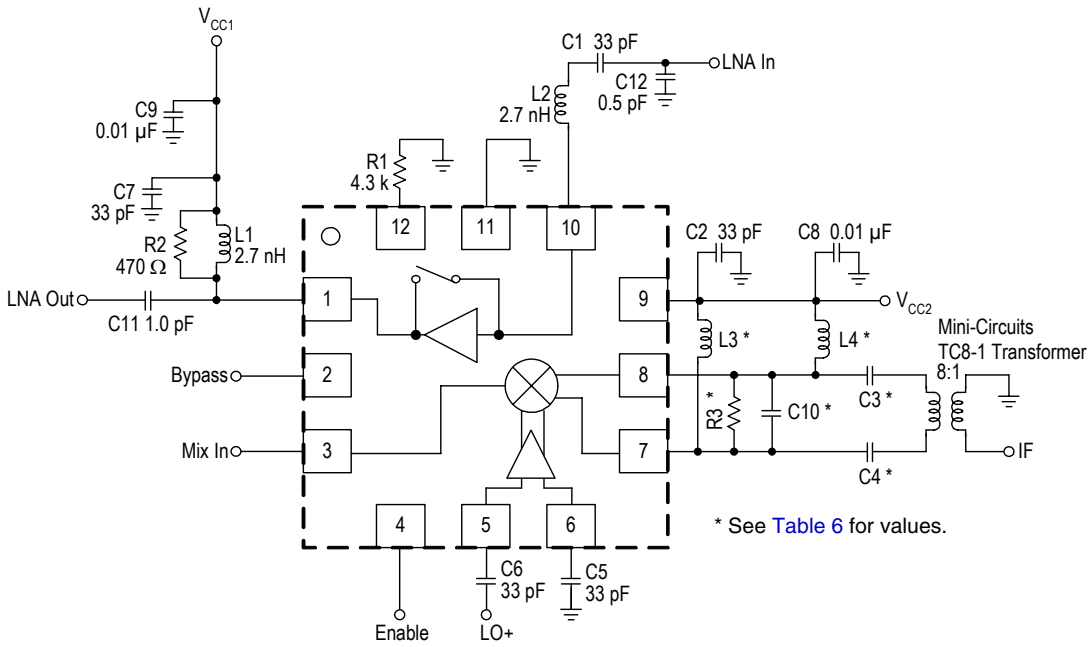

Figure 2. Application Schematic

Table 6. Bill of Material for Application Schematic

Component	190 MHz IF	380 MHz IF
C3	1.2 pF	2.2 pF
C4	1.2 pF	2.2 pF
C10	1.2 pF	1.2 pF
L3	150 nH	39 nH
L4	150 nH	39 nH
R3	5.0 kΩ	20 kΩ

Note: All other components are the same for both configurations.

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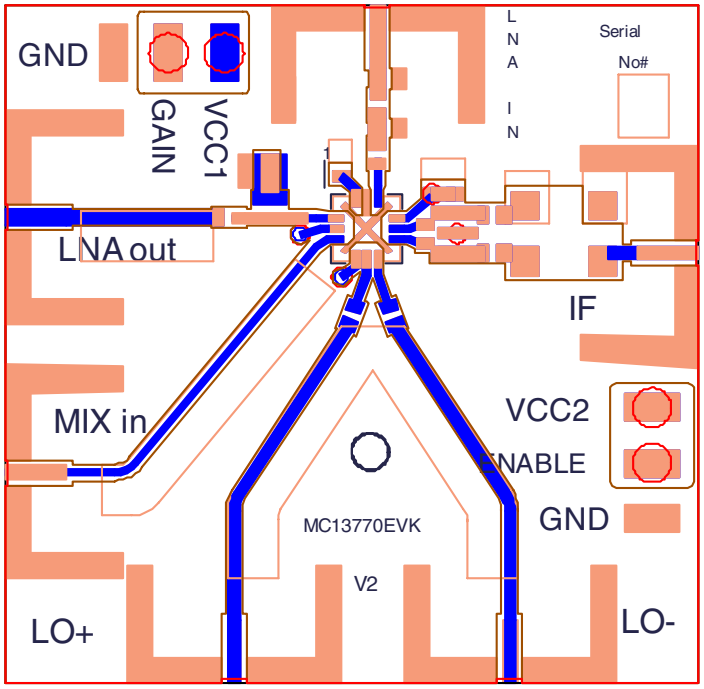

Figure 3. Application PCB (Not to Scale)

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5 Packaging Information

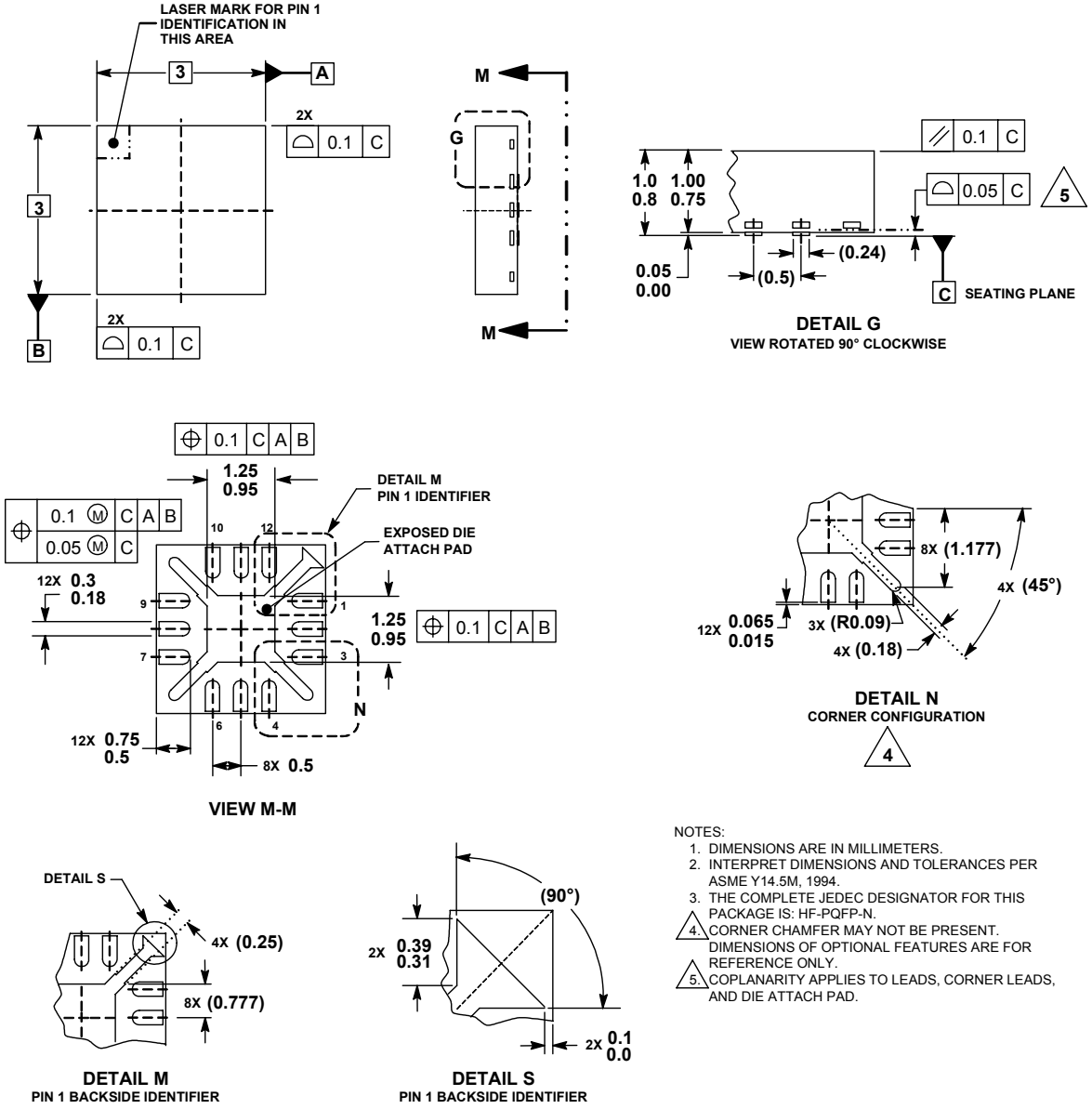

Figure 4. Outline Dimensions for QFN-12
(Case 1345-01, Issue A)

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