PTN3460

DisplayPort to LVDS bridge IC

Rev. 2 — 2 June 2011 **Product brief**

1. General description

PTN3460 is an (embedded) DisplayPort to LVDS bridge that enables connectivity between an (embedded) DisplayPort (eDP) source and LVDS display panel. It processes the incoming DisplayPort (DP) stream, performs DP to LVDS protocol conversion and transmits processed stream in LVDS format.

PTN3460 provides significant flexibility to optimally fit under different platform environments with programmability of its internal functions. PTN3460 is powered by 3.3 V and/or 1.8 V supplies and is available in the HVQFN56 7 mm × 7 mm package with 0.4 mm pitch.

2. Features and benefits

- Supports DP Main Link operation with 1 or 2 lanes
- Supports DP Main Link rate—Reduced Bit Rate (1.62 Gbit/s) and High Bit Rate (2.7 Gbit/s)
- Supports downspreading on DP Link to reduce EMI
- Supports Full Link training and Fast Link training
- Supports eDP authentication options—ASSR, alternate framing
- Supports LVDS single and dual bus operation
- Supports LVDS color depths—18 bpp, 24 bpp
- Supports LVDS pixel clock up to 112 MHz
- Supports 1920 × 1200 at 60 Hz resolution in LVDS Dual-bus mode
- Supports center spreading of LVDS clock to reduce EMI
- Supports panel power up/down control
- Supports device configurability via pins, DP AUX, I^{2}C
- eDP complying PWM generator
- Supports EDID ROM emulation
- No external timing reference
- Supports power management modes in tune with platform needs
- Power supply: (3.3 V ± 10 %) or (3.3 V ± 10 % and 1.8 V ± 5 %)
- ESD: 6 kV HBM
- Commercial operating temperature range: 0 °C to 70 °C
- HVQFN56 package 7 mm × 7 mm, 0.4 mm pitch; exposed center pad for thermal relief and electrical ground

3. Applications

- AIO platforms
- Netbook platforms
- Netbooks/nettops

Table 1. **Ordering information**

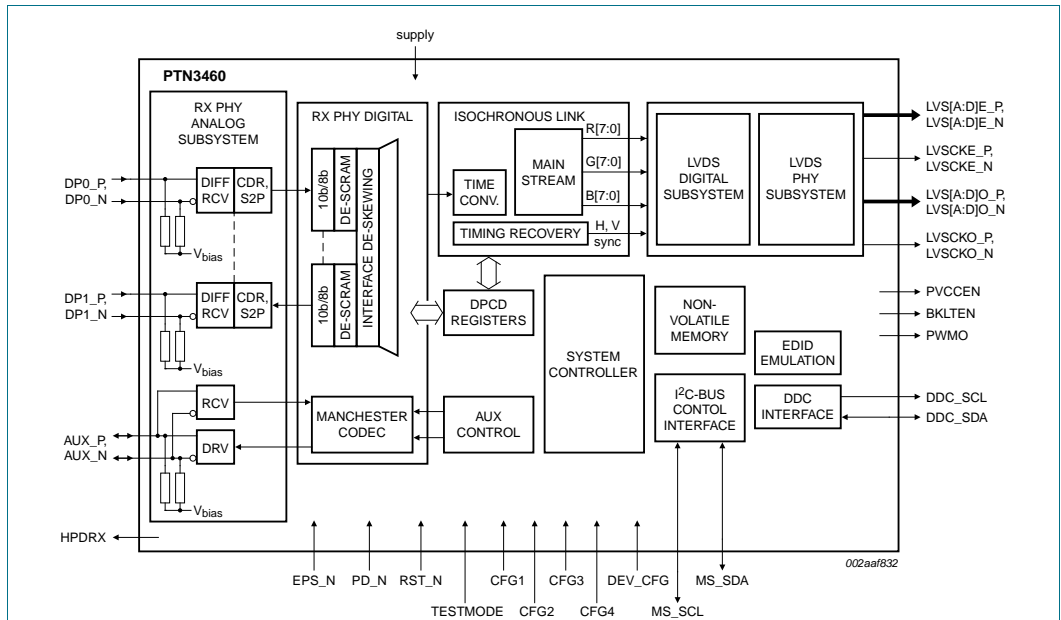| Type number	Package			Version
	Name	**Description**		
PTN3460BS	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body $7 \times 7 \times 0.85$ mm[1], 0.4 mm pitch		SOT949-2

[1] Maximum package height is 1 mm.

Fig 1. **Block diagram of PTN3460**

Fig 2. **Pin configuration for HVQFN56**

PTN3460

Product brief

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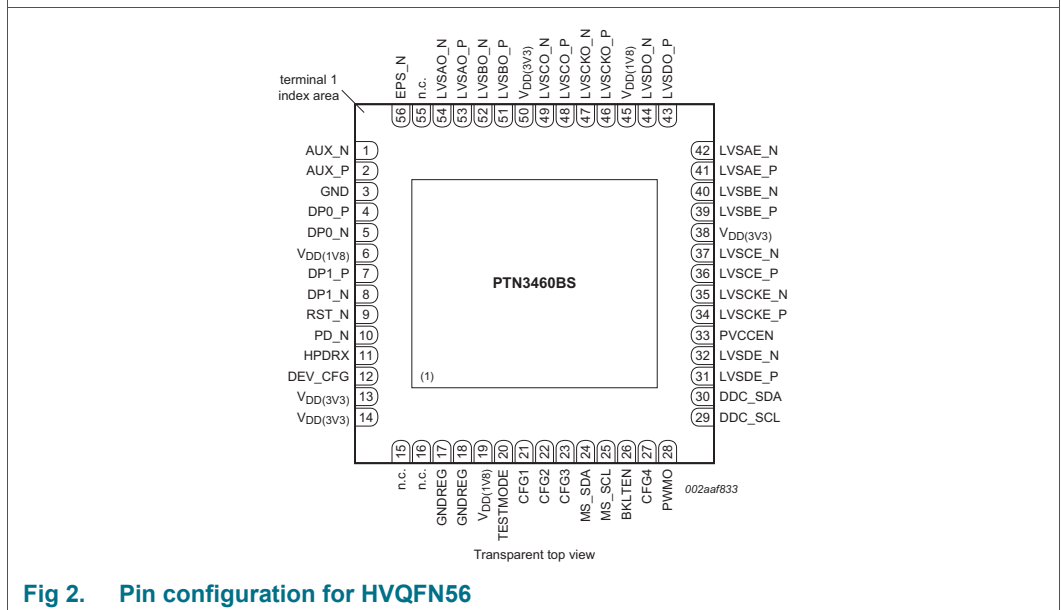
2 of 3

HVQFN56 : plastic thermal enhanced very thin quad flat package; no leads;
56 therminals; body 7 x 7 x 0.85 mm

SOT949-2

terminal 1
index area
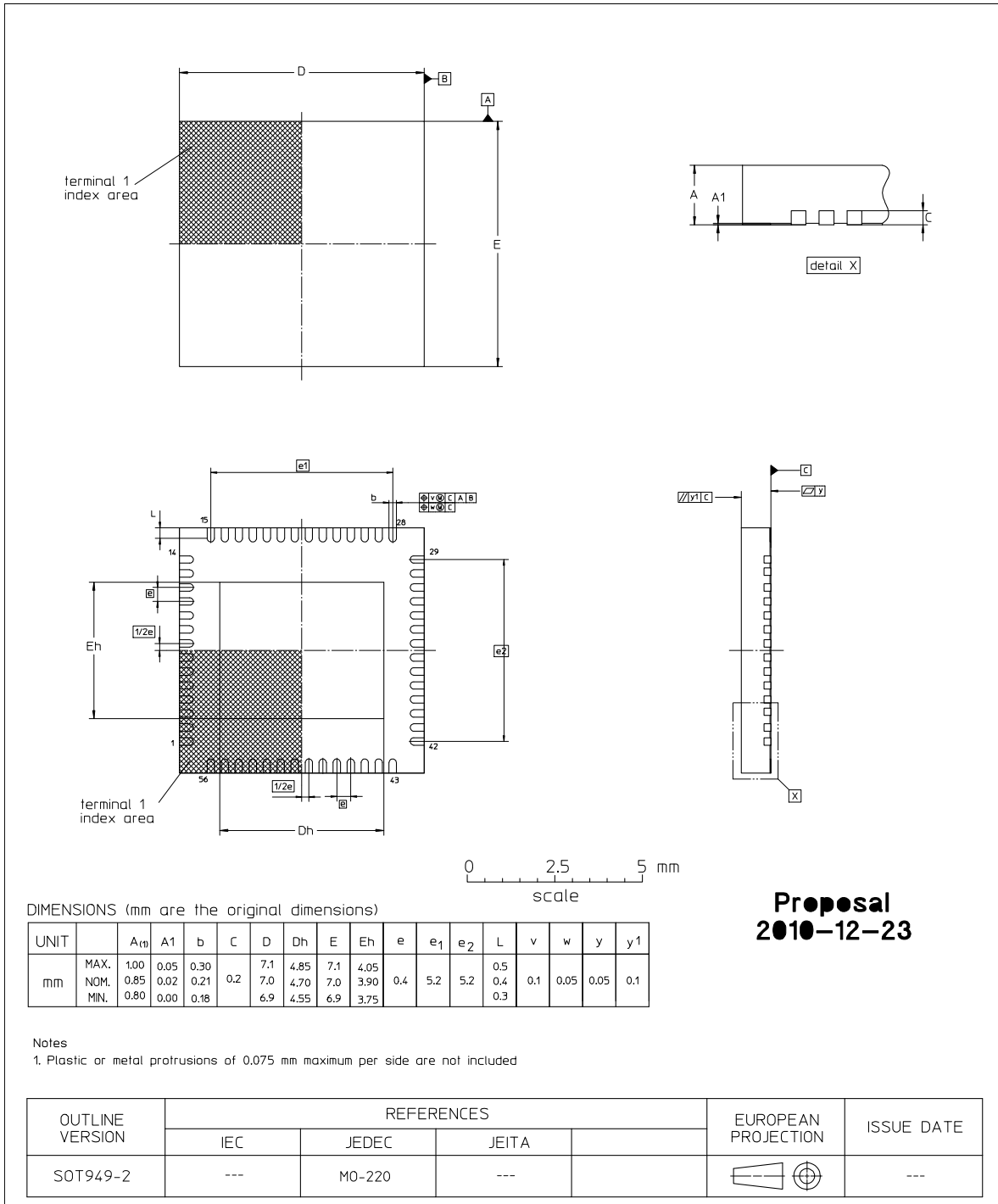
detail X

terminal 1
index area

Proposal
2010-12-23

0   2.5   5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT		A (1)	A1	b	C	D	Dh	E	Eh	e	e1	e2	L	v	w	y	y1
mm	MAX.	1.00	0.05	0.30	0.2	7.1	4.85	7.1	4.05	0.4	5.2	5.2	0.5	0.1	0.05	0.05	0.1
	NOM.	0.85	0.02	0.21		7.0	4.70	7.0	3.90				0.4				
	MIN.	0.80	0.00	0.18		6.9	4.55	6.9	3.75				0.3				

Notes
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT949-2	---	MO-220	---			---

Fig 3.   Package outline SOT949-2 (HVQFN56)

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