19-1624; Rev 2; 2/03

EVALUATION KIT AVAILABLE

MAXIM

2.5GHz, +20dBm Power Amplifier IC in UCSP Package

MAX2240

General Description

The MAX2240 single-supply, low-voltage power amplifier (PA) IC is designed specifically for applications in the 2.4GHz to 2.5GHz frequency band. The PA is compliant with Bluetooth, HomeRF, and 802.11 standards, as well as other FSK modulation systems. The PA provides a nominal +20dBm (100mW) output power in the highest power mode.

The PA includes a digital power control circuit to greatly simplify control of the output power. Four digitally controlled output power levels are provided: from +3dBm to +20dBm. A digital input controls the active or shutdown operating modes of the PA. In the shutdown mode, the current reduces to 0.5µA.

The IC integrates the RF input and interstage matching to simplify application of the IC. Temperature and supply-independent biasing are also included to provide stable performance under all operating conditions.

The IC operates from a +2.7V to +5V single-supply voltage. No negative bias voltage is required. Current consumption is a modest 105mA at the highest power level.

The part is packaged in the UCSP™ package significantly reducing the required PC board area. The chip occupies only a 1.56mm x 1.56mm area. The 3 x 3 array of solder bumps are spaced with a 0.5mm bump pitch.

Applications

Bluetooth

HomeRF

802.11 FHSS WLAN

2.4GHz ISM Proprietary Radios

Features

- ♦ 2.4GHz to 2.5GHz Frequency Range
- ♦ High +20dBm Output Power
- ♦ 2-Bit Digital Power Control: Four Output Levels
- ♦ Integrated Input Match to 50Ω
- ♦ Low 105mA Operating Current
- ♦ 0.5µA Low-Power Shutdown Mode Current
- ♦ +2.7V to +5V Single-Supply Operation
- ♦ Miniature Chip-Scale Package (1.56mm x 1.56mm)

Ordering Information

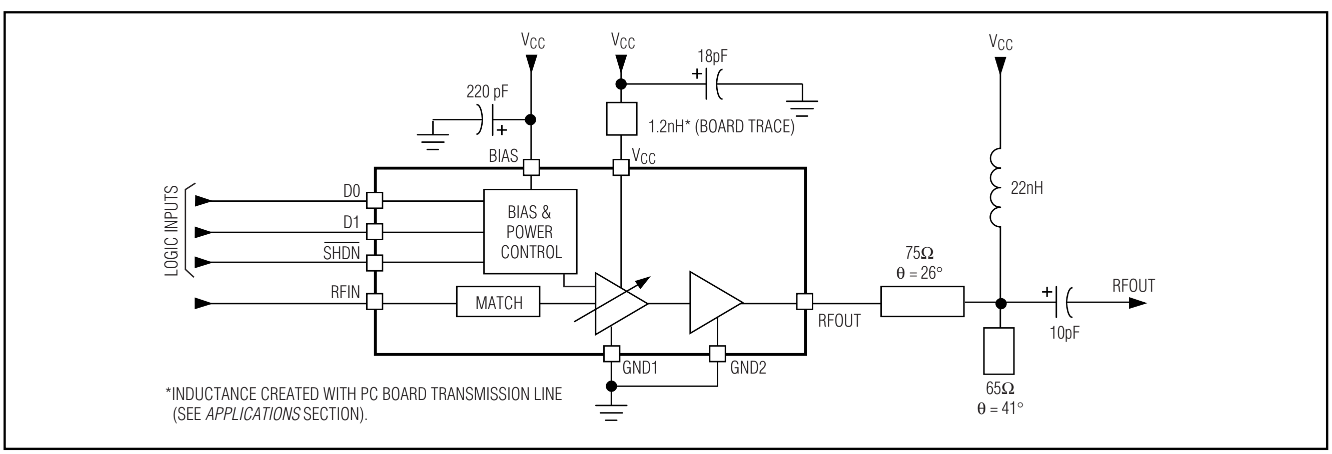
PART	TEMP RANGE	PIN-PACKAGE
MAX2240EBL	-40°C to +85°C	9 UCSP*

**UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. Refer to the UCSP Reliability Notice in the UCSP Reliability section of this data sheet for more information.*

Pin Configuration appears at end of data sheet.

UCSP is a trademark of Maxim Integrated Products, Inc.

Typical Application Circuit/Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

BIAS, V_{CC}, RFOUT to GND ....-0.3V to +6V
Input Voltages
(SHDN, D0, D1, to GND).......................-0.3V to (V_{BIAS} + 0.3V)
(RFIN to GND) ....-0.7V to +0.7V
Input Current (SHDN, D0, D1) ....±10mA
Continuous Operating Lifetime..........10 years x $0.935^{(T_A - 77°C)}$
(for operating temperature +77°C < T_A < +86°C)

RF Input Power (RFIN)...+10dBm
Continuous Power Dissipation (T_A = +85°C)
9-Pin UCSP...810mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(Using *Typical Application Circuit*, V_{CC} = +2.7V to +5V, P_{RFIN} = 0dBm to +4dBm, f_{RFIN} = 2.4GHz to 2.5GHz, $\overline{SHDN}$ = V_{CC}, T_A = -40°C to +85°C. Typical values measured at V_{CC} = +3.2V, P_{RFIN} = +3dBm, f_{RFIN} = 2.45GHz, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Note 2)	V_{D1} ≤ 0.8V, V_{D0} ≤ 0.8V, T_A = +25°C, P_{RFIN} = +3dBm, V_{CC} = 3.2V, f_{RFIN} = 2.45GHz (Note 3)		65	80	mA
	V_{D1} ≤ 0.8V, V_{D0} ≤ 0.8V			110	
	V_{D1} ≤ 0.8V, V_{D0} ≥ 2.0V, T_A = +25°C, P_{RFIN} = +3dBm, V_{CC} = 3.2V, f_{RFIN} = 2.45GHz (Note 3)		68	85	
	V_{D1} ≤ 0.8V, V_{D0} ≥ 2.0V			111	
	V_{D1} ≥ 2.0V, V_{D0} ≤ 0.8V, T_A = +25°C, P_{RFIN} = +3dBm, V_{CC} = 3.2V, f_{RFIN} = 2.45GHz (Note 3)		75	90	
	V_{D1} ≥ 2.0V, V_{D0} ≤ 0.8V			115	
	V_{D1} ≥ 2.0V, V_{D0} ≥ 2.0V, T_A = +25°C, P_{RFIN} = +3dBm, V_{CC} = 3.2V, f_{RFIN} = 2.45GHz (Note 3)		105	125	
	V_{D1} ≥ 2.0V, V_{D0} ≥ 2.0V			155	
Shutdown Supply Current	SHDN ≤ 0.8V, V_{D0} ≤ 0.8V, V_{D1} ≤ 0.8V, no input signal		0.5	10.0	µA
DIGITAL CONTROL INPUT (D0, D1, AND SHDN)					
Input Logic Voltage High		2			V
Input Logic Voltage Low				0.8	V
Input Current	GND ≤ V_{IN} ≤ V_{BIAS}	1		1	µA

AC ELECTRICAL CHARACTERISTICS

(MAX2240 EV kit, V_{CC} = +2.7V to +5V, P_{RFIN} = 0dBm to +4dBm, f_{RFIN} = 2.4GHz to 2.5GHz, $\overline{SHDN}$ = V_{CC}, T_A = +25°C. Typical values measured at V_{CC} = +3.2V, P_{RFIN} = +3dBm, f_{RFIN} = 2.45GHz, unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range		2400		2500	MHz
Input Power Range		0		4	dBm
Output Power	V_{D1} ≤ 0.8V, V_{D0} ≤ 0.8V		3		dBm
	V_{D1} ≤ 0.8V, V_{D0} ≥ 2V		8		
	V_{D1} ≥ 2V, V_{D0} ≤ 0.8V		12		
	V_{CC} = 3.2V, P_{RFIN} = 3dBm, f_{RFIN} = 2.45GHz, V_{D1} ≥ 2V, V_{D0} ≥ 2V, T_A = +25°C (Note 9)	17.3	19		
	V_{D1} ≥ 2V, V_{D0} ≥ 2V, T_A = -40°C to +85°C (Note 1)	15.3	19	24	
Power Control Steps (Notes 4, 9)	V_{CC} = 5.0V	2	6	8	dB
	V_{CC} = 2.7V to 5.0V	2		8.6	
Harmonic Output (Notes 3, 9)			-15	-5	dBm
Input VSWR (Note 9)	R_S = 50Ω, over full P_{in} range		1.5:1	2:1	dBm
In-Band Spurious Noise (Notes 5, 9)	Frequency offset = ±550kHz		-21	-20	dBc
	Frequency offset = ±1.5MHz		-20		dBm
	Frequency offset = ±2.5MHz		-40		
Power Ramp Turn-On Time (Notes 6, 9)	$\overline{SHDN}$ = 0 to 1, D0 = D1 = logic low-to-high transition			2	µs
Power Ramp Turn-Off Time (Notes 7, 9)	$\overline{SHDN}$ = 1 to 0, D0 = D1 = logic high-to-low transition			2	µs
Nonharmonic Spurious Output (Note 9)	All power levels set by D0, D1; load VSWR ≤ 3:1			-30	dBm
Input to Output Isolation in Shutdown			45		dB
Maximum Output VSWR Without Damage (Note 8)	All power levels set by D0, D1; any load phase angle, any duration		6:1		

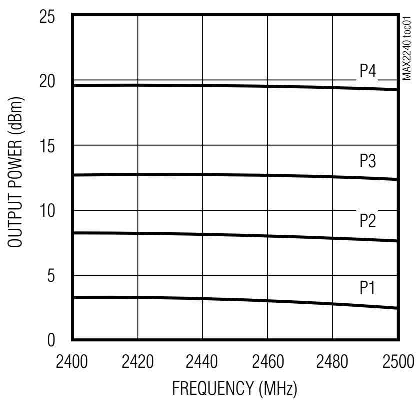
Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the entire operating temperature range are guaranteed by design and characterization but are not production tested.
Note 2: Supply current is measured with RF power applied to the input.
Note 3: Measured with an output-matching network to minimize the 2nd and 3rd harmonics (see *Applications* section).
Note 4: Power steps between adjacent power levels. All other operating conditions remain constant during power step change.
Note 5: Output measured in 100kHz RBW. Test signal modulation shall comply with GFSK, BT = 0.5, 1-bit/symbol, 1Mbps, frequency deviation = 175kHz.
Note 6: The total turn-on time for the PA output power to settle within 1dB of the final value.
Note 7: The total turn-off time for the PA output power to drop to -10dBm.
Note 8: After removal of the load mismatch, the PA returns to operation under normal conditions.
Note 9: Guaranteed by design and characterization.

2.5GHz, +20dBm Power Amplifier IC in UCSP Package

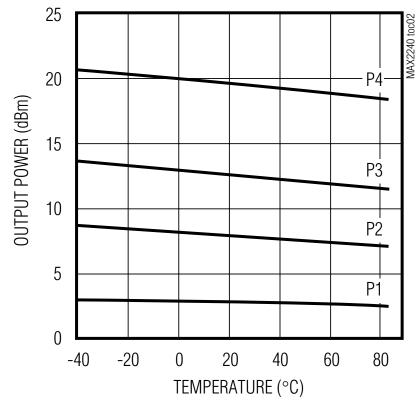
Typical Operating Characteristics

(MAX2240 EV kit, V_{CC} = +3.2V, P_{RFIN} = +3dBm, f_{RFIN} = 2.45GHz, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted. See Table 1 for power level settings P1, P2, P3, P4.)

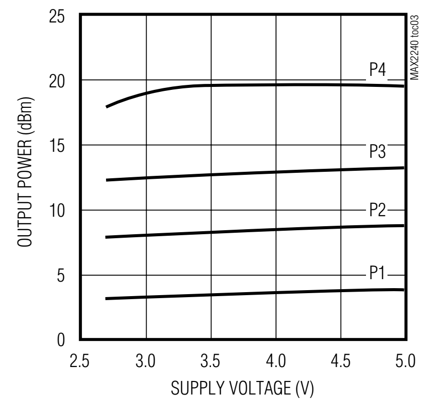
OUTPUT POWER vs. FREQUENCY



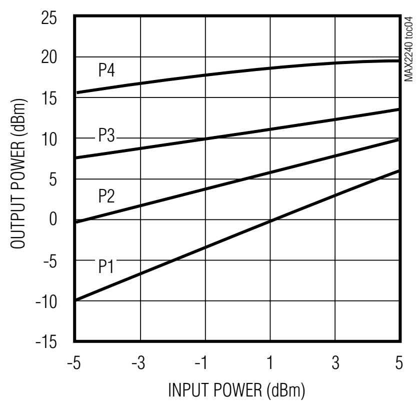
OUTPUT POWER vs. TEMPERATURE



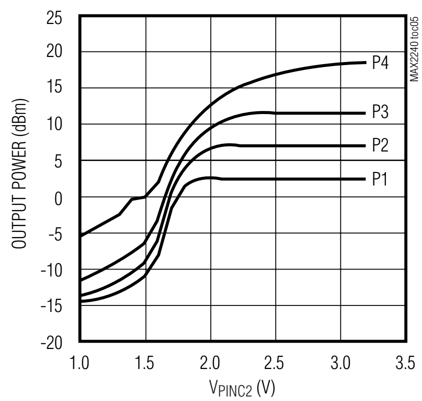
OUTPUT POWER vs. SUPPLY VOLTAGE



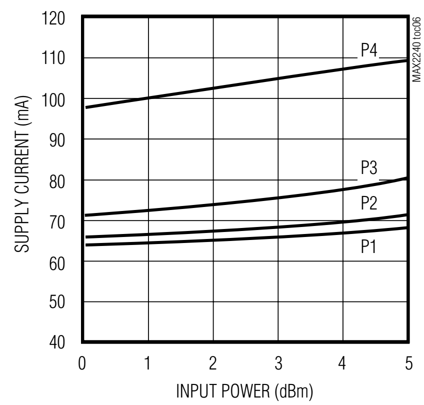
OUTPUT POWER vs. INPUT POWER



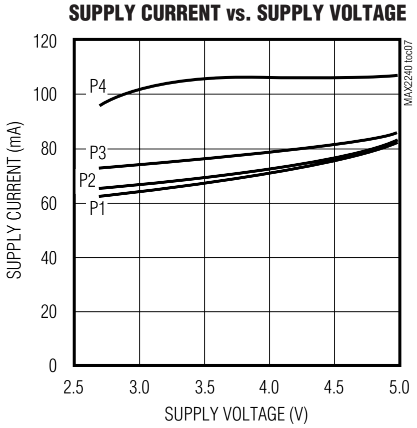
OUTPUT POWER vs. PINC2 VOLTAGE



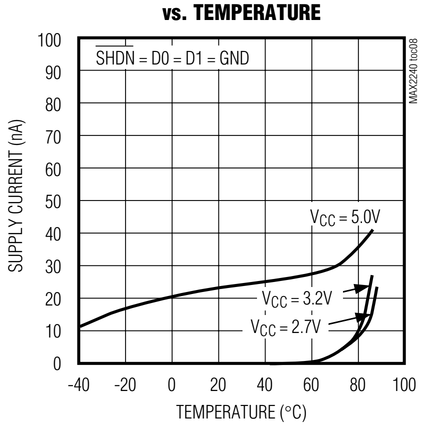
SUPPLY CURRENT vs. INPUT POWER



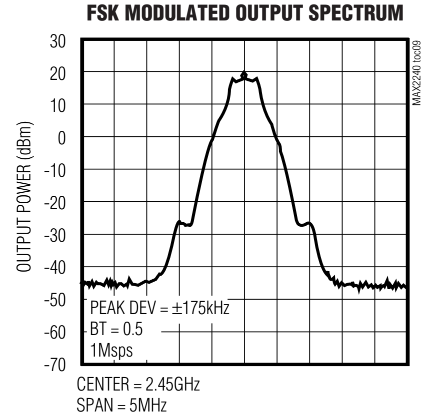
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



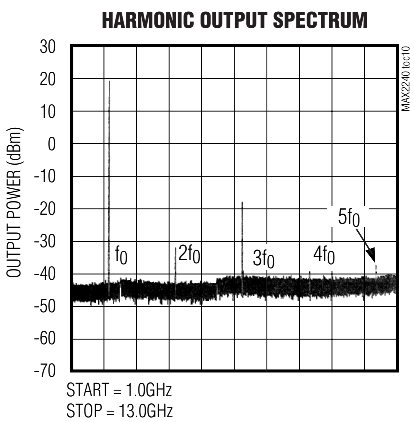
FSK MODULATED OUTPUT SPECTRUM

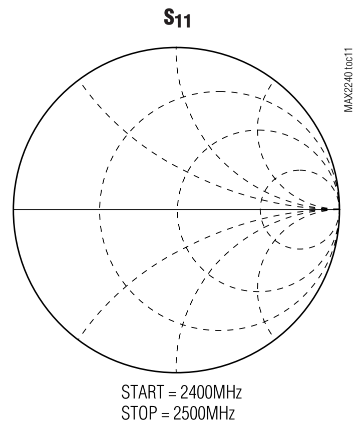


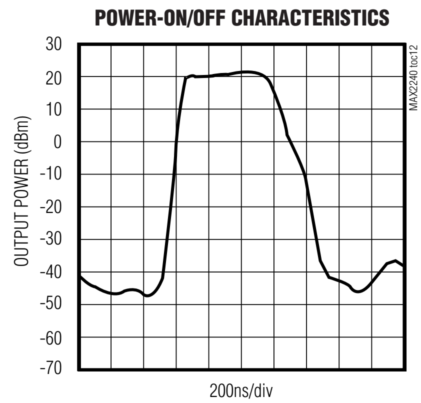
2.5GHz, +20dBm Power Amplifier IC in UCSP Package

Typical Operating Characteristics (continued)

(MAX2240 EV kit, V_{CC} = +3.2V, P_{RFIN} = +3dBm, f_{RFIN} = 2.45GHz, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted. See Table 1 for power level settings P1, P2, P3, P4.)







Pin Description

PIN	NAME	FUNCTION
C3	RFIN	Power Amplifier RF Input. Internally DC blocked and matched to 50Ω.
C2	V_{CC}	DC Voltage Supply for 1st Stage. A 1.2nH series inductance required for optimum output power and efficiency, followed by an external RF bypass capacitor to ground.
C1	GND2	Ground Connection to the Amplifier 2nd Stage. Requires a low-inductance/low thermal resistance path to the ground plane with multiple vias.
B3	GND1	Ground Connection for Bias and 1st Stage. Requires a low-inductance/low thermal resistance path to the ground plane with multiple vias.
B2	$\overline{SHDN}$	Power Amplifier Shutdown Control Input. Drive $\overline{SHDN}$ low to enable low-power shutdown mode. Drive $\overline{SHDN}$ high for normal operation.
B1	RFOUT	Power Amplifier RF Output. Open-collector output requires external pull-up inductor to V_{CC}. Requires an external matching network for optimum output power and efficiency.
A3	BIAS	DC Voltage Supply for Bias and Control Circuitry. An external RF bypass capacitor to ground is required. Place capacitor as close to the pin as possible.
A2	D1	Digital Power Control Input (MSB) (Table 1)
A1	D0	Digital Power Control Input (LSB) (Table 1)

Detailed Description

The MAX2240 PA is guaranteed to operate over a 2.4GHz to 2.5GHz frequency range with a +2.7V to +5V single supply. The PA provides a nominal +20dBm output power in the highest power mode setting (D0 = D1 = 1). The signal path consists of two amplifier stages: an input amplifier stage and a PA stage. A matching circuit is provided between the two stages to match the amplifiers' impedance. The PA also contains bias circuits that interface to external logic commands (D0, D1, and $\overline{SHDN}$) to control output power and power-up/down of the amplifier.

The input amplifier is an AC-coupled variable gain amplifier (VGA) with its input port internally matched to 50Ω. The amplifier is AC-coupled; hence, a DC blocking capacitor is not required at the RFIN port. The VGA gain is varied by changing the bias current through a current driver circuit. The current driver circuit provides

2.5GHz, +20dBm Power Amplifier IC in UCSP Package

Table 1. Control Inputs

DIGITAL CONTROL INPUTS			OUTPUT POWER AND SUPPLY CURRENT			
$\overline{SHDN}$	D1	D0	POWER LEVEL	P_{IN} (dBm)	P_{OUT} (dBm)	I_{CC} (mA)
0	0	0	PA OFF-	3	-22	<1µA
1	0	0	P1	3	3	65
1	0	1	P2	3	8	68
1	1	0	P3	3	12	75
1	1	1	P4	3	19	105

four levels (magnitudes) of precisely controlled currents to the VGA, depending on power control digital inputs D0 and D1. Each current level presents a different power level to the final amplifier stage, therefore controlling the output power.

The digital power control circuit of the PA greatly simplifies control of the output power. The two digital bits D0 and D1 control the output power in four steps with approximately a 6dB/step. The PA is optimized to provide power control steps within a 2dB/step to 8.6dB/step over the full temperature range and V_{CC} and RF input power variations. Table 1 shows the D0 and D1 digital control states, the corresponding nominal output power, and the typical current consumption of the IC.

The bias circuit provides separate bias voltages and currents to the amplifier stages. An internal lowpass RC filter isolates the bias circuit from being corrupted by the RF signals. The bias circuit is optimized to minimize output power variations due to the variations in temperature, V_{CC}, and RF power input. The bias circuit design also ensures the stability of the PA when connected to high VSWR loads over all power levels. A digital low at the $\overline{SHDN}$ port turns the amplifier down with a current consumption of less than 1µA.

The MAX2240 integrates all the RF matching components on-chip, except for the output stage match. The internal input match enables the RF input with 50Ω impedance to be directly connected to the RFIN port through a 50Ω transmission line.

The MAX2240 PA requires an external match at the RFOUT port to optimize the amplifier for output power and efficiency. For an optimum match at 2.45GHz, the load impedance at the RFOUT port is approximately 15Ω + j18Ω (Figure 1). There are numerous ways of transforming 50Ω to the optimum impedance. The output matching in the typical operating circuit is implemented using a series transmission line of 75Ω and electrical length of 26°, and an open-ended shunt stub of 65Ω and 41° in length. The shunt stub also reduces the second harmonic at the output.

Applications Information

The MAX2240 power amplifier requires a relatively small number of external components. These components are small, low-cost surface-mount passive elements. The capacitors are all 0402 multilayer ceramic chip capacitors. These capacitors possess excellent high-frequency properties and are cost effective. The *Typical Application Circuit* is shown on page 1.

The inductor is a Q (>25) 0603 chip inductor. All transmission lines are simple microstrip structures printed on the PC board.

Power-Supply Considerations

The MAX2240 is designed to operate from a single, positive supply voltage (V_{CC}). Three pins are fed by the supply voltage: BIAS, V_{CC}, and RFOUT. Each supply voltage connection requires a separate RF bypass capacitor for proper operation. Use a 0.1µF bypass capacitor to filter the supply at the common V_{CC} node (see *Typical Application Circuit*).

BIAS requires a 220pF capacitor to ground. Locate one end of the capacitor as close as possible to BIAS and the other end of the capacitor near GND1 with several vias to the ground plane.

V_{CC} powers the amplifier 1st stage output. A 1.2nH inductor in series with V_{CC} and the V_{CC} bypass capacitor is needed for optimal output power and efficiency. An 18pF bypass capacitor to ground is required at the supply end of the 1.2nH inductor.

RFOUT is connected to the power supply through a choke inductor (through transmission line section T1). Select a choke with a self-resonant frequency at or slightly below 2.4GHz. A 220pF bypass capacitor is needed at the supply voltage end of the inductor.

RF Input

The internal input stage impedance matching network is integrated on the MAX2240, so it is possible to directly connect a 50Ω transmission line to RFIN. No external matching is required.

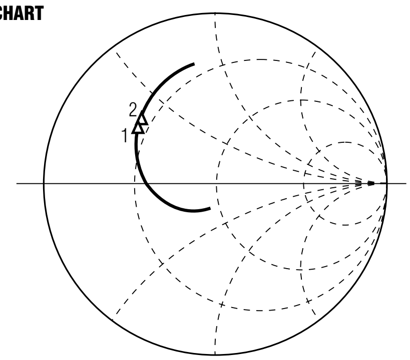
Output Stage (RF Output)

The output stage of the MAX2240 power amplifier is the collector of a transistor. The DC bias and impedance matching network are off-chip as shown in the *Typical Application Circuit*.

An off-chip external network, as with most PA ICs, is used to achieve higher efficiency and output power than is typically achieved using low-Q on-chip matching elements. Optimum output power and efficiency are achieved with a particular impedance on the output at the operating frequencies of interest and a short at the RF harmonic frequencies. This impedance is specified relative to a reference plane at the amplifier output into the matching network and load. This is the impedance that achieves the output power and current consumption listed in the electrical specifications. It is shown below in the chart and table of Figure 1.

MATCHING IMPEDANCE FOR RF_{OUT} PIN

SMITH CHART



1: (15.5Ω + J16.7Ω), 2.4GHz
2: (15.0Ω + 19.0Ω), 2.5GHz

MATCHING IMPEDANCE

FREQUENCY (GHz)	R	X	I Γ I	<Γ
2.4	15.5	16.7	0.57	140
2.45	15.2	17.9	0.58	138
2.5	15.0	19.0	0.59	136

Figure 1. Output Impedance

The primary power-matching structure is a lowpass network formed by the series transmission line section T1 and the open-stub transmission line section T2. The transmission line network acts like a series inductance and shunt capacitance. T1 and T2 are expressed as electrical lengths of a particular characteristic impedance line, but could be designed with different impedance lines.

Choose the length of T2 to provide a short at the 2nd harmonic frequency of the fundamental, and significantly attenuate its amplitude at the output—1/4 wave at the 2nd harmonic frequency of 4.9GHz. The 3rd harmonic is attenuated through the clever use of the parasitic capacitance in the choke. This capacitance rolls off the choke impedance at higher frequencies and appears as a low impedance at the 3rd harmonic frequency.

The output series capacitor is used as a DC-blocking capacitor and a final matching element. A value of 10pF is recommended.

As explained in the *Power-Supply Considerations* section, for proper DC biasing, the PA requires a connection to V_{CC} through an inductor, serving as a choke. Locate the inductor on the load side of transmission line T1. The recommended inductor value is 22nH. However, its value is not critical but must provide an impedance that is several hundred ohms. Choose an inductor with a self-resonant frequency at or slightly below 2.4GHz. The inductor Q is not critical; a moderate Q (>25) is sufficient. Remember to provide sufficient current-handling capability for the inductor, in this case at least 200mA. Also, a 220pF bypass capacitor is recommended at the supply voltage end of the inductor.

Layout

Design the layout for the PA IC to be as compact as possible to minimize the magnitude of parasitics. The chipscale IC package uses a bump pitch of 0.5mm (19.7 mil) and bump diameter of 0.3mm (~12 mil). Therefore, lay out the solder pad spacing on 0.5mm (19.7 mil) centers, use a pad size of 0.25mm (~10 mil) and a solder mask opening of 0.33mm (13 mil). Round or square pads are permissible. (Refer to the Maxim document, *Wafer Level Ultra-Chipscale Packaging* for additional detailed information on UCSP layout and handling.) Connect multiple vias from the ground plane as close to the ground pins as possible.

As already described, locate the capacitors as close as possible to the IC supply voltage pin or supply end of the series inductor. Place the ground end of these capacitors near the IC GND pins to provide a low-impedance return path for the signal current.

2.5GHz, +20dBm Power Amplifier IC in UCSP Package

$\overline{SHDN}$

$\overline{SHDN}$ is located in the center of the bump layout of the MAX2240. Therefore, the $\overline{SHDN}$ line requires the use of either a via to a buried line or a trace that fits inside a 10-mil gap between solder pads to bring out a connection from $\overline{SHDN}$.

D0, D1 Pins

Digital power control inputs D0 and D1 have CMOS-logic level inputs. As in any PC board circuit, the length of the logic signal traces determines the susceptibility to high-frequency noise that can interfere with normal switching. Therefore, in some cases, it can be necessary to provide some local lowpass filtering of the logic traces to suppress HF noise coupling to these inputs.

Output Match Layout

It is possible to lay out the output matching network transmission traces in a more compact manner if PC board area is limited. Series lines T1 and T2 can be constructed as folded lines, though it can be necessary to chamfer the corners for wide lines.

Prototype Chip Installation

Alignment keys on the PC board around the area where the chip is located are helpful in the prototype assembly process. The MAX2240 EV kit PC board has L-shaped alignment keys at the diagonal corners of the chip. It is better to align the chip on the board before any other components are placed, and then place the board on a hotplate or hot surface until the solder starts melting. Remove the board from the hotplate without disturbing the position of the chip, and let it cool down to room temperature before processing the board further.

UCSP Reliability

The UCSP represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. CSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a CSP package. Performance through Operating Life Test and Moisture Resistance remains uncompromised as it is primarily determined by the wafer-fabrication process.

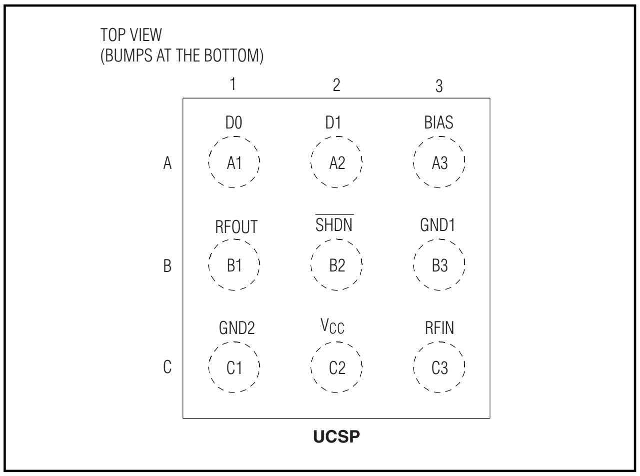
Mechanical stress performance is a greater consideration for a CSP package. CSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder joint contact integrity must be considered. Table 2 shows the testing done to characterize the CSP reliability performance. In conclusion, the UCSP is capable of performing reliably through environmental stresses as indicated by the results in the table. Additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's web- site at www.maxim-ic.com.

Users should also be aware that, as with any interconnect system, there are electromigration-based current limits that, in this case, apply to the maximum allowable current in the bumps. Reliability is a function of this current, the duty cycle, lifetime, and bump temperature. See the *Absolute Maximum Ratings* section for any specific limitations, listed under Continuous Operating Lifetime.

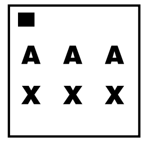
Table 2. Reliability Test Data

TEST	CONDITIONS	DURATION	NO. OF FAILURES PER SAMPLE SIZE
Temperature Cycle	-35°C to +85°C, -40°C to +100°C	150 cycles, 900 cycles	0/10, 0/200
Operating Life	T_A = +70°C	240hr	0/10
Moisture Resistance	+20°C to +60°C, 90% RH	240hr	0/10
Low-Temperature Storage	-20°C	240hr	0/10
Low-Temperature Operational	-10°C	24hr	0/10
Solderability	8hr steam age	—	0/15
ESD	±2000V, Human Body Model	—	0/5
High-Temperature Operating Life	T_J = +150°C	168hr	0/45

Pin Configuration



Marking Information



■: Pin 1 ID

AAA: Product ID code

XXX: Lot Code

Chip Information

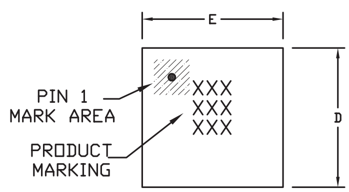
TRANSISTOR COUNT: 771

2.5GHz, +20dBm Power Amplifier IC in UCSP Package

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

9LUCSP, 3x3.EPS

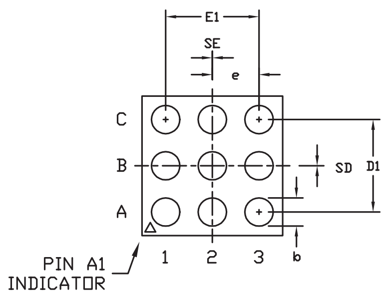


TOP VIEW

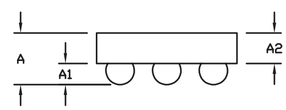
COMMON DIMENSIONS	
A	0.60±0.05
A1	0.27±0.03
A2	0.33 REF.
b	Ø0.37 BASIC
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 3x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0093	H	1/1

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