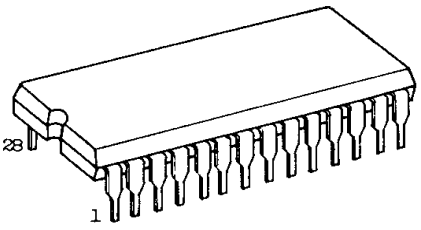
TC5032P

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5032P 6-DIGIT DECADE COUNTER

TC5032P is six digit decimal counter whose BCD output of each digit is dynamically output in sequence from the higher order digit on BCD OUTPUT in synchronism with SCAN input. As the carry outputs are available from all the digits, other counters and control circuits can be easily driven.
By using BC (Blanking Control) input, leading zero suppress from arbitrary digit can be achieved without external circuits.
Since the first stage counter can respond up to 10MHz (V_{DD}=5 volts), this is also suitable for counting and frequency dividing of high frequency pulses.

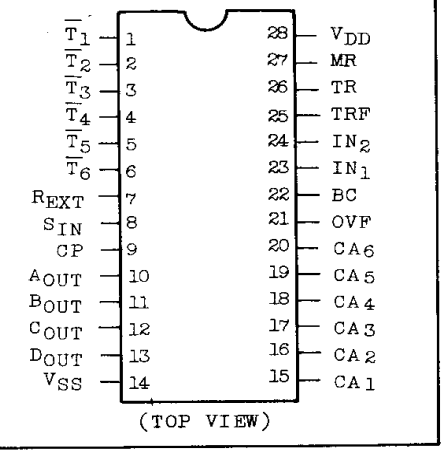


DIP 28 (6D28A-P)

ABSOLUTE MAXIMUM RATINGS

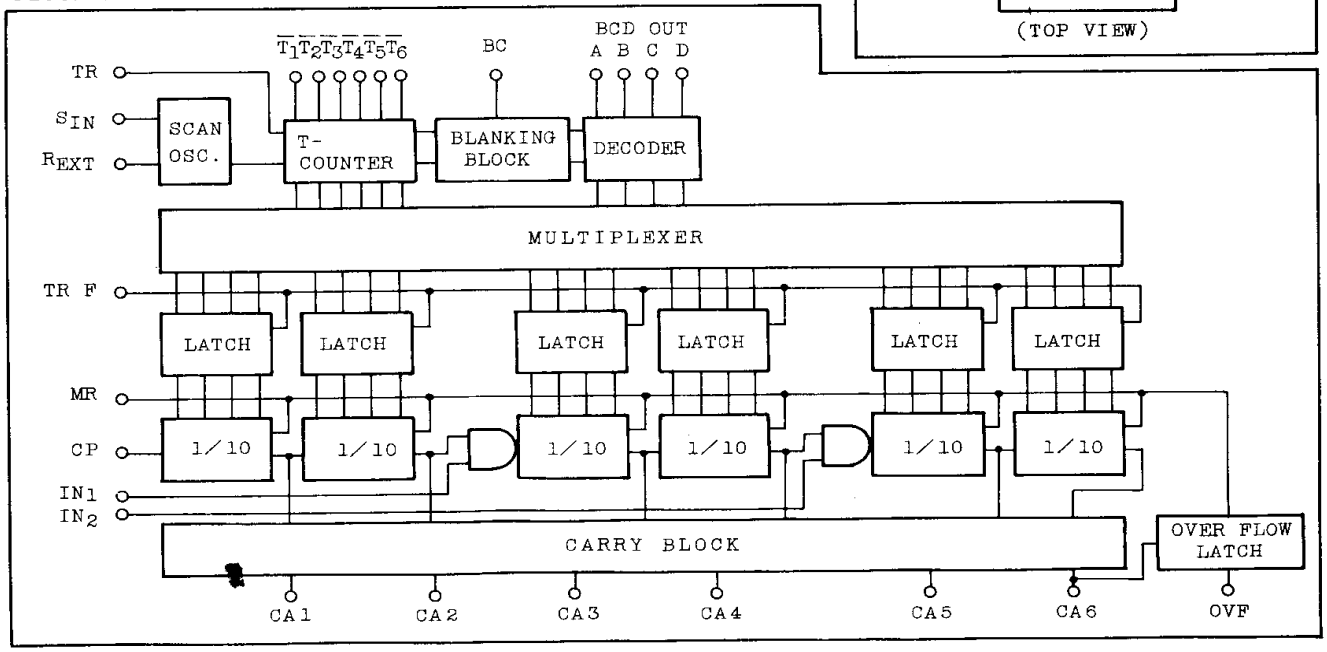
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-55 ~ 125	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



(TOP VIEW)

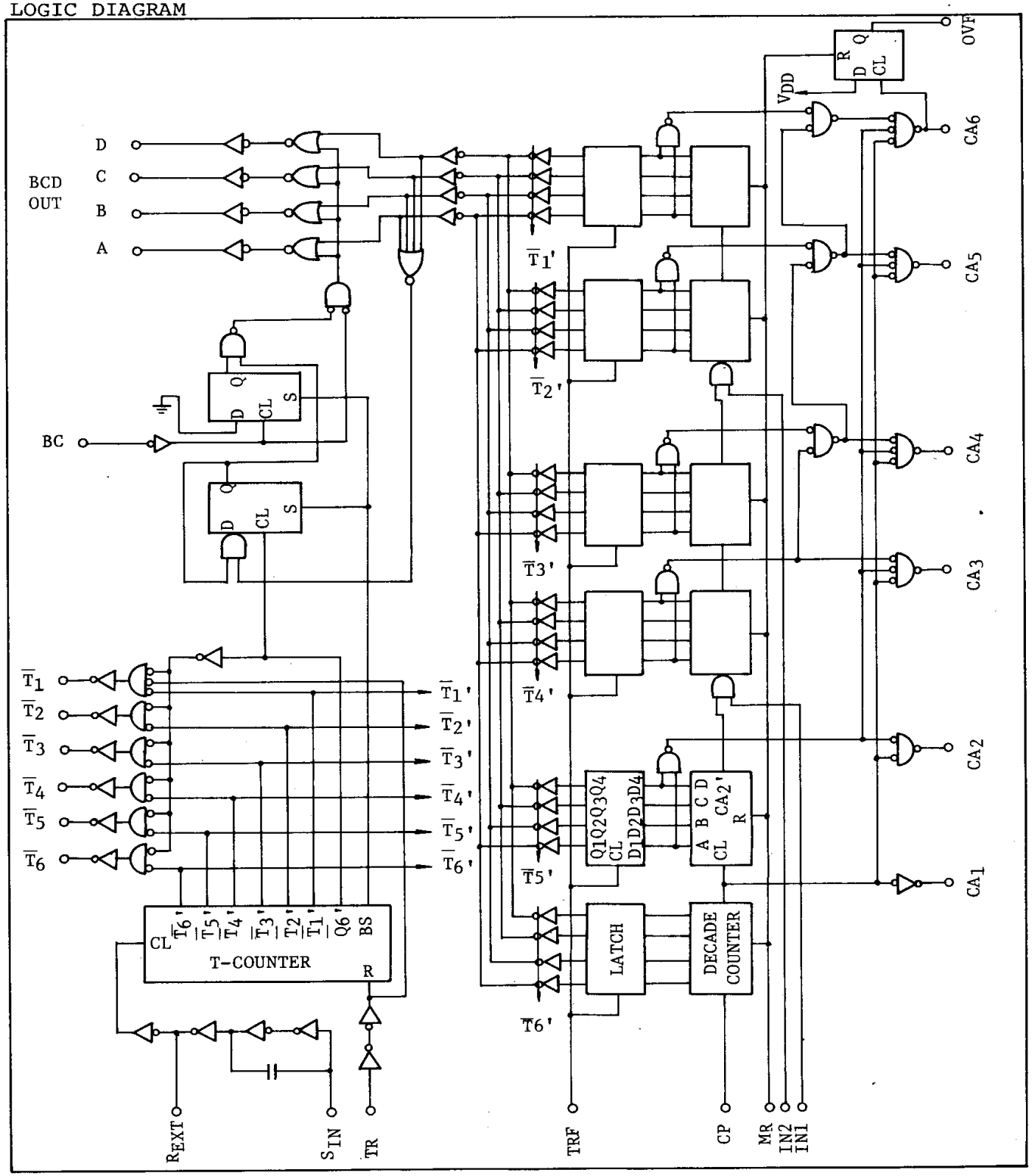
BLOCK DIAGRAM



PIN FUNCTION & NAME

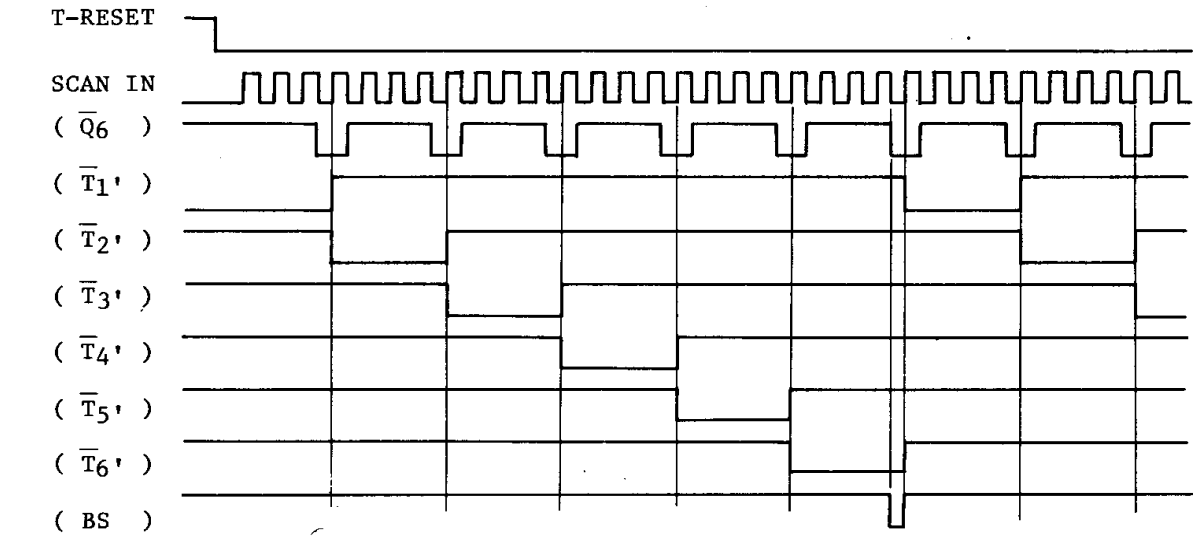
PIN NO.	SYMBOL	NAME	FUNCTION
1	$\overline{T1}$	$\overline{T1}$	Outputs to indicate the digit of output signals A_{OUT} through D_{OUT}, the sequence is descending order from $\overline{T1}$. With TR="H", all of $\overline{T1}$ through $\overline{T6}$ become "H", and when TR falls, $\overline{T1}$ becomes "L". Then, "L" is shifted in sequence $\overline{T2}$, $\overline{T3}$ --- by each 4 clocks of S_{IN}.
2	$\overline{T2}$	$\overline{T2}$	
3	$\overline{T3}$	$\overline{T3}$	
4	$\overline{T4}$	$\overline{T4}$	
5	$\overline{T5}$	$\overline{T5}$	
6	$\overline{T6}$	$\overline{T6}$	
7	R_{EXT}	RESISTOR EXTERNAL	Leave open when an external clock is applied from S_{IN}. When no external clock is available, clock can be generated by externally connecting a resistor between S_{IN} and R_{EXT}.
8	S_{IN}	SCAN INPUT	T-COUNTER CLOCK input. T-COUNTER changes its state at the rising edge of S_{IN}.
9	CP	CLOCK INPUT	Decimal counter clock input for the lowest order digit.
10	A_{OUT}	A-OUTPUT	Decimal counter BCD output. When $\overline{T1}$="L", the highest order digit (6th digit) is output. Then, 5th digit is output with $\overline{T2}$="L", 4th digit with $\overline{T3}$="L", ---, 1st digit with $\overline{T6}$="L". During BLANKING, all the outputs become "H".
11	B_{OUT}	B-OUTPUT	
12	C_{OUT}	C-OUTPUT	
13	D_{OUT}	D-OUTPUT	
14	V_{SS}	V_{SS}	(GND)
15	CA1	CARRY 1	Carry output from n-th digit: "L" when count is "xxxxx6"~"xxxxx9", otherwise "H".
16	CA2	CARRY 2	"L" when count is "xxxx96"~"xxxx99", otherwise "H".
17	CA3	CARRY 3	"L" when count is "xxx996"~"xxx999", otherwise "H".
18	CA4	CARRY 4	"L" when count is "xx9996"~"xx9999", otherwise "H".
19	CA5	CARRY 5	"L" when count is "x99996"~"x99999", otherwise "H".
20	CA6	CARRY 6	"L" when count is "999996"~"999999", otherwise "H".
21	OVF	OVER FLOW	Detection terminal of OVER FLOW condition of counter. When the counter advances by one from "999999", it becomes "H". Once it has become "H", only MR can restore it to "L".
22	BC	BLANKING CONTROL	"H": Zero suppress for all the digits. "L": No zero suppress. If $\overline{Tn}$ is connected to BC, zero suppress is activated for the higher order digits than (n-1)th digit.
23	IN1	INPUT 1	"H": All the digits are counted. "L": Only the lower order two digits are counted.
24	IN2	INPUT 2	"H": All the digits are counted. "L": Only the lower order four digits are counted.
25	TRF	TRANSFER	"H": Decimal counter output is transferred to the multiplexer as it is. "L": Counter output at the falling edge of TRF is latched.
26	TR	T-COUNTER RESET	T-counter is initialized to $\overline{T1}$ by "H" level input and $\overline{T1}$ retains "H" level only for the period of TR="H".
27	MR	MASTER RESET	"H" level input resets the counter to count "000000" and OVER FLOW to "L".
28	V_{DD}	V_{DD}	V_{DD} power supply (3~8 volts)

LOGIC DIAGRAM

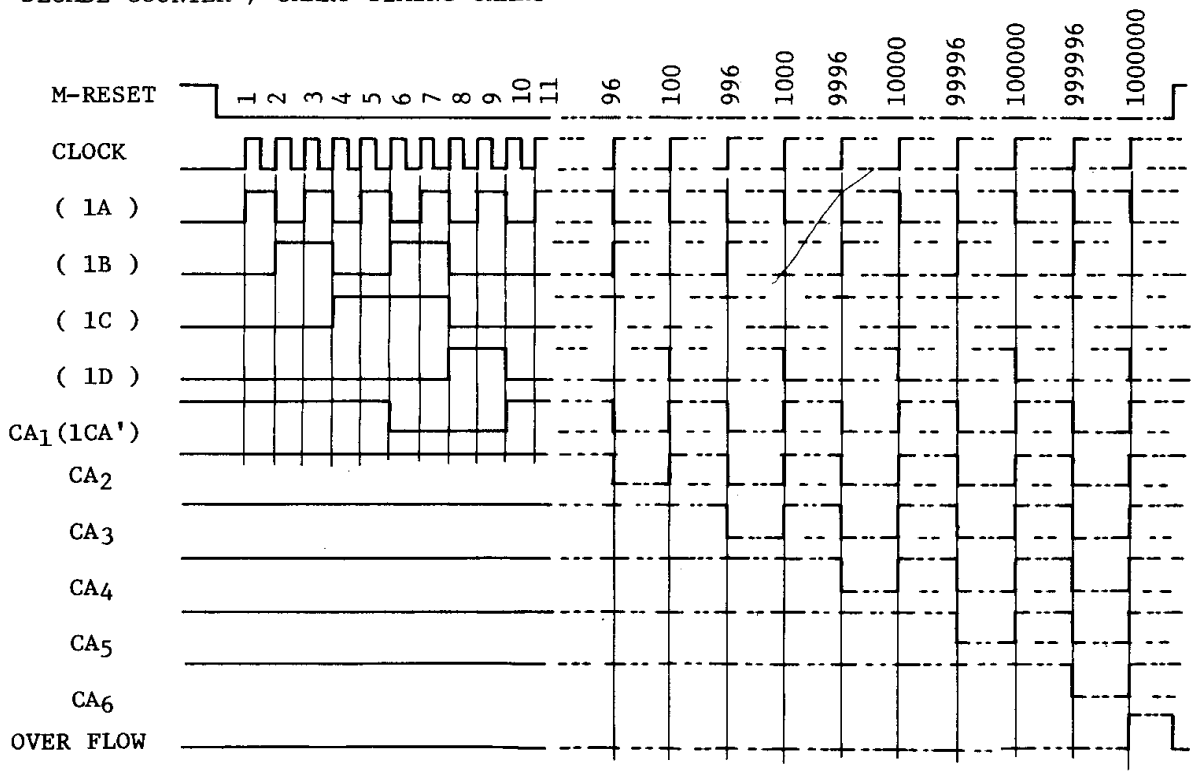


TIMING CHART

T-COUNTER TIMING CHART



DECADE COUNTER / CARRY TIMING CHART



* Waveforem marked with ( ) are timings of LSI's internals.(Refer to LOGIC DIAGRAM)

OPERATING CONSIDERATION

* Count Operation

Set input terminals IN1, IN2 and TRANSFER to "H" and apply "H" level to M-RESET terminal, then return it to "L" level. If pulse is fed to CLOCK terminal in this condition, the counter advances its count at the rising edge of CLOCK up to 999999.

Since CARRY outputs from all the digits are output in negative logic, the control of other CMOS logics can be easily achieved.

$\overline{CA1}$ - $\overline{CA6}$ are output with "L" level for four clock periods. (Refer to the timing chart.)

If one more clock is given in the count of 999999, OVER FLOW terminal becomes "H" indicating the overflow condition of COUNTER. Once OVER FLOW terminal has become "H", it will never return to "L" unless M-RESET is applied.

* Latch Operation

When the level of TRANSFER terminal is "H", the counter output is transferred to the multiplexer as it is with the output always indicating the counter output, but if TRANSFER terminal changes the level from "H" to "L", the count output which has been being output immediately prior to the falling edge of TRANSFER is stored in the latch and even if the counter output varies, A_{OUT} - D_{OUT} will not vary.

If TRANSFER terminal is returned to "H" again, the correct counter output appears on A_{OUT} - D_{OUT}.

* Scan Operation

BCD outputs of all digits are output to common A_{OUT} - D_{OUT} on the time sharing basis and the basic clock for this operation is fed from outside to SCAN IN (leaving R_{EXT} open in this case) or obtained by connecting a resistor between R_{EXT} and SCAN IN.

BCD output for each digit appears on A_{OUT} - D_{OUT} corresponding to each digit of 6 digit scan signals (digit signals) which are in synchronism with the rising edge of SCAN IN. The digit output for digit selection is output with "L" level on $\overline{T1}$ - $\overline{T6}$. As BCD outputs are output starting from the highest order digit ($\overline{T1}$ — 6th digit, ... $\overline{T6}$ — 1st digit), data transfer can be easily achieved.

* The relationship between external resistor between R_{EXT} and SCAN IN and oscillating frequency is given below

$$f \doteqdot \frac{1}{44 \times R} \times 10^{12} \ [Hz]$$

* Blanking

By controlling BLANKING CONTROL terminal, leading zero suppress to an arbitrary digit can be easily achieved. When zero suppress is activated, all of A_{OUT} - D_{OUT} become "H".

BC Terminal and Zero Suppress

BRANKING CONTROL	Leading Zero Suppress
L	No zero suppress
H	Zero suppress for all digits *
Connected to $\overline{T_6}$	Zero suppress for five higher order digits and no zero suppress for the lowest order digit. *
Connected to $\overline{T_5}$	Zero suppress for four higher order digits and no zero suppress for two lower order digits. *
Connected to $\overline{T_4}$	Zero suppress for three higher order digits and no zero suppress for three lower order digits. *
Connected to $\overline{T_3}$	Zero suppress for two higher order digits and no zero suppress for four lower order digits. *
Connected to $\overline{T_2}$	Zero suppress for the highest order digit and no zero suppress for five lower order digits. *

* When carry is generated from lower order digit, the normal output may not be obtained only one cycle of T-COUNTER.

RECOMMENDED OPERATING CONDITIONS (V_{SS}=OV)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	8	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	T_{opr}		-30	-	85	°C
R_{EXT} External Registance	R_{EXT}		20K	-	10M	Ω

ELECTRICAL CHARACTERISTICS (V_{SS}=OV)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD} (V)	-30°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Voltage	High Level	V_{OH}	I_{OH}=-1μA	5	4.95	-	4.95	-	-	4.95	-	V
	Low Level	V_{OL}	I_{OL}=1μA	5	-	0.05	-	-	0.05	-	0.05	
Output Current	High Level	I_{OH}	V_{OH}=2.5V	5	-0.7	-	-0.6	-2	-	-0.5	-	mA
	Low Level	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44	1.3	-	0.36	-	
Input Voltage	High Level	V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
	Low Level	V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
Input Current	High Level	I_{IH}	V_{IH}=8V	8	-	0.15	-	-	0.15	-	1.0	μA
	Low Level	I_{IL}	V_{IL}=0V	8	-	-0.15	-	-	-0.15	-	-1.0	
Quiescent Current Consumption		I_{DD}	At all conditions	5	-	0.4	-	10^{-5}	0.4	-	0.8	mA
				8	-	0.5	-	10^{-5}	0.5	-	1.0	

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=OV, C_L=15pF)

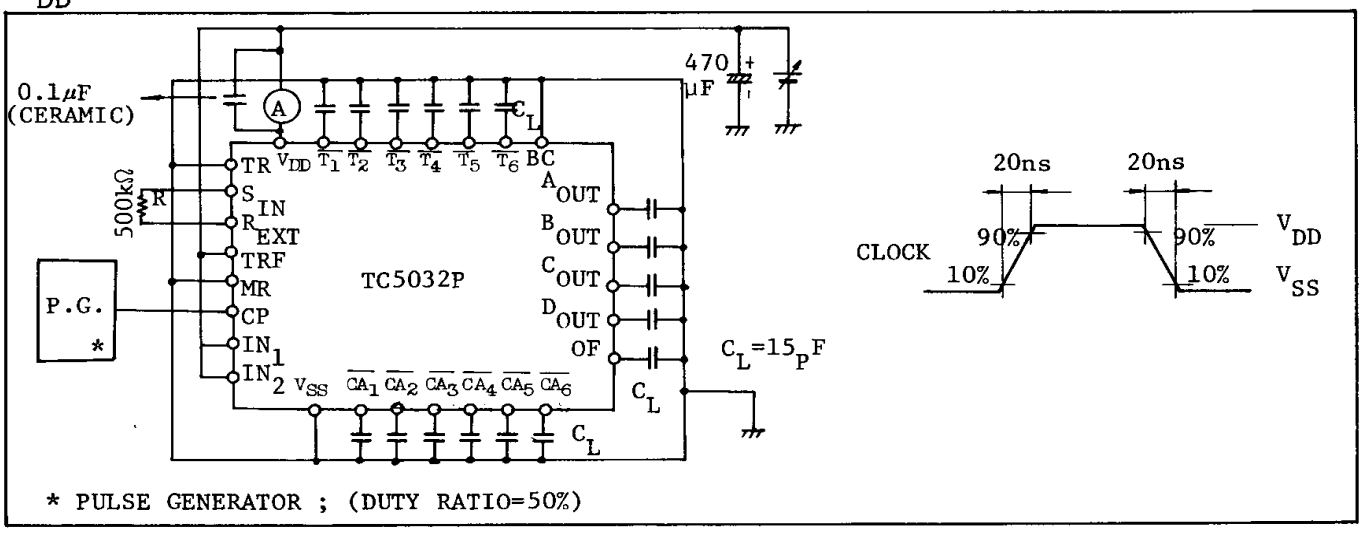
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (CP - BCD OUT)	t_{pLH}, t_{pHL}	($\overline{T6}$ = L)	5	-	800	2000	ns
		($\overline{T5}$ = L)	5	-	1000	2200	
		($\overline{T4}$ = L)	5	-	1250	2500	
		($\overline{T3}$ = L)	5	-	1500	3000	
		($\overline{T2}$ = L)	5	-	1750	3500	
		($\overline{T1}$ = L)	5	-	2000	4000	
Propagation Delay Time (CP - CARRY OUT)	t_{pLH}, t_{pHL}	CA1	5	-	(200)	500	ns
		CA2	5	-	(200)	500	
		CA3	5	-	(250)	750	
		CA4	5	-	(250)	750	
		CA5	5	-	(300)	1000	
		CA6	5	-	(300)	1000	
Max. Clock Rise Time / Max. Clock Fall Time	$t_{r\phi}$ $t_{f\phi}$	CP, IN_1, IN_2	5	20	-	-	μs
Min. Clear Pulse Width	$t_{w(MR)}$	MASTER RESET	5	-	-	500	ns
	$t_{w(TR)}$	T-COUNTER RESET		-	-	400	

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=OV, C_L=15$_P$F)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time	(High-Low)	t_{pHL}	MR-BCD OUT	5	-	-	2000	ns
	(Low-High)	t_{pLH}	TR-DIGIT OUT	5	-	-	1500	
Propagation Delay Time		t_{pLH}, t_{pHL}	SIN-BCD OUT	5	-	1000	2500	
		t_{pLH}, t_{pHL}	SIN-DIGIT OUT	5	-	500	1000	
Max. Frequency		f_{CL}-1	CLOCK IN *	5	10.0	14.0	-	MHz
		f_{CL}-2		5	1.0	2.0	-	
		f_{CL}SIN	SCAN IN	5	0.5	-	-	

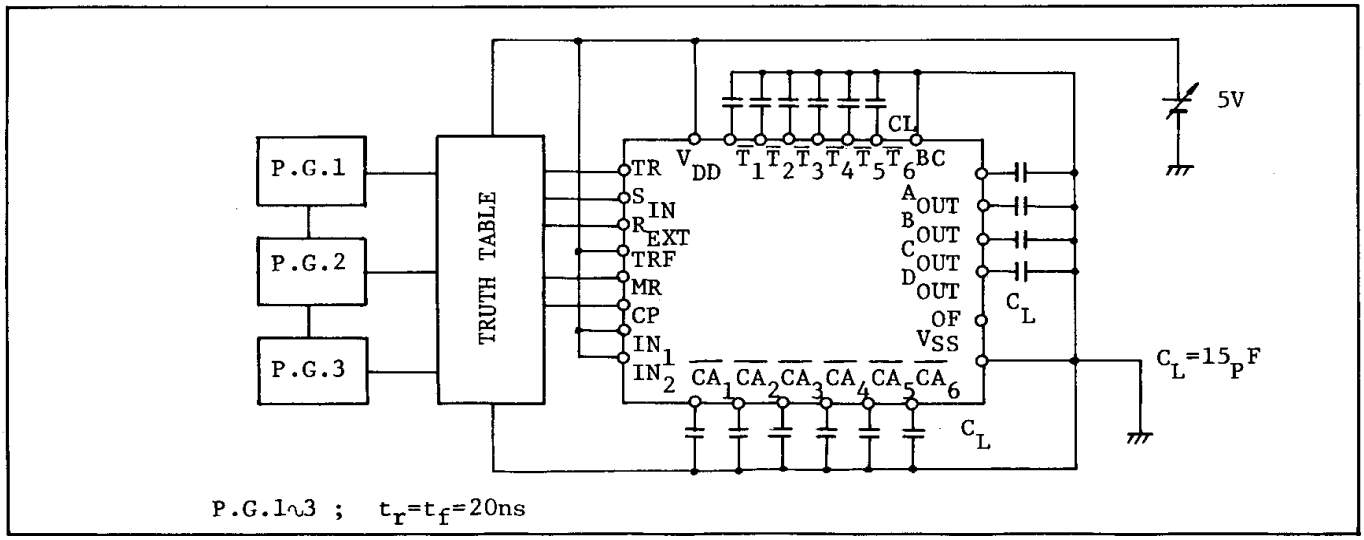
* f_{CL}-1; Clock burst mode. f_{CL}-2; BCD outputs enable.

I_{DD} TEST CIRCUIT



* PULSE GENERATOR ; (DUTY RATIO=50%)

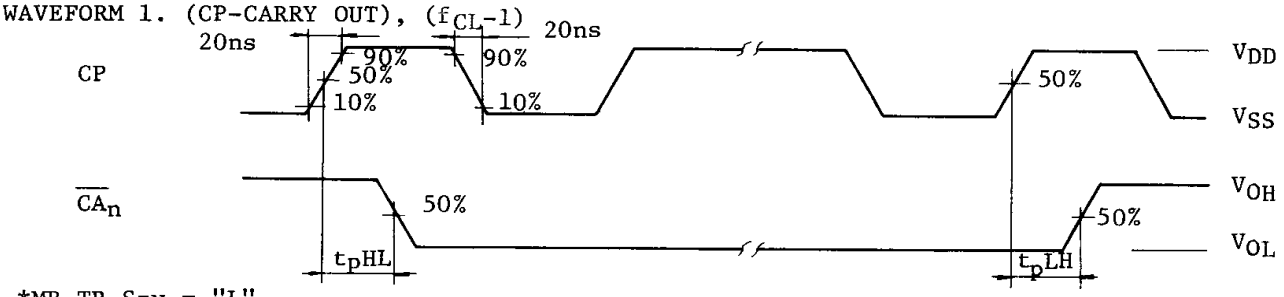
SWITCHING TIME TEST CIRCUIT



P.G.1∿3 ; t_r=t_f=20ns

SWITCHING TIME TEST WAVEFORMS

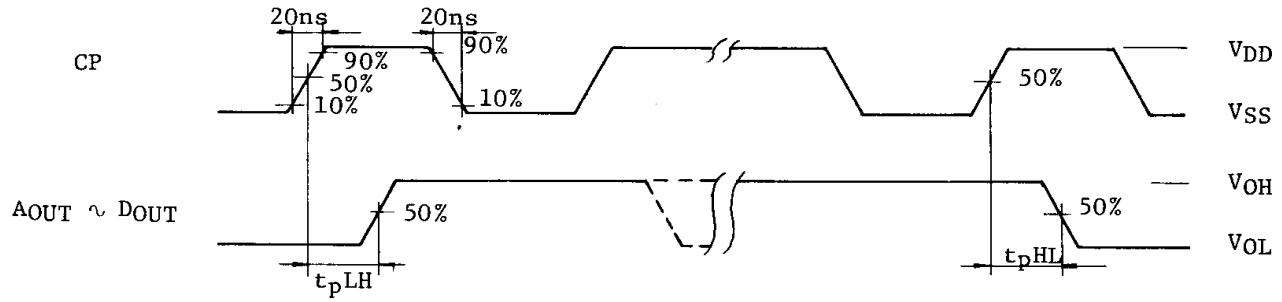
WAVEFORM 1. (CP-CARRY OUT), (f_{CL}-1)



*MR, TR, S_{IN} = "L"

**CP INPUT : f=500kHz(except f_{CL}), DUTY RATIO=50%

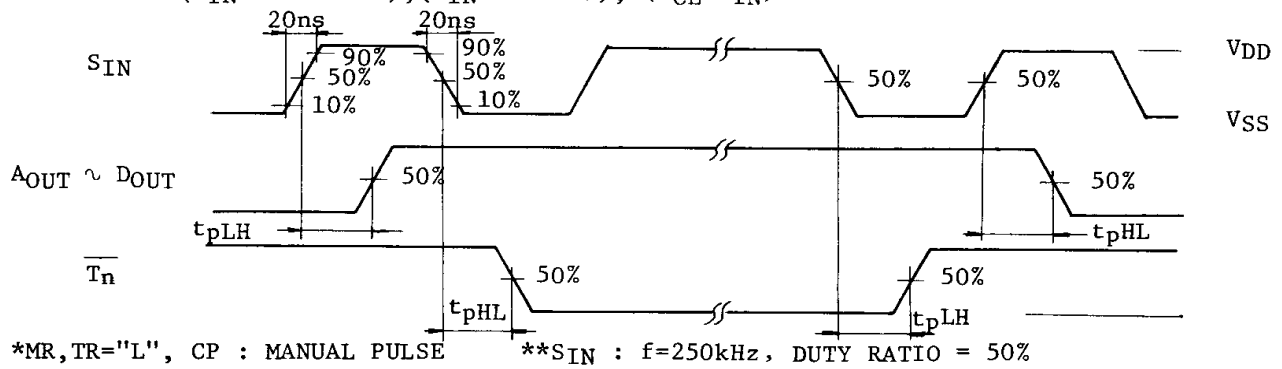
WAVEFORM 2. (CP-BCD OUT), (f_{CL}-2)



* MR, TR="L" S_{IN}=MANUAL PULSE

**CP INPUT : f=250kHz (except f_{CL}), DUTY RATIO=50%

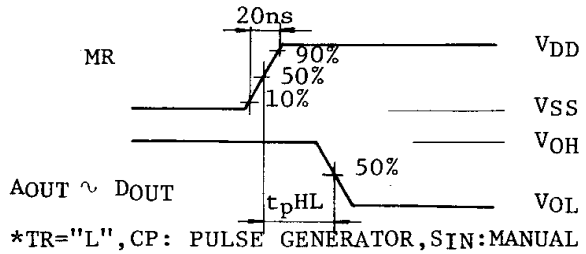
WAVEFORM 3. (S_{IN}-DIGIT OUT), (S_{IN}-BCD OUT), (f_{CL} S_{IN})



*MR, TR="L", CP : MANUAL PULSE

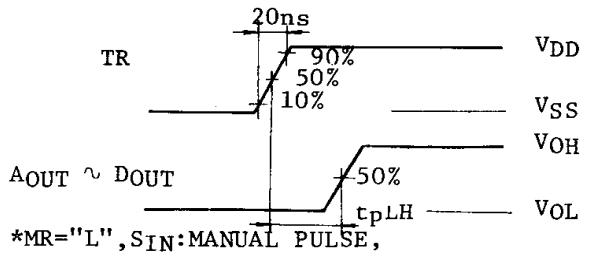
**S_{IN} : f=250kHz, DUTY RATIO = 50%

WAVEFORM 4. (MR-BCD OUT)



*TR="L", CP: PULSE GENERATOR, S_{IN}:MANUAL PULSE

WAVEFORM 5. (TR-DIGIT OUT)



*MR="L", S_{IN}:MANUAL PULSE, CP: PULSE GENERATOR