National Semiconductor

DP8511 BITBLT Processing Unit (BPU)

General Description

The DP8511 BITBLT Processing Unit (BPU), a member of National Semiconductor's Advanced Graphics Chip Set (AGCS), is a high performance microCMOS device intended for use in raster graphics applications. Specifically designed to complement the DP8500 Raster Graphics Processor (RGP), the BPU performs data operations that are elementary to BITBLT (BIT boundary Block Transfer) graphics: Shift, mask, and bitwise logical manipulation of memory. Under the control of the RGP, the BPU performs the necessary BITBLT data path operations at pipelined hardware speeds. A simple set of control lines interfaces the BPU to the RGP and to the system memory.

The BPU has two modes of operation: BITBLT and Line Drawing. BITBLT performs shift and logical operations on blocks of 16-bit data words. Line drawing performs similar operations on single-bit pixel data by utilizing a single bit pixel port (PDn). This port allows data read and read-modify-write operations on single pixels across a number of bitplanes, giving access to pixel depth. The BPU provides both pixel level processing commonly used in image processing applications and extremely fast planar operations used most frequently in color graphics.

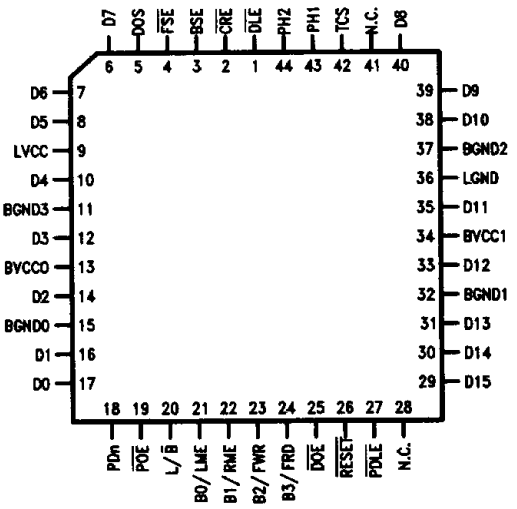
The BPU's operation is controlled by the values loaded to the Control Register (CR) and the Function Select Register (FSR). This dual register configuration of the DP8511 allows for high throughput in multi-plane systems that incorporate a BPU per plane. This performance advantage is achieved by allowing the flexibility of changing the FSR's contents independent of the CR, so that multiple bitplanes can be updated simultaneously while each BPU performs different logical operations on its own destination data.

Features

- Interfaces directly to the DP8500 Raster Graphics Processor or any general purpose controller
- 20 MHz operation
- Supports all 16 classical BITBLT functions
- Pipelined data input for high system throughput
- Provides performance independent of the number of bitplanes
- Line Drawing support
- Compatible with static, dynamic RAMs, and Video RAMs
- Compatible with page mode, nibble mode and static column RAMs
- 32-bit to 16-bit barrel shifter
- 16-bit data port, single bit pixel port
- 16-word FIFO
- 16-bit logic operations
- Single +5V supply
- All inputs and outputs TTL compatible
- 2 micron microCMOS technology
- Packaged in a 44-pin PCC (commercial) or 44-pin PGA (MIL)

Connection Diagrams

44-Pin Plastic Chip Carrier (PCC)



TL/F/9337–1

N.C. = No Connection

Top View

Order Number DP8511V
See NS Package Number V44A

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