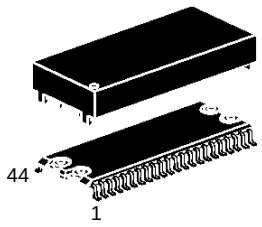
SGS-THOMSON MICROELECTRONICS

M48T36

CMOS 32K x 8 TIMEKEEPER SRAM

PRODUCT PREVIEW

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT and BATTERY
- FREQUENCY TEST OUTPUT for REAL TIME CLOCK
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGE:
  - M48T36Y: 4.2V ≤ V_{PFD} ≤ 4.5V
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY and CRYSTAL
- SNAPHAT HOUSING (BATTERY and CRYSTAL) REPLACEABLE
- MICROPROCESSOR POWER-ON RESET
- PROGRAMMABLE ALARM OUTPUT ACTIVE in the BATTERY BACK-UP MODE
- BATTERY LOW WARNING



SOH44 (MH)
Battery SNAPHAT

Figure 1. Logic Diagram

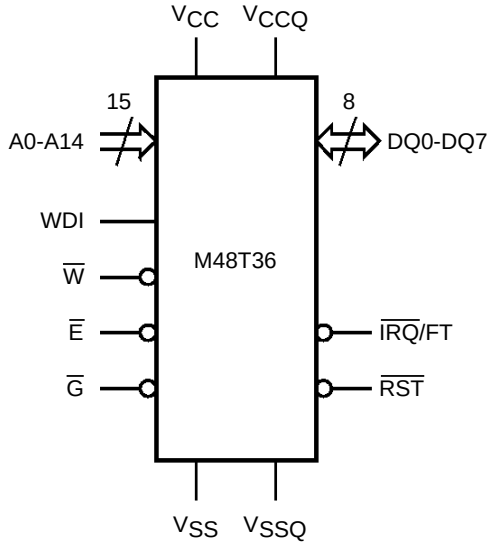


Table 1. Signal Names

A0-A14	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{IRQ}$/FT	Interrupt / Frequency Test Output (Open Drain)
$\overline{RST}$	Power Fail Reset Output (Open Drain)
WDI	Watchdog Interrupt
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{CCQ}	Supply Voltage (DQ)
V_{SS}	Ground
V_{SSQ}	Ground (DQ)

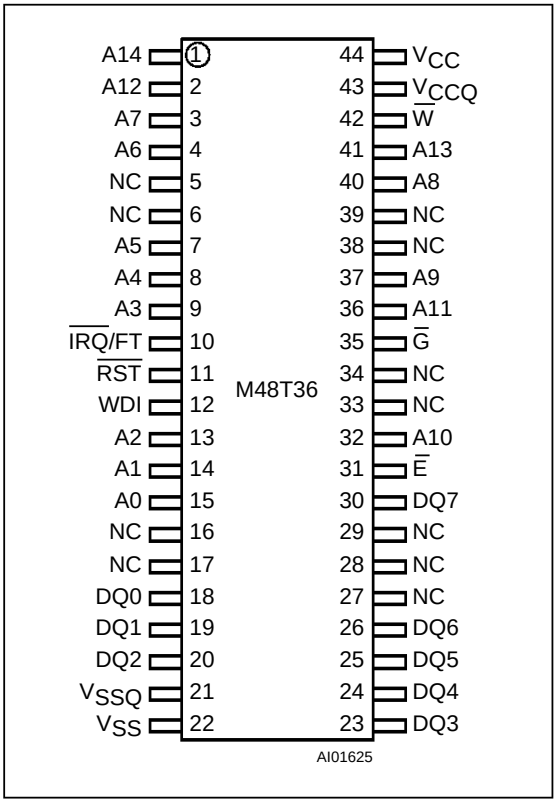
Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Figure 2A. DIP Pin Connections



Warning: NC = Not Connected

DESCRIPTION

The M48T36 TIMEKEEPER™ RAM is a 32K x 8 non-volatile static RAM and real time clock. The monolithic chip is available in a special package to provide a highly integrated battery backed-up memory and real time clock solution. The M48T36 is a non-volatile pin and function equivalent to any JEDEC standard 32K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 44 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 44 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T44-BR12SH1".

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T36 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 7FF9h-7FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically.

Figure 3. Block Diagram

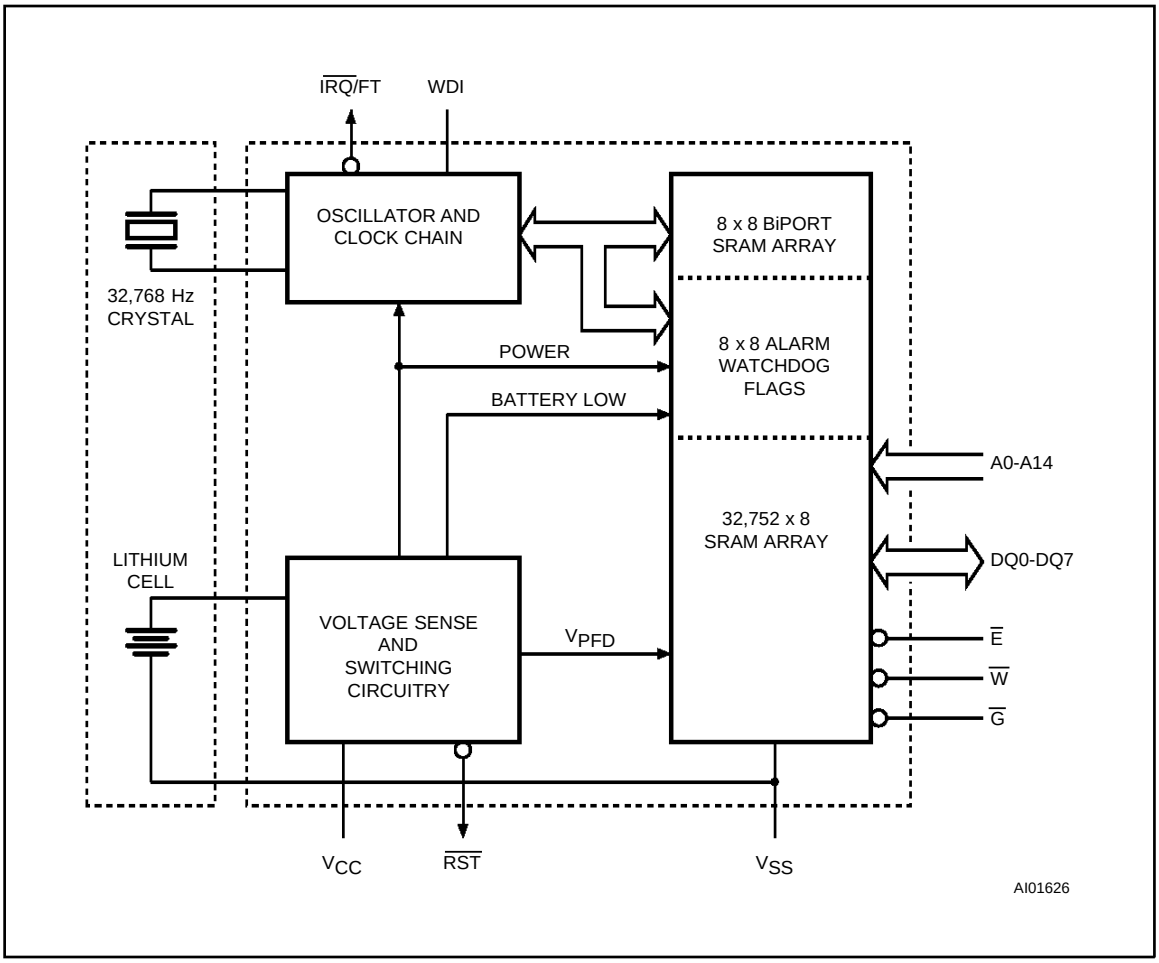


Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Notes: 1. X = V_{IH} or V_{IL}
2. See Table 6 for details.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

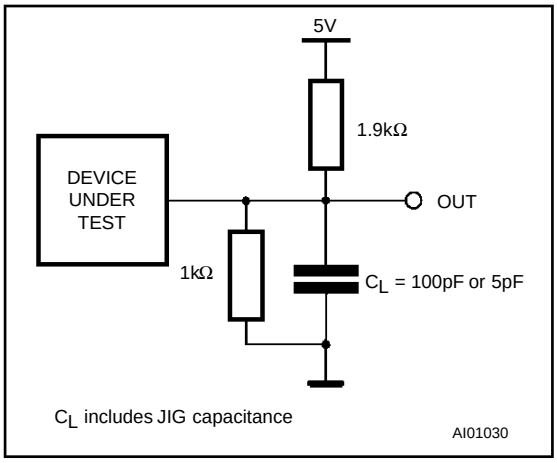


Table 4. Capacitance (1, 2) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (3)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL} (2)	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
	Output Low Voltage ($\overline{IRQ}$/FT and $\overline{RST}$) (3)	I_{OL} = 10mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Negative spikes of –1V allowed for up to 10ns once per Cycle.
3. The $\overline{IRQ}$/FT and $\overline{RST}$ pins are Open Drain.

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T36Y)	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} (2)	Expected Data Retention Time	7			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	V_{PFD} (max) to $\overline{RST}$ High	40	200	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

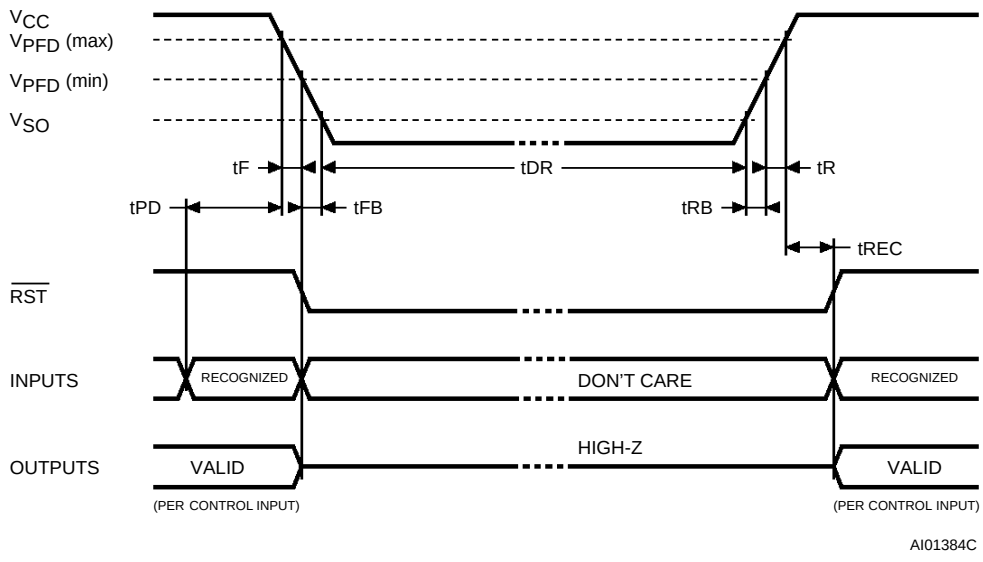
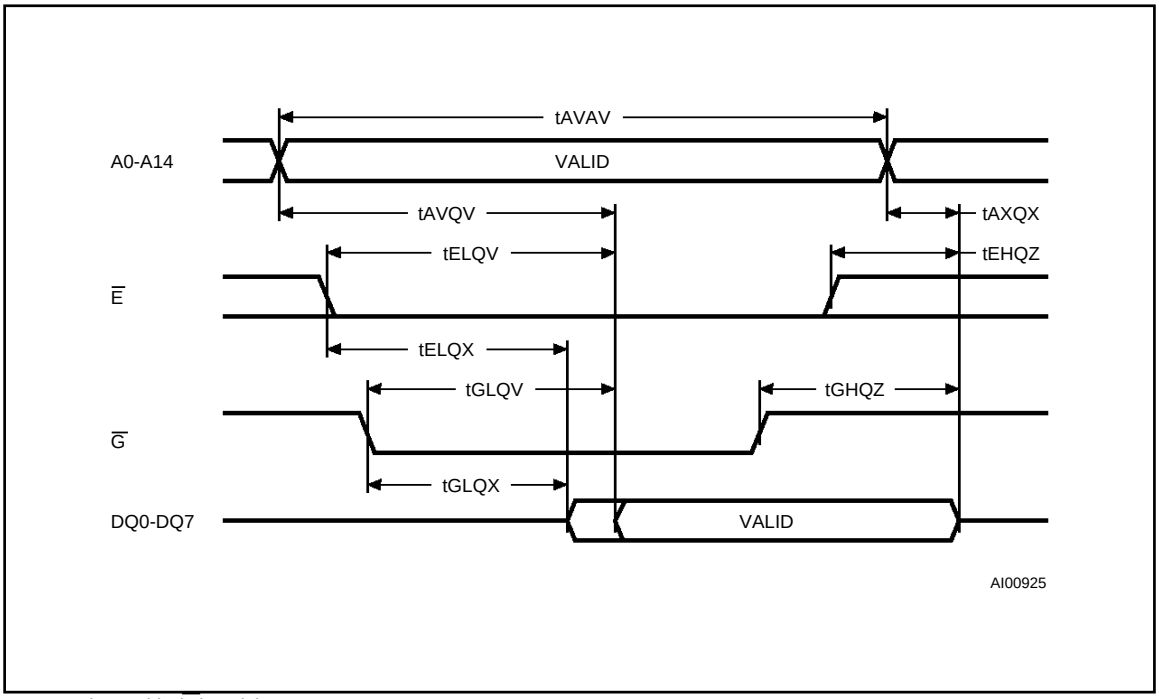


Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	M48T36Y -70		Unit
		Min	Max	
t_{AVAV}	Read Cycle Time	70		ns
t_{AVQV} (1)	Address Valid to Output Valid		70	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		70	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		35	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		25	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		ns

Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4).

Figure 6. Read Mode AC Waveforms



Note: Write Enable (W) = High

Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	M48T36Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Write Cycle Time	70		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		ns
t_{WLWH}	Write Enable Pulse Width	50		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		ns
t_{WHAX}	Write Enable High to Address Transition	0		ns
t_{EHAX}	Chip Enable High to Address Transition	0		ns
t_{DVWH}	Input Valid to Write Enable High	30		ns
t_{DVEH}	Input Valid to Chip Enable High	30		ns
t_{WHDX}	Write Enable High to Input Transition	5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		25	ns
t_{AVWH}	Address Valid to Write Enable High	60		ns
t_{AVEH}	Address Valid to Chip Enable High	60		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	5		ns

Notes: 1. C_L = 5pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

DESCRIPTION (cont'd)

Byte 7FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

Byte 7FF7h contains the watchdog timer setting. The watchdog timer detects an out-of-control microprocessor and provides a reset or interrupt to it. Byte 7FF2h-7FF5h are reserved for clock alarm programming. These bytes can be used to set the alarm. This will generate an active low signal on the $\overline{IRQ}$/FT pin when the alarm bytes match the date, hours, minutes and seconds of the clock.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T36 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T36 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

READ MODE

The M48T36 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The unique address specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met,

Figure 7. Write Enable Controlled, Write AC Waveforms

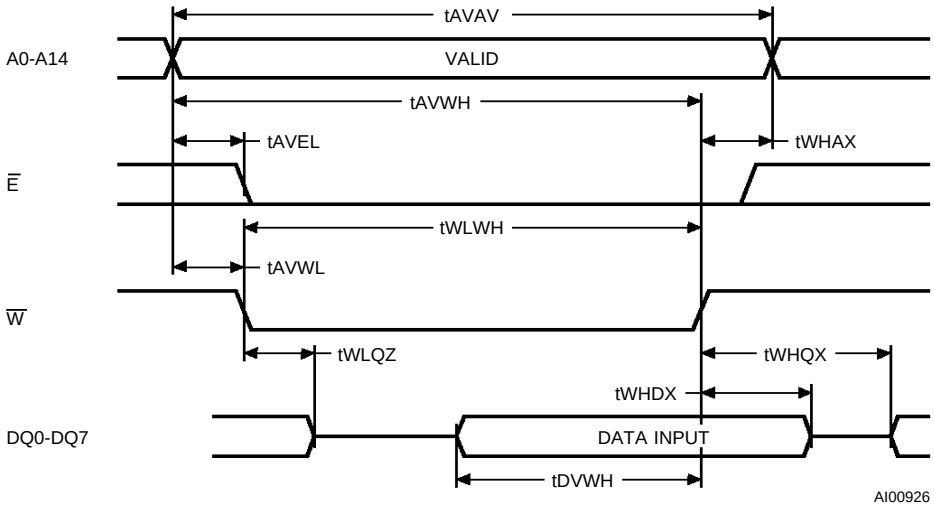
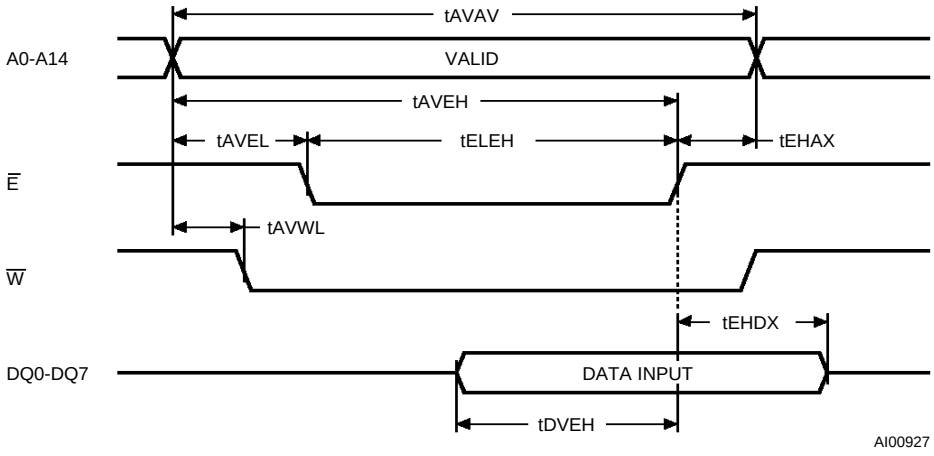


Figure 8. Chip Enable Controlled, Write AC Waveforms



READ MODE (cont'd)

valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48T36 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$ a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48T36 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T36 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T36 for an accumulated period of at least 7 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Deselect continues for t_{REC} after V_{CC} reaches V_{PFD}(max).

POWER-ON RESET

The M48T36 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for 40ms to 200ms after V_{CC} passes V_{PFD}. A 1kΩ resistor is recommended in order to control the rise time. The reset pulse remains active with V_{CC} at V_{SS}.

PROGRAMMABLE INTERRUPTS

The M48T36 has two programmable interrupts: an alarm and a watchdog. When an interrupt condition occurs, the M48T36 sets the appropriate flag bit in the flag register 7FF0h. The interrupt enable bits in 7FF6h and the WDS (Watchdog Steering) bit in 7FF7h allow the interrupt to activate the $\overline{IRQ}$/FT pin.

The interrupt flags and the $\overline{IRQ}$/FT output are cleared by a read to the flags register. An interrupt condition reset will not occur unless the addresses are stable at the flag location for at least 15ns while the device is in the read mode as shown in Figure 10.

The $\overline{IRQ}$/FT pin is an open drain output and requires a pull-up resistor. The pin remains in the high impedance state unless an interrupt occurs or the frequency test mode is enabled.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

CLOCK OPERATIONS (cont'd)

Updating is halted when a '1' is written to the READ bit, D6 in the Control Register 7FF8h. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Setting the Clock

Bit D7 of the Control Register 7FF8h is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10). Resetting the WRITE bit to a '0' then transfers the values of all time registers 7FF9h-7FFFh to the actual TIMEKEEPER counters and allows normal operation to resume. After the WRITE bit is reset, the next clock update will occur in one second.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T36 is shipped from SGS-THOMSON with the STOP bit set to a '1'.

Table 10. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFFh	10 Years				Year				Year	00-99
7FFEh	0	0	0	10 M.	Month				Month	01-12
7FFDh	0	0	10 Date		Date				Date	01-31
7FFCh	0	FT	0	0	0	Day			Day	01-07
7FFBh	0	0	10 Hours		Hours				Hour	00-23
7FFAh	0	10 Minutes			Minutes				Minutes	00-59
7FF9h	ST	10 Seconds			Seconds				Seconds	00-59
7FF8h	W	R	S	Calibration					Control	
7FF7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
7FF6h	AFE	Y	ABE	Y	Y	Y	Y	Y	Interrupts	
7FF5h	RPT4	Y	Al. 10 Date		Alarm Date				Alarm Date	01-31
7FF4h	RPT3	Y	Al. 10 Hours		Alarm Hours				Alarm Hours	00-23
7FF3h	RPT2	Alarm 10 Minutes			Alarm Minutes				Alarm Minutes	00-59
7FF2h	RPT1	Alarm 10 Seconds			Alarm Seconds				Alarm Seconds	00-59
7FF1h	Y	Y	Y	Y	Y	Y	Y	Y	Unused	
7FF0h	WDF	AF	Z	BL	Z	Z	Z	Z	Flags	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'
Y = '1' or '0'
Z = '0' and are Read only
AF = Alarm Flag
BL = Battery Low
WDS = Watchdog Steering Bit
BMB0–BMB4 = Watchdog Multiplier Bits
RB0–RB1 = Watchdog Resolution Bits
AFE = Alarm Flag Enable
ABE = Alarm in Battery Back-up Mode Enable
RPT1–RPT4 = Alarm Repeat Mode Bits
WDF = Watchdog Flag

When reset to a '0', the M48T36 oscillator starts within 1 second.

Calibrating the Clock

The M48T36 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T36 improves to better than ±4 PPM at 25°C.

Of course the oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T36 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 9. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits (D4-D0) in the Control Register 7FF8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

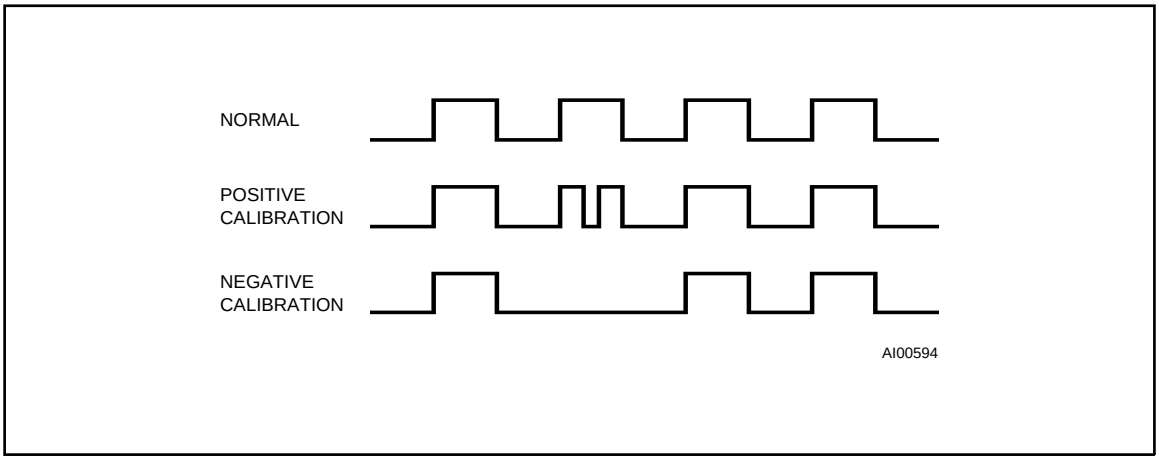
Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T36 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{IRQ}$/FT pin. The pin will toggle at 512Hz when the Stop bit (D7 of 7FF9h) is '0', the FT bit (D6 of 7FFCh) is '1', the AFE bit (D7 of 7FF6h) is '0', and the Watchdog Steering bit (D7 of 7FF7h) is '1' or the Watchdog Register is reset (7FF7h = 0).

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

Figure 9. Clock Calibration



CLOCK OPERATIONS (cont'd)

The $\overline{IRQ}$/FT pin is an open drain output which requires a pull-up resistor for proper operation. A 500-10kΩ resistor is recommended in order to control the rise time. The FT bit is cleared on power-up.

SETTING ALARM CLOCK

Registers 7FF5h-7FF2h contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific day of the month or repeat every day, hour, minute, or second. It can also be programmed to go off while the M48T36 is in the battery back-up mode of operation to serve as a system wake-up call.

RPT1-RPT4 put the alarm in the repeat mode of operation. Table 11 shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

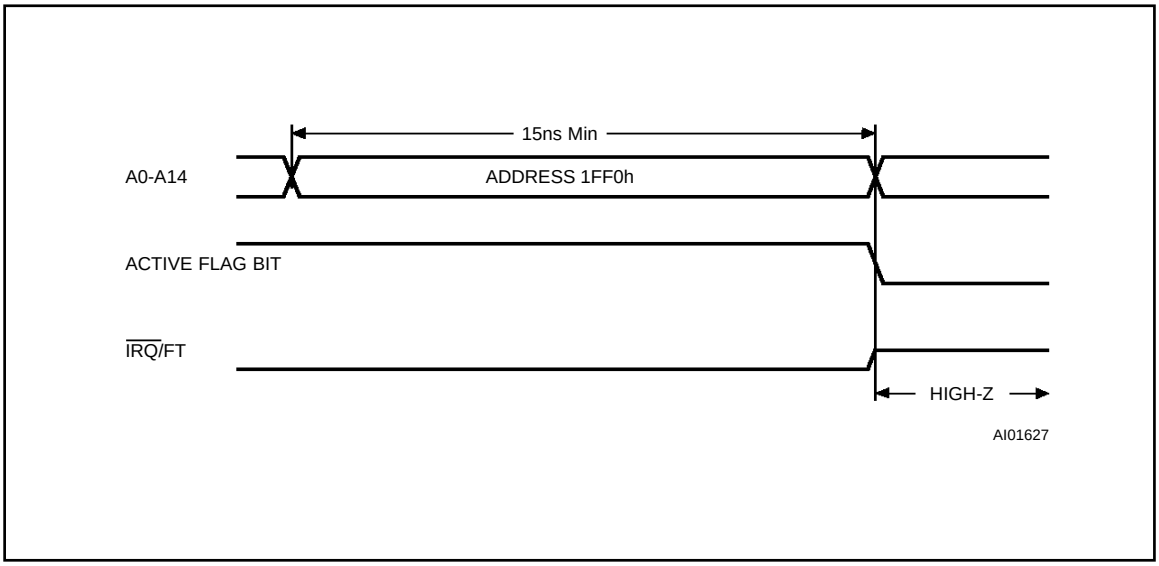
When the clock information matches the alarm clock settings based on the match criteria defined by RPT1-RPT4, AF (Alarm Flag) is set. If AFE (Alarm Flag Enable) is also set, the alarm condition activates the $\overline{IRQ}$/FT pin. The alarm flag and the $\overline{IRQ}$/FT output are cleared by a read to the Flags register as shown in Figure 10.

The $\overline{IRQ}$/FT pin can also be activated in the battery back-up mode. The $\overline{IRQ}$/FT will go low if an alarm occurs and both ABE (Alarm in Battery Back-up Mode Enable) and AFE are set. The ABE and AFE bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the Flag Register at system boot-up to determine if an alarm was generated while the M48T36 was in the deselect mode during power-up. Figure 11 illustrates the back-up mode alarm timing.

Table 11. Alarm Repeat Mode

RPT4	RPT3	RPT2	RPT1	Alarm Activated
1	1	1	1	Once per Second
1	1	1	0	Once per Minute
1	1	0	0	Once per Hour
1	0	0	0	Once per Day
0	0	0	0	Once per Month

Figure 10. Interrupt Reset Waveforms



WATCHDOG TIMER

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the eight bit Watchdog Register, address 7FF7h. The five bits (BMB4-BMB0) store a binary multiplier and the two lower order bits (RB1-RB0) select the resolution, where 00=1/16 second, 01=1/4 second, 10=1 second, and 11=4 seconds. The amount of time-out is then determined to be the multiplication of the five bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog Register = 3 x 1 or 3 seconds). If the processor does not reset the timer within the specified period, the M48T36 sets the WDF (Watchdog Flag) and generates a watchdog interrupt or a microprocessor reset.

The most significant bit of the Watchdog Register is the Watchdog Steering Bit. When set to a '0', the watchdog will activate the $\overline{IRQ}$/FT pin when timed-out. When WDS is set to a '1', the watchdog will output a negative pulse on the $\overline{RST}$ pin for a duration of 40ms to 200ms. The Watchdog register and the FT bit will reset to a '0' at the end of a watchdog time-out when the WDS bit is set to a '1'.

The watchdog timer resets when the microprocessor performs a read of the Watchdog Register. The time-out period then starts over. The watchdog timer is disabled by writing a value of 00000000 to the eight bits in the Watchdog Register. The watchdog function is automatically disabled upon power-up and the Watchdog Register is cleared. If the watchdog function is set to output to the $\overline{IRQ}$/FT pin and the frequency test function is activated, the watchdog function prevails and the frequency test function is denied. The WDI pin contains a pull-up resistor which is greater than 100kΩ, and therefore can be left unconnected if not used.

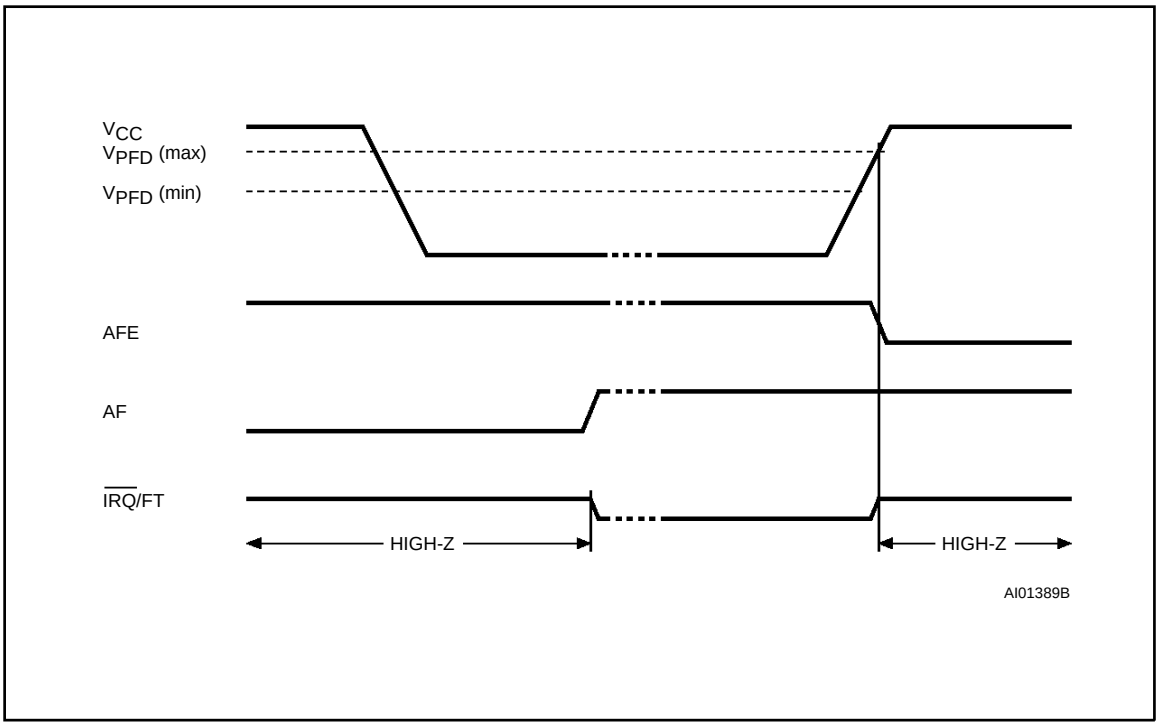
BATTERY LOW WARNING

The M48T36 checks it's battery voltage on power-up. The BL (Battery Low) bit D4 of 7FF0h will be set on power-up if the battery voltage is less than 2.5V (typical).

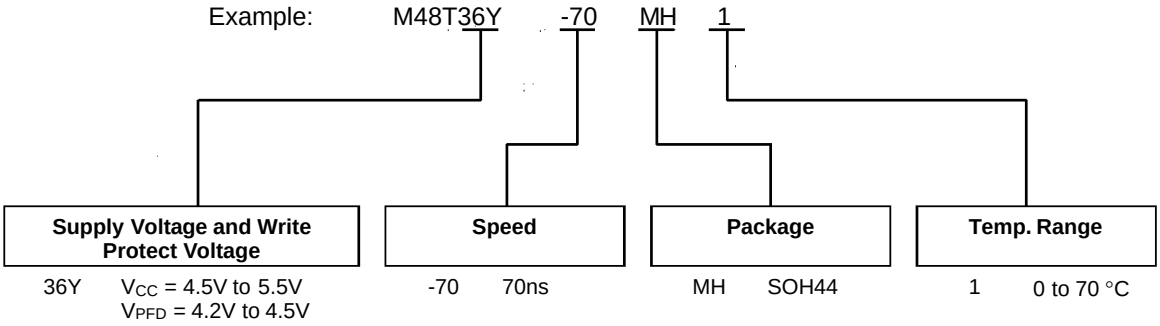
POWER-ON DEFAULTS

Upon application of power to the device, the following register bits are set to a '0' state: WDS = 0; BMB0-BMB4 = 0; RB0-RB1 = 0; AFE = 0; ABE = 0.

Figure 11. Back-up Mode Alarm Waveforms



ORDERING INFORMATION SCHEME



The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 44 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T44-BR12SH1".

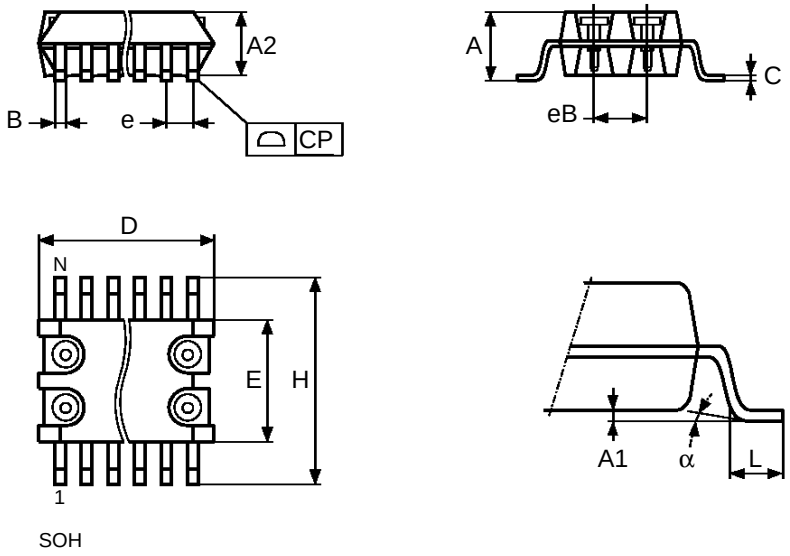
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

SOH44 - 44 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D	–	–	–	–	–	–
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	44			44		
CP			0.10			0.004

SOH44



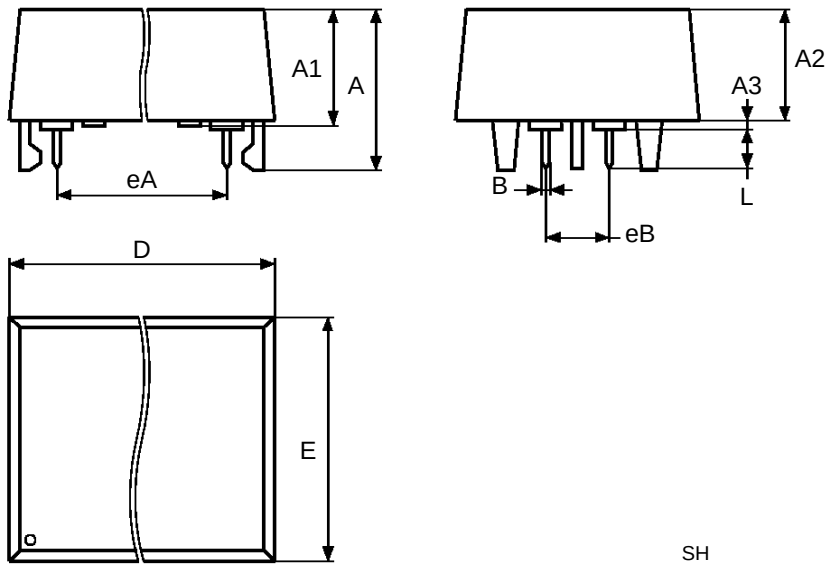
SOH

Drawing is not to scale

SH44 - SNAPHAT Housing for 44 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D	–	–	–	–	–	–
E		14.22	14.99		0.560	0.590
eA	–	–	–	–	–	–
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH44



SH

Drawing is not to scale