National Semiconductor

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DS64EV400 Programmable Quad Equalizer

DS64EV400
Programmable Quad Equalizer

General Description

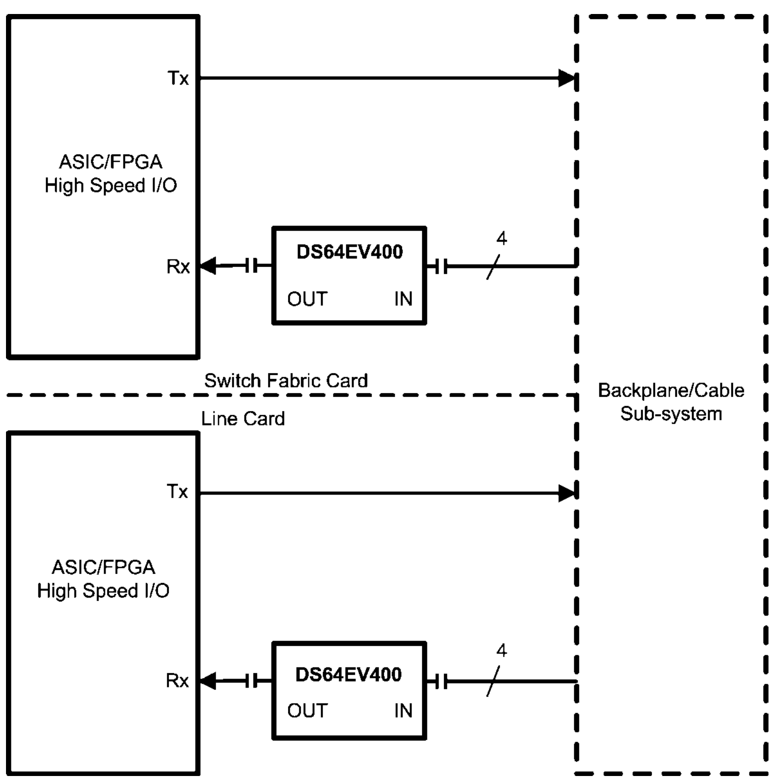
The DS64EV400 programmable quad equalizer provides compensation for transmission medium losses and reduces the medium-induced deterministic jitter for four NRZ data channels. The DS64EV400 is optimized for operation up to 10 Gbps for both cables and FR4 traces. Each equalizer channel has eight levels of input equalization that can be programmed by three control pins, or individually through a Serial Management Bus (SMBus) interface.

The equalizer supports both AC and DC-coupled data paths for long run length data patterns such as PRBS-31, and balanced codes such as 8b/10b. The device uses differential current-mode logic (CML) inputs and outputs, and is available in a 7 mm x 7 mm 48-pin leadless LLP package. Power is supplied from either a 2.5V or 3.3V supply.

Features

- Equalizes up to 24 dB loss at 10 Gbps
- Equalizes up to 22 dB loss at 6.4 Gbps
- 8 levels of programmable equalization
- Settable through control pins or SMBus interface
- Operates up to 10 Gbps with 30” FR4 traces
- Operates up to 6.4 Gbps with 40” FR4 traces
- 0.175 UI residual deterministic jitter at 6.4 Gbps with 40” FR4 traces
- Single 2.5V or 3.3V power supply
- Signal Detect for individual channels
- Standby mode for individual channels
- Supports AC or DC-Coupling with wide input common-mode
- Low power consumption: 375 mW Typ at 2.5V
- Small 7 mm x 7 mm 48-pin LLP package
- 9 kV HBM ESD
- -40 to 85°C operating temperature range

Simplified Application Diagram



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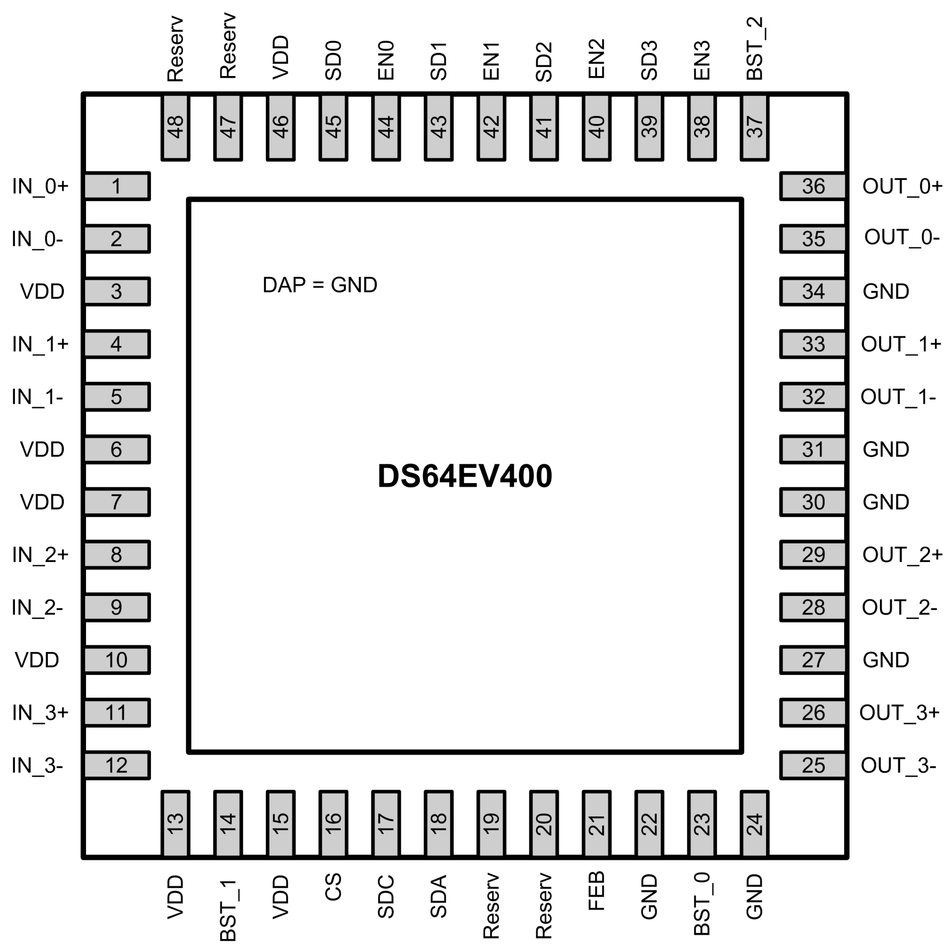
Pin Descriptions

Pin Name	Pin Number	I/O, Type	Description
HIGH SPEED DIFFERENTIAL I/O			
IN_0+ IN_0-	1 2	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN_0+ and IN_0-.
IN_1+ IN_1-	4 5	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN_1+ and IN_1-.
IN_2+ IN_2-	8 9	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN_2+ and IN_2-.
IN_3+ IN_3-	11 12	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN_3+ and IN_3-.
OUT_0+ OUT_0-	36 35	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_0+ to V_{DD} and OUT_0- to V_{DD}.
OUT_1+ OUT_1-	33 32	O, CML	An on-chip 50Ω terminating resistor connects OUT_1+ to V_{DD} and OUT_1- to V_{DD}.
OUT_2+ OUT_2-	29 28	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_2+ to V_{DD} and OUT_2- to V_{DD}.
OUT_3+ OUT_3-	26 25	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_3+ to V_{DD} and OUT_3- to V_{DD}.
EQUALIZATION CONTROL			
BST_2 BST_1 BST_0	37 14 23	I, CMOS	BST_2, BST_1, and BST_0 select the equalizer strength for EQ channel 1. BST_2 is internally pulled high. BST_1 and BST_0 are internally pulled low.
DEVICE CONTROL			
EN0	44	I, CMOS	Enable Equalizer Channel 0 input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High.
EN1	42	I, CMOS	Enable Equalizer Channel 1 input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High.
EN2	40	I, CMOS	Enable Equalizer Channel 2 input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High.
EN3	38	I, CMOS	Enable Equalizer Channel 3 input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High.
FEB	21	I, CMOS	Force External Boost. When held high, the equalizer boost setting is controlled by BST_[2:0] pins. When held low, the equalizer boost setting is controlled by SMBus (see Table 1) control pins. FEB is internally pulled High.
SD0	45	O, CMOS	Equalizer Channel 0 Signal Detect Output. Produces a High when signal is detected.
SD1	43	O, CMOS	Equalizer Channel 1 Signal Detect Output. Produces a High when signal is detected.
SD2	41	O, CMOS	Equalizer Channel 2 Signal Detect Output. Produces a High when signal is detected.
SD3	39	O, CMOS	Equalizer Channel 3 Signal Detect Output. Produces a High when signal is detected.
POWER			
V_{DD}	3, 6, 7, 10, 13, 15, 46	Power	V_{DD} = 2.5V ± 5% or 3.3V ± 10%. V_{DD} pins should be tied to V_{DD} plane through low inductance path. A 0.01µF bypass capacitor should be connected between each V_{DD} pin to GND planes.
GND	22, 24, 27, 30, 31, 34	Power	Ground reference. GND should be tied to a solid ground plane through a low impedance path.
Exposed Pad	PAD	Power	Ground reference. The exposed pad at the center of the package must be connected to ground plane of the board.

Pin Name	Pin Number	I/O, Type	Description
SERIAL MANAGEMENT BUS (SMBus) INTERFACE CONTROL PINS			
SDA	18	I, CMOS	Data input. Internally pulled high.
SDC	17	I, CMOS	Clock input. Internally pulled high.
CS	16	I, CMOS	Chip select. When held high, access to the equalizer SMBus registers are enabled. When held low, access to the equalizer SMBus registers are disabled. CS is internally gated with SDC.
OTHER			
Reserv	19, 20 47, 48		Reserved. Do not connect.

Note: I = Input O = Output

Connection Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +4.0V
CMOS Input Voltage	−0.5V + 4.0V
CMOS Output Voltage	−0.5V to 4.0V
CML Input/Output Voltage	−0.5V to 4.0V
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 Seconds)	+260°C
ESD Rating	
HBM, 1.5 kΩ, 100 pF	>9 kV
CML Inputs	>250V
Thermal Resistance	
$θ_{JA}$, No Airflow	30°C/W

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
$V_{DD2.5}$ to GND	2.375	2.5	2.625	V
$V_{DD3.3}$ to GND	3.0	3.3	3.6	V
Ambient Temperature	−40	25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges with default register settings unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER						
P	Power Supply Consumption	Device Enabled, $V_{DD3.3}$		490	700	mW
		EN0 — EN3 = Low, $V_{DD3.3}$			100	mW
P	Power Supply Consumption	Device Enabled, $V_{DD2.5}$		360	490	mW
		EN0 — EN3 = Low, $V_{DD2.5}$		30		mW
N	Supply Noise Tolerance (Note 4)	50 Hz – 100 Hz 100 Hz – 10 MHz 10 MHz – 3.2 GHz		100 40 10		mV_{P-P} mV_{P-P} mV_{P-P}
LVTTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage	$V_{DD3.3}$	2.0		V_{DD}	V
		$V_{DD2.5}$	1.6		V_{DD}	V
V_{IL}	Low Level Input Voltage		-0.3		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -3mA, $V_{DD3.3}$	2.4			V
		I_{OH} = -3mA, $V_{DD2.5}$	2.0			V
V_{OL}	Low Level Output Voltage	I_{OL} = 3mA			0.4	V
I_{IN}	Input Current	$V_{IN} = V_{DD}$			+15	μA
		V_{IN} = GND	-15			μA
I_{IN-P}	Input Leakage Current with Internal Pull-Down/Up Resistors	$V_{IN} = V_{DD}$, with internal pull-down resistors			+120	μA
		$V_{IN} = V_{DD}$, with internal pull-up resistors	-20			μA
SIGNAL DETECT						
SDH	Signal Detect High	Default input signal level to assert SD, 6.4 Gbps		80		mV_{P-P}
SDL	Signal Detect Low	Default input signal level to de-assert SD, 6.4 Gbps		40		mV_{P-P}
CML RECEIVER INPUTS (IN_n+, IN_n-						
V_{INTRE}	Input Threshold Voltage	Differential measurement at point B (Figure 1)		120		mV_{P-P}
V_{IN}	Input Voltage Swing	AC-Coupled or DC-Coupled Requirement Differential measurement at point A (Figure 1)	400		1600	mV_{P-P}

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DDTX}	Supply Voltage of Transmitter to EQ	DC-Coupled Requirement (Note 9)	1.6		V_{DD}	V
V_{ICMDC}	Input Common-Mode Voltage	DC-Coupled Requirement Differential measurement at point A (Figure 1) (Note 7)	V_{DDTX} – 0.8		V_{DDTX} – 0.2	V
R_{LI}	Differential Input Return Loss	100 MHz – 3.2 GHz, with fixture's effect de-embedded		10		dB
R_{IN}	Input Resistance	Differential across IN_n+ and IN_n-	85	100	115	Ω
CML OUTPUTS (OUT_n+, OUT_n-						
V_O	Output Voltage Swing	Differential measurement with OUT_n+ and OUT_n- terminated by 50Ω to GND AC-Coupled (Figure 2)	500		725	mV_{P-P}
V_{OCM}	Output Common-Mode Voltage	Single-ended measurement DC-Coupled with 50Ω terminations (Note 7)	V_{DD} – 0.2		V_{DD} – 0.1	V
t_R, t_F	Transition Time	20% to 80% of differential output voltage, measured within 1" from output pins (Figure 2) (Note 7)	25		45	ps
R_O	Output Resistance	Single-ended to V_{DD}	42	50	58	Ω
R_{LO}	Differential Output Return Loss	100 MHz – 3.2 GHz, with fixture's effect de-embedded. IN_n+ = static high		10		dB
t_{PLHD}	Differential Low to High Propagation Delay	Propagation delay measurement at 50% V_O between input to output, 100 Mbps (Figure 3) (Note 7)		240		ps
t_{PHLD}	Differential High to Low Propagation Delay			240		ps
t_{CCSK}	Inter Pair Channel to Channel Skew	Difference in 50% crossing between channels		7		ps
EQUALIZATION						
DJ1	Residual Deterministic Jitter at 10 Gbps	30" of 6 mil microstrip FR4, EQ Setting 0x06, PRBS-7 (2^7-1) pattern (Note 6)		0.20		UI_{P-P}
DJ2	Residual Deterministic Jitter at 6.4 Gbps	40" of 6 mil microstrip FR4, EQ Setting 0x06, PRBS-7 (2^7-1) pattern (Note 5, 6)		0.17	0.26	UI_{P-P}
DJ3	Residual Deterministic Jitter at 5 Gbps	40" of 6 mil microstrip FR4, EQ Setting 0x07, PRBS-7 (2^7-1) pattern (Note 5, 6)		0.12	0.20	UI_{P-P}
DJ4	Residual Deterministic Jitter at 2.5 Gbps	40" of 6 mil microstrip FR4, EQ Setting 0x07, PRBS-7 (2^7-1) pattern (Note 5, 6)		0.1	0.16	UI_{P-P}
RJ	Random Jitter	(Note 7, 8)		0.5		psrms

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SIGNAL DETECT and ENABLE TIMING						
t_{ZISD}	TRI-STATE to input SD Delay	Propagation delay measurement at V_{IN} to SD output, V_{IN} = 800 mV_{P-P}, 100 Mbps, 40” of 6 mil microstrip FR4 (Figure 1, 4) (Note 7)		35		ns
t_{IZSD}	Input to Tri-Sate SD Delay			400		ns
t_{OZED}	EN TRI-STATE to Output Delay	Propagation delay measurement at EN input to V_O, V_{IN} = 800 mV_{P-P}, 100 Mbps, 40” of 6 mil microstrip FR4 (Figure 1, 4) (Note 7)		150		ns
t_{ZOED}	EN Output to TRI-STATE Delay			5		ns

Note 1: “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are guaranteed for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

Note 2: Typical values represent most likely parametric norms at V_{DD} = 3.3V or 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 3: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 4: Allowed supply noise (mV_{P-P} sine wave) under typical conditions.

Note 5: Specification is guaranteed by characterization at optimal boost setting and is not tested in production.

Note 6: Deterministic jitter is measured at the differential outputs (point C of Figure 1), minus the deterministic jitter before the test channel (point A of Figure 1). Random jitter is removed through the use of averaging or similar means.

Note 7: Measured with clock-like {11111 00000} pattern.

Note 8: Random jitter contributed by the equalizer is defined as sqrt ($J_{OUT}^2 - J_{IN}^2$). J_{OUT} is the random jitter at equalizer outputs in ps-rms, see point C of Figure 1; J_{IN} is the random jitter at the input of the equalizer in ps-rms, see point B of Figure 1.

Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		V_{DD}	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source		4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	(Note 9)	-200		+200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SDC	(Note 9, 10)			10	pF
R_{TERM}	Termination Resistance	$V_{DD3.3}$, (Note 9, 10, 11)		2000		Ω
		$V_{DD2.5}$, (Note 9, 10, 11)		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS						
FSMB	Bus Operating Frequency	(Note 12)	10		100	kHz
TBUF	Bus Free Time Between Stop and Start Condition		4.7			µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	4.0			µs
TSU:STA	Repeated Start Condition Setup Time		4.7			µs
TSU:STO	Stop Condition Setup Time		4.0			µs
THD:DAT	Data Hold Time		300			ns
TSU:DAT	Data Setup Time		250			ns
$T_{TIMEOUT}$	Detect Clock Low Timeout		25		35	ms
T_{LOW}	Clock Low Period		4.7			µs
T_{HIGH}	Clock High Period		4.0		50	µs
T_{LOW}:SEXT	Cumulative Clock Low Extend Time (Slave Device)				2	ms
t_F	Clock/Data Fall Time				300	ns
t_R	Clock/Data Rise Time				1000	ns
t_{POR}	Time in which a device must be operational after power-on reset				500	ms

Note 9: Recommended value. Parameter not tested in production.

Note 10: Recommended maximum capacitance load per bus segment is 400pF.

Note 11: Maximum termination voltage should be identical to the device supply voltage.

Note 12: Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

Serial Management Bus (SMBus) Configuration Registers

The Serial Management Bus interface is compatible to the SMBus 2.0 physical layer specification, except for bus termination voltages. Holding the CS pin high enables the SMBus port allowing access to the SMBus registers. The configuration registers can be read and written using SMBus through the SDA and SDC pins. In the STANDBY state, the Searial Management Bus remains active. Please see Table 1 for more information.

TABLE 1. SMBus Register Address

Name	Address	Default	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	0x00	0x00	RO	ID Revision				SD3	SD2	SD1	SD0
Status	0x01	0x00	RO	EN1	Boost 1			EN0	Boost 0		
Status	0x02	0x00	RO	EN3	Boost 3			EN2	Boost 2		
Enable/ Boost (BST_1, BST_0)	0x03	0x44	RW	EN1 1: Enable 0: Disable	Boost Control (BC for CH1) 000 (Min Boost) 001 010 011 100 (Default) 101 110 111 (Max Boost)			EN0 1: Enable 0: Disable	Boost Control (BC for CH0) 000 (Min Boost) 001 010 011 100 (Default) 101 110 111 (Max Boost)		
Enable/ Boost (BST_3, BST_2)	0x04	0x44	RW	EN3 1: Enable 0: Disable	Boost Control (BC for CH3) 000 (Min Boost) 001 010 011 100 (Default) 101 110 111 (Max Boost)			EN2 1: Enable 0: Disable	Boost Control (BC for CH2) 000 (Min Boost) 001 010 011 100 (Default) 101 110 111 (Max Boost)		
Signal Detect ON (SD_ON)	0x05	0x00	RW	SD3 ON Threshold Select 00: 70 mV (Default) 01: 55 mV 10: 90 mV 11: 75 mV		SD2 ON Threshold Select 00: 70 mV (Default) 01: 55 mV 10: 90 mV 11: 75 mV		SD1 ON Threshold Select 00: 70 mV (Default) 01: 55 mV 10: 90 mV 11: 75 mV		SD0 ON Threshold Select 00: 70 mV (Default) 01: 55 mV 10: 90 mV 11: 75 mV	
Signal Detect OFF (SD_OFF)	0x06	0x00	RW	SD3 OFF Threshold Select 00: 40 mV (Default) 01: 30 mV 10: 55 mV 11: 45 mV		SD2 OFF Threshold Select 00: 40 mV (Default) 01: 30 mV 10: 55 mV 11: 45 mV		SD1 OFF Threshold Select 00: 40 mV (Default) 01: 30 mV 10: 55 mV 11: 45 mV		SD0 OFF Threshold Select 00: 40 mV (Default) 01: 30 mV 10: 55 mV 11: 45 mV	
SMBus Control	0x07	0x00	RW	Reserved							SMBus Enable 0: Disable 1: Enable
Output Level	0x08	0x78	RW	Reserved				Output Level: 00: 400 mV$_{P-P}$ 01: 540 mV$_{P-P}$ 10: 620 mV$_{P-P}$ (Default) 11: 760 mV$_{p-p}$		Reserved	

Note: RO = Read Only, RW = Read/Write

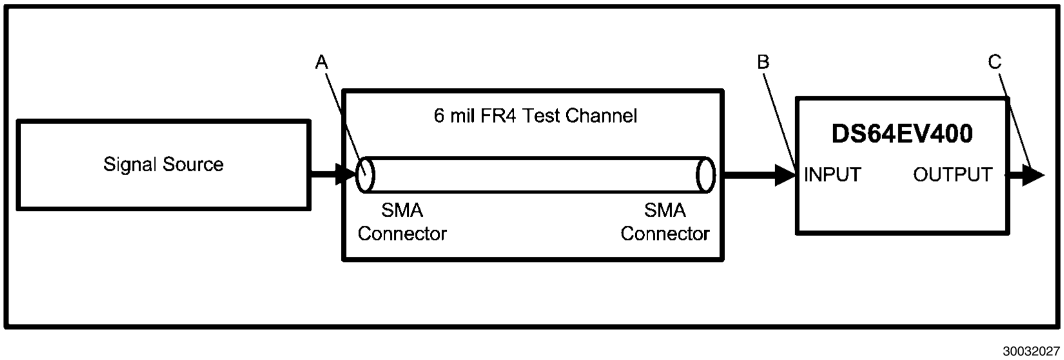


FIGURE 1. Test Setup Diagram

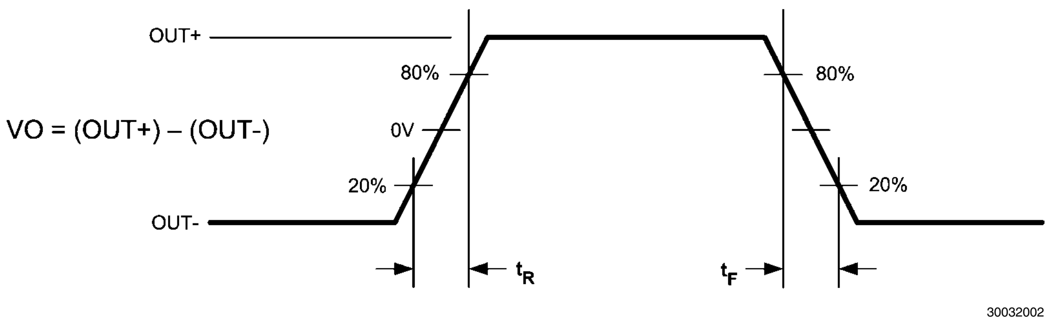


FIGURE 2. CML Output Transition Times

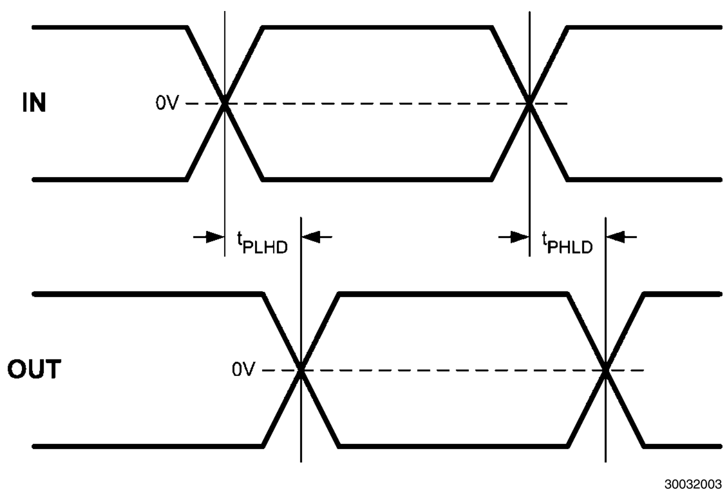


FIGURE 3. Propagation Delay Timing Diagram

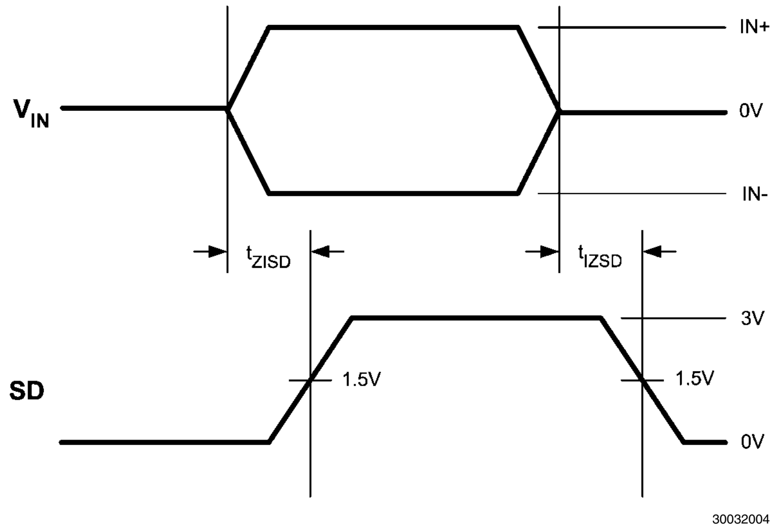


FIGURE 4. Signal Detect (SD) Delay Timing Diagram

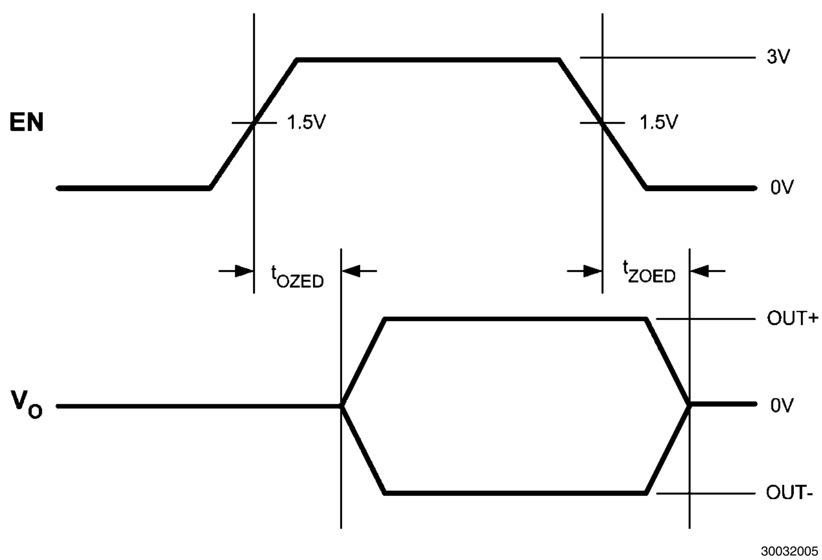


FIGURE 5. Enable (EN) Delay Timing Diagram

DS64EV400 Applications Information

The DS64EV400 is a programmable quad equalizer optimized for operation up to 10 Gbps for backplane and cable applications.

DATA CHANNELS

The DS64EV400 provides four data channels. Each data channel consists of an equalizer stage, a limiting amplifier, a DC offset correction block, and a CML driver as shown in Figure 6.

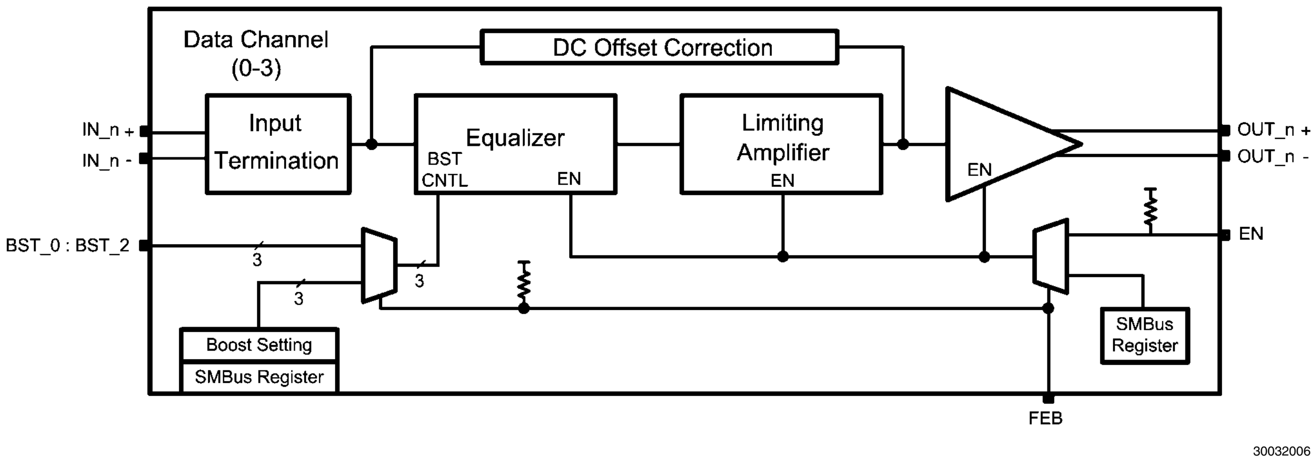


FIGURE 6. Simplified Block Diagram

EQUALIZER BOOST CONTROL

Each data channel support eight programmable levels of equalization boost. The state of the FEB pin determines how the boost settings are controlled. If the FEB pin is held High, then the equalizer boost setting is controlled by the Boost Set pins (BST_[2:0]) in accordance with Table 2. If this programming method is chosen, then the boost setting selected on the Boost Set pins is applied to all channels. When the FEB pin is held Low, the equalizer boost level is controlled through the SMBus. This programming method is accessed via the appropriate SMBus registers (see Table 1). Using this approach, equalizer boost settings can be programmed for each channel individually. FEB is internally pulled High (default setting); therefore if left unconnected, the boost settings are controlled by the Boost Set pins (BST_[0:2]). The eight levels of boost settings enables the DS64EV400 to address a wide range of media loss and data rates.

TABLE 2. EQ Boost Control Table

6 mil Microstrip FR4 Trace Length (m)	24 AWG Twin-AX cable length (m)	Channel Loss at 3.2 GHz (dB)	Channel Loss at 5 GHz (dB)	[BST_2, BST_1, BST_0]
0	0	0	0	0 0 0
5	2	5	6	0 0 1
10	3	7.5	10	0 1 0
15	4	10	14	0 1 1
20	5	12.5	18	1 0 0 (Default)
25	6	15	21	1 0 1
30	7	17	24	1 1 0
40	10	22	30	1 1 1

DEVICE STATE AND ENABLE CONTROL

The DS64EV400 has an Enable feature on each data channel which provides the ability to control device power consumption. This feature can be controlled either via each Enable Pin (ENn Pin) or via the Enable Control Bit which is accessed through the SMBus port (see Table 1 and Table 3). If the Enable is activated, the corresponding data channel is placed in the ACTIVE state and all device blocks function as described. The DS64EV400 can also be placed in STANDBY mode to save power. In this mode only the control interface including the SMBus port, as well as the signal detection circuit remain active.

TABLE 3. Controlling Device State

Register 07[0] (SMBus)	ENn Pin (CMOS)	Channel 0: Register 03[3] Channel 1: Register 03[7] Channel 2: Register 04[3] Channel 3: Register 04[7] (EN Control) (SMBus)	Device State
0 : Disable	1	X	ACTIVE
0 : Disable	0	X	STANDBY
1 : Enable	X	0	ACTIVE
1 : Enable	X	1	STANDBY

SIGNAL DETECT

The DS64EV400 features a signal detect circuit on each data channel. The status of the signal of each channel can be determined by either reading the Signal Detect bit (SDn) in the SMBus registers (see Table 1) or by the state of each SDn pin. A logic High indicates the presence of a signal that has exceeded a specified maximum threshold value (called

SD_ON). A logic Low means that the input signal has fallen below a minimum threshold value (called SD_OFF). These values are programmed via the SMBus (Table 1). If not programmed via the SMBus, the minimum and maximum thresholds take on the default values for the minimum and maximum values as indicated in Table 4. The Signal Detect threshold values can be changed through the SMBus. All threshold values specified are DC peak-to-peak differential signals (positive signal minus negative signal) at the input of the device.

TABLE 4. Signal Detect Threshold Values

Channel 0: Bit 1 Channel 1: Bit 3 Channel 2: Bit 5 Channel 3: Bit 7	Channel 0: Bit 0 Channel 1: Bit 2 Channel 2: Bit 4 Channel 3: Bit 6	Minimum Threshold Register 06 (mV)	Maximum Threshold Register 05 (mV)
0	0	40 (Default)	70 (Default)
0	1	30	55
1	0	55	90
1	1	45	75

OUTPUT LEVEL CONTROL

The output amplitude of the CML drivers for each channel can be controlled via the SMBus (see Table 1). The default output level is 650 mV_{p-p}. The following Table presents the output level values supported:

TABLE 5. Output Level Control Settings

All Channels : Bit 3	All Channels : Bit 2	Output Level Register 08 (mV_{P-P})
0	0	400
0	1	540
1	0	620 (Default)
1	1	760

AUTOMATIC ENABLE FEATURE

It may be desirable to place unused channels in power-saving Standby mode. This can be accomplished by connecting the Signal detect (SDn) pin to the Enable (ENn) pin for each channel (See Figure 7). In order for this option to function properly, the FEB pin must be either tied High or not connected (the FEB pin is internally pulled High by default). If an input signal swing applied to a data channel is above the maximum level specified in the threshold register via the SMBus, then the SDn pin is asserted High. If the SDn pin is connected to the ENn pin, this will enable the equalizer, limiting amplifier, and output buffer on the data channels (provided that the FEB pin is High); thus the DS64EV400 will automatically enter the ACTIVE state. If the input signal swing falls below the minimum level specified in the threshold register, then the SDn pin will be asserted Low, causing the aforementioned blocks to be placed in the STANDBY state.

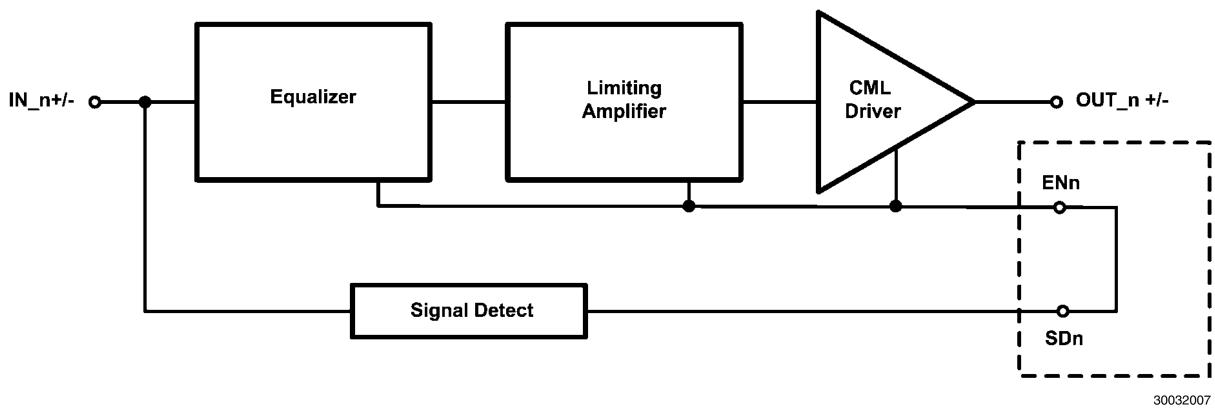


FIGURE 7. Automatic Enable Configuration

UNUSED EQUALIZER CHANNELS

It is recommended to put all unused channels into standby mode.

GENERAL RECOMMENDATIONS

The DS64EV400 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high-speed design tips to address signal integrity design issues.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and outputs must have a controlled differential impedance of 100Ω. It is preferable to route CML lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the CML signals away from other signals and noise sources on the printed circuit board. See AN-1187 for additional information on LLP packages.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS64EV400 is provided with an adequate power supply. First, the supply (V_{DD}) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.01μF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS64EV400. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2 μF to 10 μF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic and should be placed as close as possible to the DS64EV400.

Typical Performance Eye Diagrams and Curves

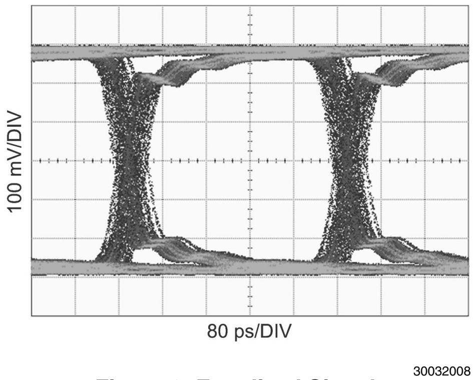


Figure 8. Equalized Signal (40 In FR4, 2.5Gbps, PRBS7, 0x07 Setting)

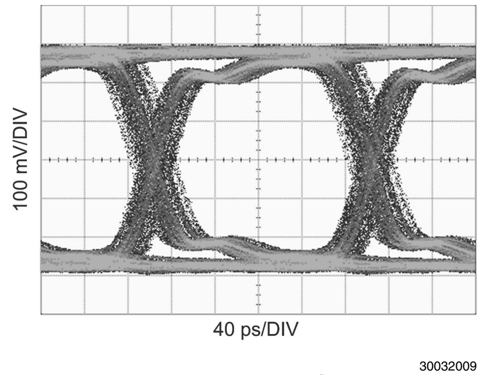


Figure 9. Equalized Signal (40 In FR4, 5Gbps, PRBS7, 0x07 Setting)

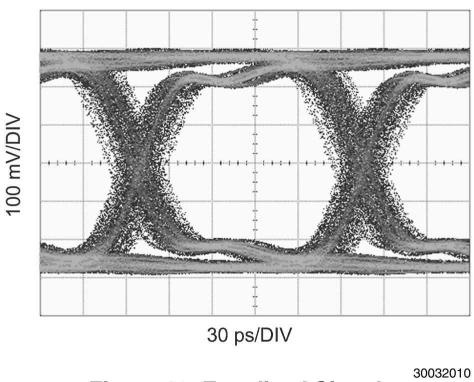


Figure 10. Equalized Signal (40 In FR4, 6.4 Gbps, PRBS7, 0x06 Setting)

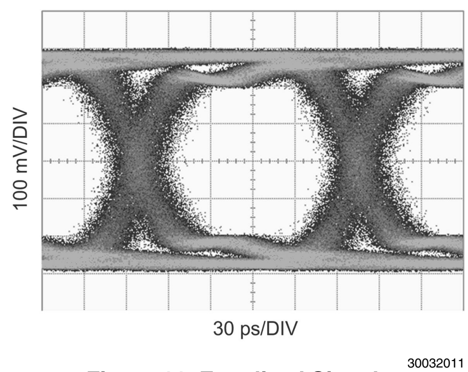
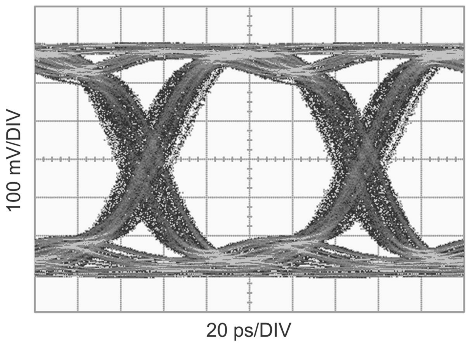
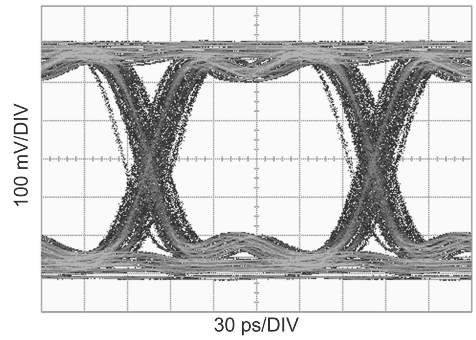


Figure 11. Equalized Signal (40 In FR4, 6.4 Gbps, PRBS31, 0x06 Setting)



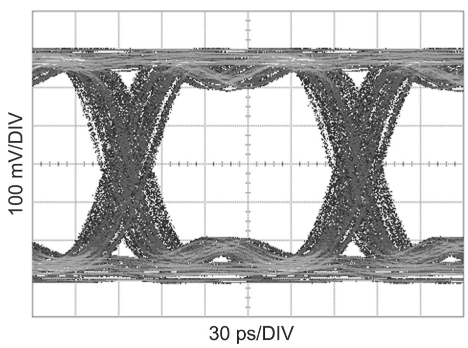
30032012

Figure 12. Equalized Signal (30 In FR4, 10 Gbps, PRBS7, 0x06 Setting)



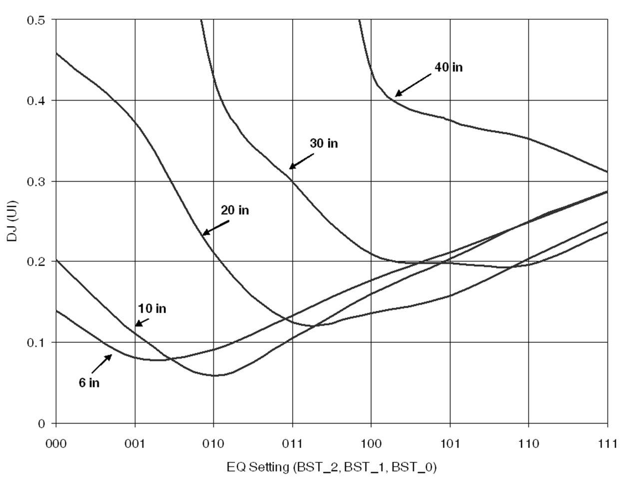
30032013

Figure 13. Equalized Signal (10m 24 AWG Twin-Ax Cable, 6.4 Gbps, PRBS7, 0x07 Setting)



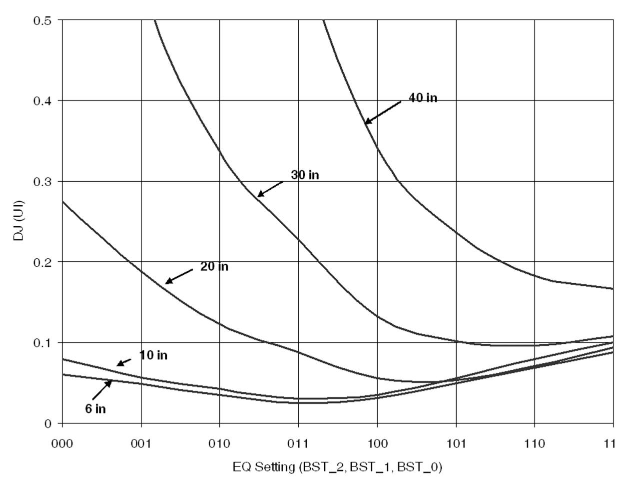
30032014

Figure 14. Equalized Signal (32 In Tyco XAUI Backplane, 6.25 Gbps, PRBS7, 0x06 Setting)



30032015

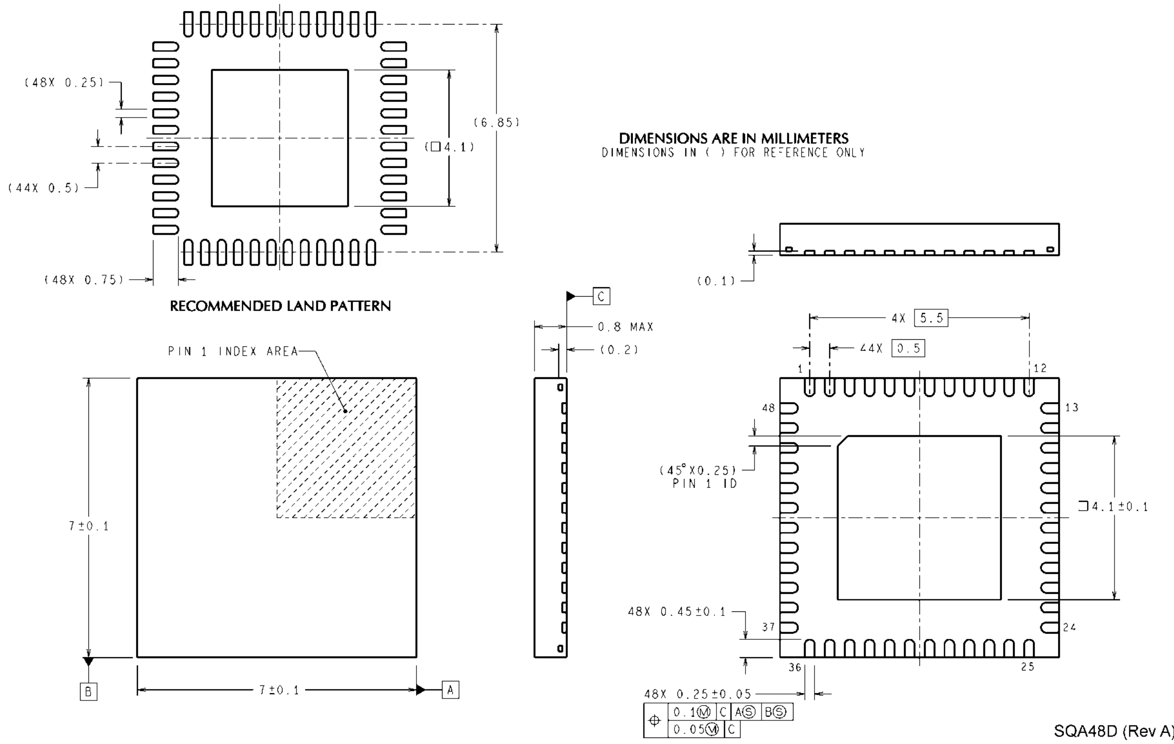
Figure 15. DJ vs. EQ Setting (10 Gbps)



30032016

Figure 16. DJ vs EQ Setting (6.4 Gbps)

Physical Dimensions inches (millimeters) unless otherwise noted



7mm x 7mm 48-pin LLP Package
Order Number DS64EV400
Package Number SQA48D

To order lead-free products, call your National Semiconductor distributors. They can order products for you with an "NOPB" specification. For more information on our Lead-free program, please check out our Lead-Free Status page.

Notes

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