National Semiconductor

June 3, 2010

LMH6629

Ultra-Low Noise, High Speed Operational Amplifier

General Description

The LMH6629 is a high speed, ultra low-noise amplifier designed for applications requiring wide bandwidth with high gain and low noise such as in communication, test and measurement, optical and ultrasound systems.

The LMH6629 operates on 2.7 to 5.5V supply with an input common mode range that extends below ground and outputs that swing to within 0.8V of the rails for ease of use in single supply applications. The LMH6629 has user-selectable internal compensation for minimum gains of 4 or 10 controlled by pulling the COMP pin low or high, thereby avoiding the need for external compensation capacitors required in competitive devices.

The low-input noise (0.69nV/√Hz and 2.6 pA/√Hz), low distortion (HD2/ HD3 = −90 dBc/ −94 dBc) and ultra-low DC errors (780 μV V_{OS} Max @ 25°C, ±0.45 μV/°C drift) allow precision operation in both AC- and DC-coupled applications.

The LMH6629 is fabricated in National Semiconductor's proprietary SiGe process and is available in a 3mm x 3mm, 8 pin LLP package.

Features

Specified for $V_S = 5V$, $R_L = 100\Omega$, $A_V = 10V/V$

■ −3dB bandwidth	900MHz
■ Input voltage noise	0.69 nV/√Hz
■ Input offset voltage max. @ 25°C	±780 μV
■ Slew rate	1600 V/ μs
■ HD2 @ f = 1MHz, $2V_{PP}$	−90 dBc
■ HD3 @ f = 1MHz, $2V_{PP}$	−94 dBc
■ Supply voltage range	2.7V to 5.5V
■ Typical supply current	15.5 mA
■ Selectable min. gain	≥4 or ≥10
■ Package	LLP-8

Applications

- Instrumentation Amplifiers
- Ultrasound Pre-amps
- Wide-band Active Filters
- Opto-electronics
- Medical imaging systems
- Base-station Amplifiers
- Trans-impedance amplifier

Typical Application Circuit

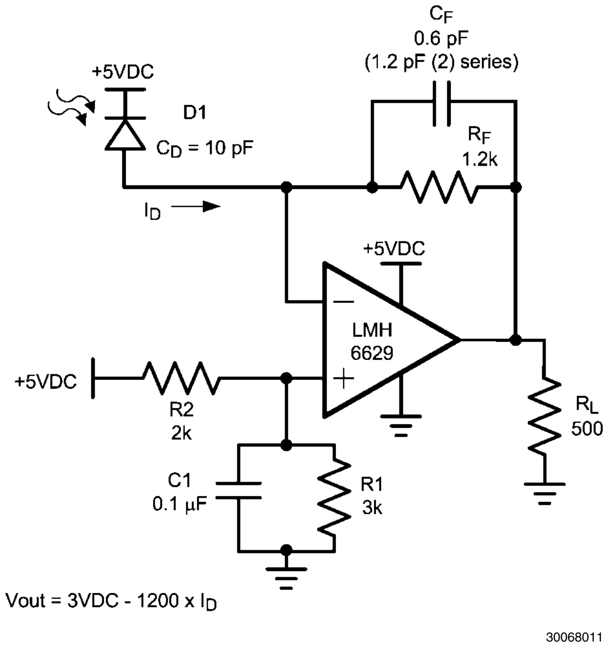
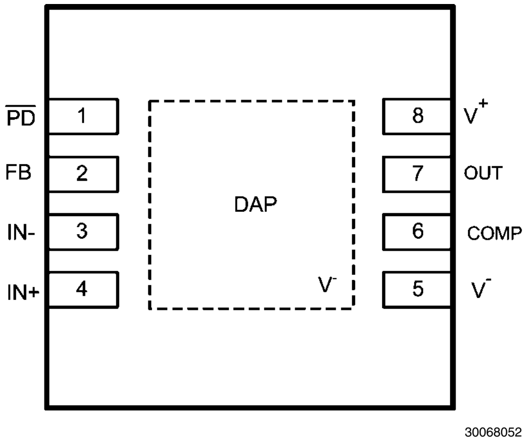


FIGURE 1. Transimpedance Amplifier

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
LLP-8	LMH6629SD	L6629	1k Units Tape and Reel	SDA08A
	LMH6629SDE		250 Units Tape and Reel	
	LMH6629SDX		4.5k Units Tape and Reel	

Connection Diagram



8-Pin LLP SDA088AD (Top View)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 4)	
Human Body Model	2kV
Machine Model	200V
Charge-Device Model	750V
Positive Supply Voltage	−0.5 to 6.0V
Differential Input Voltage	3V
Analog Input Voltage Range	−0.5 to V_S
Digital Input Voltage	−0.5 to V_S
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C

Soldering Information

See Product Folder at www.national.com and http://www.national.com/ms/MS/MS-SOLDERING.pdf

Operating Ratings (Note 1)

Supply Voltage (V+ - V−	2.7V to 5.5V
Operating Temperature Range	−40°C to +125°C
Package	(θ_{JA})
LLP-8	71°C/W

5V Electrical Characteristics

The following specifications apply for single supply with $V_S = 5V$, $R_L = 100\Omega$ terminated to 2.5V, gain = 10V/V, $V_O = 2V_{PP}$, $V_{CM} = V_S/2$, COMP Pin = HI, unless otherwise noted. **Boldface** limits apply at the temperature extremes. (Note 2).

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
DYNAMIC PERFORMANCE						
SSBW	Small signal −3dB bandwidth	$V_O = 200\ mV_{PP}$		900		MHz
		COMP Pin = LO, $A_V = 4$, $V_O = 200\ mV_{PP}$		800		
LSBW	Large signal −3dB bandwidth	$V_O = 2V_{PP}$		380		MHz
		COMP Pin = LO, $A_V = 4$, $V_O = 2V_{PP}$		190		
	0.1 dB bandwidth	$A_V = 10$, $V_O = 200\ mV_{PP}$		330		MHz
		COMP Pin = LO, $A_V = 4$, $V_O = 200\ mV_{PP}$		95		
SR	Slew rate	$A_V = 10$, 2V step		1600		V/µs
		$A_V = 4$, 2V step, COMP Pin = LO		530		
t_r/t_f	Rise/fall time	$A_V = 10$, 2V step, 10% to 90%		0.9		ns
		$A_V = 4$, 2V step, 10% to 90%, COMP Pin = LO, (Slew Rate Limited)		2.8		
T_s	Settling time	$A_V = 10$, 1V step, ±0.1%		42		
	Overload Recovery	$V_{IN} = 1V_{PP}$		2		
NOISE AND DISTORTION						
HD2	2nd order distortion	fc = 1MHz, $V_O = 2V_{PP}$		−90		dBc
		COMP Pin = LO, $A_V = 4$, fc = 1 MHz, $V_O = 2V_{PP}$		−88		
		fc = 10 MHz, $V_O = 2V_{PP}$		−70		
		COMP Pin = LO, fc = 10 MHz, $A_V = 4V$, $V_O = 2V_{PP}$		−65		
HD3	3rd order distortion	fc = 1MHz, $V_O = 2V_{PP}$		−94		dBc
		COMP Pin = LO, $A_V = 4$, fc = 1MHz, $V_O = 2V_{PP}$		−87		
		fc = 10 MHz, $V_O = 2V_{PP}$		−82		
		COMP Pin = LO, fc = 10 MHz, $V_O = 2V_{PP}$		−75		
OIP3	Two-tone 3rd order intercept point	fc = 25 MHz, $V_O = 2\ V_{PP}$ composite		31		dBm
		fc = 75 MHz, $V_O = 2V_{PP}$ composite		27		
e_n	Noise Voltage	Input referred f > 1MHz		0.69		nV/√Hz
i_n	Noise current			2.6		pA/√Hz

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
NF	Noise Figure	$R_S = R_T = 50\Omega$		8.0		dB
ANALOG I/O						
CMVR	Input voltage range	CMRR > 70 dB	−0.30		3.8	V
V_O	Output voltage range	$R_L = 100\Omega$ to $V_S/2$	0.89 **0.95**	0.82 to 4.19	4.0 **3.9**	V
		No Load	0.76 **0.85**	0.72 to 4.28	4.1 **4.0**	
I_{OUT}	Linear output current	$V_O = 2.5V$ (Note 3)		250		mA
V_{OS}	Input offset voltage			±150	±780 **±800**	μV
TcV_{OS}	Input offset voltage temperature drift	(Note 7)		±0.45		μV/°C
I_{BI}	Input bias current	(Note 6)		−15	−23 **−37**	μA
I_{OS}	Input offset current			±0.1	±1.8 **±3.0**	μA
T_CI_{OS}	Input offset voltage temperature drift	(Note 7)		±2.8		nA/°C
C_{CM}	Input capacitance	Common Mode		1.7		pF
R_{CM}	Input resistance	Common Mode		450		kΩ
MISCELLANEOUS PARAMETERS						
CMRR	Common mode rejection ratio	V_{CM} from 0V to 3.7V	82 **70**	87		dB
PSRR	Power supply rejection ratio		81 **78**	83		
A_{VOL}	Open loop gain		74 **72**	78		
DIGITAL INPUTS/TIMING						
V_{IL}	Logic low-voltage threshold	$\overline{PD}$ and COMP pins			0.8	V
V_{IH}	Logic high-voltage threshold	$\overline{PD}$ and COMP pins	2.5			
I_{IL}	Logic low-bias current	$\overline{PD}$ and COMP pins = 0.8V (Note 6)	−23 **−19**	−28	−34 **−38**	μA
I_{IH}	Logic high-bias current	$\overline{PD}$ and COMP pins = 2.5V (Note 6)	−16 **−14**	−22	−27 **−29**	
T_{en}	Enable time			75		ns
T_{dis}	Disable time			80		
POWER REQUIREMENTS						
I_S	Supply Current	No Load, Normal Operation ($\overline{PD}$ Pin = HI or open)		15.5	16.7 **18.2**	mA
		No Load, Shutdown ($\overline{PD}$ Pin =LO)		1.1	1.85 **2.0**	

3.3V Electrical Characteristics

The following specifications apply for single supply with V_S = 3.3V, R_L = 100Ω terminated to 1.65V, gain = 10V/V, V_O = $1V_{PP}$, V_{CM} = $V_S/2$, COMP Pin = HI, unless otherwise noted. **Boldface** limits apply at the temperature extremes. (Note 2)

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 5)	Max (Note 5)	Units
DYNAMIC PERFORMANCE						
SSBW	Small signal –3dB bandwidth	V_O = 200 mV_{PP}		820		MHz
		COMP Pin = LO, A_V= 4, V_O = 200 mV_{PP}		730		
LSBW	Large signal –3dB bandwidth	V_O = $1V_{PP}$		540		MHz
		COMP Pin = LO, A_V= 4, V_O = $1V_{PP}$		320		
	0.1 dB bandwidth	A_V= 10, V_O = 200 mV_{PP}		330		MHz
		COMP Pin = LO, A_V= 4, V_O = 200 mV_{PP}		85		
SR	Slew rate	A_V= 10, 1.3V step		1100		V/µs
		COMP Pin = LO, A_V= 4, 1.3V step		500		
t_r/t_f	Rise/fall time	A_V= 10, 1V step, 10% to 90%		0.7		ns
		COMP Pin = LO, A_V= 4, 1V step, 10% to 90% (Slew Rate Limited)		1.3		
T_s	Settling time	A_V= 10, 1V step, ±0.1%		70		
	Overload Recovery	V_{IN} = $1V_{PP}$		2		
NOISE AND DISTORTION						
HD2	2nd order distortion	fc = 1MHz, V_O = $1V_{PP}$		–82		dBc
		COMP Pin = LO, A_V= 4, fc = 1MHz, V_O = $1V_{PP}$		-88		
		fc = 10 MHz, V_O = $1V_{PP}$		-67		
		COMP Pin = LO, fc = 10 MHz, A_V= 4V, V_O = $1V_{PP}$		-74		
HD3	3rd order distortion	fc = 1MHz, V_O = $1V_{PP}$		-94		dBc
		COMP Pin = LO, A_V= 4, fc = 1MHz, V_O = $1V_{PP}$		-112		
		fc = 10 MHz, V_O = $1V_{PP}$		-79		
		COMP pin = LO, fc = 10 MHz, V_O = $1V_{PP}$		–96		
OIP3	Two-tone 3rd Order Intercept Point	fc = 25 MHz, V_O = $1V_{PP}$ composite		30		dBm
		fc = 75 MHz, V_O = $1V_{PP}$ composite		26		
e_n	Noise voltage	Input referred, f > 1MHz		0.69		nV/√HZ
i_n	Noise current			2.6		pA/√HZ
NF	Noise figure	R_S = R_T = 50Ω		8.0		dB
ANALOG I/O						
CMVR	Input voltage range	CMRR > 70 dB	–0.30		2.1	V
V_O	Output voltage range	R_L = 100Ω to $V_S/2$	0.90 **0.95**	0.79 to 2.50	2.4 **2.3**	V
		No load	0.76 **0.80**	0.70 to 2.60	2.5 **2.4**	
I_{OUT}	Linear output current	V_O = 1.65V (Note 3)		230		mA
V_{OS}	Input Offset Voltage			±150	±680 **±700**	µV
TcV_{OS}	Input offset voltage temperature drift	(Note 7)		±1		µV/°C

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 5)	Max (Note 5)	Units
I_{BI}	Input Bias Current	(Note 6)		−15	−23 **−35**	μA
I_{OS}	Input Offset Current			±0.13	±1.8 **±3.0**	μA
T_CI_{OS}	Input offset voltage temperature drift	(Note 7)		±3.2		nA/°C
C_{CM}	Input Capacitance	Common Mode		1.7		pF
R_{CM}	Input Resistance	Common Mode		1		MΩ
MISCELLANEOUS PARAMETERS						
CMRR	Common Mode Rejection Ratio	V_{CM} from 0V to 2.0V	84 **81**	87		dB
PSRR	Power supply rejection ratio		82 **79**	84		
A_{VOL}	Open Loop Gain		78 **73**	79		
DIGITAL INPUTS/TIMING						
V_{IL}	Logic low-voltage threshold	$\overline{PD}$ and COMP pins			0.8	V
V_{IH}	Logic high-voltage threshold		2.0			
I_{IL}	Logic low-bias current	$\overline{PD}$ and COMP pins = 0.8V (Note 6)	-17 **−14**	−23	−28 **−32**	μA
I_{IH}	Logic high-bias current	$\overline{PD}$ and COMP pins = 2.0V (Note 6)	−16 **−13**	−22	-27 **−31**	
T_{en}	Enable time			75		ns
T_{dis}	Disable time			80		
POWER REQUIREMENTS						
I_S	Supply Current	No Load, Normal Operation ($\overline{PD}$ Pin = HI or open)		13.7	14.9 **16.0**	mA
		No Load, Shutdown ($\overline{PD}$ Pin = LO)		0.89	1.4 **1.5**	

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 3: The maximum continuous output current (I_{OUT}) is determined by device power dissipation limitations. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C

Note 4: Human Body Model, applicable std. JESD22-A114C. Machine Model, applicable std. JESD22-A115-A. Field Induced Charge Device Model, applicable std. JESD22-C101-C.

Note 5: Typical numbers are the most likely parametric norm. Bold numbers refer to over-temperature limits.

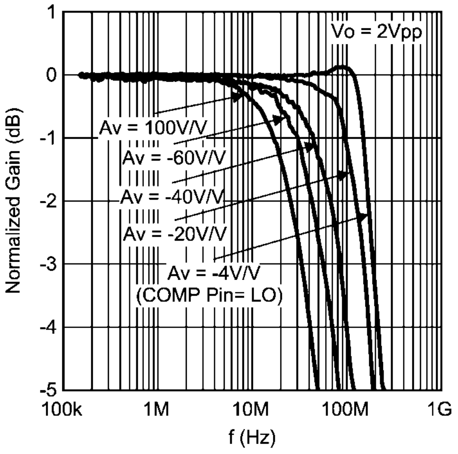
Note 6: Negative input current implies current flowing out of the device.

Note 7: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Typical Performance Characteristics

Unless otherwise specified, $V_S = \pm 2.5V$, $R_f = 240\Omega$, $R_L = 100\Omega$, $V_{OUT} = 2V_{PP}$, COMP pin = HI, $A_V = +10$ V/V.

Inverting Frequency Response



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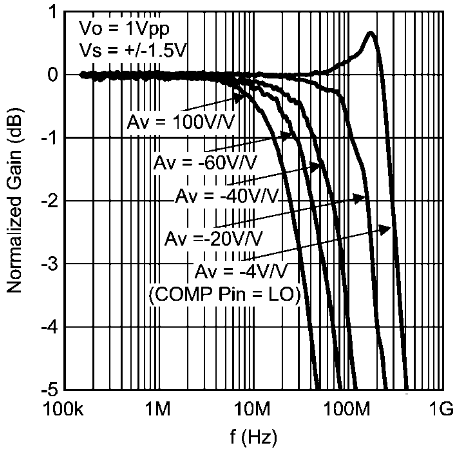
Inverting Frequency Response



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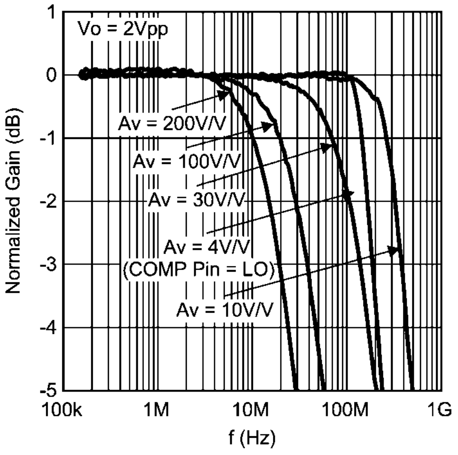
Non-Inverting Frequency Response



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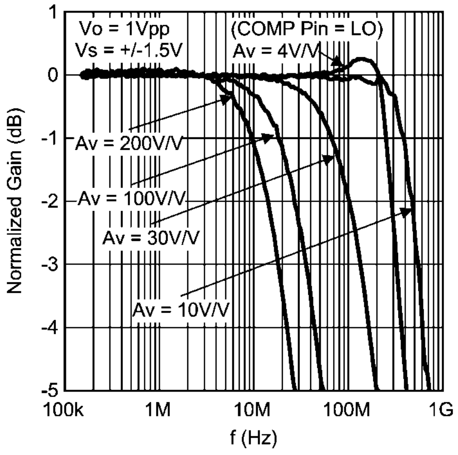

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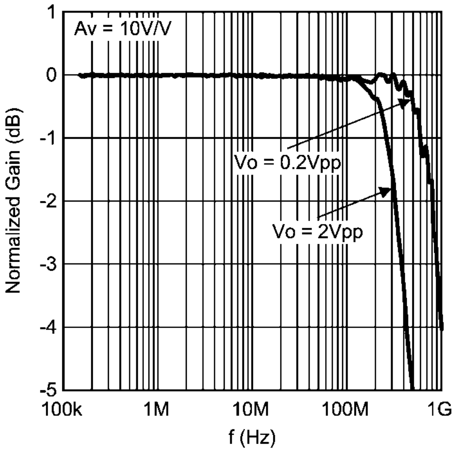
Non-Inverting Frequency Response with Varying V_O



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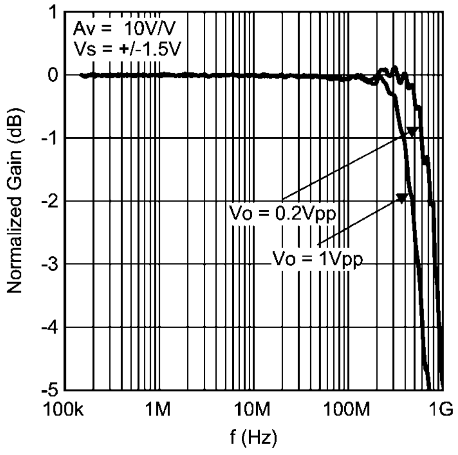
Non-Inverting Frequency Response with Varying V_O



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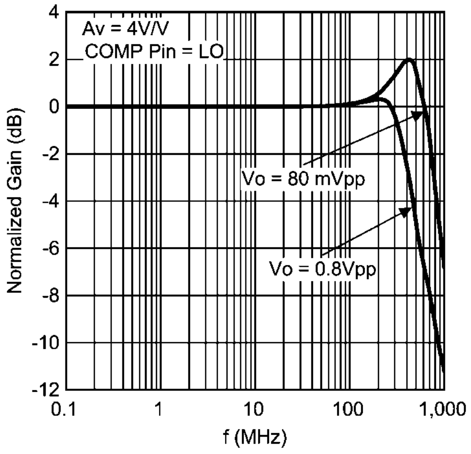
Non-Inverting Frequency Response with Varying V_O



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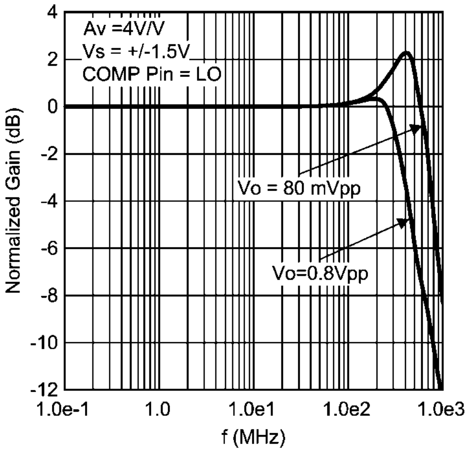
Non-Inverting Frequency Response with Varying V_O



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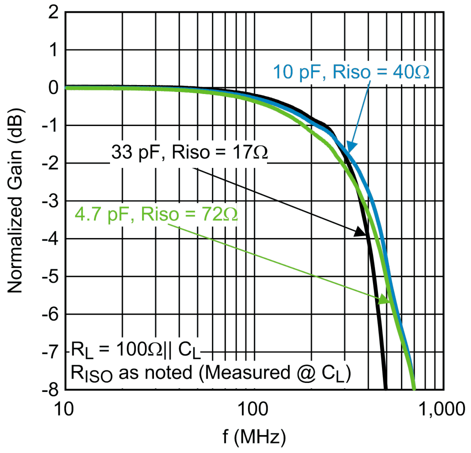
Frequency Response with Cap. Loading



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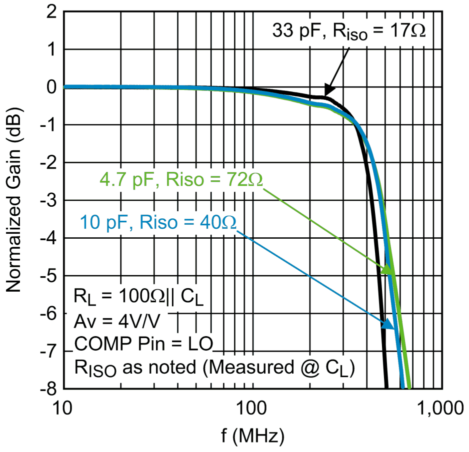
Frequency Response Cap. Loading



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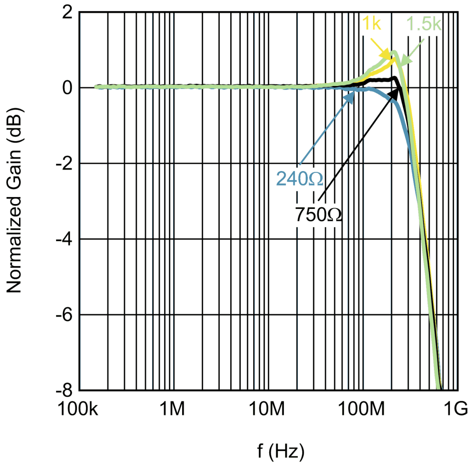
Frequency Response vs. R_f



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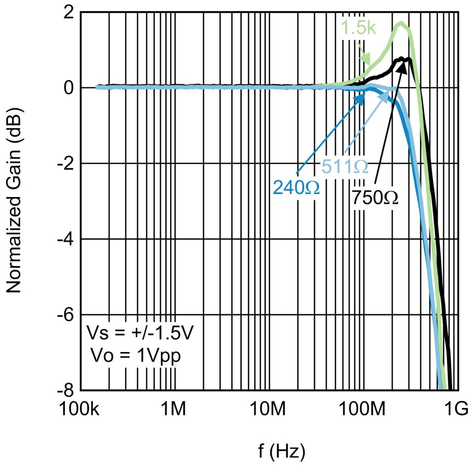
Frequency Response vs. R_f



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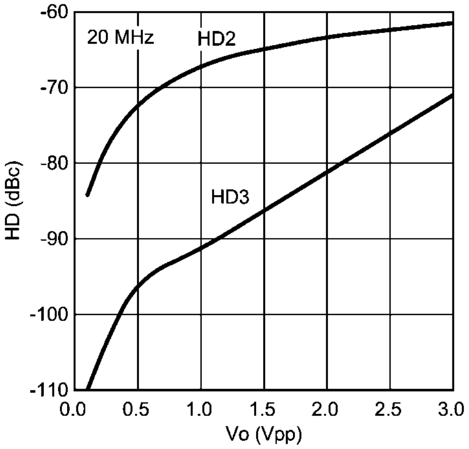
Distortion vs. Swing



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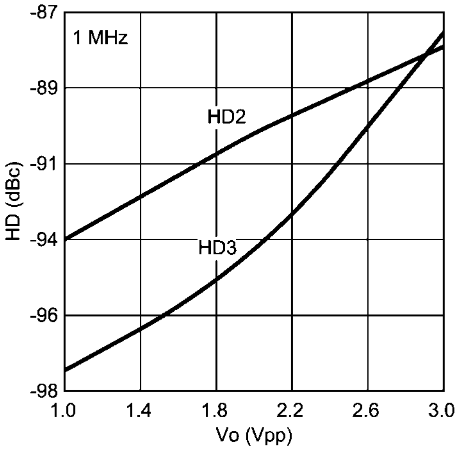
Distortion vs. Swing



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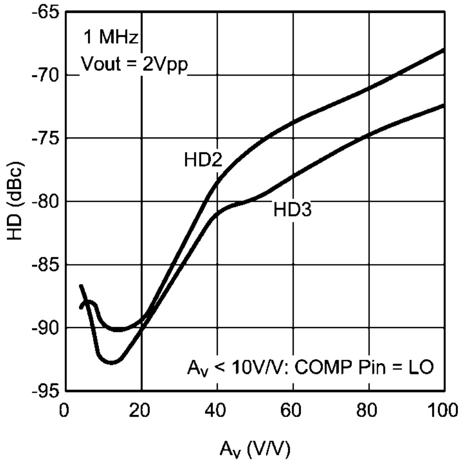
Distortion vs. Gain



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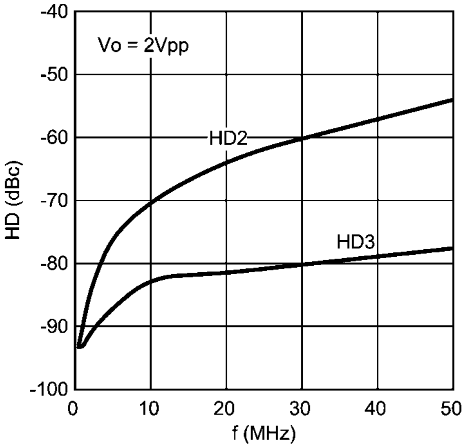
Distortion vs. Frequency



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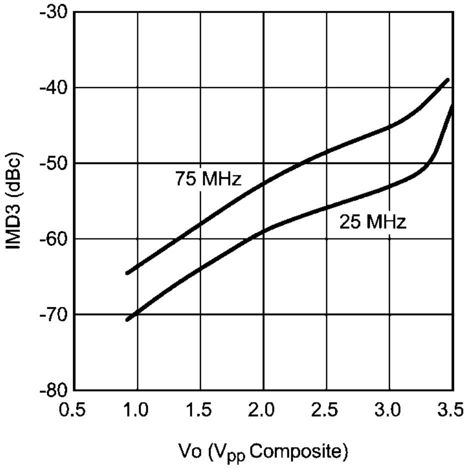
3rd Order Intermodulation Distortion vs. Output Voltage



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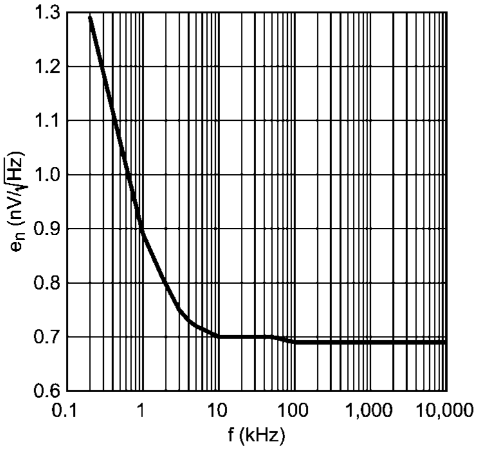
Input Noise Voltage vs. Frequency



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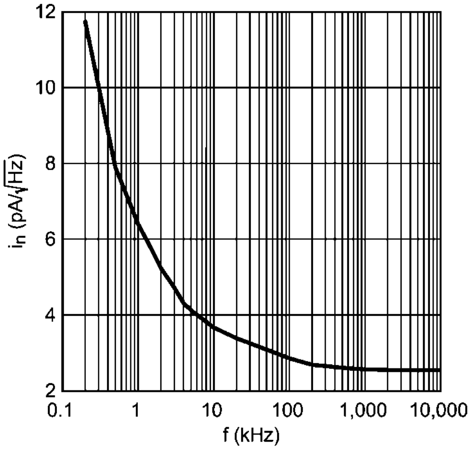
Input Noise Current vs. Frequency



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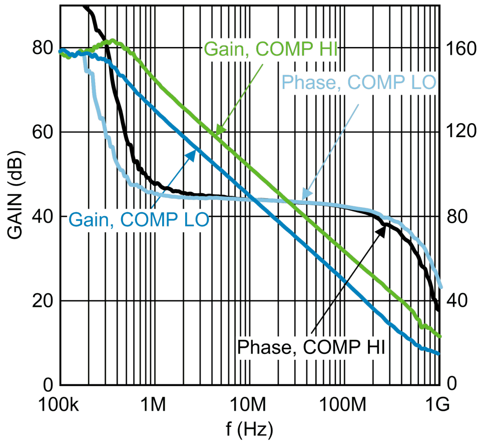
Open Loop Gain/Phase Response



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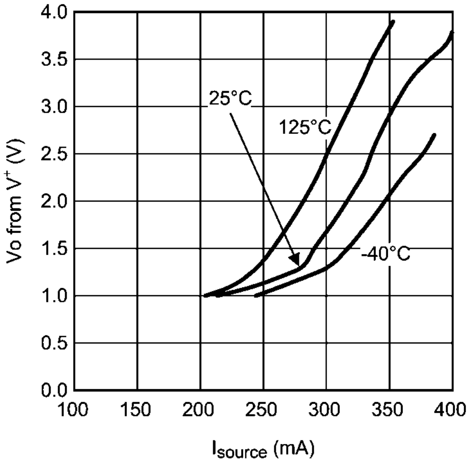
Output Source Current



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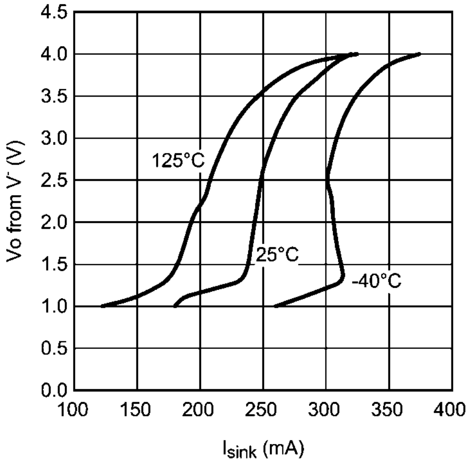
Output Sink Current



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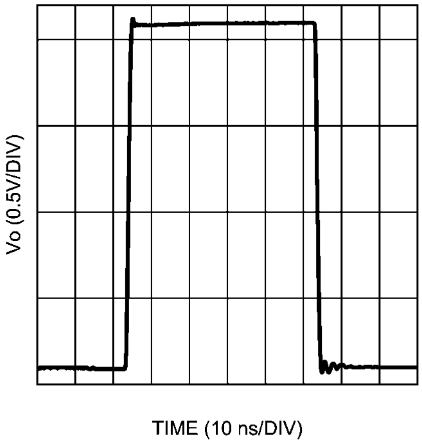
Large Signal Step Response



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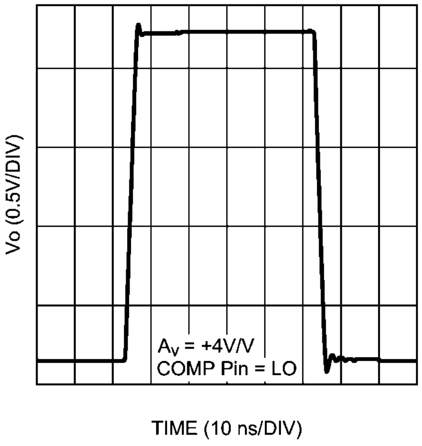
Large Signal Step Response



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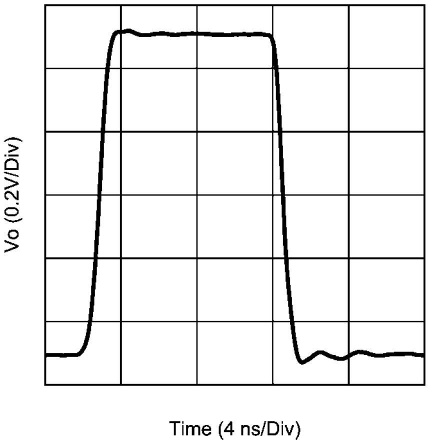
Large Signal Step Response



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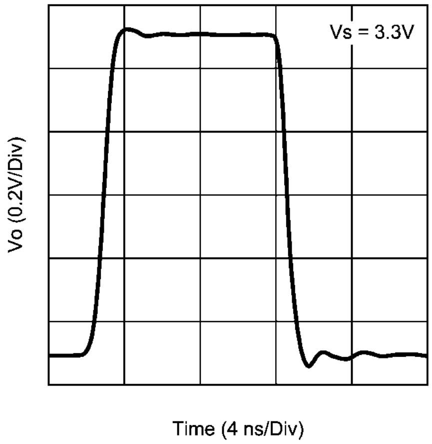
Large Signal Step Response



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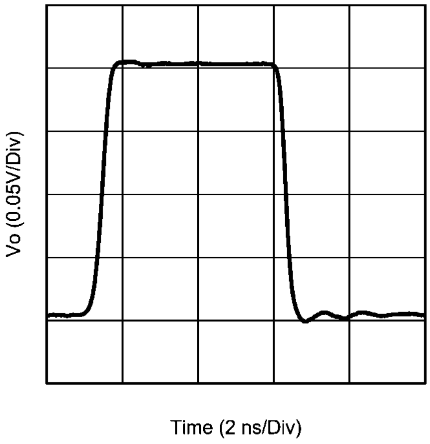
Small Signal Step Response



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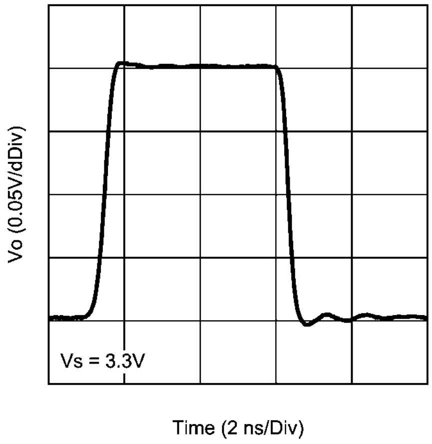
Small Signal Step Response



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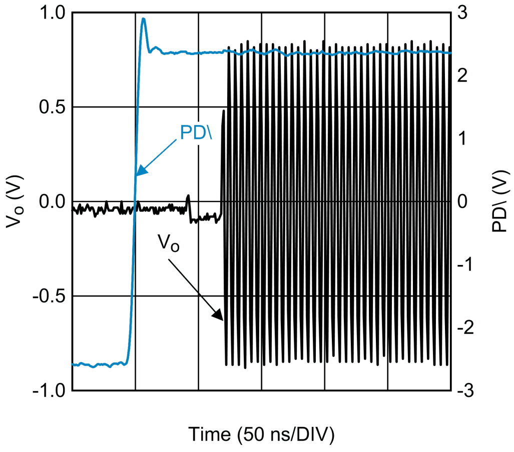
Turn-On Waveform



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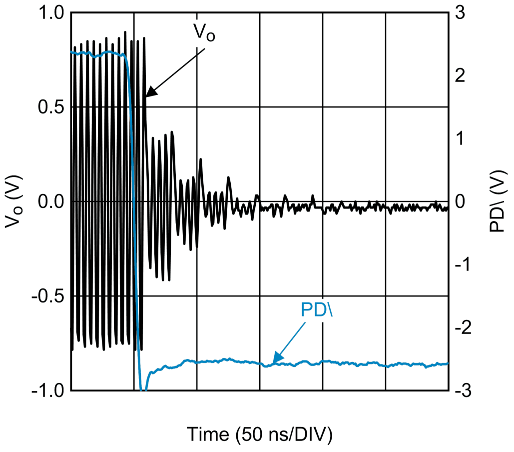
Turn-Off Waveform



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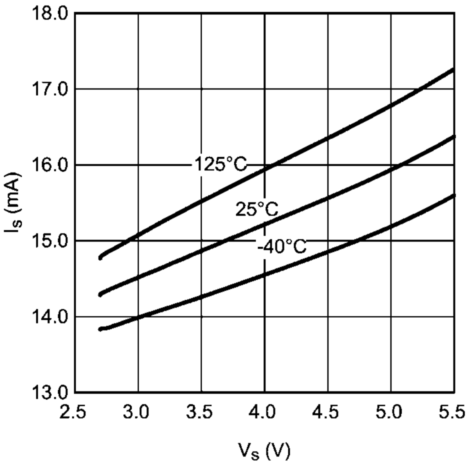
Supply Current vs. Supply Voltage



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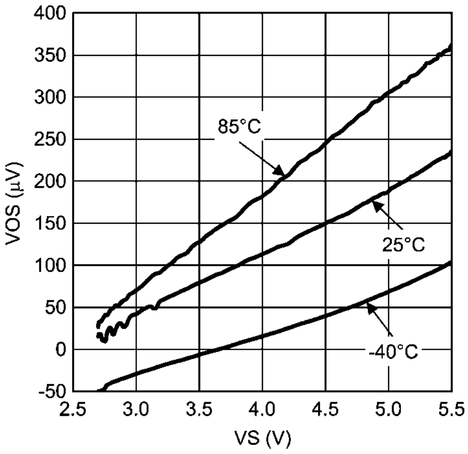
Offset Voltage vs. Supply Voltage (Typical Unit)



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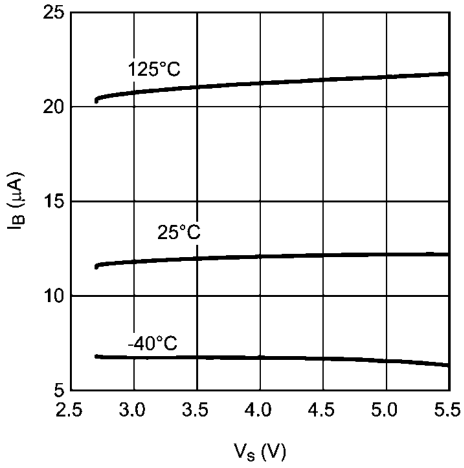
Input Bias Current vs. Supply Voltage (Typical Unit)



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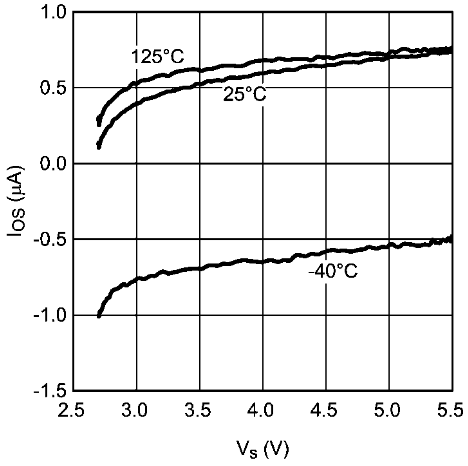
Input Offset Current vs. Supply Voltage (Typical Unit)



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Application Section

INTRODUCTION

The LMH6629 is a very wide gain bandwidth, ultra low-noise voltage feedback operational amplifier. The excellent noise and bandwidth enables applications such as medical diagnostic ultrasound, magnetic tape & disk storage and fiberoptics to achieve maximum high frequency signal-to-noise ratios. The following discussion will enable the proper selection of external components to achieve optimum system performance.

The LMH6629 has some additional features to allow maximum performance. As shown in *Figure 2* there are provisions for low power shut down and two internal compensation settings, which are further discussed below. Also provided is a feedback (FB) pin which allows the placement of the feedback resistor directly adjacent to the inverting input (IN-) pin. This pin simplifies board layout and minimizes the possibility of unwanted interaction between the feedback path and other circuit elements.

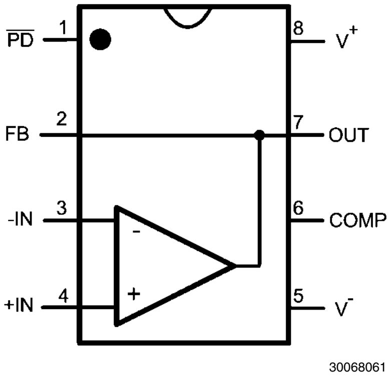

FIGURE 2. 8-Pin LLP Pinout Diagram

The LLP-8 package requires the bottom-side Die Attach Paddle (DAP) to be soldered to the circuit board for proper thermal dissipation and to get the thermal resistance number specified. The DAP is tied to the V^- potential within the LMH6629 package. Thus, the circuit board copper area devoted to DAP heatsinking connection should be at the V- potential as well. Please refer to the package drawing for the recommended land pattern and recommended DAP connection dimensions.

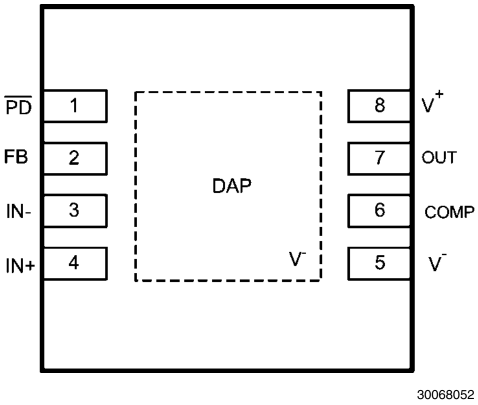

FIGURE 3. 8-Pin LLP SDA088AD (Top View)

CONTROL PINS

The LMH6629 has two digital control pins; $\overline{PD}$ and COMP pins. The $\overline{PD}$ pin, used for powerdown, floats high (on) when not driven. When the $\overline{PD}$ pin is pulled low, the amplifier is disabled and the amplifier output stage goes into a high impedance state so the feedback and gain set resistors determine the output impedance of the circuit. The other control pin, the COMP pin, allows control of the internal compensation and defaults to the lower gain mode or logic 0.

COMPENSATION

Nearly all high-speed operational amplifiers are now internally compensated. To use external compensation capacitors would compromise stability and performance due to bond wire and board parasitic reactances. The LMH6629 gives a degree of flexibility that was lost with on chip compensation. There are two compensation settings that can be controlled by the COMP pin. The default setting is set through an internal pull down resistor and places the COMP pin at the logic 0 state. In this configuration the on chip compensation is set to the maximum and bandwidth is reduced to enable stability at gains as low as 4V/V.

When this pin is driven to the logic 1 state the internal compensation is decreased to allow higher bandwidth at higher gains. In this state the minimum stable gain is 10V/V. Due to the reduced compensation slew rate and large signal bandwidth are significantly enhanced for the higher gains.

BIAS CURRENT CANCELLATION

The LMH6629 offers exceptional offset voltage accuracy. In order to preserve the low offset voltage errors, care must be taken to avoid voltage errors due to input bias currents. This is important in both inverting and non inverting applications.

The non-inverting circuit is used here as an example. To cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain setting (R_g) and feedback (R_f) resistors should equal the equivalent source resistance (R_{seq}) as defined in *Figure 4*. Combining this constraint with the non-inverting gain equation also seen in *Figure 4* allows both R_f and R_g to be determined explicitly from the following equations:

$$R_f = A_V R_{seq} \text{ and } R_g = R_f/(A_V-1)$$

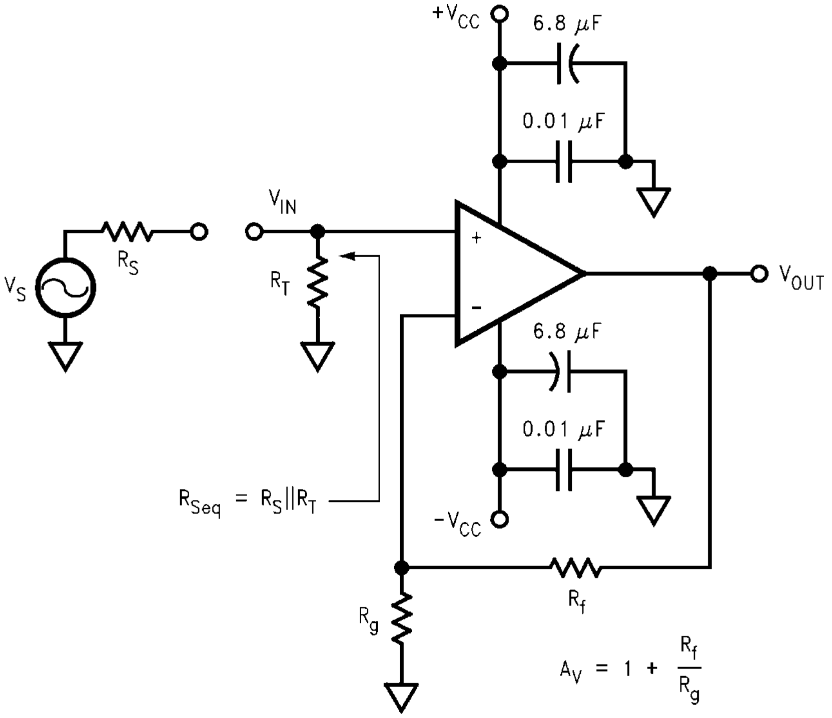

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FIGURE 4. Non-Inverting Amplifier Configuration

When driven from a 0Ω source, such as the output of an op amp, the non-inverting input of the LMH6629 should be isolated with at least a 25Ω series resistor.

As seen in *Figure 5*, bias current cancellation is accomplished for the inverting configuration by placing a resistor (R_b) on the non-inverting input equal in value to the resistance seen by the inverting input (R_f || (R_g+R_s)). R_b should to be no less than 25Ω for optimum LMH6629 performance. A shunt capacitor (not shown) can minimize the additional noise of R_b.

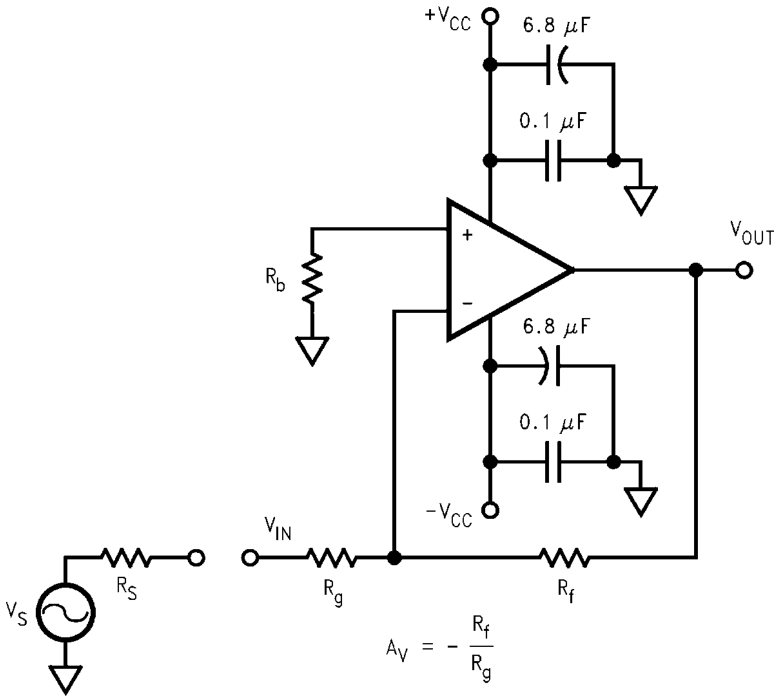

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FIGURE 5. Inverting Amplifier Configuration

TOTAL INPUT NOISE vs. SOURCE RESISTANCE

To determine maximum signal-to-noise ratios from the LMH6629, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary. *Figure 6* describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_n^+ = i_n^-$) source, there is also thermal voltage noise ($e_t = \sqrt{(4KTR)}$) associated with each of the external resistors.

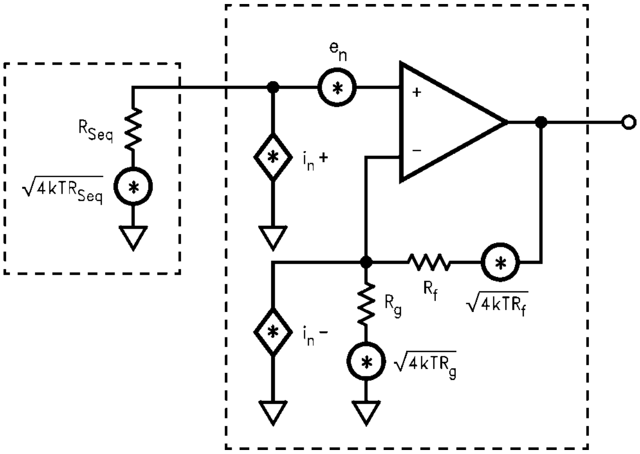

FIGURE 6. Non-Inverting Amplifier Noise Model

Equation 1 provides the general form for total equivalent input voltage noise density (e_{ni}).

$$e_{ni} = \sqrt{e_n^2 + \left(i_{n+}R_{Seq}\right)^2 + 4kTR_{Seq} + \left(i_{n-}\left(R_f||R_g\right)\right)^2 + 4kT\left(R_f||R_g\right)}$$

Equation 1: General Noise Equation (1)

Equation 2 is a simplification of *Equation 1* that assumes R_f || $R_g = R_{seq}$ for bias current cancellation:

$$e_{ni} = \sqrt{e_n^2 + 2(i_nR_{Seq})^2 + 4kT(2R_{Seq})}$$

Equation 2: Noise Equation with R_f || $R_g = R_{seq}$ (2)

Figure 7 schematically shows e_{ni} alongside V_{IN} (the portion of V_S source which reaches the non-inverting input of *Figure 4*) and external components affecting gain ($A_V = 1 + R_f / R_g$), all connected to an ideal noiseless amplifier.

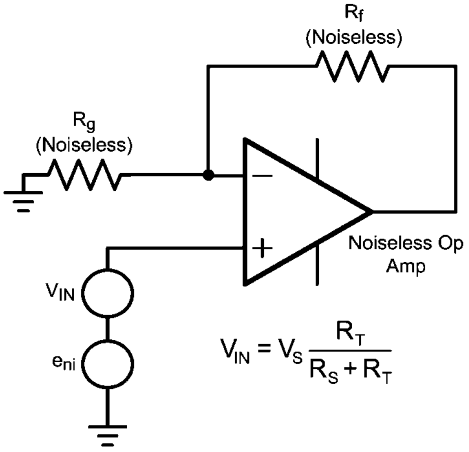

FIGURE 7. Non-Inverting Amplifier Equivalent Noise Source Schematic

Figure 8 illustrates the equivalent noise model using this assumption. *Figure 9* is a plot of e_{ni} against equivalent source resistance (R_{seq}) with all of the contributing voltage noise source of *Equation 2*. This plot gives the expected e_{ni} for a given (R_{seq}) which assumes $R_f||R_g = R_{seq}$ for bias current cancellation. The total equivalent output voltage noise (e_{no}) is e_{ni}*A_V.

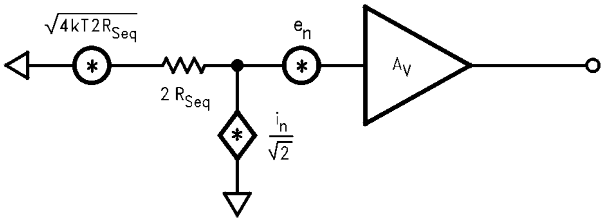

FIGURE 8. Noise Model with $R_f||R_g = R_{seq}$

As seen in *Figure 9*, e_{ni} is dominated by the intrinsic voltage noise (e_n) of the amplifier for equivalent source resistances below 15Ω. Between 15Ω and 2.5 kΩ, e_{ni} is dominated by the thermal noise ($e_t = \sqrt{(4kT(2R_{seq}))}$) of the equivalent source resistance R_{seq}; incidentally, this is the range of R_{seq} values where the LMH6629 has the best (lowest) Noise Figure (NF) for the case where $R_{seq} = R_f$ || R_g.

Above 2.5 kΩ, e_{ni} is dominated by the amplifier's current noise ($i_n = \sqrt{(2)}\ i_nR_{seq}$). When R_{seq} = 190Ω (i.e., $R_{seq} = e_n/\sqrt{(2)}\ i_n$), the contribution from voltage noise and current noise of LMH6629 is equal. For example, configured with a gain of +10V/V giving a –3dB of 825 MHz and driven from $R_{seq} = R_f||R_G$ = 20Ω (e_{ni} = 1.07 nV√Hz from *Figure 9*), the LMH6629 produces a total equivalent output noise voltage (e_{ni} * 10 V/V * √(1.57 * 825 MHz)) of 385 μV_{rms}.

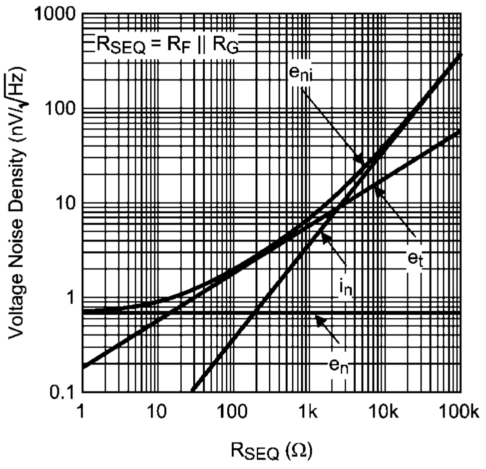

FIGURE 9. Voltage Noise Density vs. Source Resistance

If bias current cancellation is not a requirement, then $R_f \| R_g$ need not equal R_{seq}. In this case, according to *Equation 1*, $R_f \| R_g$ should be as low as possible to minimize noise. Results similar to *Equation 1* are obtained for the inverting configuration of *Figure 5* if R_{seq} is replaced by R_b and R_g is replaced by $R_g + R_s$. With these substitutions, *Equation 1* will yield an e_{ni} referred to the non-inverting input. Referring e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains $(1+R_g/R_f)$.

NOISE FIGURE

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10LOG\left\{\frac{S_i / N_i}{S_o / N_o}\right\} = 10LOG\left\{\frac{e_{ni}^2}{e_t^2}\right\}$$

Equation 3: General Noise Figure Equation (3)

Looking at the two parts of the NF expression (inside the log function) yields:

$S_i/S_o \rightarrow$ Inverse of the power gain provided by the amplifier

$N_o/N_i \rightarrow$ Total output noise power, including the contribution of R_S, divided by the noise power at the input due to R_S

To simplify this, consider N_a as the noise power added by the amplifier (reflected to its input port):

$S_i/S_o \rightarrow 1/G$

$N_o/N_i \rightarrow G * (N_i+N_a) / N_i$ (where $G*(N_i + N_a) = N_o$)

Substituting these two expressions into the NF expression:

$$NF = 10\log\left[\frac{1}{G}\left(\frac{G(N_i + N_a)}{N_i}\right)\right] = 10\log\left(1 + \frac{N_a}{N_i}\right)$$

Equation 4: Simplified Noise Figure Equation (4)

The noise figure expression has simplified to depend only on the ratio of the noise power added by the amplifier at its input (considering the source resistor to be in place but noiseless in getting N_a) to the noise power delivered by the source resistor (considering all amplifier elements to be in place but noiseless in getting N_i).

For a given amplifier with a desired closed loop gain, to minimize noise figure:

- Minimize $R_f \| R_g$
- Choose the Optimum R_S (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \approx e_n/i_n$$

Figure 10 is a plot of NF vs R_S with the circuit of *Figure 4* (R_f = 240Ω, A_V = +10V/V). The NF curves for both Unterminated (R_T = open) and Terminated systems ($R_T = R_S$) are shown. *Table 1* indicates NF for various source resistances including $R_S = R_{OPT}$.

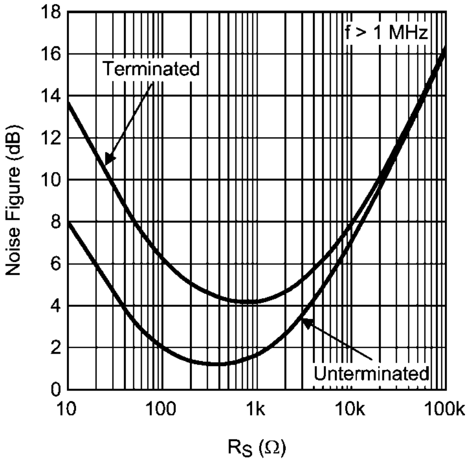

FIGURE 10. Noise Figure vs. Source Resistance

TABLE 1. Noise Figure for Various R_s

R_S (Ω)	NF (Terminated) (dB)	NF (Unterminated) (dB)
50	7.96	3.18
R_{OPT}	4.13 (R_{OPT} = 750Ω)	1.12 (R_{OPT} = 350Ω)

SINGLE SUPPLY OPERATION

The LMH6629 can be operated with single power supply as shown in *Figure 11*. Both the input and output are capacitively coupled to set the DC operating point.

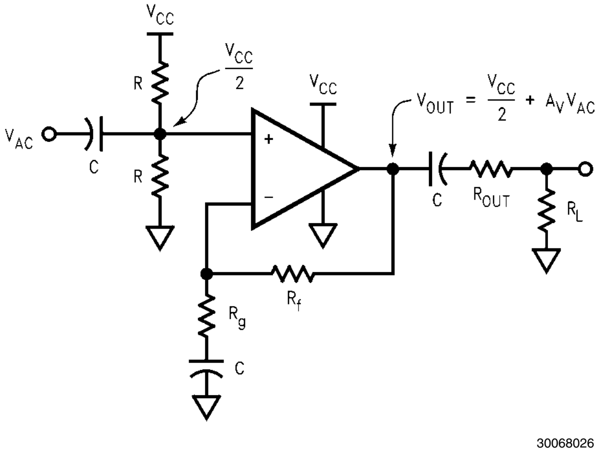

FIGURE 11. Single Supply Operation

LOW-NOISE TRANSIMPEDANCE AMPLIFIER

Figure 12 implements a high speed, single supply, low-noise Transimpedance amplifier commonly used with photodiodes. The transimpedance gain is set by R_F.

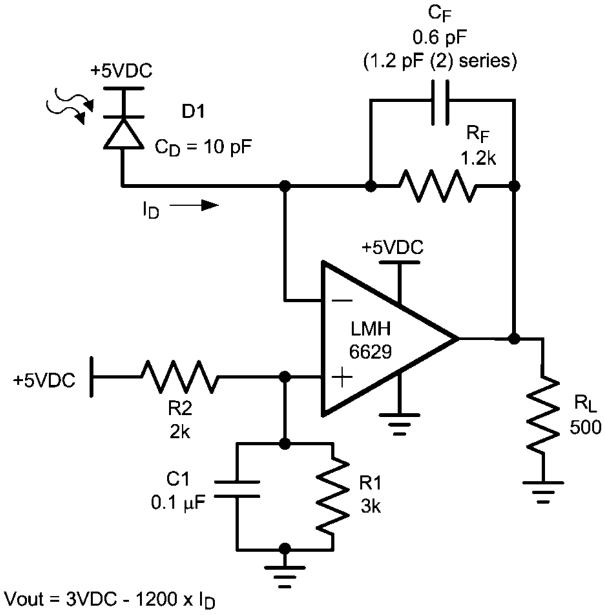

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FIGURE 12. 200MHz Transimpedance Amplifier Configuration

Figure 13 shows the Noise Gain (NG) and transfer function (I-V Gain). As with most Transimpedance amplifiers, it is required to compensate for the additional phase lag (Noise Gain zero at f_Z) created by the total input capacitance (C_D (diode capacitance) + C_{CM} (LMH6629 input capacitance)) looking into R_F; this is accomplished by placing C_F across R_F to create enough phase lead (Noise Gain pole at f_P) to stabilize the loop.

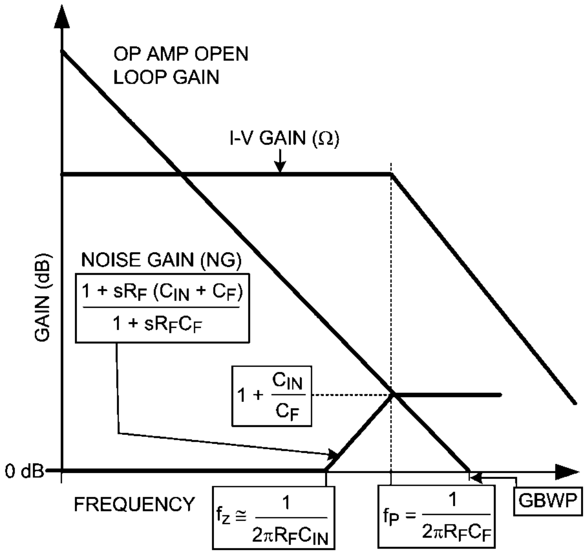

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FIGURE 13. Transimpedance Amplifier Noise Gain & Transfer Function

The optimum value of C_F is given by *Equation 5* resulting in the I-V -3dB bandwidth shown in *Equation 6*, or around 200MHz in this case (assuming GBWP= 4GHz with COMP pin = HI). This C_F value is a “starting point” and C_F needs to be tuned for the particular application as it is often less than 1pF and thus is easily affected by board parasitics, etc. For maximum speed, the LMH6629 COMP pin should be HI.

$$C_F = \sqrt{\frac{C_{IN}}{2\pi(GBWP)R_F}}$$

Equation 5: Optimum C_F Value (5)

$$f_{-3\,dB} \cong \sqrt{\frac{GBWP}{2\pi R_F C_{IN}}}$$

Equation 6: Resulting -3dB Bandwidth (6)

Equation 7 provides the total input current noise density (i_{ni}) equation for the basic Transimpedance configuration and is plotted against feedback resistance (R_F) showing all contributing noise sources in *Figure 14*. The plot indicates the expected total equivalent input current noise density (i_{ni}) for a given feedback resistance (R_F). This is depicted in the schematic of *Figure 15* where total equivalent current noise density (i_{ni}) is shown at the input of a noiseless amplifier and noiseless feedback resistor (R_F). The total equivalent output voltage noise density (e_{no}) is i_{ni}*R_F.

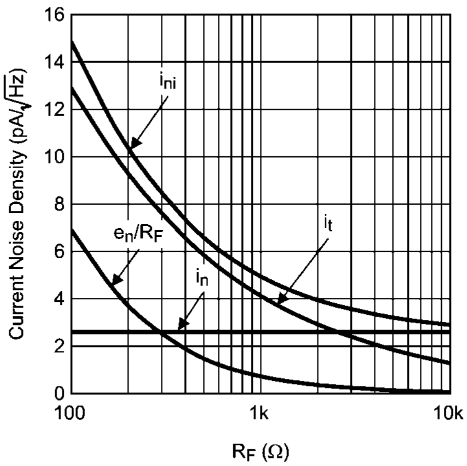

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FIGURE 14. Current Noise Density vs. Feedback Resistance

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_f}\right)^2 + \frac{4kT}{R_f}}$$

Equation 7: Noise Equation for Transimpedance Amplifier (7)

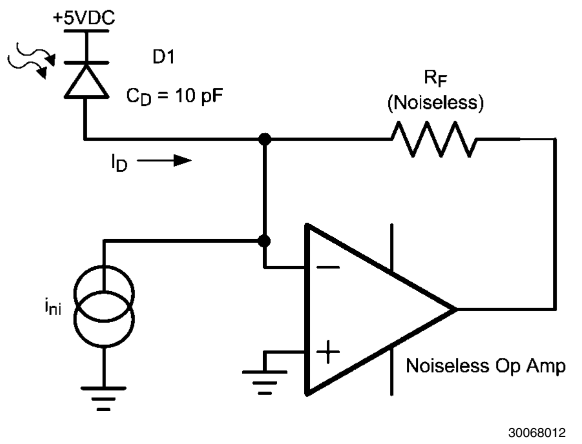


FIGURE 15. Transimpedance Amplifier Equivalent Input Source Model

From *Figure 14*, it is clear that with LMH6629's extremely low noise characteristics, for $R_F < 2.5k\Omega$, the noise performance is entirely dominated by R_F thermal noise. Only above this R_F threshold, LMH6629's input noise current (i_n) starts being a factor and at no R_F setting does the LMH6629 input noise voltage play a significant role. This noise analysis has ignored the possible noise gain increase, due to photo-diode capacitance, at higher frequencies.

LOW-NOISE INTEGRATOR

The LMH6629 implement a deBoo integrator shown in *Figure 16*. Positive feedback maintains integration linearity. The LMH6629's low input offset voltage and matched inputs allow bias current cancellation and provide for very precise integration. Keeping R_G and R_S low helps maintain dynamic stability.

$$V_O \cong V_{IN} \frac{K_O}{sR_SC} \quad ; \quad K_O = 1 + \frac{R_F}{R_G}$$

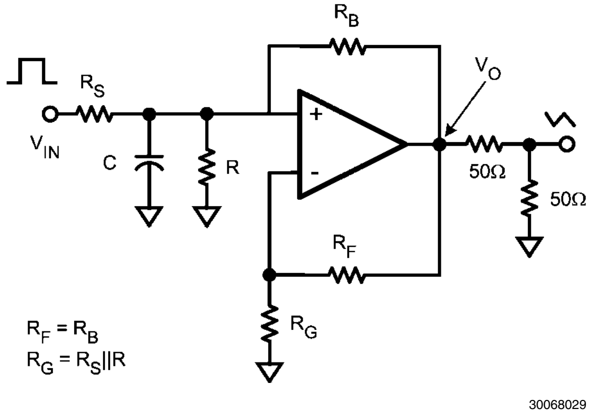
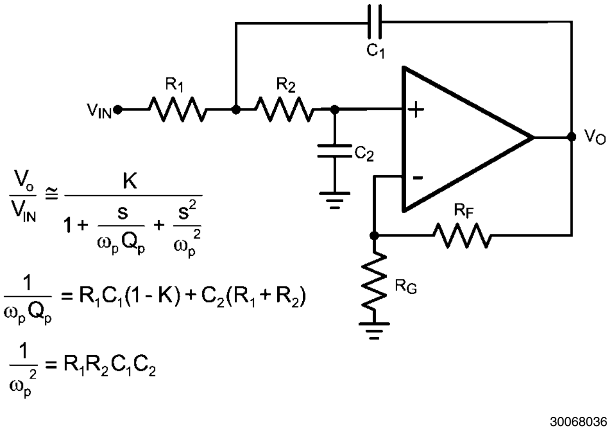


FIGURE 16. Noise Integrator

HIGH-GAIN SALLEN-KEY ACTIVE FILTERS

The LMH6629 is well suited for high-gain Sallen-Key type of active filters. *Figure 17* shows the 2nd order Sallen-Key low-pass filter topology. Using component predistortion methods discussed in OA-21 enables the proper selection of components for these high-frequency filters.



$$\frac{V_o}{V_{IN}} \cong \frac{K}{1 + \frac{s}{\omega_p Q_p} + \frac{s^2}{\omega_p^2}}$$

$$\frac{1}{\omega_p Q_p} = R_1C_1(1-K) + C_2(R_1+R_2)$$

$$\frac{1}{\omega_p^2} = R_1R_2C_1C_2$$

FIGURE 17. Low Pass Sallen-Key Active Filter Topology

LOW-NOISE MAGNETIC MEDIA EQUALIZER

The LMH6629 implement a high-performance low-noise equalizer for such application as magnetic tape channels as shown in *Figure 18*. The circuit combines an integrator (used to limit noise) with a bandpass filter (used to boost the response centered at a frequency or over a band of interest) to produce the low noise equalization. The circuit's simulated frequency response is illustrated in *Figure 19*.

In this circuit, the bandpass filter center frequency is set by

$$f_C = \frac{1}{2\pi\sqrt{LC}}$$

For higher selectivity, use high C values; for wider bandwidth, use high L values, while keeping the product of L and C values the same to keep f_c intact. The integrator's -3dB roll-off is set by

$$\frac{1}{2\pi C_1(R_1 + R)}$$

If

$$\frac{1}{2\pi C_1R_1} << f_C$$

the integrator and the bandpass filter frequency interaction is minimized so that the operating frequencies of each can be set independently. Lowering the value of R2 increases the bandpass gain (boost) without affecting the integrator frequencies. With the LMH6629's wide Gain Bandwidth (4GHz), the center frequency could be adjusted higher without worries about loop gain limitation. This increases flexibility in tuning the circuit.

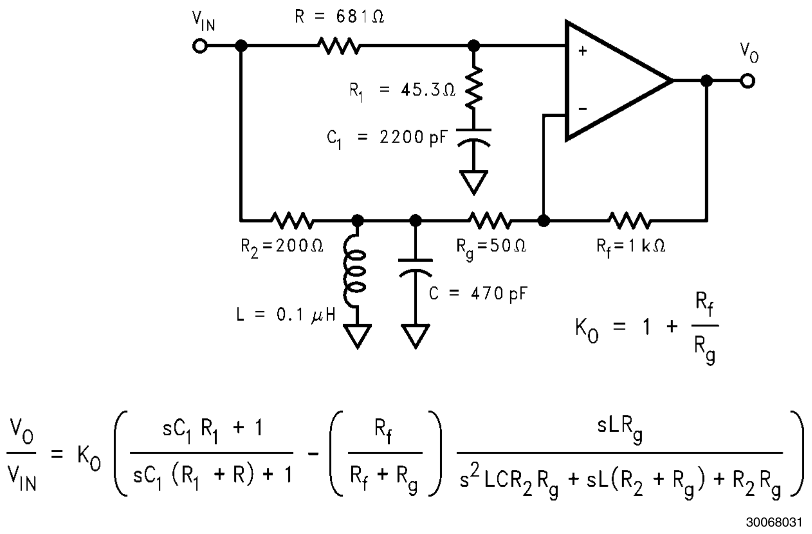


FIGURE 18. Low-Noise Magnetic Media Equalizer

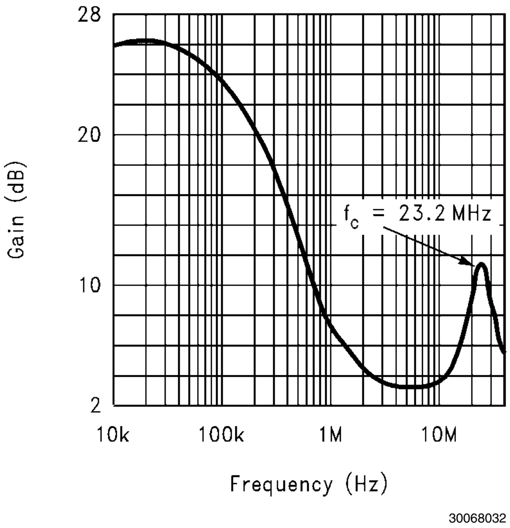


FIGURE 19. Equalizer Frequency Response

LAYOUT CONSIDERATIONS

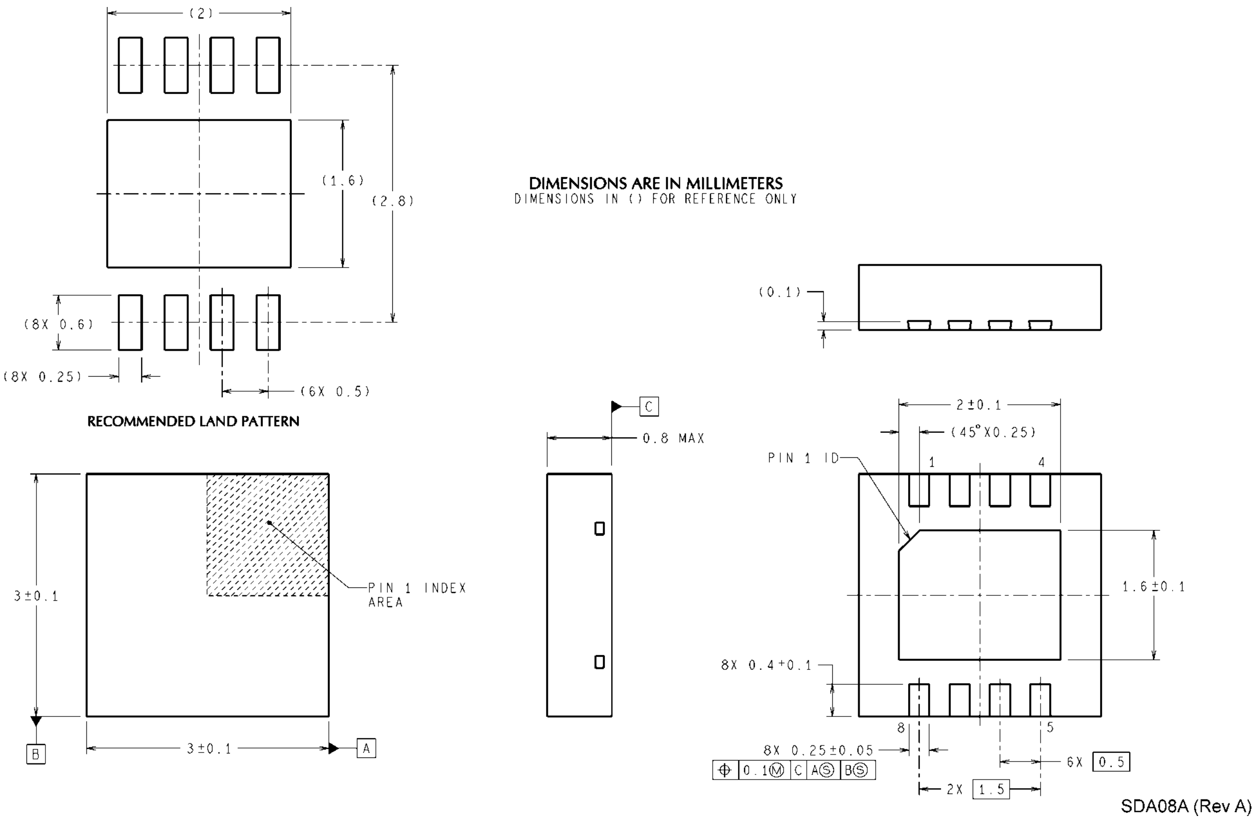
National Semiconductor suggests the copper patterns on the evaluation board(s) for this product. These board(s) are also useful as an aid in device testing and characterization. As is the case with all high-speed amplifiers, accepted-practice RF design technique on the PCB layout is mandatory. Generally, a good high frequency layout exhibits a separation of power supply and ground traces from the inverting input and output pins. Parasitic capacitances between these nodes and ground may cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). Use high-quality chip capacitors with values in the range of 1000 pF to 0.1F for power supply bypassing. One terminal of each chip capacitor is connected to the ground plane and the other terminal is connected to a point that is as close as possible to each supply pin as allowed by the manufacturer's design rules. In addition, connect a tantalum capacitor with a value between 4.7 μF and 10 μF in parallel with the chip capacitor.

Signal lines connecting the feedback and gain resistors should be as short as possible to minimize inductance and microstrip line effect. Place input and output termination resistors as close as possible to the input/output pins. Traces greater than 1 inch in length should be impedance matched to the corresponding load termination.

Symmetry between the positive and negative paths in the layout of differential circuitry should be maintained to minimize the imbalance of amplitude and phase of the differential signal.

Component value selection is another important parameter in working with high-speed/high-performance amplifiers. Choosing external resistors that are large in value compared to the value of other critical components will affect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These parasitic capacitors could either be inherent to the device or be a by-product of the board layout and component placement. Moreover, a large resistor will also add more thermal noise to the signal path. Either way, keeping the resistor values low will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation and high distortion.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin LLP
NS Package Number SDA08A

Notes

Notes

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Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
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