National Semiconductor

December 3, 2010

LMH6628QML

Dual Wideband, Low Noise, Voltage Feedback Op Amp

General Description

The National LMH6628 is a high speed dual op amp that offers a traditional voltage feedback topology featuring unity gain stability and slew enhanced circuitry. The LMH6628's low noise and very low harmonic distortion combine to form a wide dynamic range op amp that operates from a single (5V to 12V) or dual (±5V) power supply.

Each of the LMH6628's closely matched channels provides a 300MHz unity gain bandwidth and low input voltage noise density (2nV/$\sqrt{\text{Hz}}$). Low 2nd/3rd harmonic distortion (−65/−74dBc at 10MHz) make the LMH6628 a perfect wide dynamic range amplifier for matched I/Q channels.

With its fast and accurate settling (12ns to 0.1%), the LMH6628 is also an excellent choice for wide dynamic range, anti-aliasing filters to buffer the inputs of hi resolution analog-to-digital converters. Combining the LMH6628's two tightly matched amplifiers in a single package reduces cost and board space for many composite amplifier applications such as active filters, differential line drivers/receivers, fast peak detectors and instrumentation amplifiers.

The LMH6628 is fabricated using National's VIP10™ complimentary bipolar process.

To reduce design times and assist in board layout, the LMH6628 is supported by an evaluation board (CLC730036).

Features

- Available with radiation guraranteed 300 krad(Si)
- Wide unity gain bandwidth: 300MHz
- Low noise: 2nV/$\sqrt{\text{Hz}}$
- Low Distortion: −65/−74dBc (10MHz)
- Settling time: 12ns to 0.1%
- Wide supply voltage range: ±2.5V to ±6V
- High output current: ±85mA
- Improved replacement for CLC428

Applications

- High speed dual op amp
- Low noise integrators
- Low noise active filters
- Driver/receiver for transmission systems
- High speed detectors
- I/Q channel amplifiers

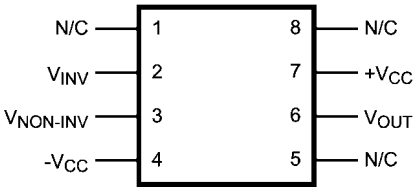
Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
LMH6628J-QMLV	5962-0254501VPA	J08A	8LD CERDIP
LMH6628WG-QML	5962-0254501MZA	WG10A	10LD CERAMIC SOIC
LMH6628WGFQMLV	5962-0254501VZA 300 krad(Si)	WG10A	10LD CERAMIC SOIC

VIP10™ is a trademark of National Semiconductor Corporation.

Connection Diagrams

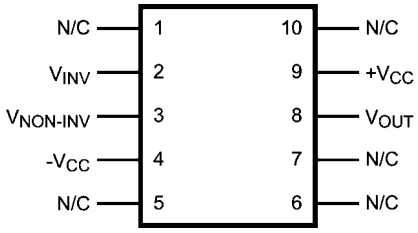
8 Lead Cerdip (J)



20151549

Top View
See NS Package Number J08A

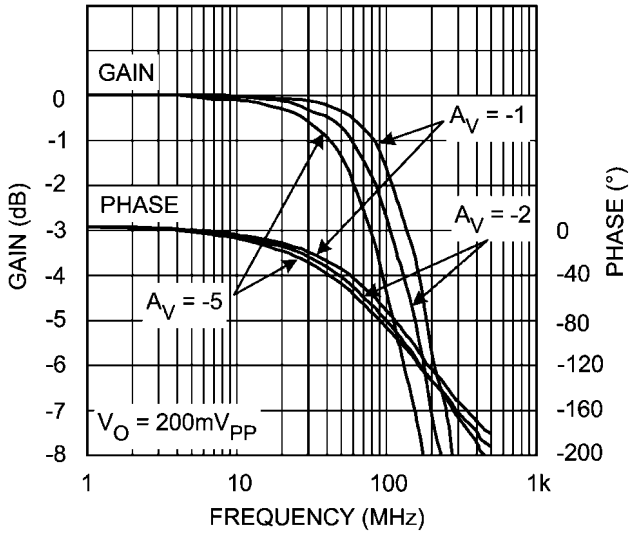
10 Lead Ceramic SOIC (WG)



20151550

Top View
See NS Package Number WG10A

Inverting Frequency Response



20151515

Absolute Maximum Ratings (*Note 1*)

Supply Voltage	$\pm 7V_{DC}$
Maximum Junction temperature (*Note 2*)	+175°C
Lead temperature (Soldering, 10 seconds)	+300°C
Differential input voltage	$V^+ - V^-$
Common mode input voltage	$V^+ - V^-$
Storage temperature range	$-65°C \leq T_A \leq +150°C$
Power Dissipation (*Note 2*)	1.0W
Short circuit current (*Note 3*)	
Thermal Resistance	
θ_{JA}	
Cerdip (Still Air)	135°C/W
Cerdip (500LF/Min Air Flow)	75°C/W
Ceramic SOIC (Still Air)	200°C/W
Ceramic SOIC (500LF/Min Air Flow)	145°C/W
θ_{JC}	
Cerdip	30°C/W
Ceramic SOIC	19°C/W
Package Weight (typical)	
Cerdip	TBD
Ceramic SOIC	TBD
ESD Tolerance (*Note 4*)	4000V

Maximum Operating Ratings

Supply Voltage	±2.5V to ±6.0V
Ambient Operating Temperture Range	$-55°C \leq T_A \leq +125°C$

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

LMH6628QML Electrical Characteristics

DC Parameters Static and DC Tests

The following conditions apply, unless otherwise specified.

V_{CC} = +5V_{DC}, A_V = +2V, R_L = 100Ω, R_F = 100Ω, −55°C ≤ T_A ≤ +125°C

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_B	Input Bias Current		(*Note 7*)	-10	+10	µA	1
				-20	+20	µA	2
				-20	+20	µA	3
V_{IO}	Input Offset Voltage		(*Note 7*)	-2	+2	mV	1
				-2.6	+2.6	mV	2, 3
I_{CC}	Supply Current	R_L = ∞	(*Note 7*)		24	mA	1
					24	mA	2
					25	mA	3
PSRR	Power Supply Rejection Ratio	+V_S = +4.0V to +5.0V, -V_S = -4.0V to -5.0V		60		dB	1
				55		dB	2, 3
V_{OUT}	Output Voltage Range	R_L = ∞		-5.0	+5.0	V	1, 2, 3

AC Parameters Frequency Domain Response

The following conditions apply, unless otherwise specified.

V_{CC} = +5V_{DC}, A_V = +2V, R_L = 100Ω, R_F = 100Ω, −55°C ≤ T_A ≤ +125°C

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
SSBW	Small Signal Bandwith	-3 dB BW, V_O < 0.5 V_{PP}	(*Note 6*)	50		MHz	4
GFP	Gain Flatness Peaking	0.1 MHz to 200 MHz, V_O ≤0.5 V_{PP}	(*Note 6*)		0.6	dB	4
GFR	Gain Flatness Rolloff	0.1 MHz to 20 MHz, V_O ≤0.5 V_{PP}	(*Note 6*)		0.6	dB	4
A_{OL}	Open Loop Gain		(*Note 6*)	55		dB	4

AC Parameters Distortion and Noise Tests

The following conditions apply, unless otherwise specified.

V_{CC} = +5V_{DC}, A_V = +2V, R_L = 100Ω, R_F = 100Ω, −55°C ≤ T_A ≤ +125°C

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
HD_2	Second Harmonic Distortion	1 V_{PP}at10 MHz	(*Note 6*)		50	dBc	4
HD_3	Third Harmonic Distortion	1 V_{PP}at10 MHz	(*Note 6*)		60	dBc	4

DC Parameters Drift Values

The following conditions apply, unless otherwise specified.

Deltas not required on B Level product. Deltas required for S Level product at Group B5 only, or as specified on the Internal Processing Instructions (IPI).

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_B	Input Bias Current		(*Note 5*)	-1.0	+1.0	µA	1
V_{IO}	Input Offset Voltage		(*Note 5*)	-0.2	+0.2	mV	1
I_{CC}	Supply Current	R_L = ∞	(*Note 5*)	-1	+1	mA	1

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 160mA.

Note 4: Human body model, 1.5kΩ in series with 100pF.

Note 5: If not tested, shall be guaranteed to the limits specified in table 1

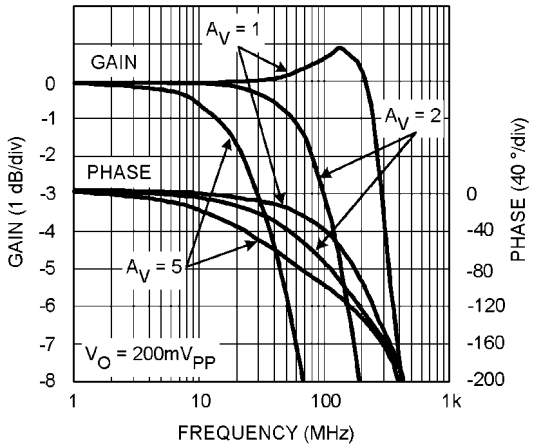
Note 6: Group A testing only.

Note 7: Pre and post irradiation limits are identical to those listed under electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019.

Typical Performance Characteristics

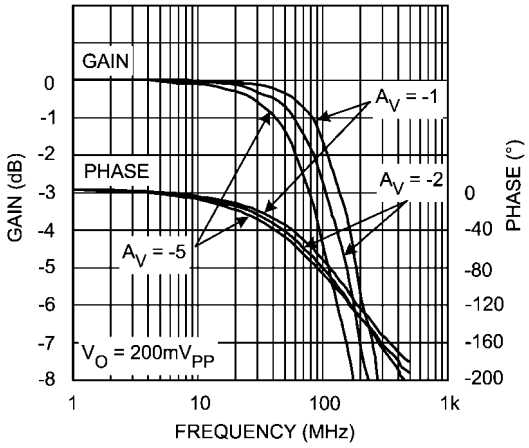
(T_A = +25°, A_V = +2, V_{CC} = ±5V, R_F =100Ω, R_L = 100Ω, unless specified)

Non-Inverting Frequency Response



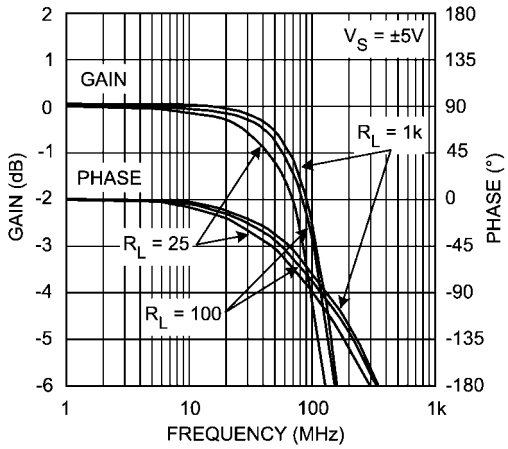
20151513

Inverting Frequency Response



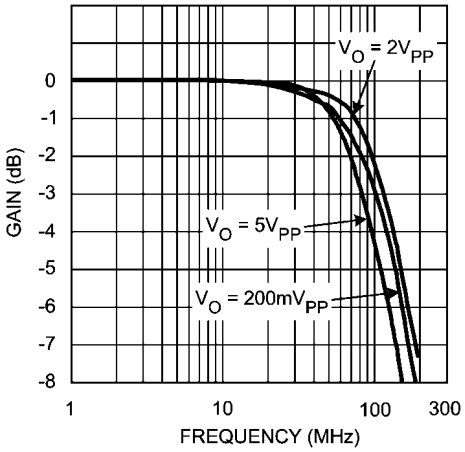
20151515

Frequency Response vs. Load Resistance



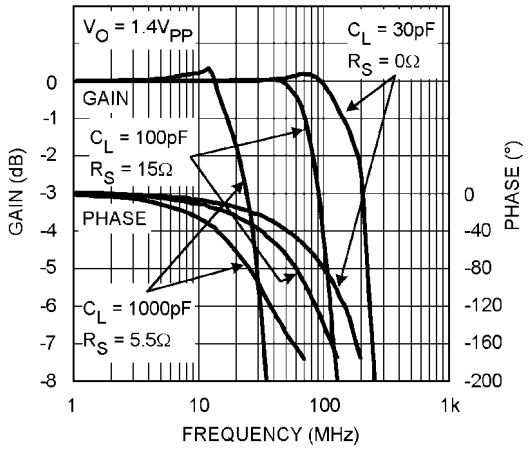
20151525

Frequency Response vs. Output Amplitude



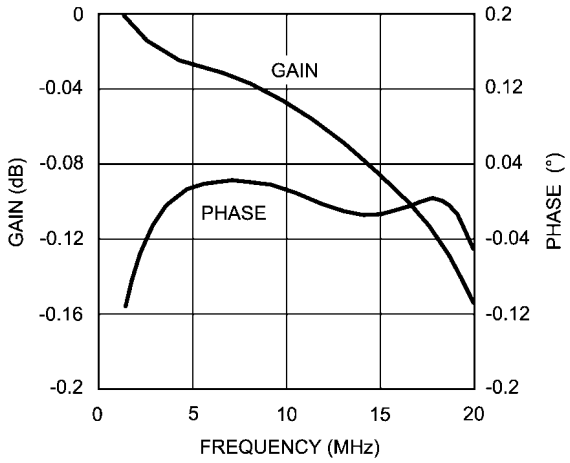
20151510

Frequency Response vs. Capacitive Load



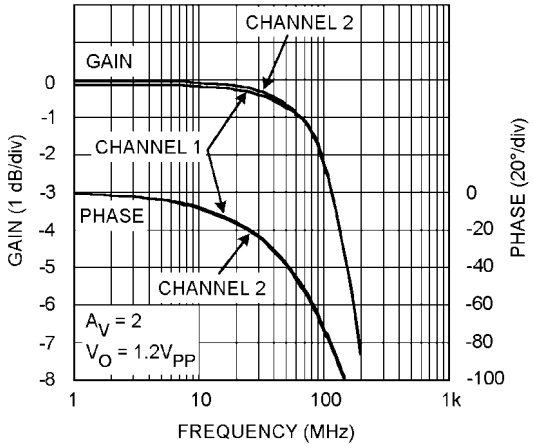
20151516

Gain Flatness & Linear Phase



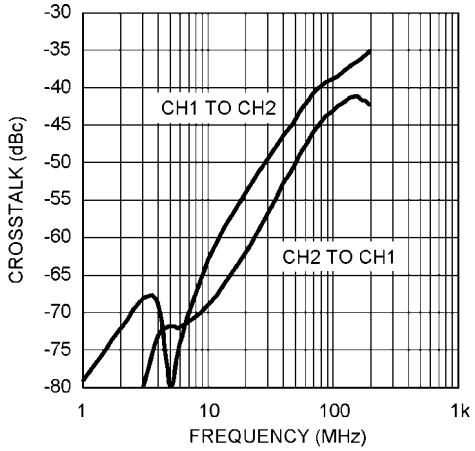
20151524

Channel Matching



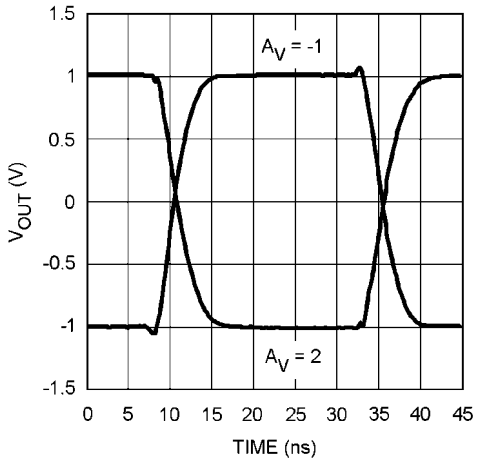
20151514

Channel to Channel Crosstalk



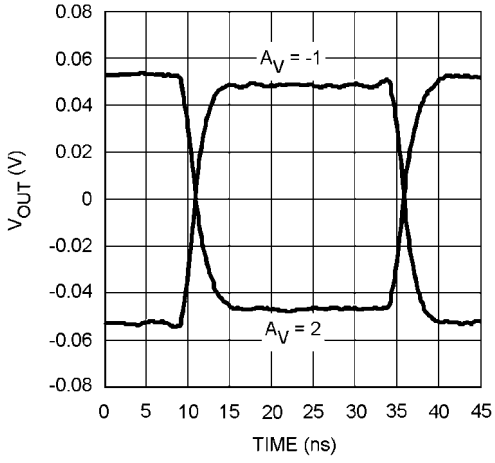
20151509

Pulse Response (V_O = 2V)



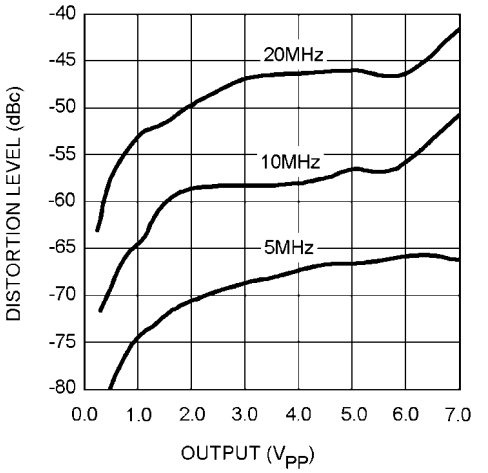
20151511

Pulse Response (V_O = 100mV)



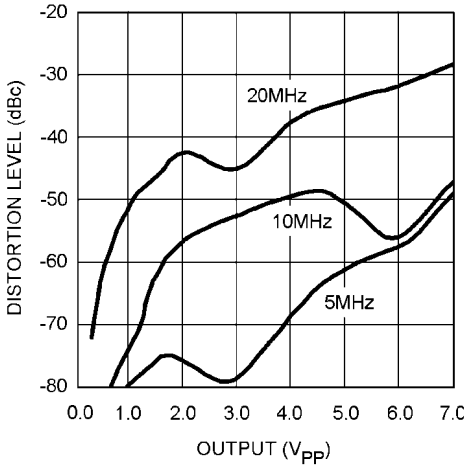
20151512

2nd Harmonic Distortion vs. Output Voltage



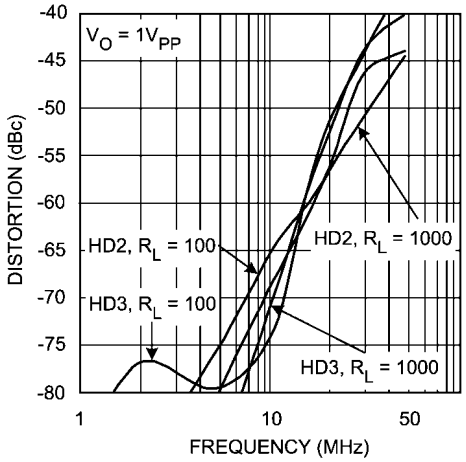
20151507

3rd Harmonic Distortion vs. Output Voltage



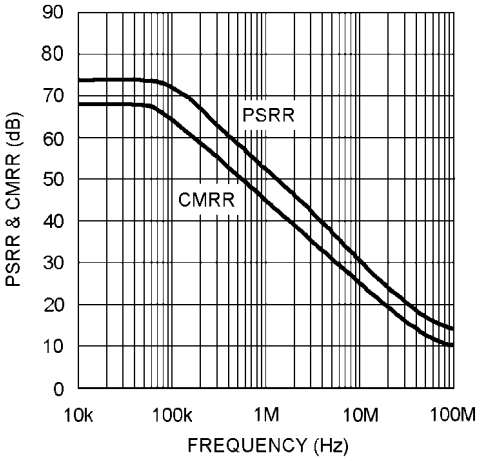
20151508

2nd & 3rd Harmonic Distortion vs. Frequency



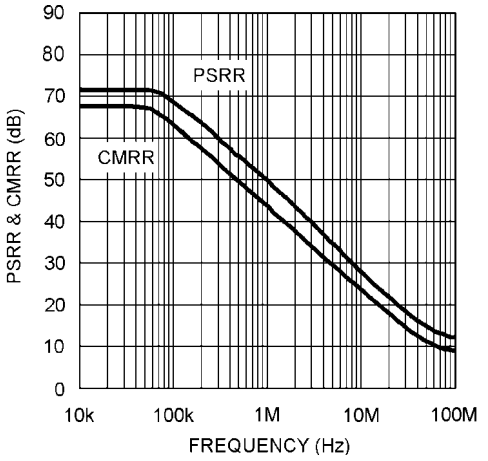
20151517

PSRR and CMRR (±5V)



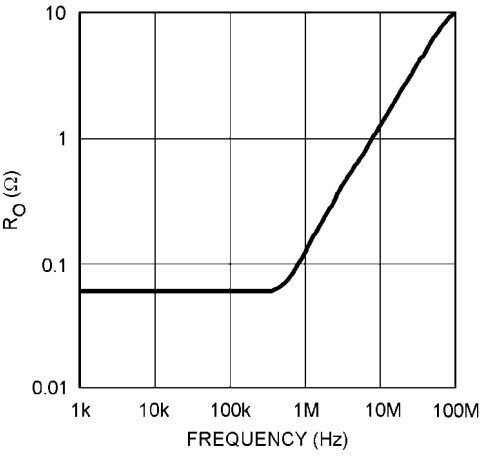
20151522

PSRR and CMRR (±2.5V)



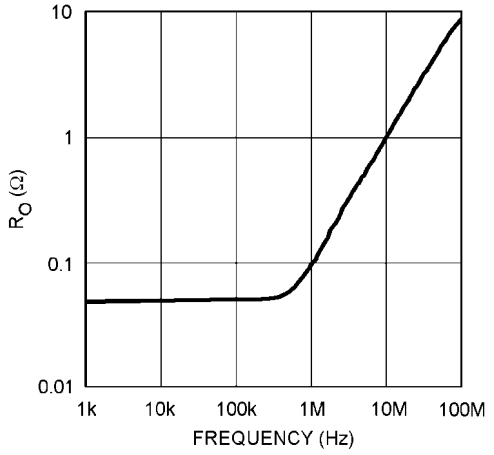
20151523

Closed Loop Output Resistance (±2.5V)



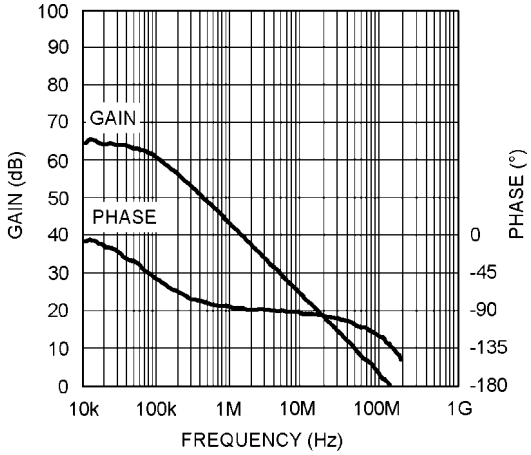
20151518

Closed Loop Output Resistance (±5V)



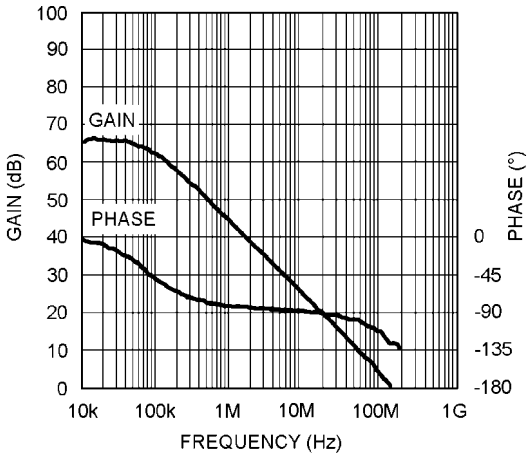
20151519

Open Loop Gain & Phase (±2.5V)



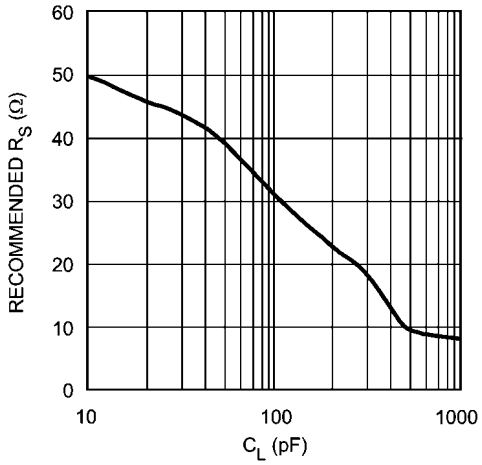
20151521

Open Loop Gain & Phase (±5V)



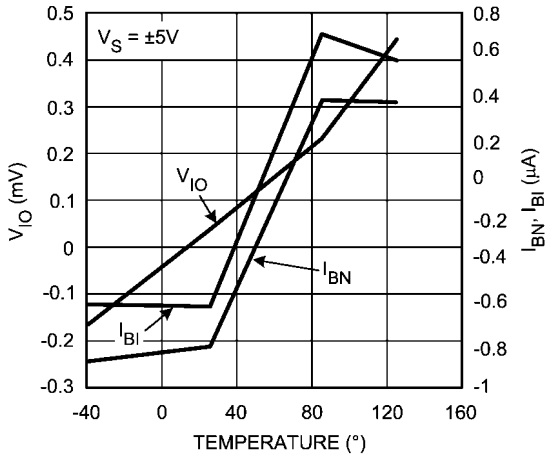
20151520

Recommended R_S vs. C_L



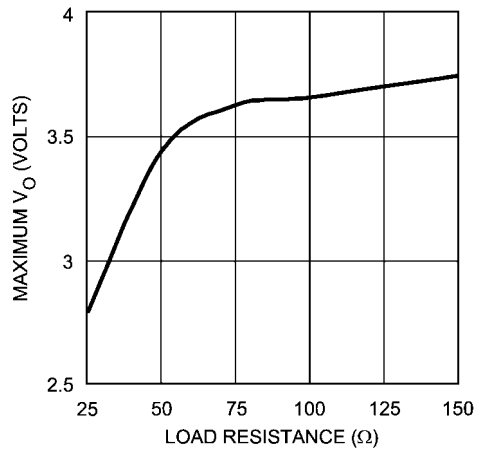
20151526

DC Errors vs. Temperature



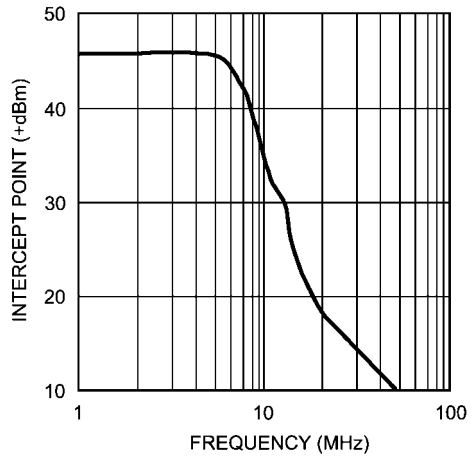
20151546

Maximum V_O vs. R_L



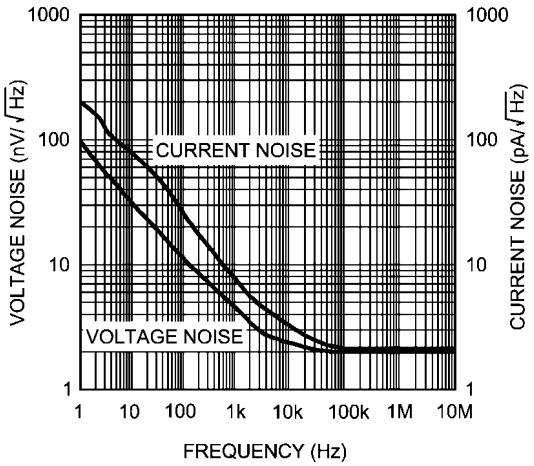
20151545

2-Tone, 3rd Order Intermodulation Intercept



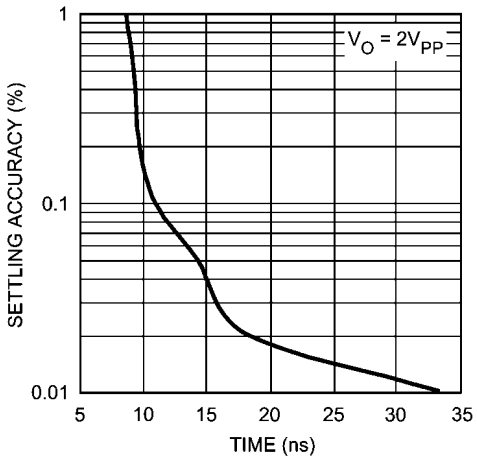
20151544

Voltage & Current Noise vs. Frequency



20151547

Settling Time vs. Accuracy



20151548

Application Section

LOW NOISE DESIGN

Ultimate low noise performance from circuit designs using the LMH6628 requires the proper selection of external resistors. By selecting appropriate low valued resistors for R_F and R_G, amplifier circuits using the LMH6628 can achieve output noise that is approximately the equivalent voltage input noise of 2nV/$\sqrt{Hz}$ multiplied by the desired gain (A_V).

DC BIAS CURRENTS AND OFFSET VOLTAGES

Cancellation of the output offset voltage due to input bias currents is possible with the LMH6628. This is done by making the resistance seen from the inverting and non-inverting inputs equal. Once done, the residual output offset voltage will be the input offset voltage (V_{OS}) multiplied by the desired gain (A_V). National Application Note OA-7 offers several solutions to further reduce the output offset.

OUTPUT AND SUPPLY CONSIDERATIONS

With ±5V supplies, the LMH6628 is capable of a typical output swing of ±3.8V under a no-load condition. Additional output swing is possible with slightly higher supply voltages. For loads of less than 50Ω, the output swing will be limited by the LMH6628's output current capability, typically 85mA.

Output settling time when driving capacitive loads can be improved by the use of a series output resistor. See the plot labeled "R_S vs. C_L" in the Typical Performance section.

LAYOUT

Proper power supply bypassing is critical to insure good high frequency performance and low noise. De-coupling capacitors of 0.1µF should be placed as close as possible to the power supply pins. The use of surface mounted capacitors is recommended due to their low series inductance.

A good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitance from these nodes to ground causes frequency response peaking and possible circuit oscillation. See OA-15 for more information. National suggests the 730036 (SOIC) dual op amp evaluation board as a guide for high frequency layout and as an aid in device evaluation.

ANALOG DELAY CIRCUIT (ALL-PASS NETWORK)

The circuit in *Figure 1* implements an all-pass network using the LMH6628. A wide bandwidth buffer (LM7121) drives the circuit and provides a high input impedance for the source. As shown in *Figure 2*, the circuit provides a 13.1ns delay (with R = 40.2Ω, C = 47pF). R_F and R_G should be of equal and low value for parasitic insensitive operation.

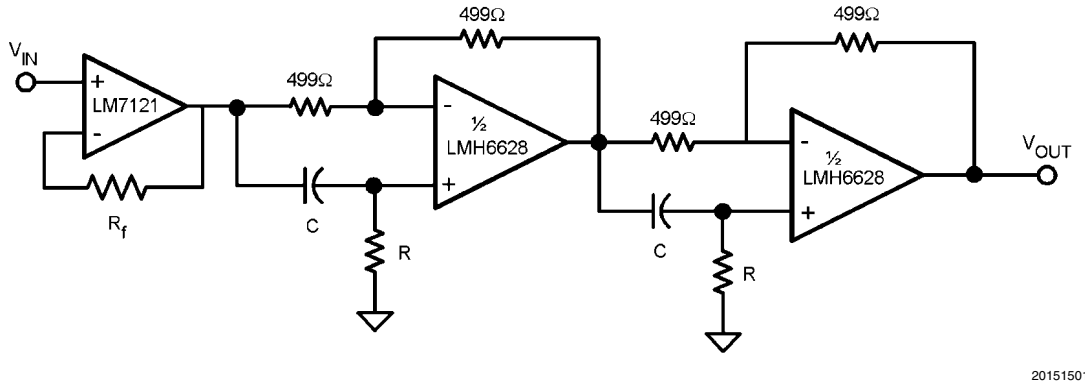


FIGURE 1.

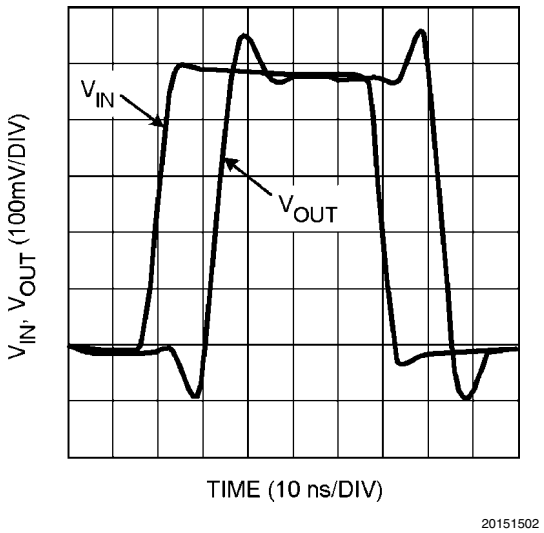


FIGURE 2. Delay Circuit Response to 0.5V Pulse

The circuit gain is +1 and the delay is determined by the following equations.

$$\tau_{delay} = 2(2RC + T_d) \quad (1)$$

$$T_d = \frac{1}{360}\frac{d\phi}{df}; \quad (2)$$

where T_d is the delay of the op amp at A_V = +1.

The LMH6628QML provides a typical delay of 2.8ns at its −3dB point.

FULL DUPLEX DIGITAL OR ANALOG TRANSMISSION

Simultaneous transmission and reception of analog or digital signals over a single coaxial cable or twisted-pair line can reduce cabling requirements. The LMH6628's wide bandwidth and high common-mode rejection in a differential amplifier configuration allows full duplex transmission of video, telephone, control and audio signals.

In the circuit shown in *Figure 3*, one of the LMH6628's amps is used as a "driver" and the other as a difference "receiver" amplifier. The output impedance of the "driver" is essentially

zero. The two R's are chosen to match the characteristic impedance of the transmission line. The "driver" op amp gain can be selected for unity or greater.

Receiver amplifier A_2 (B_2) is connected across R and forms differential amplifier for the signals transmitted by driver A_2 (B_2). If R_F equals R_G, receiver A_2 (B_1) will then reject the signals from driver A_1 (B_1) and pass the signals from driver B_1 (A_1).

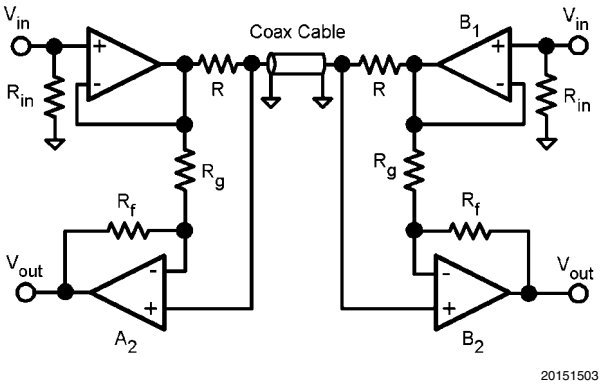


FIGURE 3.

The output of the receiver amplifier will be:

$$V_{out_{A(B)}} = \frac{1}{2} V_{in_{A(B)}} \left[1 - \frac{R_f}{R_g}\right] + \frac{1}{2} V_{in_{B(A)}} \left[1 + \frac{R_f}{R_g}\right] \quad (3)$$

Care must be given to layout and component placement to maintain a high frequency common-mode rejection. The plot of *Figure 4* shows the simultaneous reception of signals transmitted at 1MHz and 10MHz.

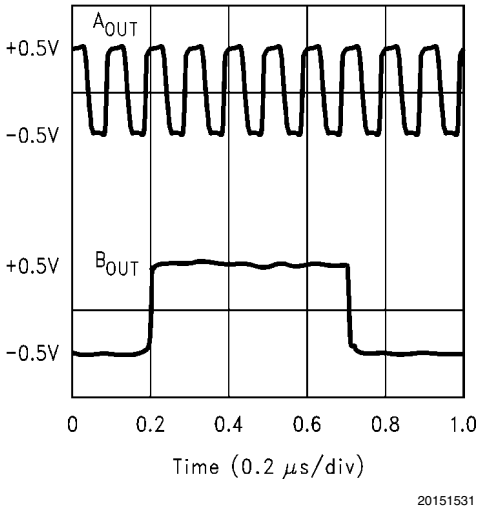


FIGURE 4.

POSITIVE PEAK DETECTOR

The LMH6628's dual amplifiers can be used to implement a unity-gain peak detector circuit as shown in *Figure 5*.

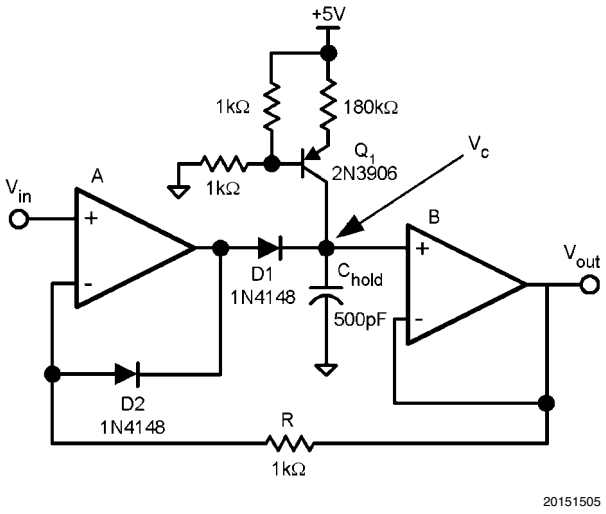


FIGURE 5.

The acquisition speed of this circuit is limited by the dynamic resistance of the diode when charging C_{hold}. A plot of the circuit's performance is shown in *Figure 6* with a 1MHz sinusoidal input.

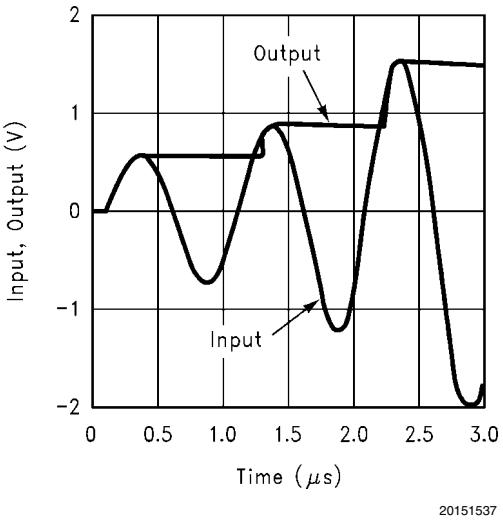


FIGURE 6.

A current source, built around Q1, provides the necessary bias current for the second amplifier and prevents saturation when power is applied. The resistor, R, closes the loop while diode D2 prevents negative saturation when V_{IN} is less than V_C. A MOS-type switch (not shown) can be used to reset the capacitor's voltage.

The maximum speed of detection is limited by the delay of the op amps and the diodes. The use of Schottky diodes will provide faster response.

ADJUSTABLE OR BANDPASS EQUALIZER

A "boost" equalizer can be made with the LMH6628 by summing a bandpass response with the input signal, as shown in *Figure 7*.

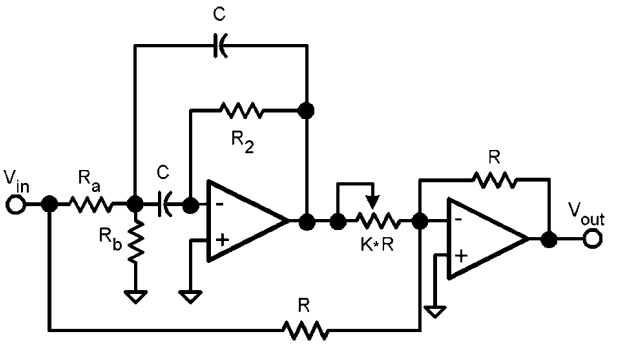


FIGURE 7.

The overall transfer function is shown in Eq. 5.

$$\frac{V_{out}}{V_{in}} = \left[\frac{R_b}{K(R_a + R_b)}\right] \frac{s2Q\omega_o}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \quad -1 \tag{4}$$

To build a boost circuit, use the design equations Eq. 6 and Eq. 7.

$$\frac{R_2 C}{2} = \frac{Q}{\omega_o} \tag{5}$$

$$2C\,(R_a \| R_b) = \frac{1}{Q\omega_o} \tag{6}$$

Select R_2 and C using Eq. 6. Use reasonable values for high frequency circuits - R_2 between 10Ω and 5kΩ, C between 10pF and 2000pF. Use Eq. 7 to determine the parallel combination of R_a and R_b. Select R_a and R_b by either the 10Ω to 5kΩ criteria or by other requirements based on the impedance V_{in} is capable of driving. Finish the design by determining the value of K from Eq. 8.

$$\text{Peak Gain} = \frac{V_{out}}{V_{in}}(\omega_o) = \frac{R_2}{2KR_a} \quad -1 \tag{7}$$

Figure 8 shows an example of the response of the circuit of Figure 9, where f_o is 2.3MHz. The component values are as follows: R_a=2.1kΩ, R_b = 68.5Ω, R_2 = 4.22kΩ, R = 500Ω, KR = 50Ω, C = 120pF.

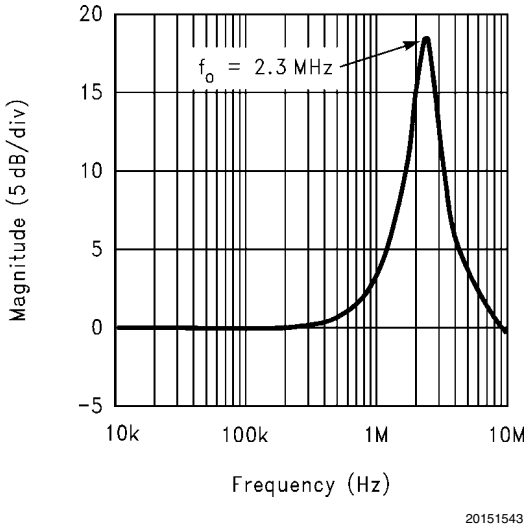
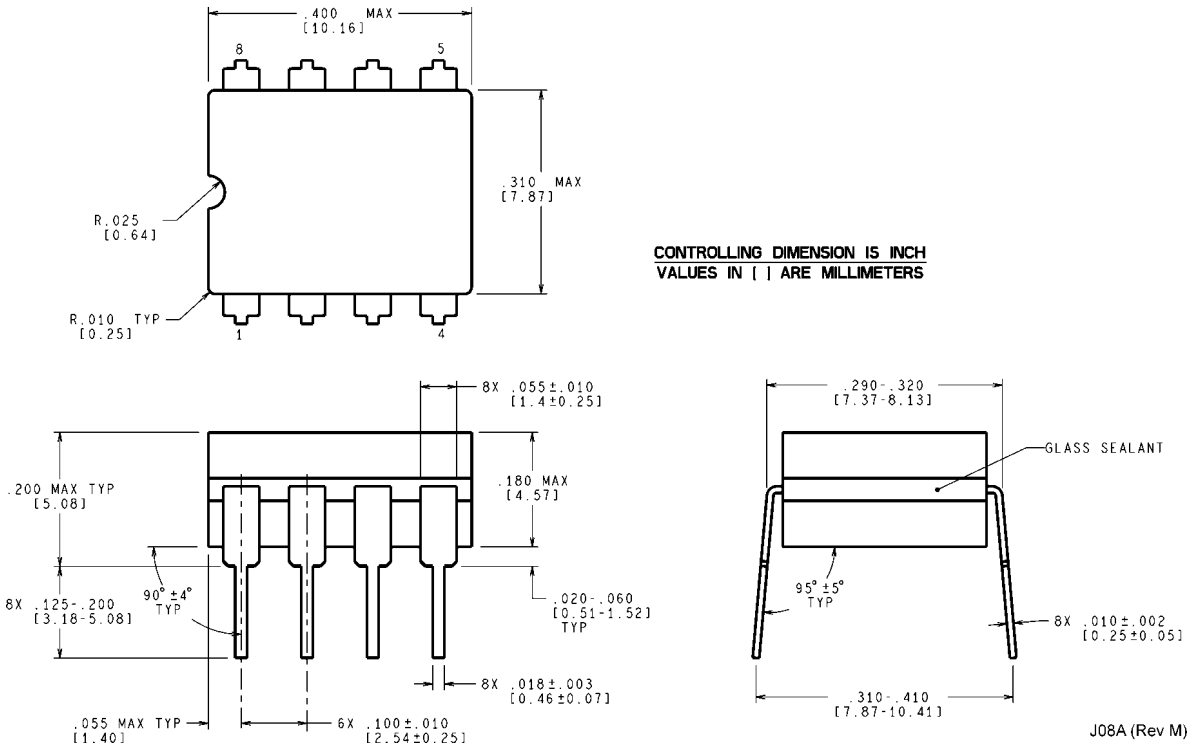


FIGURE 8.

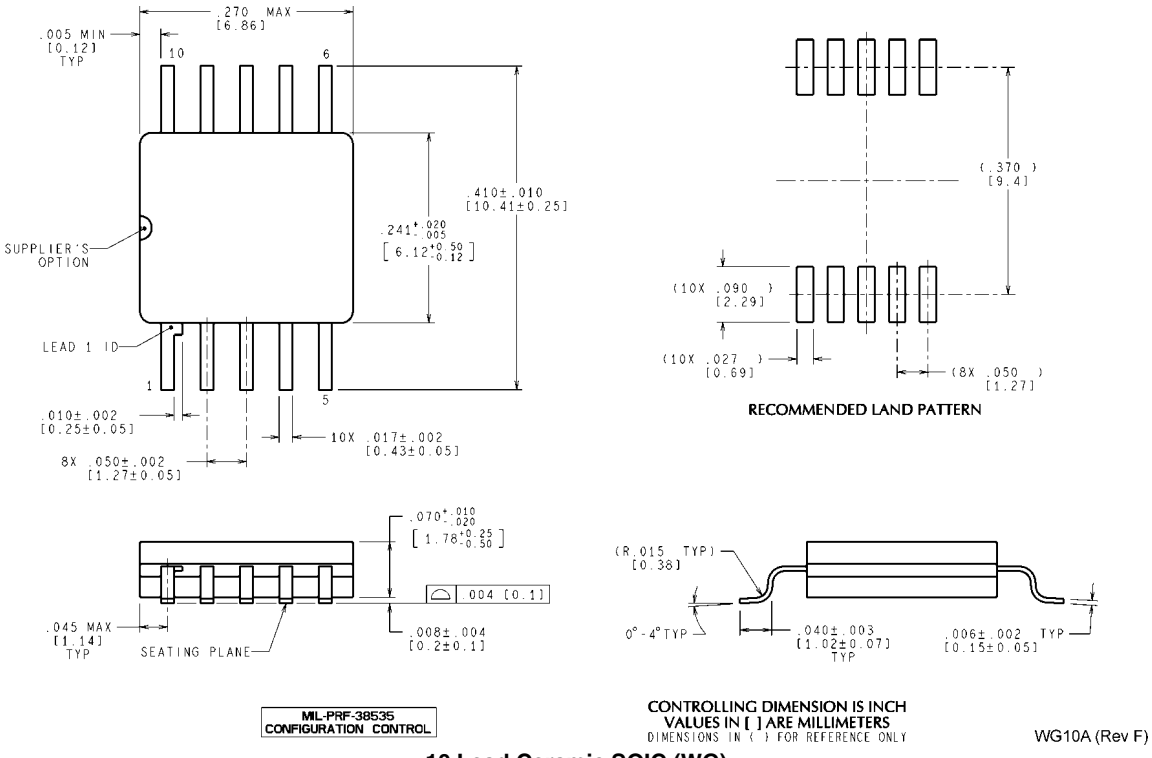
Revision History

Date Released	Revision	Section	Changes
12/03/2010	A	New Corporate Format Release	1 MDS data sheet converted into a Corp. data sheet format. Following MDS data sheet will be Archived MNLMH6628-X-RH, Rev. 0A0

Physical Dimensions inches (millimeters) unless otherwise noted



8 Lead Cerdip (J)
NS Package Number J08A



10 Lead Ceramic SOIC (WG)
NS Package Number WG10A

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at: www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

For the most current product information visit us at www.national.com

National Semiconductor Americas Technical Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com