National Semiconductor

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LMH6642/LMH6643/LMH6644
Low Power, 130MHz, 75mA Rail-to-Rail Output Amplifiers

General Description

The LMH664X family true single supply voltage feedback amplifiers offer high speed (130MHz), low distortion (−62dBc), and exceptionally high output current (approximately 75mA) at low cost and with reduced power consumption when compared against existing devices with similar performance.

Input common mode voltage range extends to 0.5V below V^- and 1V from V^+. Output voltage range extends to within 40mV of either supply rail, allowing wide dynamic range especially desirable in low voltage applications. The output stage is capable of approximately 75mA in order to drive heavy loads. Fast output Slew Rate (130V/μs) ensures large peak-to-peak output swings can be maintained even at higher speeds, resulting in exceptional full power bandwidth of 40MHz with a 3V supply. These characteristics, along with low cost, are ideal features for a multitude of industrial and commercial applications.

Careful attention has been paid to ensure device stability under all operating voltages and modes. The result is a very well behaved frequency response characteristic (0.1dB gain flatness up the 12MHz under 150Ω load and A_V = +2) with minimal peaking (typically 2dB maximum) for any gain setting and under both heavy and light loads. This along with fast settling time (68ns) and low distortion allows the device to operate well in ADC buffer, and high frequency filter applications as well as other applications.

This device family offers professional quality video performance with low DG (0.01%) and DP (0.01˚) characteristics. Differential Gain and Differential Phase characteristics are also well maintained under heavy loads (150Ω) and throughout the output voltage range. The LMH664X family is offered in single (LMH6642), dual (LMH6643), and quad (LMH6644) options. See ordering information for packages offered.

Features

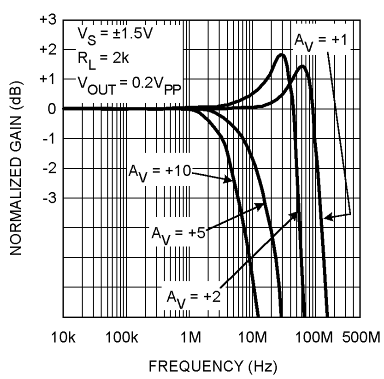
(V_S = ±5V, T_A = 25˚C, R_L = 2kΩ, A_V = +1. Typical values unless specified).

- −3dB BW (A_V = +1) 130MHz
- Supply voltage range 2.7V to 12.8V
- Slew rate (Note 8), (A_V = −1) 130V/μs
- Supply current (no load) 2.7mA/amp
- Output short circuit current +115mA/−145mA
- Linear output current ±75mA
- Input common mode volt. 0.5V beyond V^-, 1V from V^+
- Output voltage swing 40mV from rails
- Input voltage noise (100kHz) 17nV/$\sqrt{Hz}$
- Input current noise (100kHz) 0.9pA/$\sqrt{Hz}$
- THD (5MHz, R_L = 2kΩ, V_O = $2V_{PP}$, A_V = +2) −62dBc
- Settling time 68ns
- Fully characterized for 3V, 5V, and ±5V
- Overdrive recovery 100ns
- Output short circuit protected (Note 11)
- No output phase reversal with CMVR exceeded

Applications

- Active filters
- CD/DVD ROM
- ADC buffer amp
- Portable video
- Current sense buffer

Closed Loop Gain vs. Frequency for Various Gain



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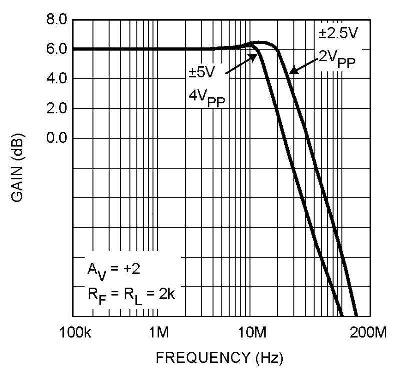
Large Signal Frequency Response



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	2KV (Note 2)
	200V (Note 9)
V_{IN} Differential	±2.5V
Output Short Circuit Duration	(Note 3), (Note 11)
Supply Voltage (V^+ - V^-)	13.5V
Voltage at Input/Output pins	V^+ +0.8V, V^- −0.8V
Input Current	±10mA
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 4)	+150˚C
Soldering Information	
Infrared or Convection Reflow(20 sec)	235˚C
Wave Soldering Lead Temp.(10 sec)	260˚C

Operating Ratings (Note 1)

Supply Voltage (V^+ – V^-)	2.7V to 12.8V
Junction Temperature Range (Note 4)	−40˚C to +85˚C
Package Thermal Resistance (Note 4) (θ_{JA})	
SOT23-5	265˚C/W
SOIC-8	190˚C/W
MSOP-8	235˚C/W
SOIC-14	145˚C/W
TSSOP-14	155˚C/W

3V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L = 2kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
BW	−3dB BW	A_V = +1, V_{OUT} = 200mV_{PP}	80	115		MHz
		A_V = +2, −1, V_{OUT} = 200mV_{PP}		46		
$BW_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, R_L = 150Ω to V+/2, R_L = 402Ω, V_{OUT} = 200mV_{PP}		19		MHz
PBW	Full Power Bandwidth	A_V = +1, −1dB, V_{OUT} = 1V_{PP}		40		MHz
e_n	Input-Referred Voltage Noise	f = 100kHz		17		nV/ $\sqrt{Hz}$
		f = 1kHz		48		
i_n	Input-Referred Current Noise	f = 100kHz		0.90		pA/ $\sqrt{Hz}$
		f = 1kHz		3.3		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A_V = −1, R_L = 100Ω to V^+/2		−48		dBc
DG	Differential Gain	V_{CM} = 1V, NTSC, A_V = +2 R_L =150Ω to V^+/2		0.17		%
		R_L =1kΩ to V^+/2		0.03		
DP	Differential Phase	V_{CM} = 1V, NTSC, A_V = +2 R_L =150Ω to V^+/2		0.05		deg
		R_L =1kΩ to V^+/2		0.03		
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: R_f = R_g = 510Ω, A_V = +2		47		dB
T_S	Settling Time	V_O = 2V_{PP}, ±0.1%, 8pF Load, V_S = 5V		68		ns
SR	Slew Rate (Note 8)	A_V = −1, V_I = 2V_{PP}	90	120		V/μs
V_{OS}	Input Offset Voltage			±1	±5 **±7**	mV
TC V_{OS}	Input Offset Average Drift	(Note 12)		±5		μV/˚C
I_B	Input Bias Current	(Note 7)		−1.50	−2.60 **−3.25**	μA
I_{OS}	Input Offset Current			20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			2		pF

3V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		−0.5	−0.2 **−0.1**	V
			1.8 **1.6**	2.0		
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 1.5V	72	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 2.5V R_L = 2kΩ to $V^+/2$	80 **75**	96		dB
		V_O = 0.5V to 2.5V R_L = 150Ω to $V^+/2$	74 **70**	82		
V_O	Output Swing High	R_L = 2kΩ to $V^+/2$, V_{ID} = 200mV	2.90	2.98		V
		R_L = 150Ω to $V^+/2$, V_{ID} = 200mV	2.80	2.93		
	Output Swing Low	R_L = 2kΩ to $V^+/2$, V_{ID} = −200mV		25	75	mV
		R_L = 150Ω to $V^+/2$, V_{ID} = −200mV		75	150	
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$ V_{ID} = 200mV (Note 10)	50 **35**	95		mA
		Sinking to $V^+/2$ V_{ID} = −200mV (Note 10)	55 **40**	110		
I_{OUT}	Output Current	V_{OUT} = 0.5V from either supply		±65		mA
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 3.0V to 3.5V, V_{CM} = 1.5V	75	85		dB
I_S	Supply Current (per channel)	No Load		2.70	4.00 **4.50**	mA

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
BW	−3dB BW	A_V = +1, V_{OUT} = 200mV_{PP}	90	120		MHz
		A_V = +2, −1, V_{OUT} = 200mV_{PP}		46		
$BW_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, R_L = 150Ω to V+/2, R_f = 402Ω, V_{OUT} = 200mV_{PP}		15		MHz
PBW	Full Power Bandwidth	A_V = +1, −1dB, V_{OUT} = 2V_{PP}		22		MHz
e_n	Input-Referred Voltage Noise	f = 100kHz		17		$nV/\sqrt{Hz}$
		f = 1kHz		48		
i_n	Input-Referred Current Noise	f = 100kHz		0.90		$pA/\sqrt{Hz}$
		f = 1kHz		3.3		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A_V = +2		−60		dBc
DG	Differential Gain	NTSC, A_V = +2 R_L =150Ω to $V^+/2$		0.16		%
		R_L =1kΩ to $V^+/2$		0.05		
DP	Differential Phase	NTSC, A_V = +2 R_L =150Ω to $V^+/2$		0.05		deg
		R_L =1kΩ to $V^+/2$		0.01		
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: R_f = R_g = 510Ω, A_V = +2		47		dB
T_S	Settling Time	V_O = 2V_{PP}, ±0.1%, 8pF Load		68		ns

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate (Note 8)	A_V = −1, V_I = $2V_{PP}$	95	125		V/μs
V_{OS}	Input Offset Voltage			±1	±5 **±7**	mV
TC V_{OS}	Input Offset Average Drift	(Note 12)		±5		μV/˚C
I_B	Input Bias Current	(Note 7)		−1.70	−2.60 **−3.25**	μA
I_{OS}	Input Offset Current			20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		−0.5	−0.2 **−0.1**	V
			3.8 **3.6**	4.0		V
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.5V	72	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.50V R_L = 2kΩ to $V^+/2$	86 **82**	98		dB
		V_O = 0.5V to 4.25V R_L = 150Ω to $V^+/2$	76 **72**	82		dB
V_O	Output Swing High	R_L = 2kΩ to $V^+/2$, V_{ID} = 200mV	4.90	4.98		V
		R_L = 150Ω to $V^+/2$, V_{ID} = 200mV	4.65	4.90		V
	Output Swing Low	R_L = 2kΩ to $V^+/2$, V_{ID} = −200mV		25	100	mV
		R_L = 150Ω to $V^+/2$, V_{ID} = −200mV		100	150	mV
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$ V_{ID} = 200mV (Note 10)	55 **40**	115		mA
		Sinking to $V^+/2$ V_{ID} = −200mV (Note 10)	70 **55**	140		mA
I_{OUT}	Output Current	V_O = 0.5V from either supply		±70		mA
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 4.0V to 6V	79	90		dB
I_S	Supply Current (per channel)	No Load		2.70	4.25 **5.00**	mA

±5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V and R_L = 2kΩ to ground. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
BW	−3dB BW	A_V = +1, V_{OUT} = $200mV_{PP}$	95	130		MHz
		A_V = +2, −1, V_{OUT} = $200mV_{PP}$		46		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, R_L = 150Ω to V+/2, R_f = 806Ω, V_{OUT} = $200mV_{PP}$		12		MHz
PBW	Full Power Bandwidth	A_V = +1, −1dB, V_{OUT} = $2V_{PP}$		24		MHz
e_n	Input-Referred Voltage Noise	f = 100kHz		17		$nV/\sqrt{Hz}$
		f = 1kHz		48		$nV/\sqrt{Hz}$

±5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = –5V, V_{CM} = V_O = 0V and R_L = 2kΩ to ground. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
i_n	Input-Referred Current Noise	f = 100kHz		0.90		$pA/\sqrt{Hz}$
		f = 1kHz		3.3		
THD	Total Harmonic Distortion	f = 5MHz, V_O = $2V_{PP}$, A_V = +2		–62		dBc
DG	Differential Gain	NTSC, A_V = +2 R_L =150Ω to V^+/2		0.15		%
		R_L =1kΩ to V^+/2		0.01		
DP	Differential Phase	NTSC, A_V = +2 R_L =150Ω to V^+/2		0.04		deg
		R_L =1kΩ to V^+/2		0.01		
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: R_f = R_g = 510Ω, A_V = +2		47		dB
T_S	Settling Time	V_O = $2V_{PP}$, ±0.1%, 8pF Load, V_S = 5V		68		ns
SR	Slew Rate (Note 8)	A_V = –1, V_I = $2V_{PP}$	100	135		V/μs
V_{OS}	Input Offset Voltage			±1	±5 **±7**	mV
TC V_{OS}	Input Offset Average Drift	(Note 12)		±5		μV/˚C
I_B	Input Bias Current	(Note 7)		–1.60	–2.60 **–3.25**	μA
I_{OS}	Input Offset Current			20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		–5.5	–5.2 **–5.1**	V
			3.8 **3.6**	4.0		
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from –5V to 3.5V	74	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = –4.5V to 4.5V, R_L = 2kΩ	88 **84**	96		dB
		V_O = –4.0V to 4.0V, R_L = 150Ω	78 **74**	82		
V_O	Output Swing High	R_L = 2kΩ, V_{ID} = 200mV	4.90	4.96		V
		R_L = 150Ω, V_{ID} = 200mV	4.65	4.80		
	Output Swing Low	R_L = 2kΩ, V_{ID} = –200mV		–4.96	–4.90	V
		R_L = 150Ω, V_{ID} = –200mV		–4.80	–4.65	
I_{SC}	Output Short Circuit Current	Sourcing to Ground V_{ID} = 200mV (Note 10)	60 **35**	115		mA
		Sinking to Ground V_{ID} = –200mV (Note 10)	85 **65**	145		
I_{OUT}	Output Current	V_O = 0.5V from either supply	±75			mA
PSRR	Power Supply Rejection Ratio	(V^+, V^-) = (4.5V, –4.5V) to (5.5V, –5.5V)	78	90		dB
I_S	Supply Current (per channel)	No Load		2.70	4.50 **5.50**	mA

±5V Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Positive current corresponds to current flowing into the device.

Note 8: Slew rate is the average of the rising and falling slew rates.

Note 9: Machine Model, 0Ω in series with 200pF.

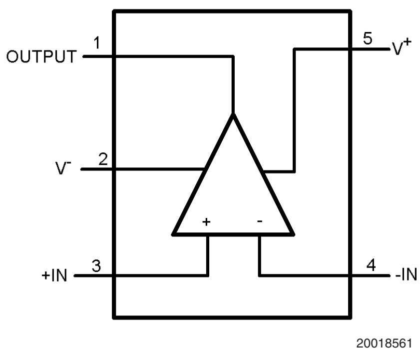
Note 10: Short circuit test is a momentary test. See Note 11.

Note 11: Output short circuit duration is infinite for $V_S < 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.

Note 12: Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.

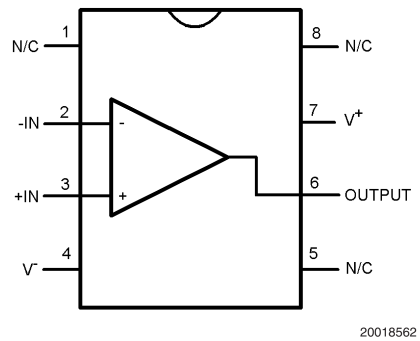
Connection Diagrams

SOT23-5 (LMH6642)



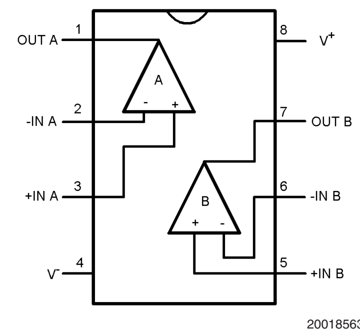
Top View

SOIC-8 (LMH6642)



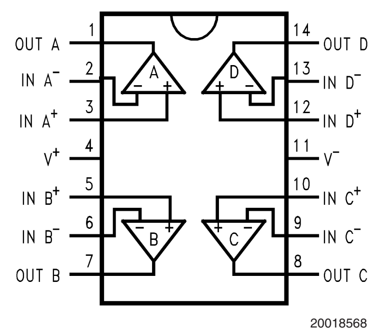
Top View

SOIC-8 and MSOP-8 (LMH6643)



Top View

SOIC-14 and TSSOP-14 (LMH6644)

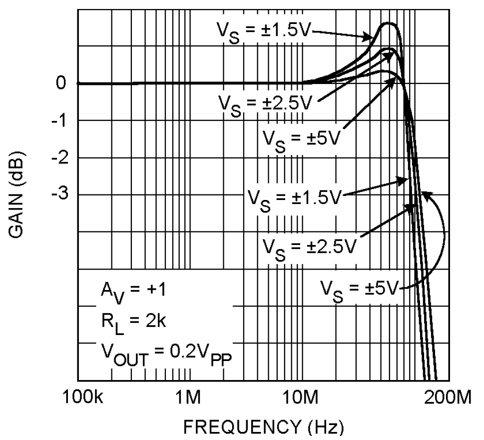


Top View

Typical Performance Characteristics

At $T_J = 25^\circ C$, $V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

Closed Loop Frequency Response for Various Supplies



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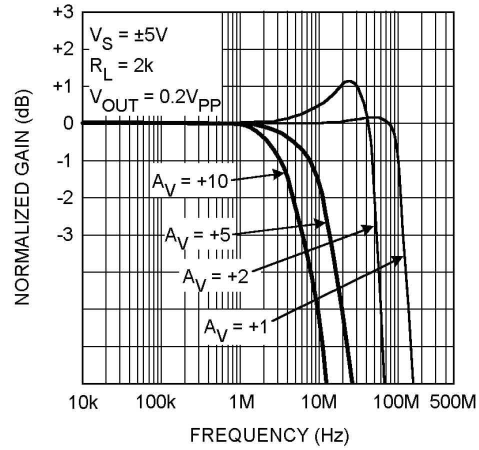
Closed Loop Gain vs. Frequency for Various Gain



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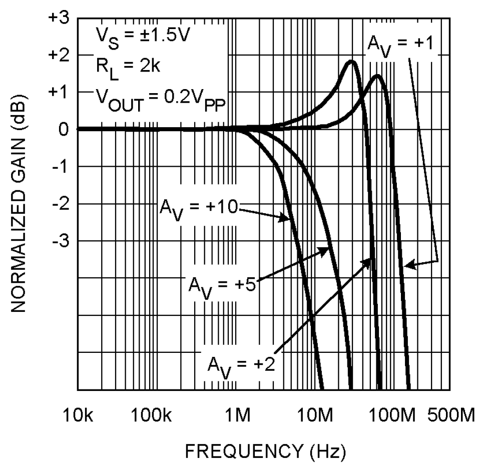
Closed Loop Gain vs. Frequency for Various Gain



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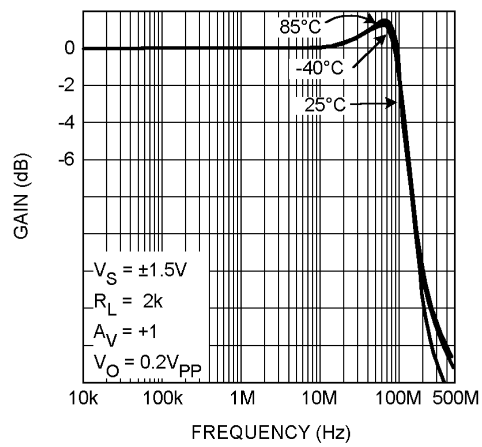
Closed Loop Frequency Response for Various Temperature



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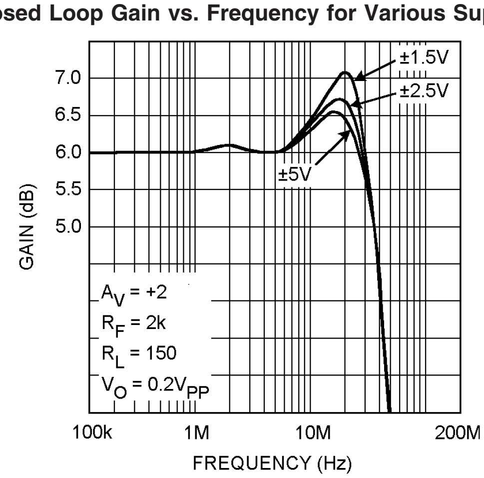
Closed Loop Gain vs. Frequency for Various Supplies



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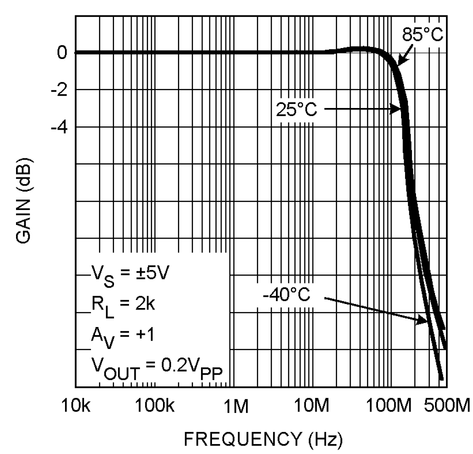
Closed Loop Frequency Response for Various Temperature



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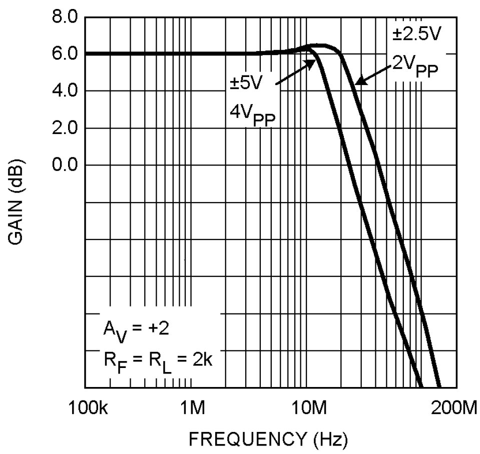
Typical Performance Characteristics At T_J = 25˚C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified. (Continued)

Large Signal Frequency Response



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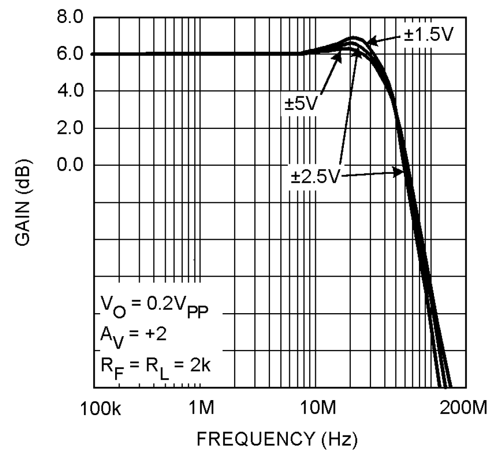
Closed Loop Small Signal Frequency Response for Various Supplies



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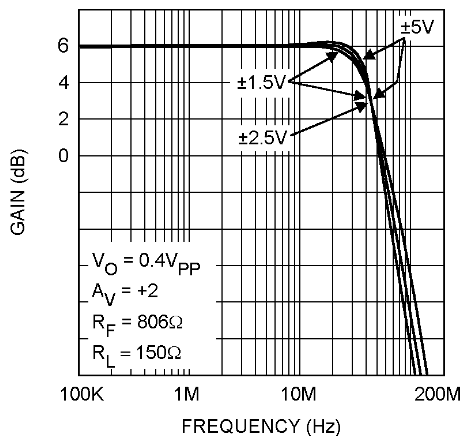
Closed Loop Frequency Response for Various Supplies



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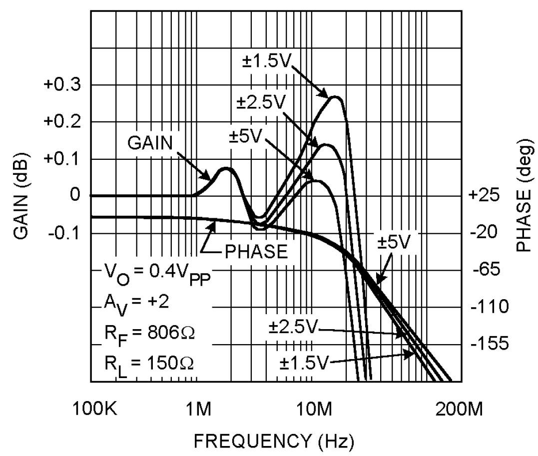
±0.1dB Gain Flatness for Various Supplies



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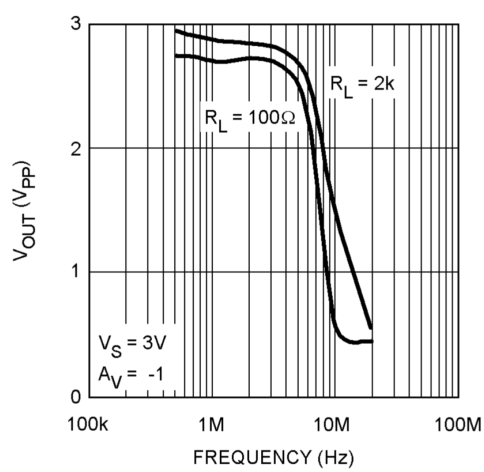
V_{OUT} (V_{PP}) for THD < 0.5%



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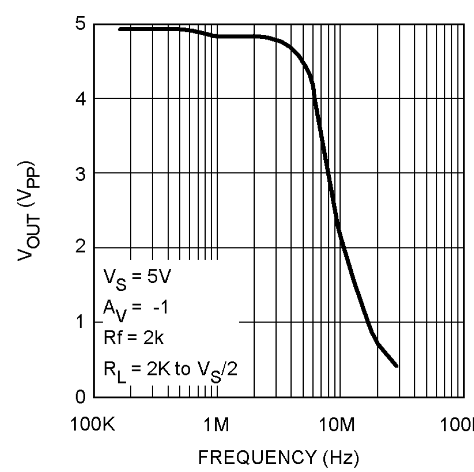
V_{OUT} (V_{PP}) for THD < 0.5%



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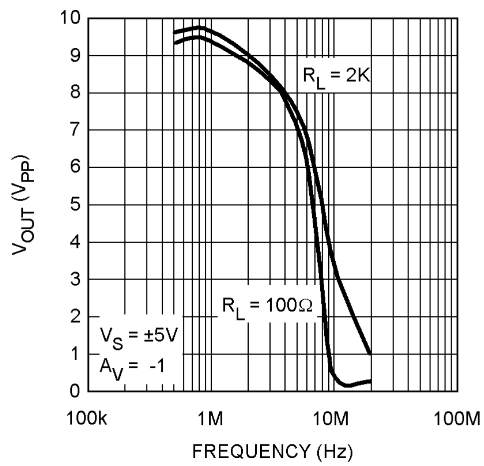
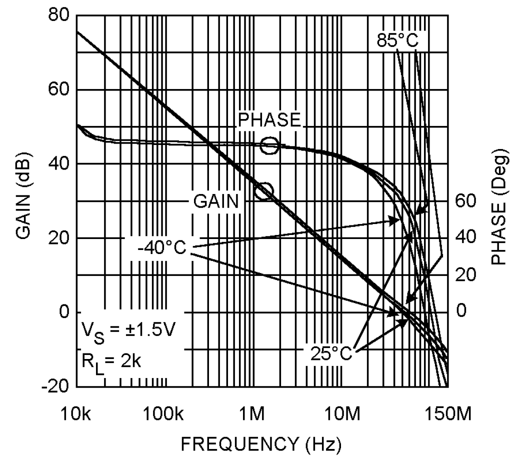
Typical Performance Characteristics
At T_J = 25˚C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified. (Continued)

V_{OUT} (V_{PP}) for THD < 0.5%



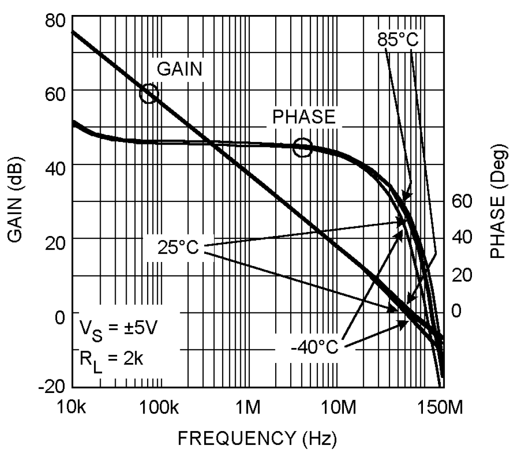
20018510

Open Loop Gain/Phase for Various Temperature



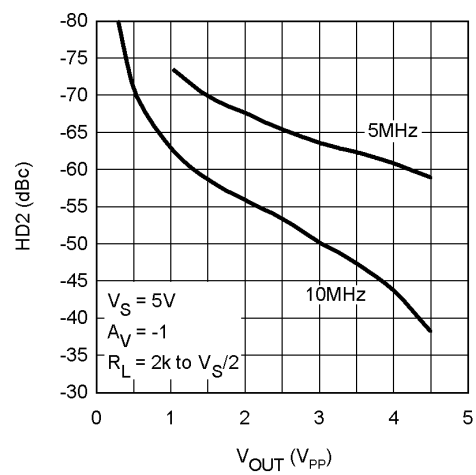
20018532

Open Loop Gain/Phase for Various Temperature



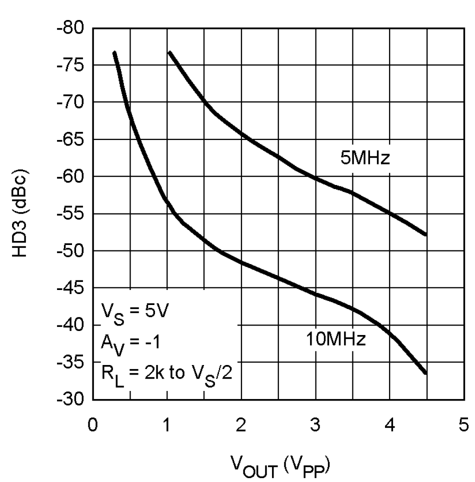
20018533

HD2 (dBc) vs. Output Swing



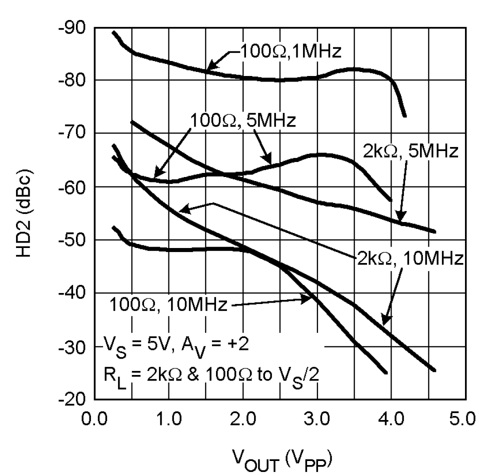
20018514

HD3 (dBc) vs. Output Swing



20018515

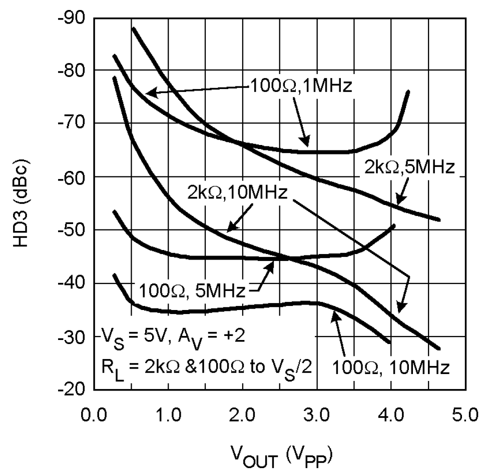
HD2 vs. Output Swing



20018504

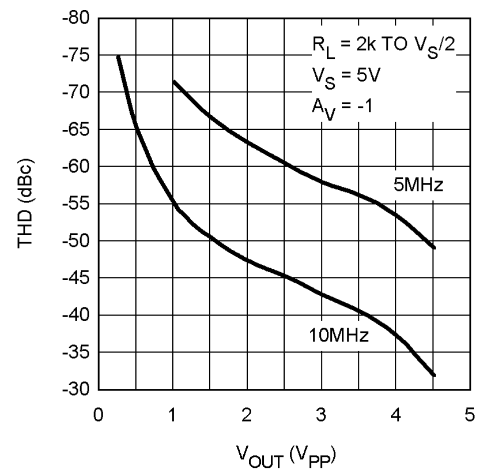
Typical Performance Characteristics
At $T_J = 25^\circ C$, $V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified. (Continued)

HD3 vs. Output Swing



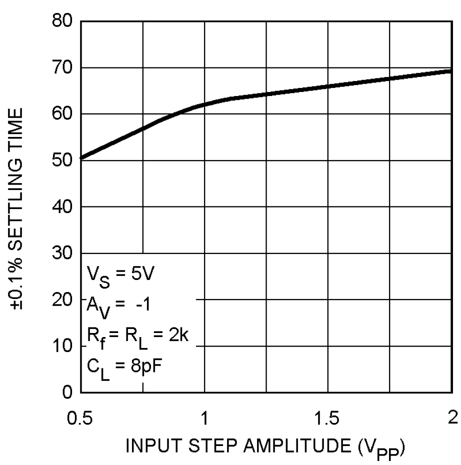
20018505

THD (dBc) vs. Output Swing



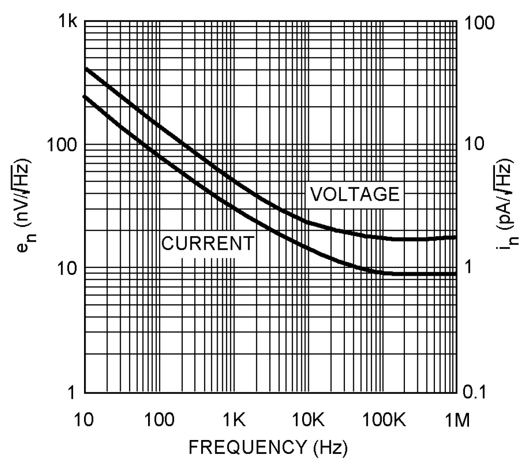
20018506

Settling Time vs. Input Step Amplitude (Output Slew and Settle Time)



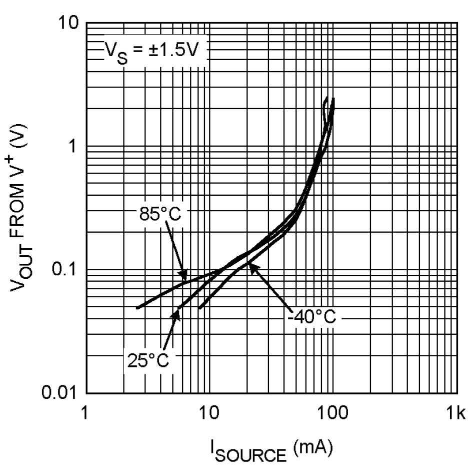
20018513

Input Noise vs. Frequency



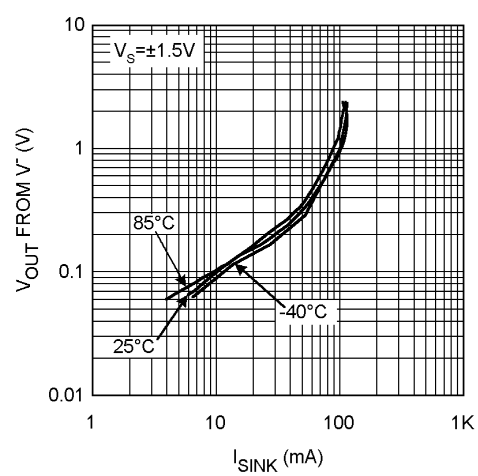
20018512

V_{OUT} from V^+ vs. I_{SOURCE}



20018518

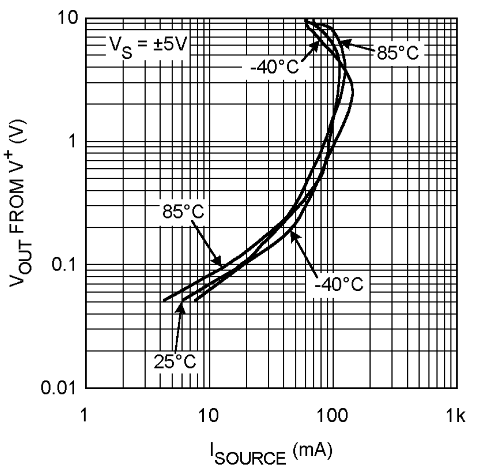
V_{OUT} from V^- vs. I_{SINK}



20018519

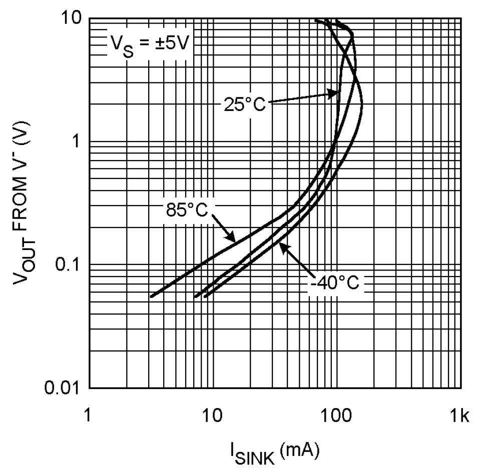
Typical Performance Characteristics At T_J = 25˚C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified. (Continued)

V_{OUT} from V^+ vs. I_{SOURCE}



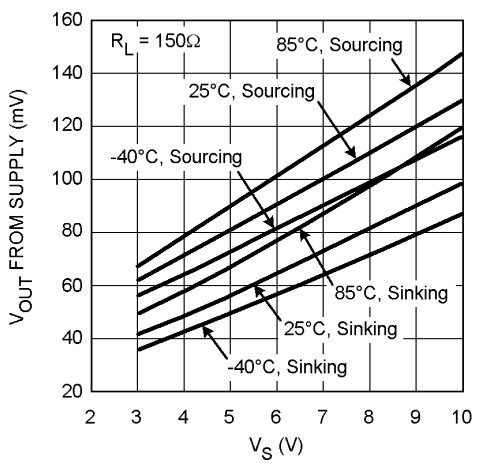
20018516

V_{OUT} from V^- vs. I_{SINK}



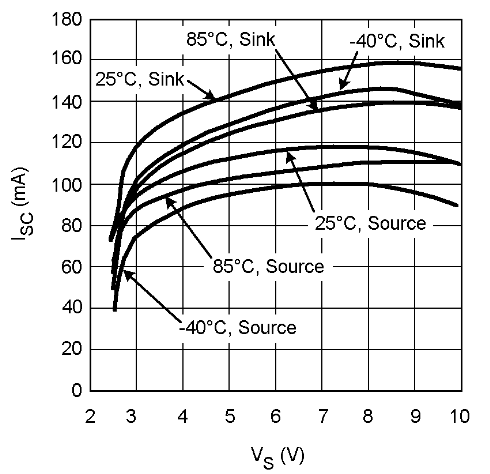
20018517

Swing vs. V_S



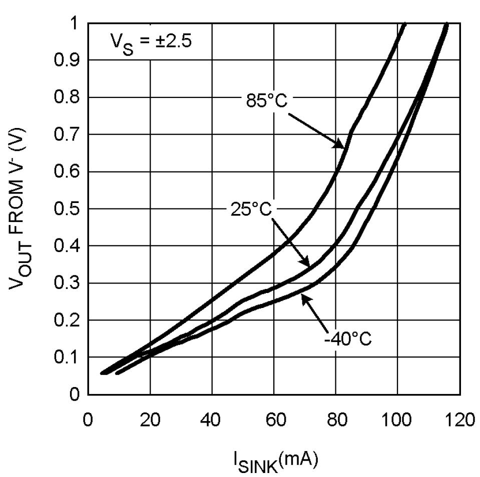
20018529

Short Circuit Current (to V_S/2) vs. V_S



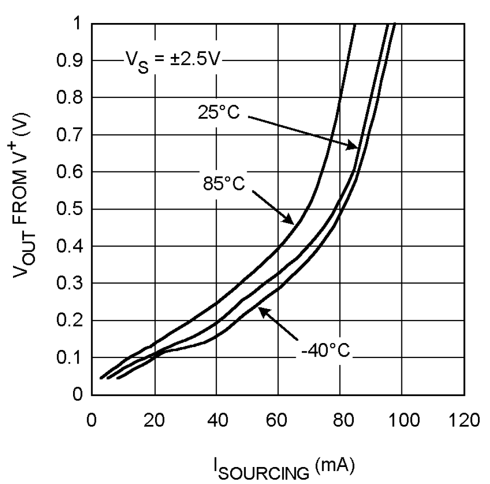
20018531

Output Sinking Saturation Voltage vs. I_{OUT}



20018520

Output Sourcing Saturation Voltage vs. I_{OUT}

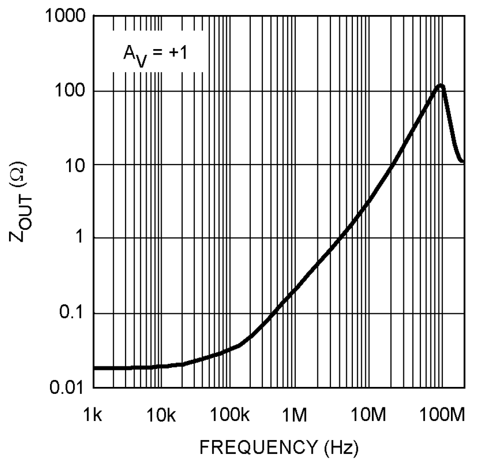


20018501

Typical Performance Characteristics

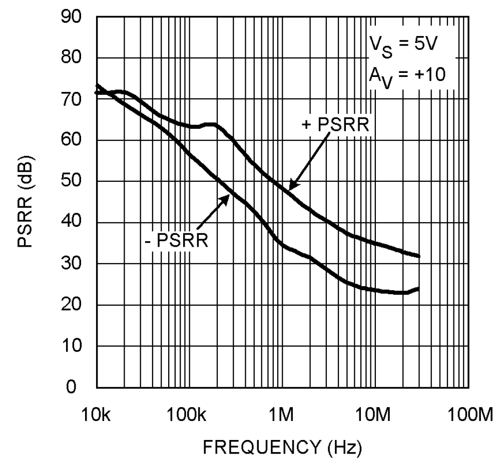
At T_J = 25˚C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified. (Continued)

Closed Loop Output Impedance vs. Frequency A_V = +1



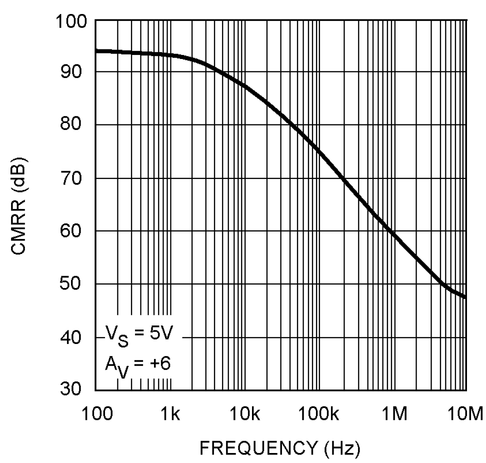
20018502

PSRR vs. Frequency



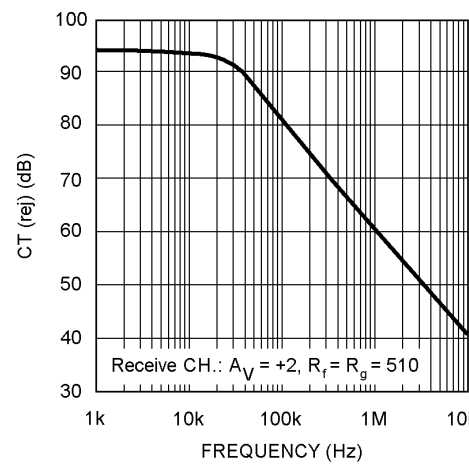
20018503

CMRR vs. Frequency



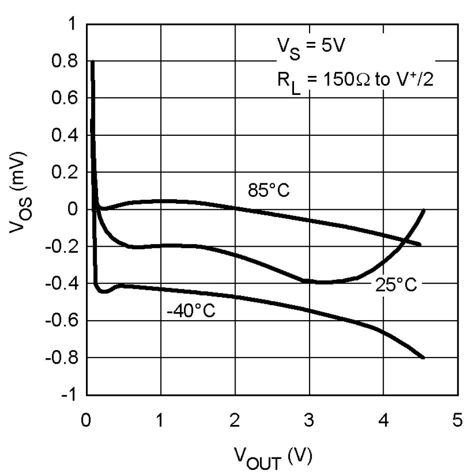
20018507

Crosstalk Rejection vs. Frequency (Output to Output)



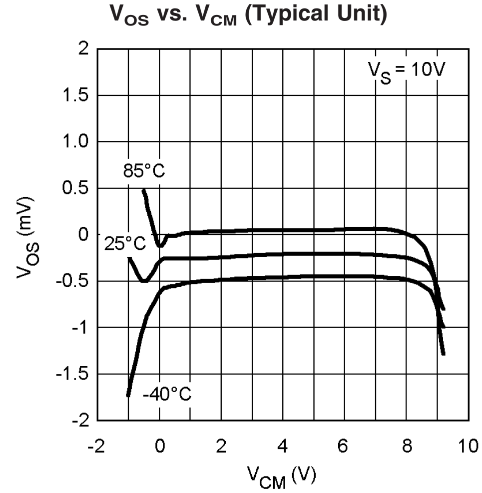
20018511

V_{OS} vs. V_{OUT} (Typical Unit)



20018530

V_{OS} vs. V_{CM} (Typical Unit)

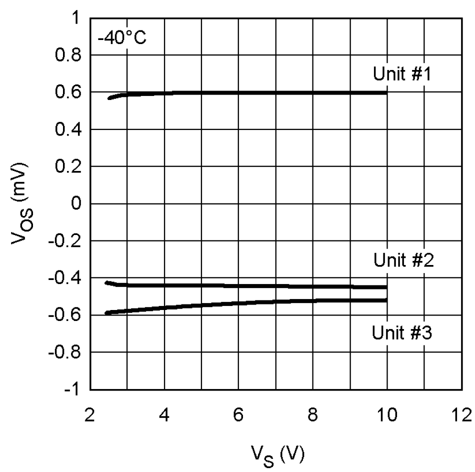


20018527

Typical Performance Characteristics

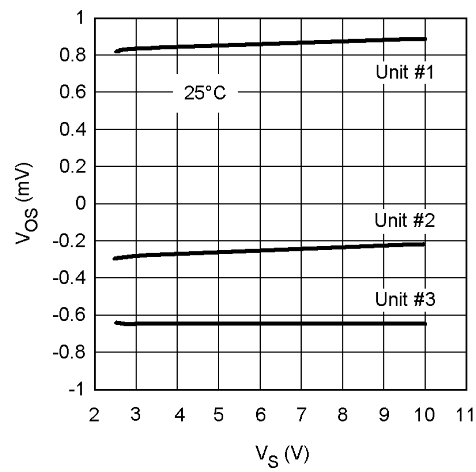
At $T_J = 25^\circ C$, $V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified. (Continued)

V_{OS} vs. V_S (for 3 Representative Units)



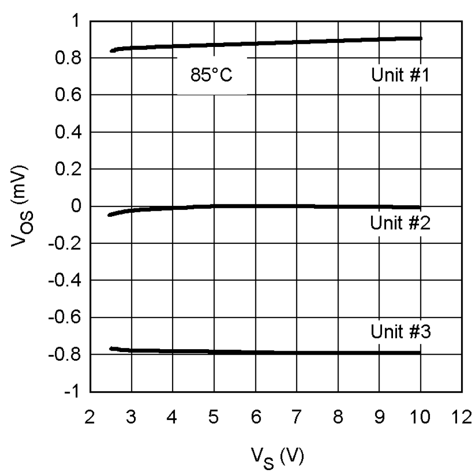
20018522

V_{OS} vs. V_S (for 3 Representative Units)



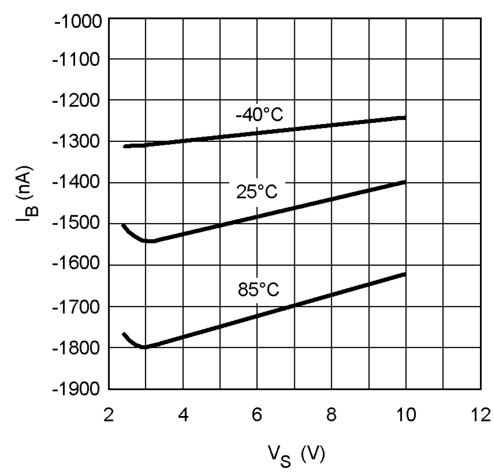
20018523

V_{OS} vs. V_S (for 3 Representative Units)



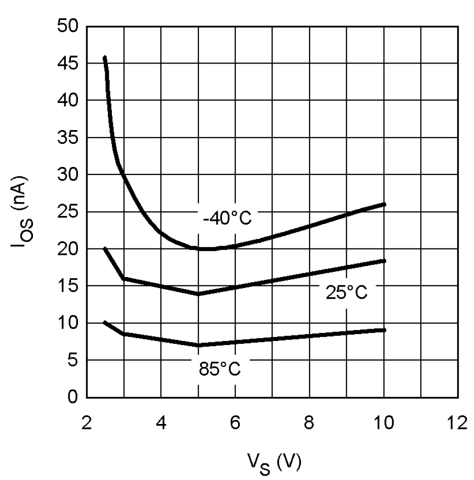
20018524

I_B vs. V_S



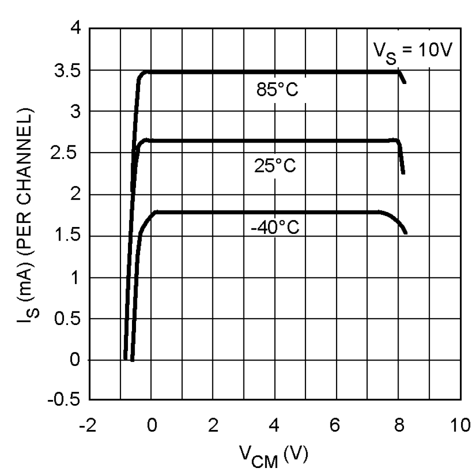
20018525

I_{OS} vs. V_S



20018526

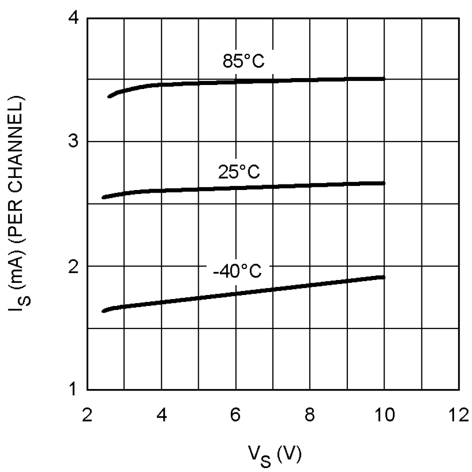
I_S vs. V_{CM}



20018528

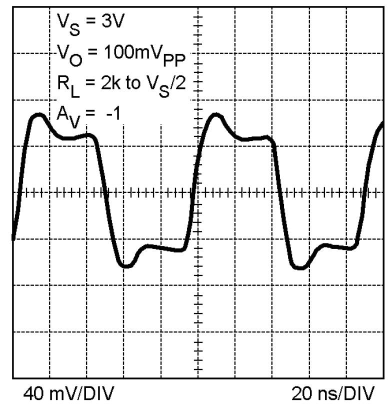
Typical Performance Characteristics At $T_J = 25^\circ C$, $V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified. (Continued)

I_S vs. V_S



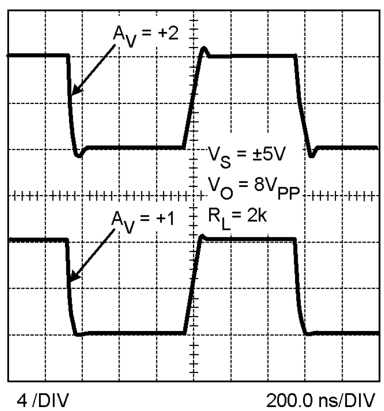
20018521

Small Signal Step Response



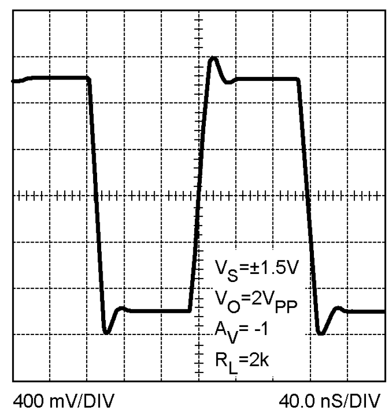
20018553

Large Signal Step Response



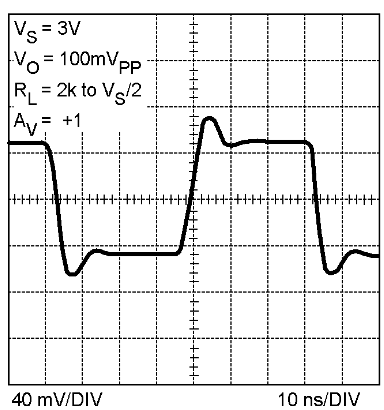
20018541

Large Signal Step Response



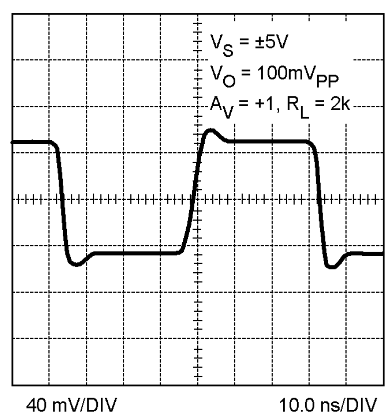
20018539

Small Signal Step Response



20018556

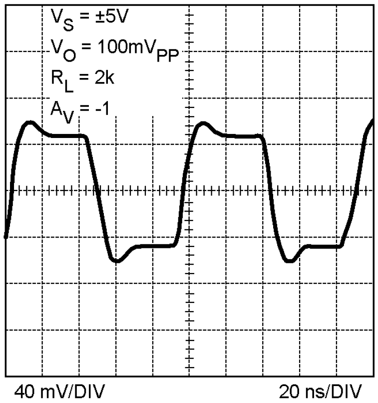
Small Signal Step Response



20018536

Typical Performance Characteristics At $T_J = 25°C$, $V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified. (Continued)

Small Signal Step Response



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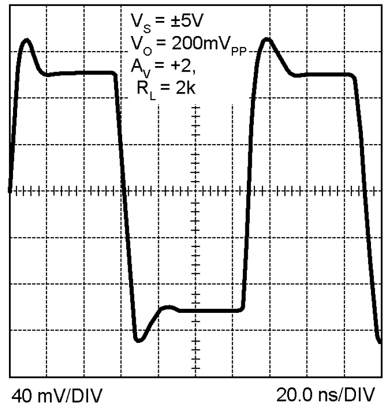
Small Signal Step Response



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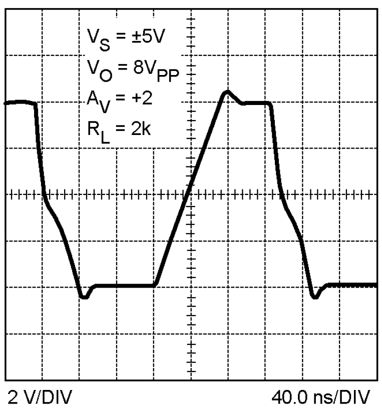
Large Signal Step Response



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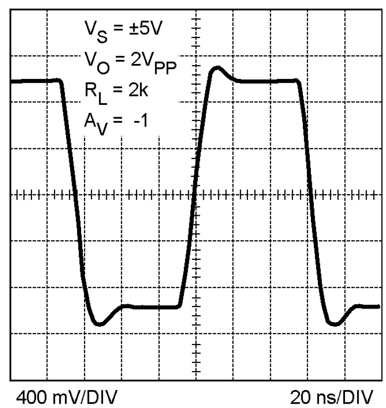
Large Signal Step Response



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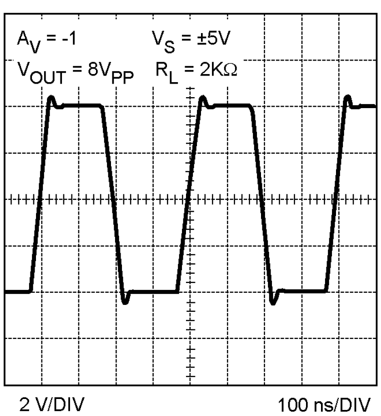
Large Signal Step Response



20018560

Application Notes

CIRCUIT DESCRIPTION

The LMH664X family is based on National Semiconductor's proprietary VIP10 dielectrically isolated bipolar process.

This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8GHz) even under low supply voltage (2.7V) and low bias current.
- A class A-B "turn-around" stage with improved noise, offset, and reduced power dissipation compared to similar speed devices (patent pending).
- Common Emitter push-push output stage capable of 75mA output current (at 0.5V from the supply rails) while consuming only 2.7mA of total supply current per channel. This architecture allows output to reach within millivolts of either supply rail.
- Consistent performance from any supply voltage (3V-10V) with little variation with supply voltage for the most important specifications (e.g. BW, SR, I_{OUT}, etc.)
- Significant power saving (~40%) compared to competitive devices on the market with similar performance.

Application Hints

This Op Amp family is a drop-in replacement for the AD805X family of high speed Op Amps in most applications. In addition, the LMH664X will typically save about 40% on power dissipation, due to lower supply current, when compared to competition. All AD805X family's guaranteed parameters are included in the list of LMH664X guaranteed specifications in order to ensure equal or better level of performance. However, as in most high performance parts, due to subtleties of applications, it is strongly recommended that the performance of the part to be evaluated is tested under actual operating conditions to ensure full compliance to all specifications.

With 3V supplies and a common mode input voltage range that extends 0.5V below V^-, the LMH664X find applications in low voltage/low power applications. Even with 3V supplies, the –3dB BW (@ A_V = +1) is typically 115MHz with a tested limit of 80MHz. Production testing guarantees that process variations with not compromise speed. High frequency response is exceptionally stable confining the typical -3dB BW over the industrial temperature range to ±2.5%.

As can be seen from the typical performance plots, the LMH664X output current capability (~75mA) is enhanced compared to AD805X. This enhancement, increases the output load range, adding to the LMH664X's versatility.

Because of the LMH664X's high output current capability attention should be given to device junction temperature in order not to exceed the Absolute Maximum Rating.

This device family was designed to avoid output phase reversal. With input overdrive, the output is kept near supply rail (or as closed to it as mandated by the closed loop gain setting and the input voltage). See *Figure 1*:

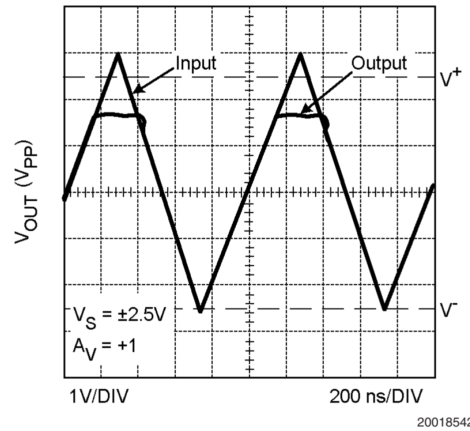


FIGURE 1. Input and Output Shown with CMVR Exceeded

However, if the input voltage range of –0.5V to 1V from V^+ is exceeded by more than a diode drop, the internal ESD protection diodes will start to conduct.The current in the diodes should be kept at or below 10mA.

Output overdrive recovery time is less than 100ns as can be seen from *Figure 2* plot:

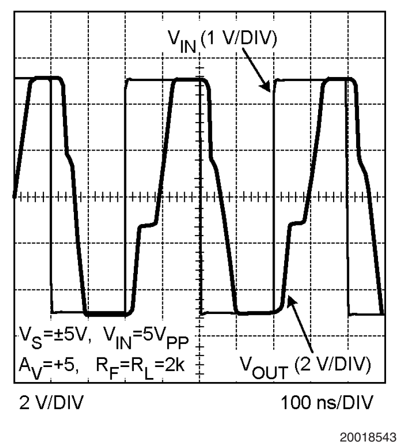


FIGURE 2. Overload Recovery Waveform

Application Notes (Continued)

SINGLE SUPPLY, LOW POWER PHOTODIODE AMPLIFIER

The circuit shown in *Figure 3* is used to amplify the current from a photo-diode into a voltage output. In this circuit, the emphasis is on achieving high bandwidth and the transimpedance gain setting is kept relatively low. Because of its high slew rate limit and high speed, the LMH664X family lends itself well to such an application.

This circuit achieves approximately 1V/mA of transimpedance gain and capable of handling up to $1mA_{pp}$ from the photodiode. Q1, in a common base configuration, isolates the high capacitance of the photodiode (C_d) from the Op Amp input in order to maximize speed. Input is AC coupled through C1 to ease biasing and allow single supply operation. With 5V single supply, the device input/output is shifted to near half supply using a voltage divider from V_{CC}. Note that Q1 collector does not have any voltage swing and the Miller effect is minimized. D1, tied to Q1 base, is for temperature compensation of Q1's bias point. Q1 collector current was set to be large enough to handle the peak-to-peak photodiode excitation and not too large to shift the U1 output too far from mid-supply.

No matter how low an R_f is selected, there is a need for C_f in order to stabilize the circuit. The reason for this is that the Op Amp input capacitance and Q1 equivalent collector capacitance together (C_{IN}) will cause additional phase shift to the signal fed back to the inverting node. C_f will function as a zero in the feedback path counter-acting the effect of the C_{IN} and acting to stabilized the circuit. By proper selection of C_f such that the Op Amp open loop gain is equal to the inverse of the feedback factor at that frequency, the response is optimized with a theoretical 45˚ phase margin.

$$C_F = \sim \mathrm{SQRT}\left[(C_{IN})/(2\pi \cdot \mathrm{GBWP} \cdot R_F)\right] \quad (1)$$

where GBWP is the Gain Bandwidth Product of the Op Amp

Optimized as such, the I-V converter will have a theoretical pole, f_p, at:

$$f_P = \mathrm{SQRT}\left[\mathrm{GBWP}/(2\pi R_F \cdot C_{IN})\right] \quad (2)$$

With Op Amp input capacitance of 3pF and an estimate for Q1 output capacitance of about 3pF as well, C_{IN} = 6pF. From the typical performance plots, LMH6642/6643 family GBWP is approximately 57MHz. Therefore, with R_f = 1k, from Equation 1 and 2 above.

C_f = ~4.1pF, and f_p = 39MHz

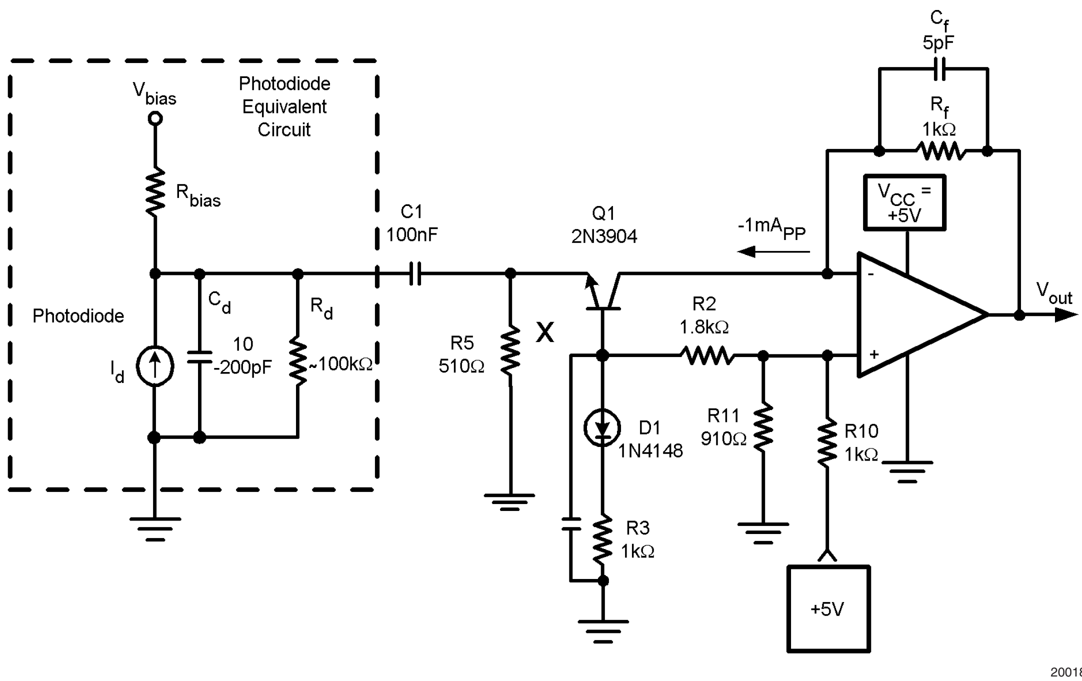


FIGURE 3. Single Supply Photodiode I-V Converter

Application Notes (Continued)

For this example, optimum C_f was empirically determined to be around 5pF. This time domain response is shown in *Figure 4* below showing about 9ns rise/fall times, corresponding to about 39MHz for f_p. The overall supply current from the +5V supply is around 5mA with no load.

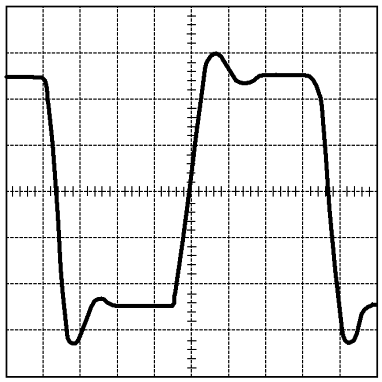


FIGURE 4. Converter Step Response ($1V_{PP}$, 20 ns/DIV)

PRINTED CIRCUIT BOARD LAYOUT AND COMPONENT VALUES SECTION

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board PN
LMH6642MF	SOT23-5	CLC730216
LMH6642MA	8-Pin SOIC	CLC730227
LMH6643MA	8-Pin SOIC	CLC730036
LMH6643MM	8-Pin MSOP	CLC730123
LMH6644MA	14-Pin SOIC	CLC730231
LMH6644MT	14-Pin TSSOP	CLC730131

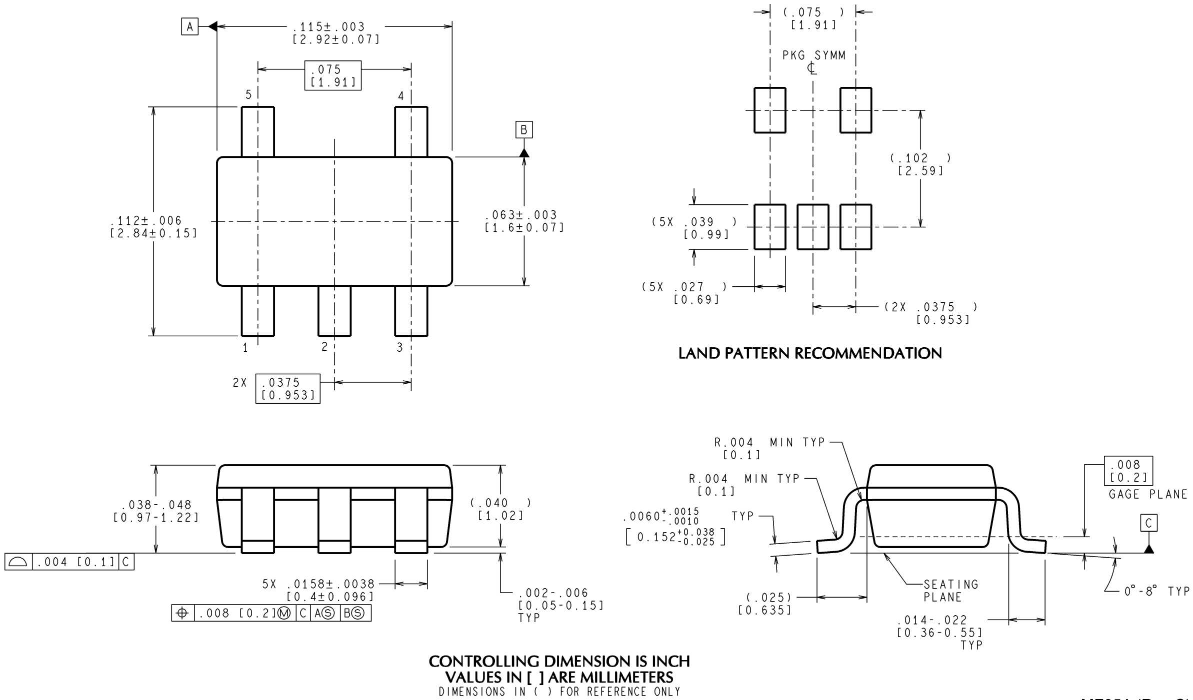
These free evaluation boards are shipped when a device sample request is placed with National Semiconductor.

Another important parameter in working with high speed/ high performance amplifiers, is the component values selection. Choosing external resistors that are large in value will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction to a large extent. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation.

Ordering Information

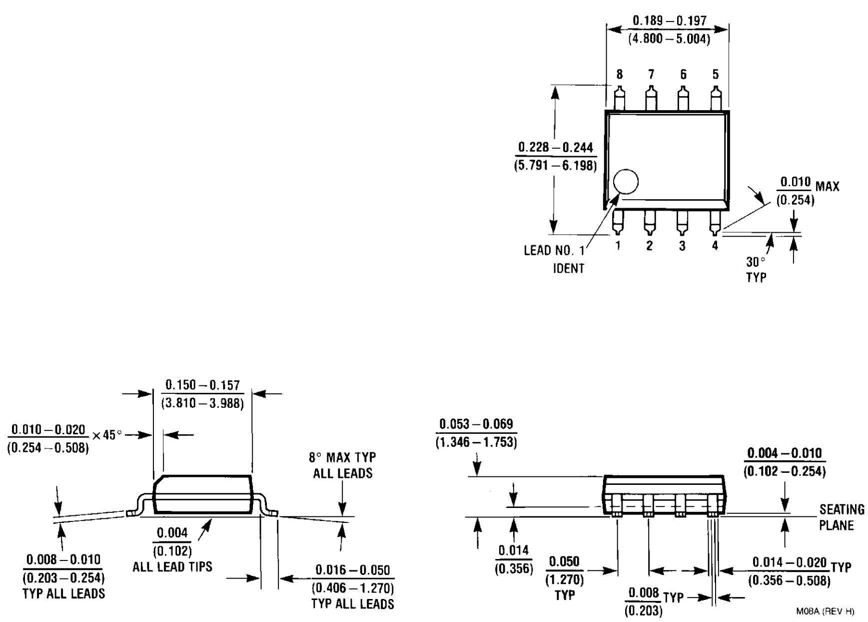
Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SOT23	LMH6642MF	A64A	1k Units Tape and Reel	MF05A
	LMH6642MFX		3k Units Tape and Reel	
8-Pin SOIC	LMH6642MA	LMH6642MA	95 Units/Rail	M08A
	LMH6642MAX		2.5k Units Tape and Reel	
	LMH6643MA	LMH6643MA	95 Units/Rail	
	LMH6643MAX		2.5k Units Tape and Reel	
8-Pin MSOP	LMH6643MM	A65A	1k Units Tape and Reel	MUA08A
	LMH6643MMX		3.5k Units Tape and Reel	
14-Pin SOIC	LMH6644MA	LMH6644MA	55 units/Rail	M14A
	LMH6644MAX		2.5k Units Tape and Reel	
14-Pin TSSO	LMH6644MT	LMH6644MT	94 Units/Rail	MTC14
	LMH6644MTX		2.5k Units Tape and Reel	

Physical Dimensions inches (millimeters) unless otherwise noted



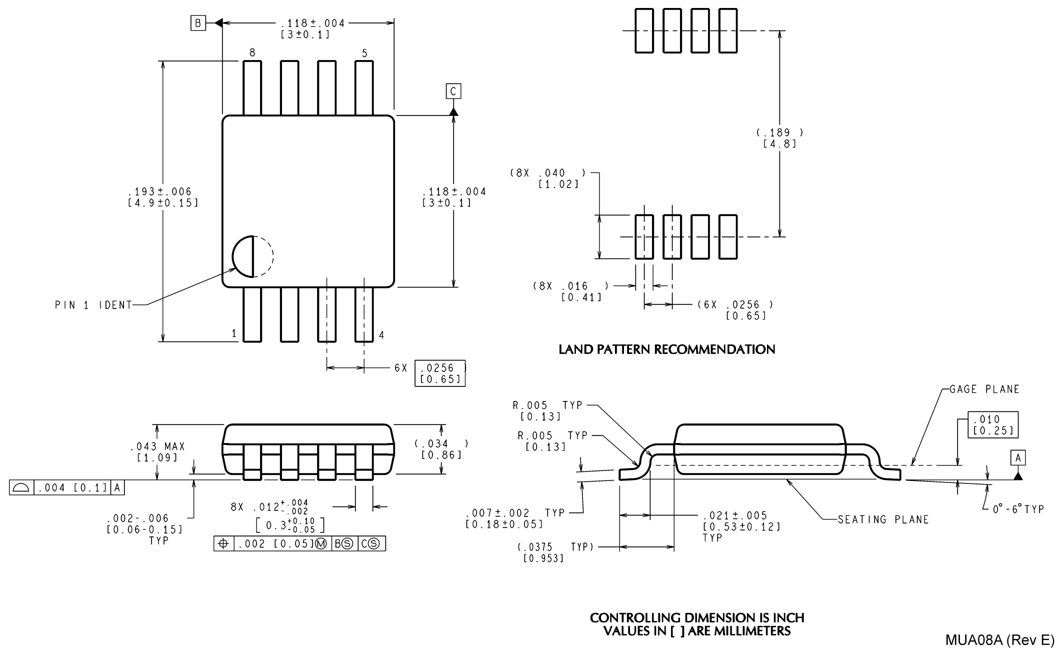
MF05A (Rev C)

5-Pin SOT23
NS Package Number MF05A

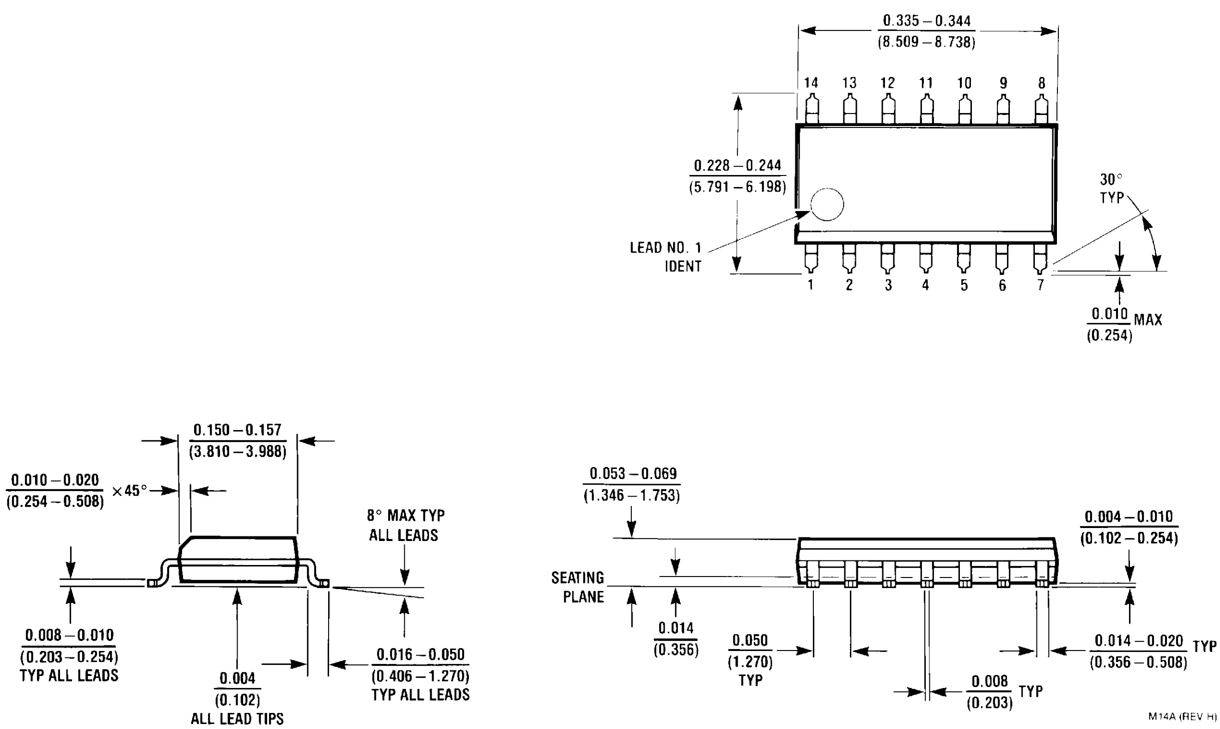


8-Pin SOIC
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

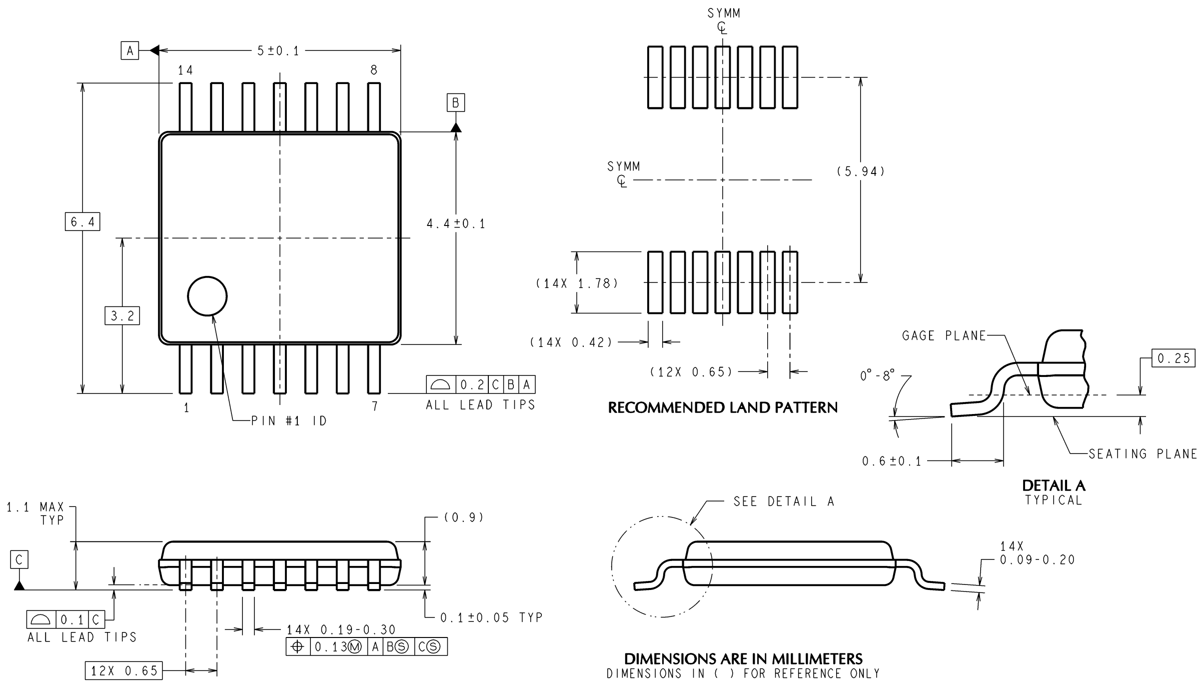


8-Pin MSOP
NS Package Number MUA08A



14-Pin SOIC
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MTC14 (Rev D)

14-Pin TSSOP
NS Package Number MTC14

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