National Semiconductor

PRELIMINARY
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LMH0340, LMH0040, LMH0070, LMH0050 3G, HD, SD, DVB-ASI SDI Serializer and Driver with LVDS Interface

General Description

The LMH0040 family of products provide a very simple 5:1 serializer and transmitter function, intended to be paired with an FPGA host which will format the data appropriately such that the output of the LMH0040 will be compliant with the output requirements of DVB-ASI, SMPTE 259M, and SMPTE 292M. The LMH0340 adds support for SMPTE 424M, the LMH0070 supports 270 Mbps operation only, and the LMH0050 requires an external cable driver. Throughout this document, if not explicitly stated, when the LMH0040 is referred to this includes all members of the family. The interface between the LMH0040 and the FPGA consists of a 5 bit wide LVDS bus, an LVDS clock and an SMBus interface. The product is packaged in a physically small 48 pin LLP package.

Key Specifications

- Output compliant with SMPTE 424M, SMPTE 292M, SMPTE 259M-C and DVB-ASI
- Typical power dissipation: 420 mW
- Typical output jitter <53 ps (HD, 3G)

Features

- LVDS Interface
- No external VCO or clock required
- Integrated Variable output Cable Driver
- 3.3V SMBus configuration interface
- 48pin LLP package

Applications

- SDI interfaces for:
  - Video Cameras
  - DVRs
  - Video Switchers
  - Video Editing Systems

LMH0340, LMH0040, LMH0070, LMH0050 3G, HD, SD, DVB-ASI SDI Serializer and Driver with LVDS Interface

Block Diagram

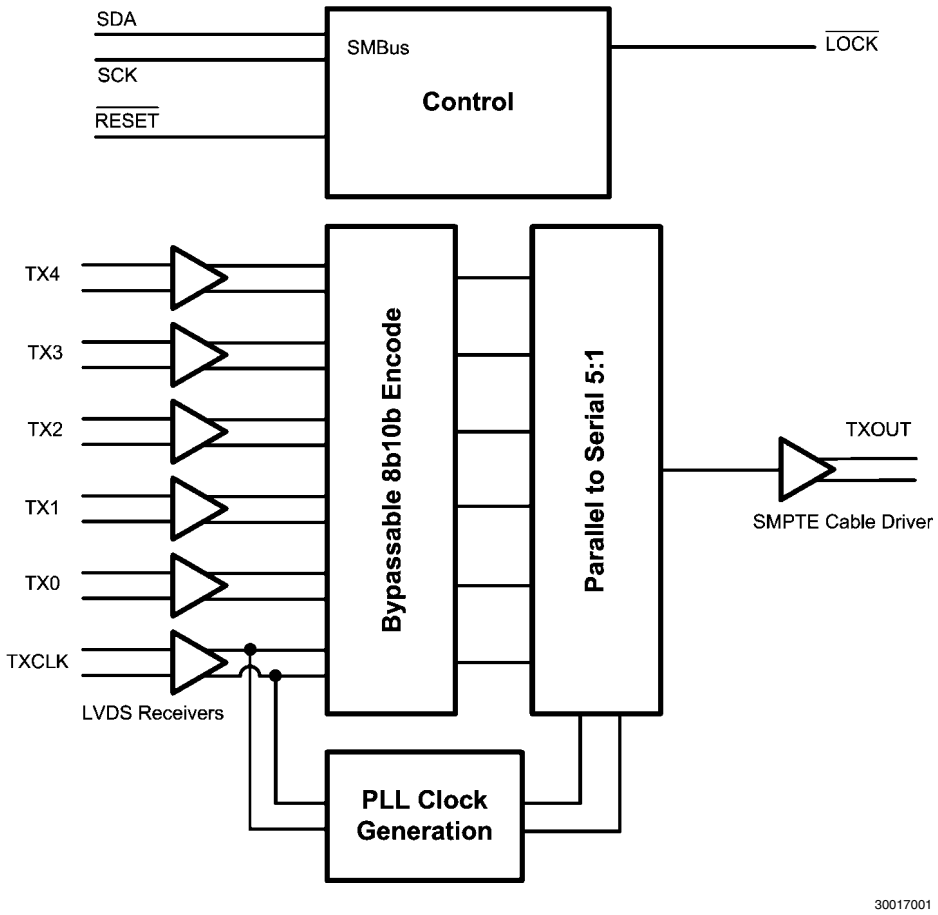


TABLE 1. Feature Table

Device	SMPTE 424M Support	SMPTE 292M Support	SMPTE 259M Support	DVB-ASI Support	SMPTE Compliant cable driver
LMH0340	X	X	X	X	X
LMH0040		X	X	X	X
LMH0070			X	X	X
LMH0050		X	X	X	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4.0V
LVCMOS (SMBus) input voltage	−0.3V to (V_{CC}+0.3V)
LVCMOS (SMBus) output voltage	−0.3V to (V_{CC}+0.3V)
LVDS Input Voltage	0.3V to 3.6V
Junction Temperature	+150°C
Storage Temperature	−65° to 150°C
Lead Temperature—Soldering 4 seconds	+260°C
Thermal Resistance— Junction to Ambient—θ_{JA}	40°C/W
ESD Rating—Human Body Model, 1.5 KΩ, 100 pF	4KV

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{CC}-GND)	3.1	3.3	3.5	V
	2.4	2.5	2.6	V
Supply noise amplitude (10 Hz to 50 MHz)			100	mV_{P-P}
Ambient Temperature	−40	+25	+85	°C
Case Temperature			100	°C
Transmitter input clock frequency	27		297	MHz
LVDS PCB board trace length (mismatch <2%)			25	cm
Output Driver Pullup Resistor Termination Voltage		2.5	3.0	V

LMH0040 Electrical Characteristics

Over supply and Operating Temperature ranges unless otherwise specified

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
$I_{DD2.5}$	2.5V supply current			76.1		mA
$I_{DD3.3}$	3.3V supply current			66.4		mA
P_D	Power Consumption	V_{DD}=3.6V All outputs terminated by 100Ω, 2.97 Gbps output LMH00340		437		mW
		LMH0040		420		mW
		LMH0050		420		mW
		LMH0070		415		mW

Control Pin Electrical Characteristics

Over supply and Operating Temperature ranges unless otherwise specified. Applies to DVB_ASI, $\overline{\text{RESET}}$ and $\overline{\text{LOCK}}$

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		0		0.8	V
V_{OH}	High Level Output Voltage	I_{OH}=−2 mA	2	3.3		V
V_{OL}	Low Level Output Voltage	I_{OL}=2 mA			0.6	V
V_{CL}	Input Clamp Voltage	I_{CL}=−18 mA		−0.79	−1.5	V
I_{IN}	Input Current	V_{IN}=0.4V, 2.5V or V_{DD}		1	65	µA
		V_{IN}=GND	−25	−1		µA
I_{OS}	Output Short Circuit Current	V_{OUT}=0V			−120	mA

LVDS Input Electrical Characteristics

Over supply and Operating Temperature ranges unless otherwise specified

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
V_{TH}	Differential Input High threshold	0.05V<V_{CM}<2.4V			+100	mV
V_{TL}	Differential Input Low threshold		−100			mV
I_{IN}	Input Current	V_{IN}=2.4V, V_{CC}=3.6V	−10		+10	µA
R_{LVIN}	Input Impedance	Measured between LVDS pairs	80	100	120	Ω

SMBus Input Electrical Characteristics

Over supply and Operating Temperature ranges unless otherwise specified

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
V_{SIL}	Data, Clock Input Low Voltage				0.8	V
V_{SIH}	Data, Clock Input High Voltage		2.1		V_{SDD}	V
$I_{SPULLUP}$	Current through pull-up resistor or current source		4			mA
V_{SDD}	Nominal Bus Voltage		2.375		3.6	V
I_{SLEAKB}	Input Leakage per bus segment	See (Note 3)	−200		200	µA
I_{SLEAKP}	Input Leakage per pin		−10		10	µA
C_{SI}	Capacitance for SMBdata and SMBclk	See (Notes 3, 4)			10	pF
R_{STERM}	Termination Resistance	$V_{SDD3.3}$ See (Notes 3, 4, 5)		2000		Ω
		$V_{SDD3.3}$ See (Notes 3, 4, 5)		1000		Ω

LVDS Switching Characteristics

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
t_{CIP}	TxCLKIN Period	See *Figure 1*	3.2	2T	37	ns
t_{CIT}	TxCLKIN Transition Time	See *Figure 2*	0.5	1.0	3.0	ns
t_{CIH}	TxCLKIN IN High Time	See *Figure 1*	0.7T	T	1.3T	ns
t_{CIL}	TxCLKIN IN Low Time	See *Figure 1*	0.7T	T	1.3T	ns
t_{XIT}	TxIN Transition time		0.15		3	ns
t_{STC}	TxIN Setup to TxCLKIN	See *Figure 1*		200		ps
t_{HTC}	TxIN Hold to TxCLKIN	See *Figure 1*		200		ps
t_{TPLD}	Transmit PLL lock time				16	ms

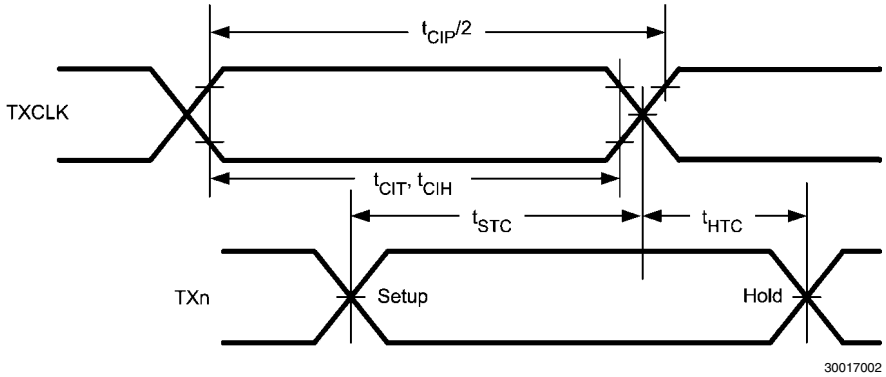


FIGURE 1. LVDS Input Timing Diagram

FIGURE 2. Transmit Clock Transition Times

SMBus Switching Characteristics

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
f_{SMB}	Bus Operating Frequency		10		100	kHz
t_{BUF}	Bus free time between stop and start condition		4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated	At $I_{SPULLUP}$ = MAX	4.0			µs
$t_{SU:STA}$	Repeated Start condition setup time		4.7			µs
$t_{SU:STO}$	Stop Condition setup time		4.0			µs
$t_{HD:DAT}$	Data hold time		300			ns
$t_{SU:DAT}$	Data setup time		250			ns
t_{LOW}	Clock Low Period		4.7			µs
t_{HIGH}	Clock high time		4.0		50	µs
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				1000	ns
t_{POR}	Time in which a device must be operational after power on				500	ms

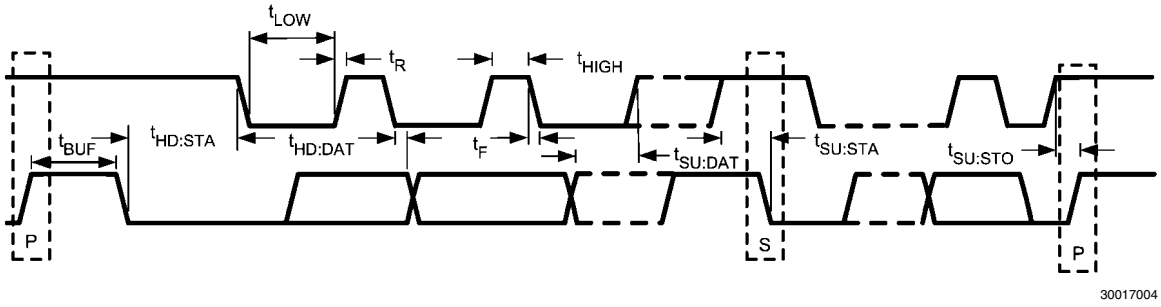


FIGURE 3. SMBus Timing Parameters

SDI Output Switching Characteristics

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
	SDI Output Datarate		270		2970	MHz
t_r	SDI Output Rise Time					ps
t_f	SDI Output Fall Time					ps
t_{BIT}	Bit Width					
t_{SD}	Propagation Delay Latency	See *Figure 4*		t_{CIP}		ns

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
t_J	Peak to Peak Alignment Jitter	≥1,483 Mbps (Note 6)		5.3	60	ps
		≤1,483 Mbps (Note 6)			0.09	UI
RL	Output Return Loss	Measured 5 MHz to 1483 MHz	15	20		dB
t_{OS}	Output Overshoot				8	%

Note 1: "Absolute Maximum Ratings" are limits beyond which the safety of the device cannot be guaranteed. It is not implied that the device will operate up to these limits.

Note 2: Typical Parameters measured at V_{DD}=3.3V, T_A=25°C. They are for reference purposes and are not production tested.

Note 3: Recommended value—Parameter is not tested.

Note 4: Recommended maximum capacitance load per bus segment is 400 pF.

Note 5: Maximum termination voltage should be identical to the device supply voltage.

Note 6: Measured in accordance with SMPTE RP184.

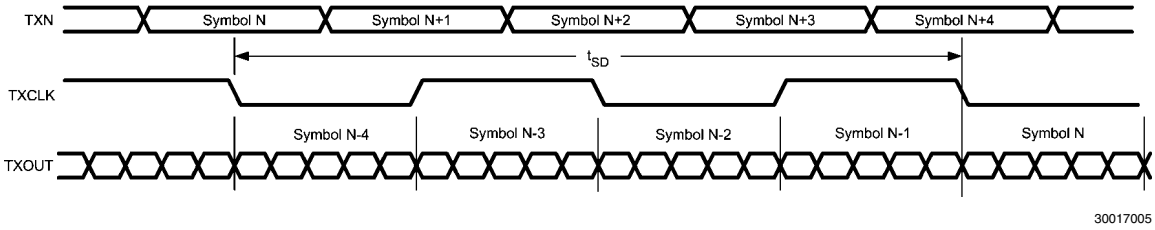


FIGURE 4. LVDS Interface Propagation Delay

Device Operation

The LMH0040 serializer is used in digital video signal origination equipment. It is intended to be operated in conjunction with an FPGA host which preprocesses data for it, and then provides this data over the five bit wide datapath. Provided the host has properly formatted the data for the LMH0040, the output of the device will be compliant with DVB-ASI, SMPTE 259M-C, SMPTE 292M or SMPTE 424M depending upon the output mode selected.

Power Supplies

The LMH0040 has several power supply pins, at 2.5V as well as 3.3V. It is important that these pins all be connected, and properly bypassed. Bypassing should consist of parallel 4.7 µF and 0.1 µF capacitors as a minimum, with a 0.1 µF capacitor on each power pin. The device has a large contact in the center of the bottom of the package. This contact must be connected to the system GND as it is the major ground connection for the device.

Power Up

After the transmitter/receiver is powered up, it goes through a power-on reset procedure, and then enters the link acquisition mode. The transmitter will first acquire the input data and clock, and once this has happened, the transmitter will begin sending serialized data. The data is serialized with the TXIN0 bit being transmitted first, and TXIN4 being the last bit transmitted.

LVDS Inputs

The LMH0040 has standard 3.3V LVDS inputs and is compliant with ANSI/TIA/EIA-644. These inputs have an internal 100Ω resistor across the inputs which allows for the closing of a current loop interface from the LVDS driver in the host. It is recommended that the PCB trace between the FPGA and the transmitter be less than 25 cm. Longer PCB traces may introduce signal degradation as well as channel skew which could cause serialization errors. This connection between the host and the LMH0040 should be over a controlled impedance transmission line with an impedance which matches the termination resistor—usually 100Ω.

DVB_ASI Mode

The LMH0040 has a special mode for DVB-ASI. In this mode, the input signal on TX4+/TX4- is treated as a data valid bit, if high, then the four bit nibbles from TX0–TX3 are taken to form an 8 bit word, which is then converted to a 10 bit code via an internal 8b10b encoder and this 10 bit word is serialized and driven on the output. The nibble taken in on the rising edge of the clock is the most significant nibble and the nibble taken in on the falling edge is the least significant nibble. If TX4+/TX4- is low, then the input on TX0–TX3 are ignored and the 10b idle character is inserted in the output stream.

SDI Output Interfacing

The serial outputs provide low-skew complimentary or differential signals. The output buffer is a current mode design, with a high impedance output. To drive a 75Ω transmission line connect a 75Ω resistor from each of the output pins to 2.5V. This resistor has two functions—it converts the current output to a voltage, which is used to drive the cable, and it acts as the back termination resistor for the transmission line. The resistor should be placed as close to the output pin as is practicable. The output driver automatically adjusts its slew rate depending on the input datarate so that it will be in compliance with SMPTE 259M, SMPTE292M or SMPTE 424M as appropriate. In addition to output amplitude and rise/fall time specifications, the SMPTE specs require that SDI outputs meet an Output Return Loss (ORL) specification. There are parasitic capacitances that will be present both at the output pin of the

device and on the application printed circuit board. To optimize the return loss implement a series network comprised of a parallel inductor and resistor. The actual values for these components will vary from application to application, but the typical interface circuit shows values that would be a good starting point. The LMH0050 does not include the internal cable driver, and its outputs are CML. The LMH0050 outputs may either be connected to a differential transmission medium such as twisted pair cable, or used to drive an external cable driver. The collectors present a high impedance current source. The external 75Ω resistors will provide the back termination resistance as well as converting the current to a voltage—with the addition of the termination resistance at the load, there will be an overall output resistance of 37.5Ω, which in conjunction with the 24 mA current source will develop the 800 mV swings called for in the standard.

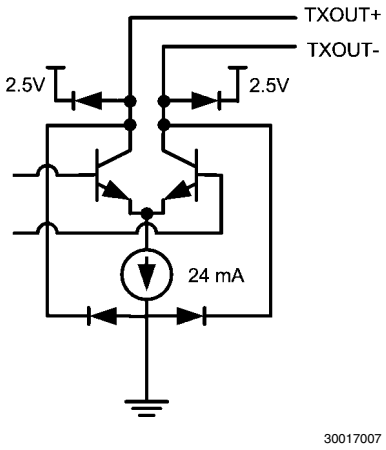


FIGURE 5. SDI Output SIC

SMBus Interface

The System Management Bus (SMBus) is a two wire interface designed for the communication between various system component chips. By accessing the control functions of the circuit via the SMBus, pincount is kept to a minimum while allowing a maximum amount of versatility. The SMBus has three pins to control it: an SMBus CS pin which enables the SMBus interface for the device, a Clock and a Data line. In applications where there might be several LMH0040s, the SDA and SCK pins can be bussed together and the individual devices to be communicated with may be selected via the CS pin. The SCL and SDA are both open drain and are pulled high by external pullup resistors. The LMH0040 has several internal configuration registers which may be accessed via the SMBus.

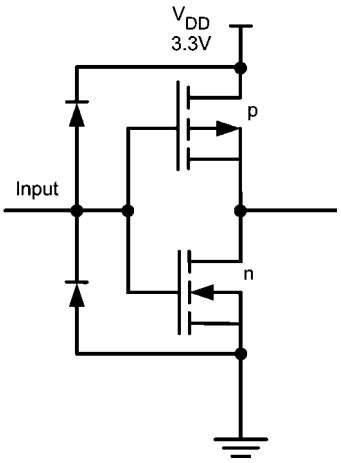


FIGURE 6. SIC CMOS Input

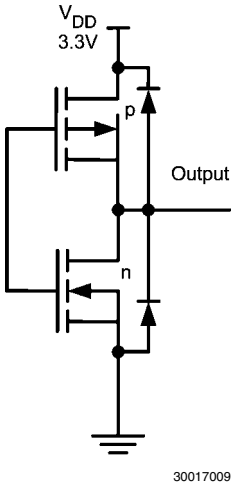


FIGURE 7. SIC CMOS Output

TRANSFER OF DATA TO THE DEVICE VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCK is high. START and STOP conditions—

There are three unique states for the SMBus:

START	A HIGH to LOW transition on SDA while SCK is high indicates a message START condition
STOP	A LOW to HIGH transition on SDA while SCK is high indicates a message STOP condition.
IDLE	If SCK and SDA are both high for a time exceeding t_{BUF} from the last detected STOP condition or if they are high for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus TRANSACTIONS

A transaction begins with the host placing the LMH0040 SMBus into the START condition. Then a byte (8 bits) is transferred, MSB first, followed by a ninth ACK bit. ACK bits are '0' to signify an ACK, or '1' to signify NACK. After this the host holds the SCL line low, and waits for the receiver to raise the SDA line as an ACKnowledge that the byte has been received.

WRITING TO REGISTERS VIA THE SMBus INTERFACE

To write a data value to a register in the LMH0040, the host writes three bytes to the LMH0040. The first byte is the device address—the device address is a 7 bit value, and if writing to the LMH0040 the last bit (LSB) is set to '0' to signify that the operation is a write. The second byte written is the register address, and the third byte written is the data to be written into the addressed register. If additional data writes are performed, the register address is automatically incremented. At the end of the write cycle the host places the bus in the STOP state.

READING FROM REGISTERS VIA THE SMBus INTERFACE

To read the data value from a register, first the host writes the device address with the LSB set to a '0' denoting a write, and then the register address is written to the device. The host then reasserts the START condition, and writes the device address once again, but this time with the LSB set to a '1' denoting a read, and following this the LMH0040 will drive the SDA line with the data from the addressed register. The host indicates that it has finished reading the data by asserting a '1' for the ACK bit. After reading the last byte, the host will assert a '0' for NACK to indicate to the LMH0040 that it does not require any more data.

Note that the SMBus pins are not 5V compliant and they must be driven by a 3.3V source.

General Purpose I/O pins (GPIO)

The LMH0040 has three pins which can be configured to provide direct access to certain register values via a dedicated pin. For example if a particular application required fast action to the condition of the serializer losing it's input clock, the PCLK detect status bit could be routed directly to an external pin where it might generate an interrupt for the host processor. GPIO pins can be configured to be in Tri-State (High Impedance) mode, the buffers can be disabled, and when used as inputs can be configured with a pullup resistor, a pulldown resistor or no input pin biasing at all.

Each of the GPIO pins has a register to control it. For each of these registers, the upper 4 bits are used to define what function is desired of the GPIO pin with options being slightly different for each of the three GPIO pins. The pins can be used to monitor the status of various internal states of the LMH0040 device, to serve as an input from some external stimulus, and for output to control some external function.

$GPIO_0$ FUNCTIONS

- Allow for the output of a signal programmed by the SMBus
- Allow the monitoring of an external signal via the SMBus
- Monitor Status of PCLK LOS signal
- Monitor Status of PCLK Detect
- Monitor Power On Reset

$GPIO_1$ FUNCTIONS

- Monitor Power On Reset
- Allow for the output of a signal programmed by the SMBus
- Allow the monitoring of an external signal via the SMBus
- Monitor LOS for data bit 0
- Monitor LOS for data bit 1
- Monitor LOS for data bit 2
- Monitor LOS for data bit 3
- Monitor LOS for data bit 4

$GPIO_2$ FUNCTIONS

- Allow for the output of a signal programmed by the SMBus
- Allow the monitoring of an external signal via the SMBus
- Serializer Clock output

Bits 2 and 3 are used to determine the status of the internal pullup/pulldown resistors on the device—they are loaded according to the following truth table:

- 00: pullup and pulldown disabled
- 01: pulldown enabled
- 10: pullup enabled
- 11: atp enabled

Bit 1 is used to enable or disable the input buffer. If the GPIO pin is to be used as an output pin, then this bit must be set to a '0' disabling the output.

The LSB is used to switch the output between normal output state and high impedance mode. If the GPIO is to be used as an input pin, this bit must be set to '0' placing the output in high Z mode.

As an example, if you wanted to use the $GPIO_0$ pin to reflect the status of the $\overline{LOCK}$ pin, you would load the appropriate register with the value 0001 0001b.

Potential Applications for GPIO Pins

In addition to being useful debug tools while bringing an LMH0040 design up, there are other practical uses to which the GPIO pins can be put:

PROGRAMMING SEVERAL LMH0040S WITH UNIQUE ADDRESSES

If there were to be a design using a large number of LMH0040 devices all supported by a single host, it might be desirable to have them all share a single SMBus connection, but not have to use separate CS lines from the host. In this case we can buss all of the SCK and SDA pins together, connect the CS line for the first device to GND (always selected) then connect the CS line for each successive part in the chain to the previous LMH0040. On initial power up, program GPIO0 to be 1, which will de-select all but the first LMH0040—now reprogram the address, using this reprogrammed address, drive GPIO to 0, enabling the second LMH0040, which can then have it's address reprogrammend, and so on down the chain until each LMH0040 has a unique address, and all have their CS lines held low.

SENSING IF A CABLE IS CONNECTED TO AN OUTPUT:

When connecting the BNC cable to the output, connect the shield of the connector to GND via a capacitor—making it an AC GND, but a DC open. Now connect that shield to one of the GPIO connections which you configure as an input with a pullup. With no cable on the BNC, the GPIO pin will see a high state, but once a terminated cable is connected, the shield will be brought down and you will read a low state.

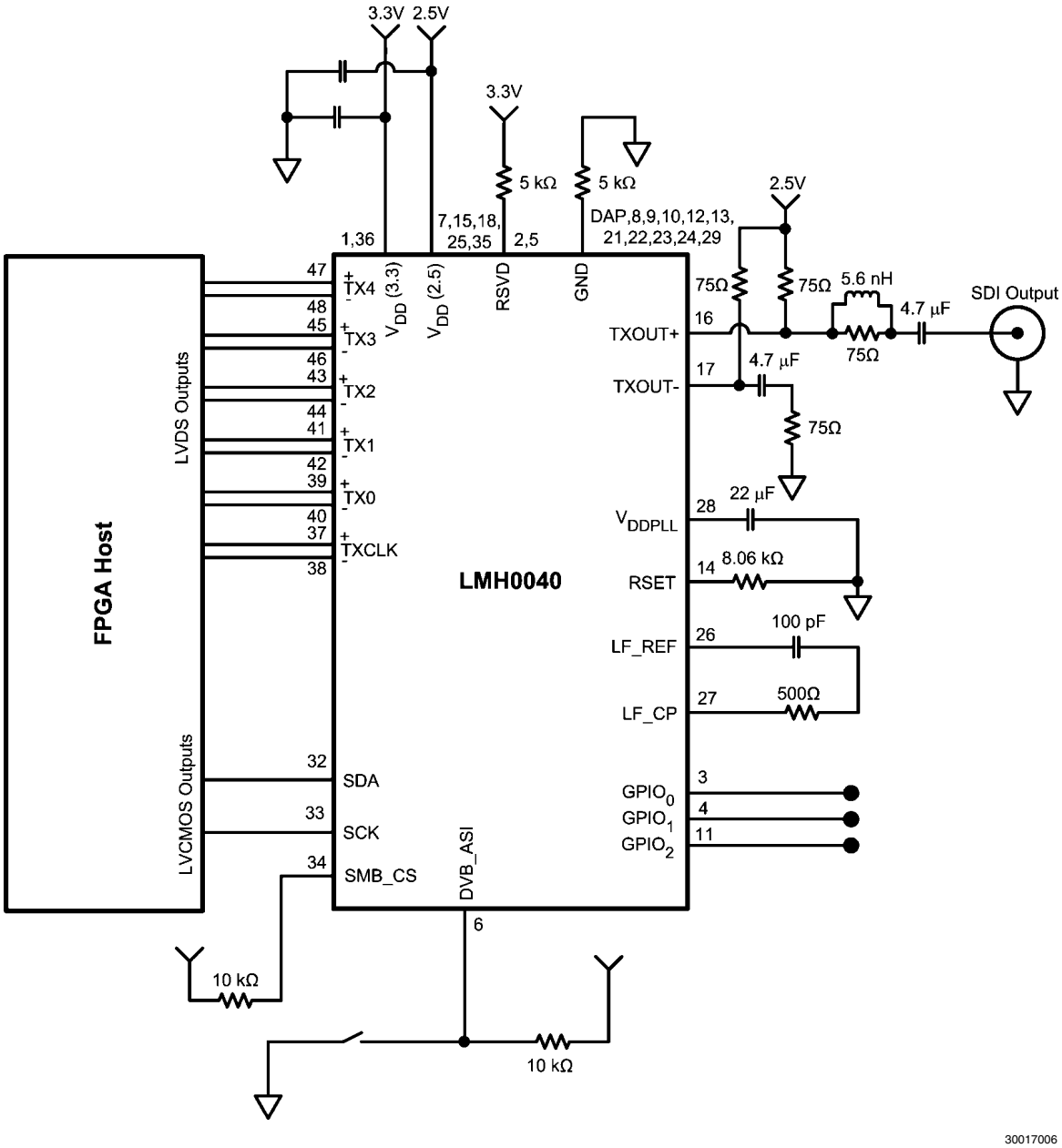
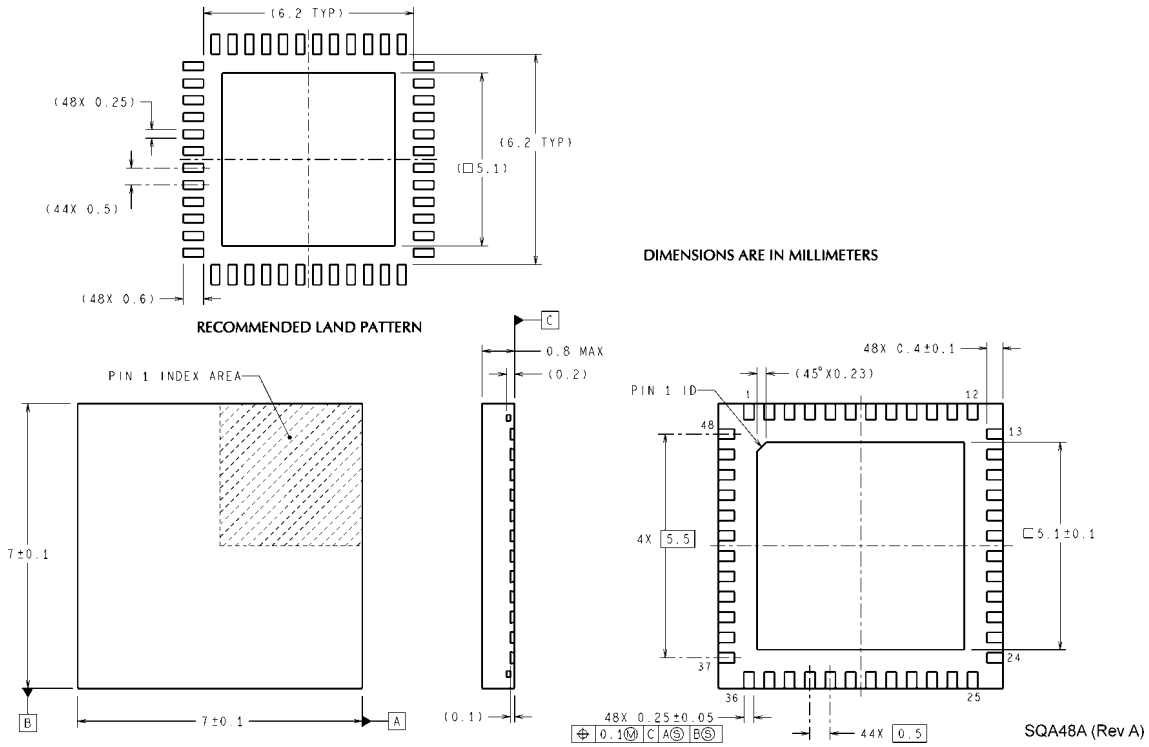


FIGURE 8. TIC

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead QFN Plastic Quad Package
NS Package Number LQA48A

Notes

Notes

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