MIC3385

8MHz Inductorless Buck Regulator with LDO Standby Mode

General Description

The Micrel MIC3385 is a high efficiency inductorless buck regulator that features a *LOWQ*® LDO standby mode that draws only 18µA of quiescent current. The MIC3385 requires no external inductor enabling an ultra-low noise, small size, and high efficiency solution for portable power applications.

In PWM mode, the MIC3385 operates with a constant frequency 8MHz PWM control. Under light load conditions, such as in system sleep or standby modes, the PWM switching operation can be disabled to reduce switching losses. In this light load *LOWQ*® mode, the LDO maintains the output voltage and draws only 18µA of quiescent current. The LDO mode of operation saves battery life while not introducing spurious noise and high ripple as experienced with pulse skipping or bursting mode regulators.

The MIC3385 operates from 2.7V to 5.5V input and features internal power MOSFETs that can supply up to 600mA output current in PWM mode. It can operate with a maximum duty cycle of 100% for use in low-dropout conditions.

The MIC3385 is available in the 14-pin 3mm x 3.5mm MLF® package with a junction operating range from –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

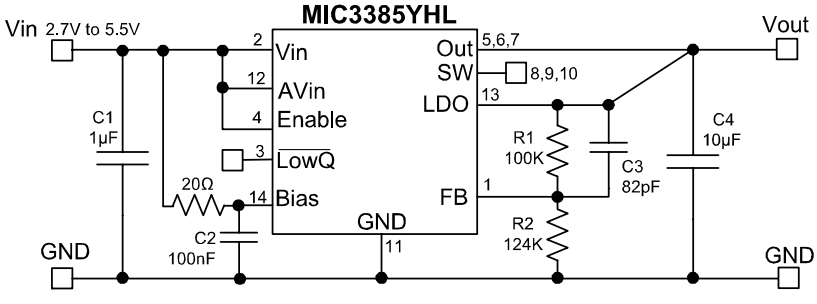
Features

- 2.7 to 5.5V supply voltage
- Light load *LOWQ*® LDO mode
  - 18µA quiescent current
  - Low noise, 75µVrms
- 8MHz PWM mode
  - Output current to 600mA
  - >90% efficiency
  - 100% maximum duty cycle
- Adjustable output voltage option down to 1V
- Ultra-fast transient response
- **NO external inductor required**
- Enables sub 1mm profile solution
- Fully integrated MOSFET switches
- Micropower shutdown
- Thermal shutdown and current limit protection
- Pb-free 14-pin 3x3.5x0.9mm MLF® package
- –40°C to +125°C junction temperature range

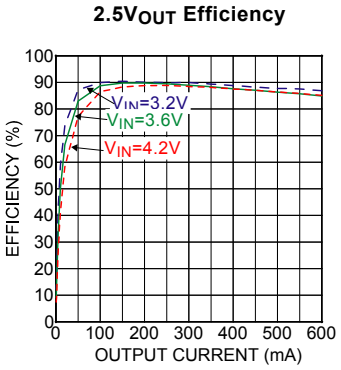
Applications

- Slim digital cameras
- MP3 players
- Portable power applications
- Cellular phones
- PDAs
- USB peripherals

Typical Application



Adjustable Output Buck Regulator with *LOWQ*® Mode



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MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology, Inc.

Ordering Information

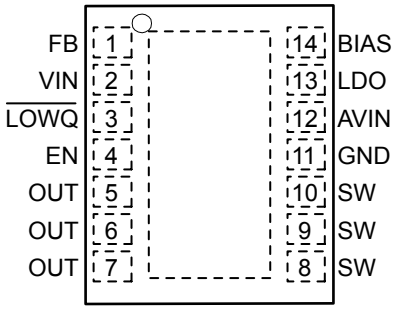
Part Number	Voltage	Temperature Range	Package	Lead Finish
MIC3385YHL	Adj.	–40° to +125°C	14-Pin 3mm x 3.5mm MLF®	Pb-free
MIC3385-1.5YHL	1.5V	–40° to +125°C	14-Pin 3mm x 3.5mm MLF®	Pb-free

Notes:

MLF® is a GREEN RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Other voltage options available. Please contact Micrel for details.

Pin Configuration



14- Pin 3mm x 3.5mm MLF® (ML)

Pin Description

Pin Number	Pin Name	Pin Function
1	FB	Feedback. Input to the error amplifier. Connect to the external resistor divider network to set the output voltage.
2	VIN	Supply Voltage (Input): Supply voltage for the internal switches and drivers.
3	$\overline{\text{LOWQ}}$	Enable LDO Mode (Input): Logic low enables the internal LDO and disables the PWM operation. Logic high enables the PWM mode and disables the LDO mode.
4	EN	Enable (Input). Logic low will shut down the device, reducing the quiescent current to less than 5μA.
5,6,7	OUT	Switch Output after inductor.
8,9,10	SW	Switch (Output): Internal power MOSFET output switches before Inductor
11	GND	Power Ground. Requires input capacitor to GND.
12	AVIN	Analog Supply Voltage (Input): Supply voltage for the analog control circuitry and LDO input power. Requires bypass capacitor to GND.
13	LDO	LDO Output (Output): Connect to V_{OUT} for LDO mode operation.
14	BIAS	Internal circuit bias supply. Must be de-coupled to signal ground with a 0.1μF capacitor and should not be loaded.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}) ..... +6V
Output Switch Voltage (V_{SW}) ..... +6V
Output Switch Current (I_{SW}) 2A
Logic Input Voltage (V_{EN}, V_{LOWQ}) ..... –0.3V to V_{IN}
Storage Temperature (T_s) ..... –60°C to +150°C
EDS Rating[3] 3kV

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +2.7V to +5.5V
Logic Input Voltage (V_{EN}, V_{LOWQ}) ..... –0.3V to V_{IN}
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
3x3.5 MLF-14 (θ_{JA}) ..... 55°C/W

Electrical Characteristics[4]

$V_{IN} = V_{EN} = V_{LOWQ}$ =3.6V; L = 0.47µH; C_{OUT} = 10µF; T_A = 25°C, unless noted. **Bold** values indicate –40°C≤ T_J ≤ +125°C.

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage Range		**2.7**		**5.5**	V
Under-Voltage Lockout Threshold	(turn-on)	2.45	2.55	2.65	V
UVLO Hysteresis			100		mV
Quiescent Current, PWM mode	V_{FB} = 0.9 * V_{NOM} (not switching)		690	**900**	µA
Quiescent Current, LDO mode	$V_{\overline{LOWQ}}$ = 0V;I_{OUT} = 0mA		16	**29**	µA
Shutdown Current	V_{EN} = 0V		0.01	**5**	µA
[Adjustable] Feedback Voltage	± 1% ± 2% (over temperature)	0.99 **0.98**	1	1.01 **1.02**	V V
FB pin input current			1		nA
Current Limit in PWM Mode	V_{FB} = 0.9 * V_{NOM}	**0.75**	1	**1.85**	A
Output Voltage Line Regulation	V_{OUT} > 2V; V_{IN} = V_{OUT}+300mV to 5.5V; I_{LOAD}= 100mA V_{OUT} < 2V; V_{IN} = 2.7V to 5.5V; I_{LOAD}= 100mA		0.13		%
Output Voltage Load Regulation, PWM Mode	20mA < I_{LOAD} < 300mA		0.2		%
Output Voltage Load Regulation, LDO Mode	100µA < I_{LOAD} < 50mA V_{LOWQ} = 0V		0.1		%
Maximum Duty Cycle	V_{FB} ≤ 0.4V	**100**			%
PWM Switch ON-Resistance	I_{SW} = 50mA V_{FB} = 0.7V_{FB_NOM} (High Side Switch) I_{SW} = -50mA V_{FB} = 1.1V_{FB_NOM} (Low Side Switch)		0.4 0.4		Ω
Oscillator Frequency		**7.2**	8	**8.8**	MHz
$\overline{LOWQ}$ threshold voltage		0.5	0.85	**1.3**	V
$\overline{LOWQ}$ Input Current			0.1	**2**	µA
Enable Threshold		**0.5**	0.85	**1.3**	V
Enable Input Current			0.1	**2**	µA
LDO Dropout Voltage	I_{OUT} = 50mA, **Note 5**		110		mV

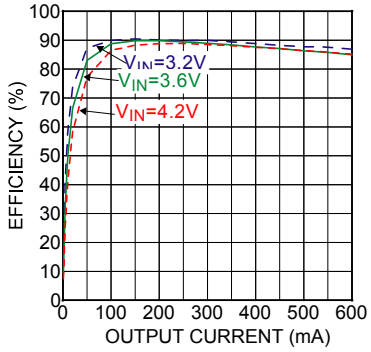
Parameter	Condition	Min	Typ	Max	Units
Output Voltage Noise	$\overline{LOWQ}$ = 0V; C_{OUT} = 10µF, 10Hz to 100kHz		75		µVrms
LDO Current Limit	$\overline{LOWQ}$ = 0V; V_{OUT} = 0V (LDO Mode)	**60**	120		mA
Over-Temperature Shutdown			160		°C
Over-Temperature Hysteresis			20		°C
Internal Inductor			0.47		µH

Notes:

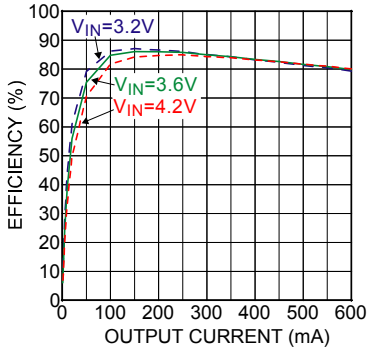
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model: 1.5kΩ in series with 100pF.
4. Specification for packaged product only.
5. Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value that is initially measured at a 1V differential. For outputs below 2.7V, the dropout voltage is the input-to-output voltage differential with a minimum input voltage of 2.7V.

Typical Characteristics — PWM Mode

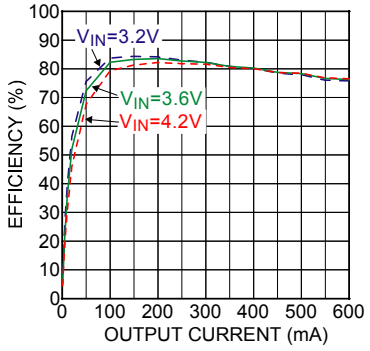
2.5V$_{OUT}$ Efficiency



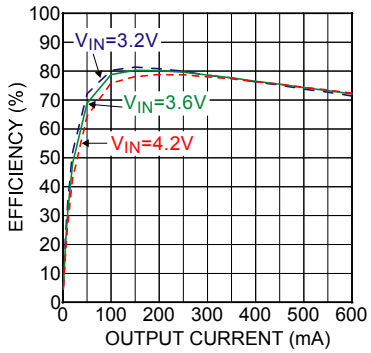
1.8V$_{OUT}$ Efficiency



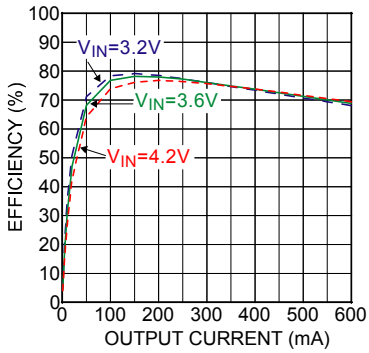
1.5V$_{OUT}$ Efficiency



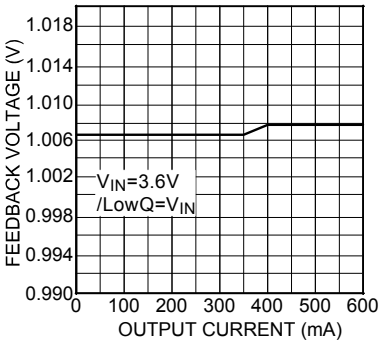
1.2V$_{OUT}$ Efficiency



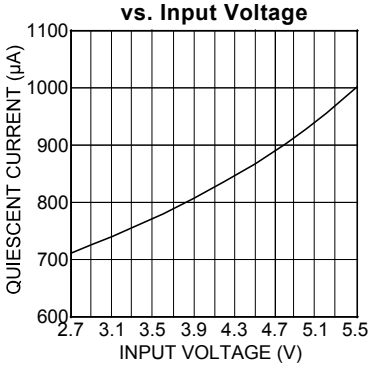
1.0V$_{OUT}$ Efficiency



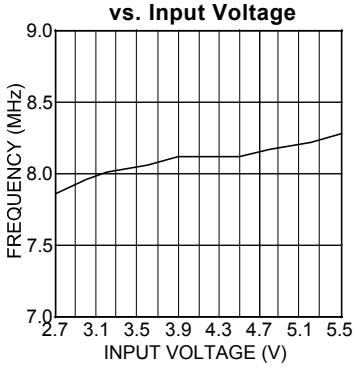
Load Regulation



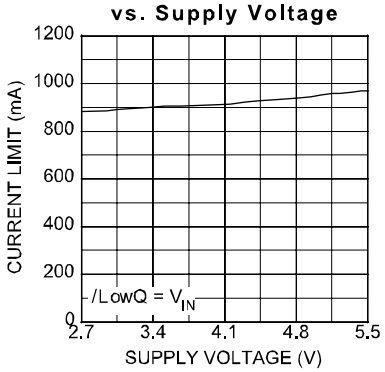
Quiescent Current vs. Input Voltage



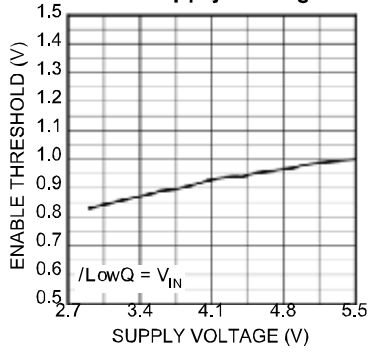
Frequency vs. Input Voltage



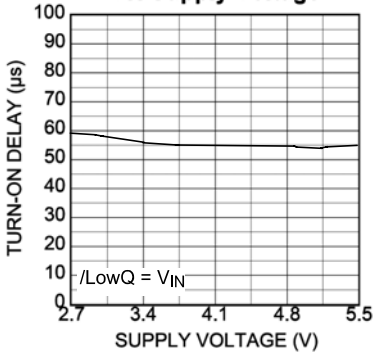
Peak Current Limit vs. Supply Voltage



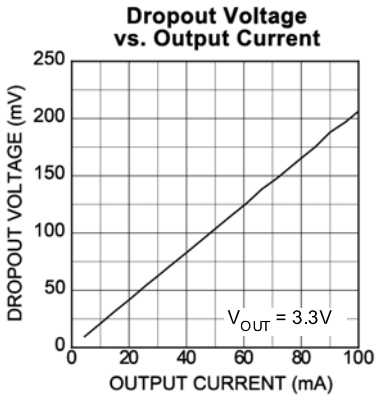
Enable Threshold vs. Supply Voltage

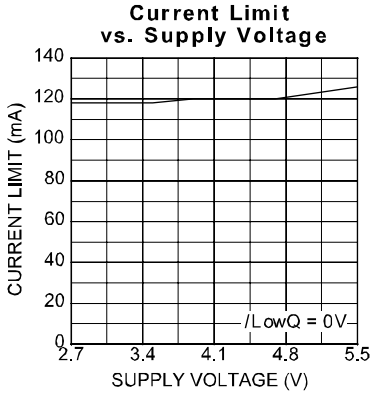


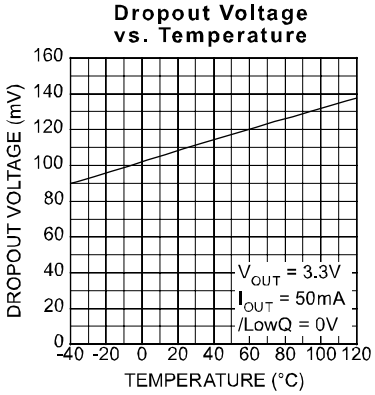
Turn-On Time vs. Supply Voltage

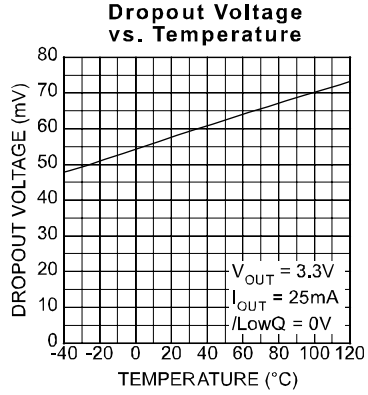


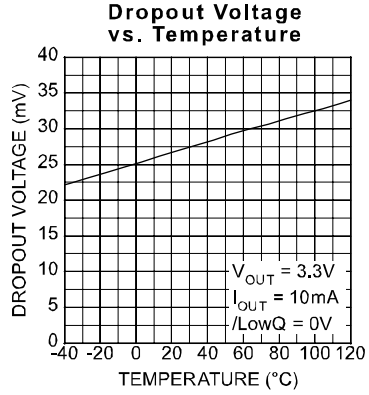
Typical Characteristics — LDO Mode

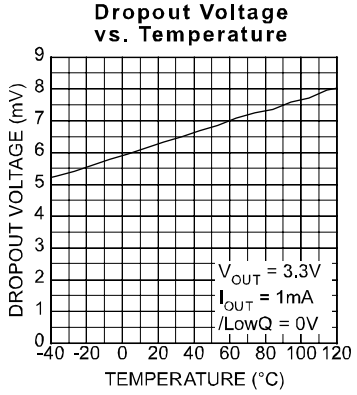


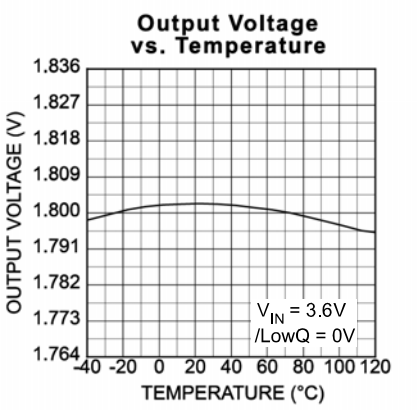


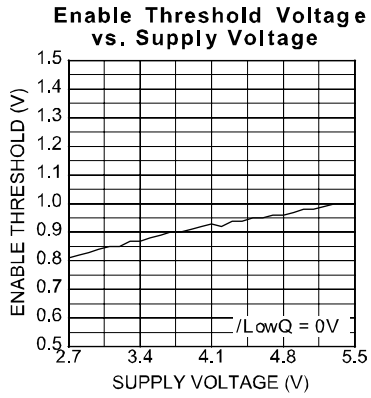


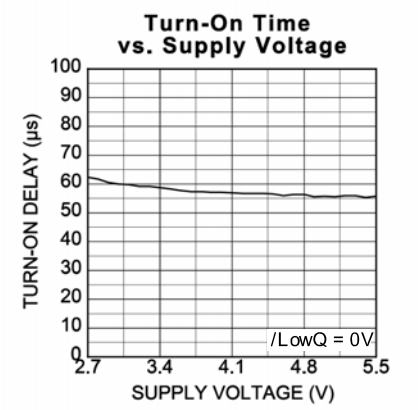


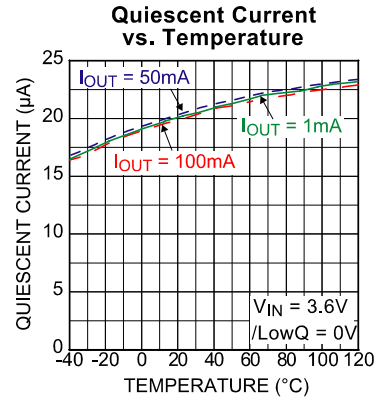


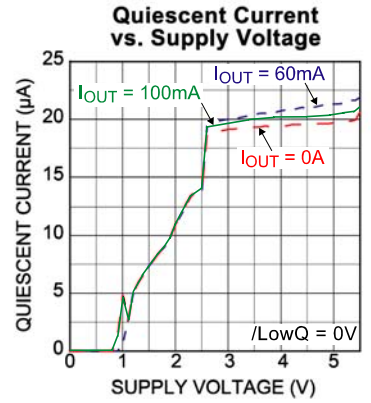


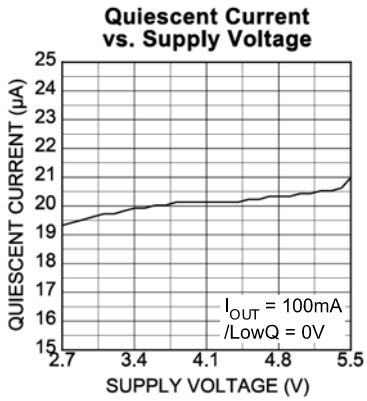




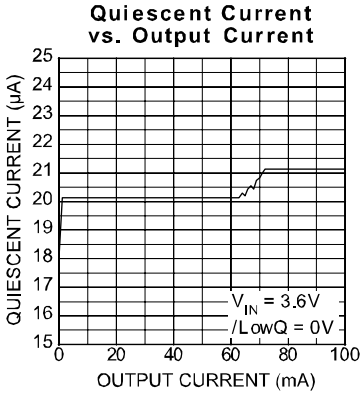


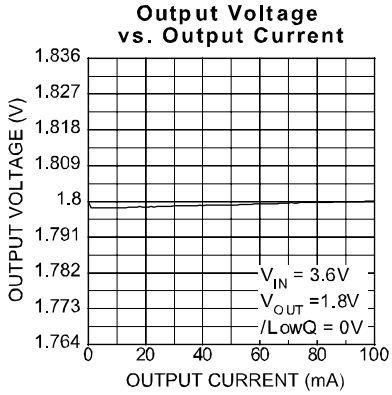






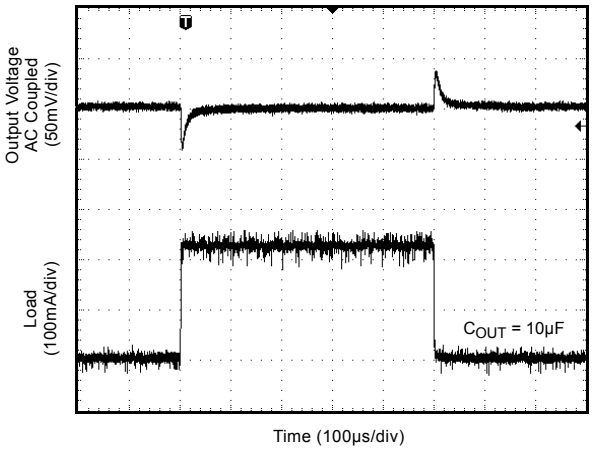
Typical Characteristics — LDO Mode (cont.)



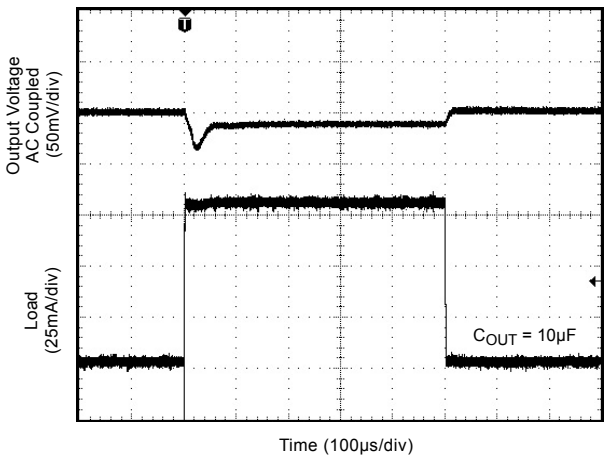


Functional Characteristics

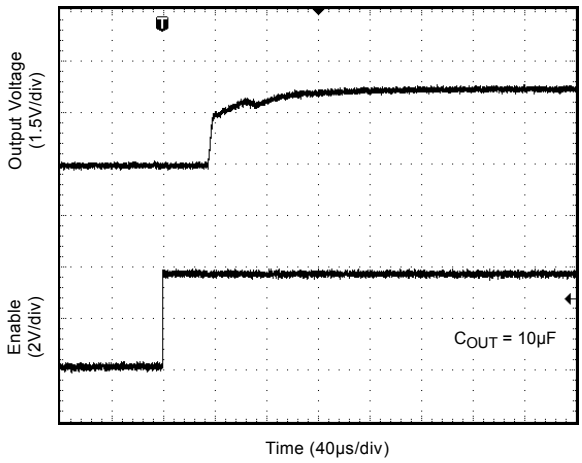
Load Transient PWM Mode



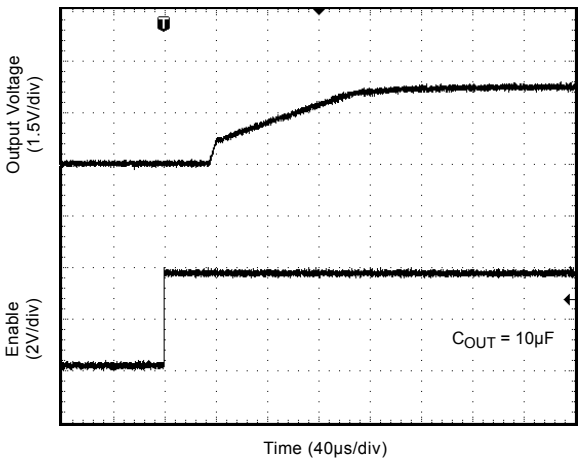
Load Transient LDO Mode



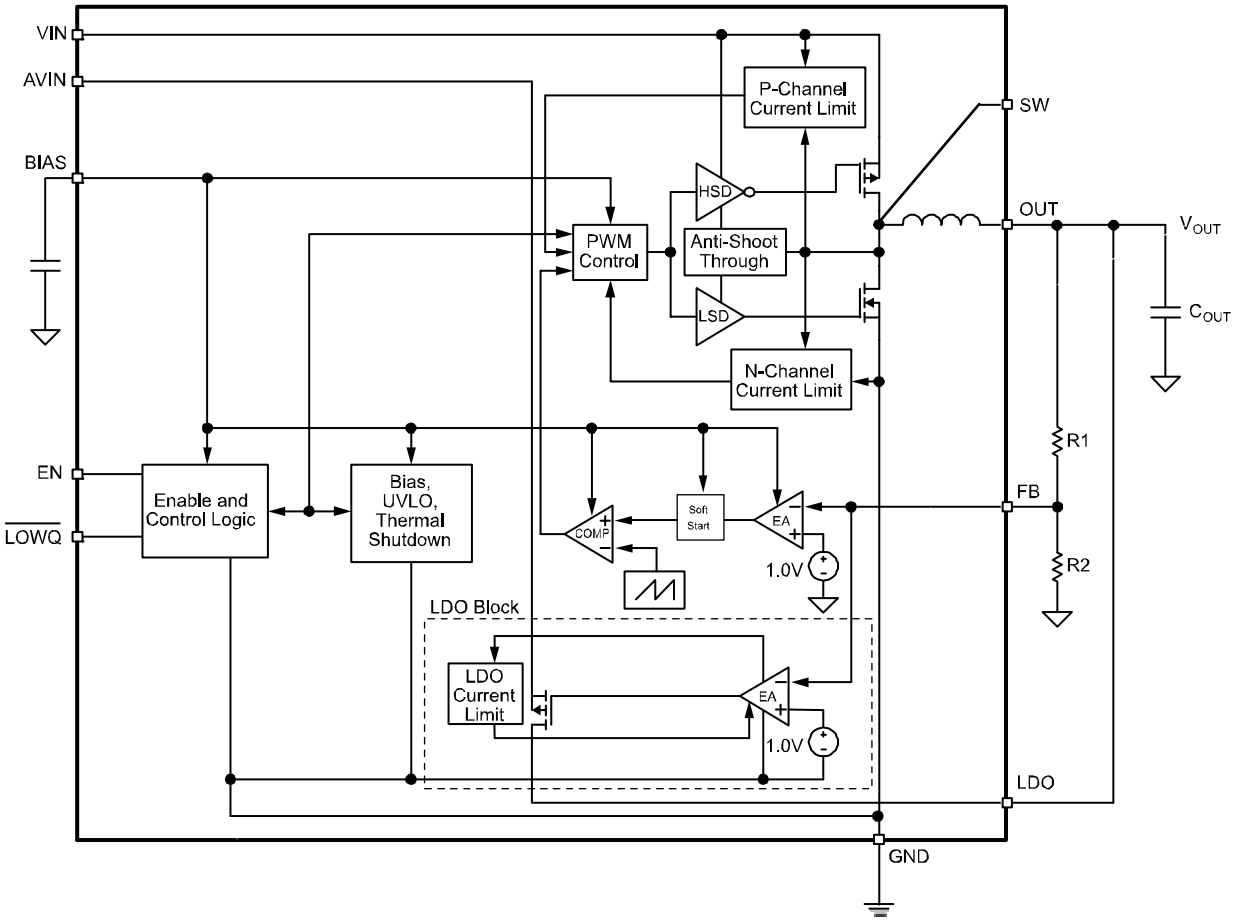
Enable Transient PWM Mode



Enable Transient LDO Mode



Functional Diagram



MIC3385 Block Diagram

Functional Description

VIN

VIN provides power to the MOSFETs for the switch mode regulator section, along with the current limiting sensing. Due to the high switching speeds, a 1µF capacitor is recommended to ground (GND) pin for bypassing. Please refer to layout recommendations.

AVIN

Analog V_{IN} (AVIN) provides power to the LDO subsection and the bias through an internal 6Ω resistor. AVIN and VIN must be tied together. Careful layout should be considered to ensure that high frequency switching noise caused by VIN is reduced before reaching AVIN.

LDO

The LDO pin is the output of the linear regulator and should be connected to the output. In $\overline{\text{LOWQ}}$ mode ($\overline{\text{LOWQ}}$ < 1.5V), the LDO provides the output voltage. In PWM mode ($\overline{\text{LOWQ}}$ > 1.5V) the LDO pin is high impedance.

EN

The enable pin provides a logic level control of the output. In the off state, supply current of the device is greatly reduced (typically <1µA). Also, in the off state, the output drive is placed in a "tri-stated" condition, where both the high side P-channel MOSFET and the low-side N-channel are in an “off” or non-conducting state. Do not drive the enable pin above the supply voltage.

$\overline{\text{LOWQ}}$

The $\overline{\text{LOWQ}}$ pin provides a logic level control between the internal PWM mode and the low noise linear regulator mode. With LOWQ pulled low (<0.5V), quiescent current of the device is greatly reduced by switching to a low noise linear regulator mode that has a typical I_Q of 18µA. In linear (LDO) mode the output can deliver 60mA of current to the output. By placing $\overline{\text{LOWQ}}$ high (>1.5V), this transitions the device into a constant frequency PWM buck regulator mode. This allows the device the ability to efficiently deliver up to 600mA of output current at the same output voltage.

BIAS

The BIAS pin supplies the power to the internal power to the control and reference circuitry. The bias is powered from input voltage through an RC lowpass filter. The RC lowpass filter frequency is:

$$\geq \frac{1}{2\pi(20)\Omega(100\text{nF})}$$

FB

The feedback pin (FB) provides the control path to control the output. For adjustable versions, a resistor divider connecting the feedback to the output is used to adjust the desired output voltage. The output voltage is calculated as follows:

$$V_{OUT} = V_{REF} \times \left(\frac{R1}{R2} + 1\right)$$

where V_{REF} is equal to 1.0V.

A feedforward capacitor is recommended for most designs using the adjustable output voltage option. To reduce battery current draw, a 100K feedback resistor is recommended from the output to the FB pin (R1). Also, a feedforward capacitor should be connected between the output and feedback (across R1). The large resistor value and the parasitic capacitance of the FB pin can cause a high frequency pole that can reduce the overall system phase margin. By placing a feedforward capacitor, these effects can be significantly reduced. Feedforward capacitance (C_{FF}) can be calculated as follows:

$$C_{FF} = \frac{1}{2\pi \times R1 \times 160\text{kHz}}$$

For fixed options a feedforward capacitor from the output to the FB pin is required. Typically a 100pF small ceramic capacitor is recommended

SW

The switch (SW) pin connects directly to the inductor and provides the switching current necessary to operate in PWM mode. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

GND

Combines PGND and SGND

Power ground (PGND) is the ground path for the high current PWM mode. Signal ground (SGND) is the ground path for the biasing and control circuitry.

Application Information

The MIC3385 is a 600mA PWM power supply that utilizes a $\overline{\text{LOWQ}}$ light load mode to maximize battery efficiency in light load conditions. This is achieved with a $\overline{\text{LOWQ}}$ control pin that when pulled low, shuts down all the biasing and drive current for the PWM regulator, drawing only 18µA of operating current. This allows the output to be regulated through the LDO output. It is capable of providing 60mA of output current. This method has the advantage of producing a clean, low current, ultra low noise output in $\overline{\text{LOWQ}}$ mode. During $\overline{\text{LOWQ}}$ mode, the SW node becomes high impedance, blocking current flow. Other methods of reducing quiescent current, such as pulse frequency modulation (PFM) or bursting techniques create large amplitude, low frequency ripple voltages that can be detrimental to system operation.

When more than 60mA is required, the $\overline{\text{LOWQ}}$ pin can be forced high, causing the MIC3385 to enter PWM mode. In this case, the LDO output makes a "hand-off" to the PWM regulator with virtually no variation in output voltage. The LDO output then turns off allowing up to 600mA of current to be efficiently supplied through the PWM output to the load.

Input Capacitor

A minimum 1µF ceramic is recommended on the VIN pin for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended.

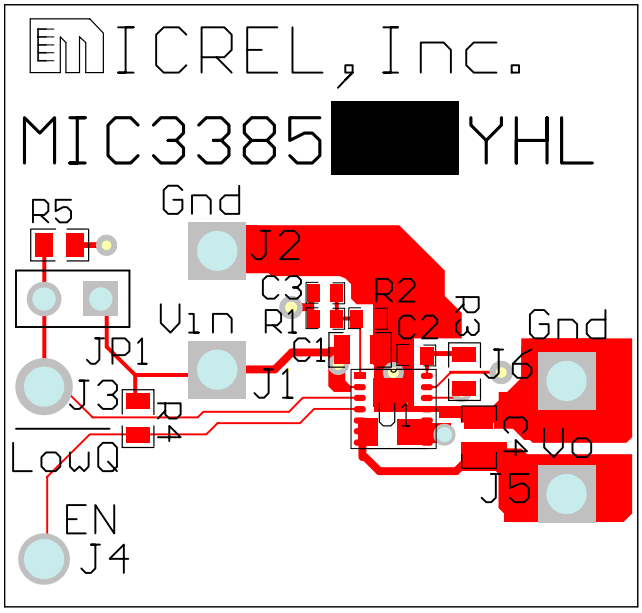
A minimum 1µF is recommended close to the VIN and PGND pins for high frequency filtering. Smaller case size capacitors are recommended due to their lower ESR and ESL. Please refer to layout recommendations for proper layout of the input capacitor.

Output Capacitor

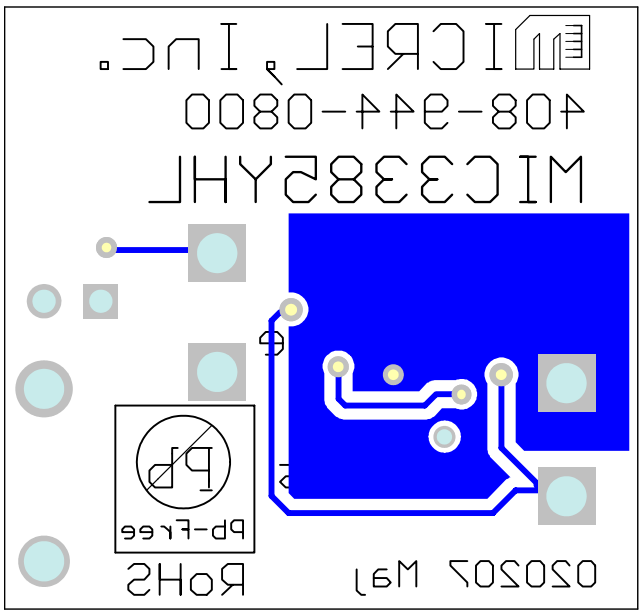
The MIC3385 is optimized for a 10µF output capacitor. A larger value can be used to improve transient response The MIC3385 utilizes type III internal compensation and utilizes an internal high frequency zero to compensate for the double pole roll off of the LC filter. For this reason, larger output capacitors can create instabilities. X5R or X7R dielectrics are recommended for the output capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended.

In addition to a 10µF, a small 10nF is recommended close to the load for high frequency filtering. Smaller case size capacitors are recommended due to there lower ESR and ESL.

Layout Recommendations



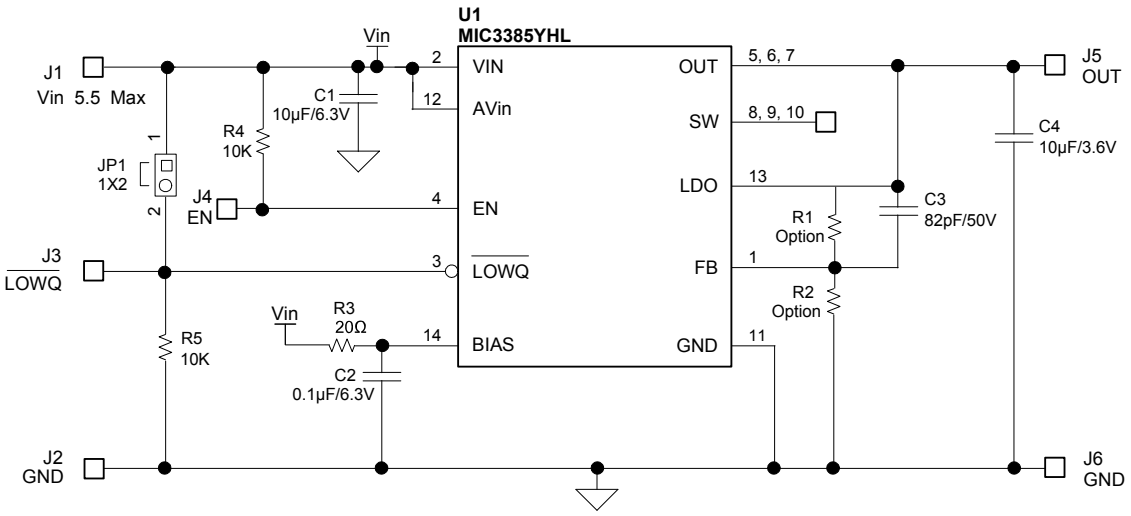
Top Layer



Bottom Layer

Note:

The above figures demonstrate the recommended layout for the MIC3385 adjustable option.



MIC3385 Adjustable Output Schematic

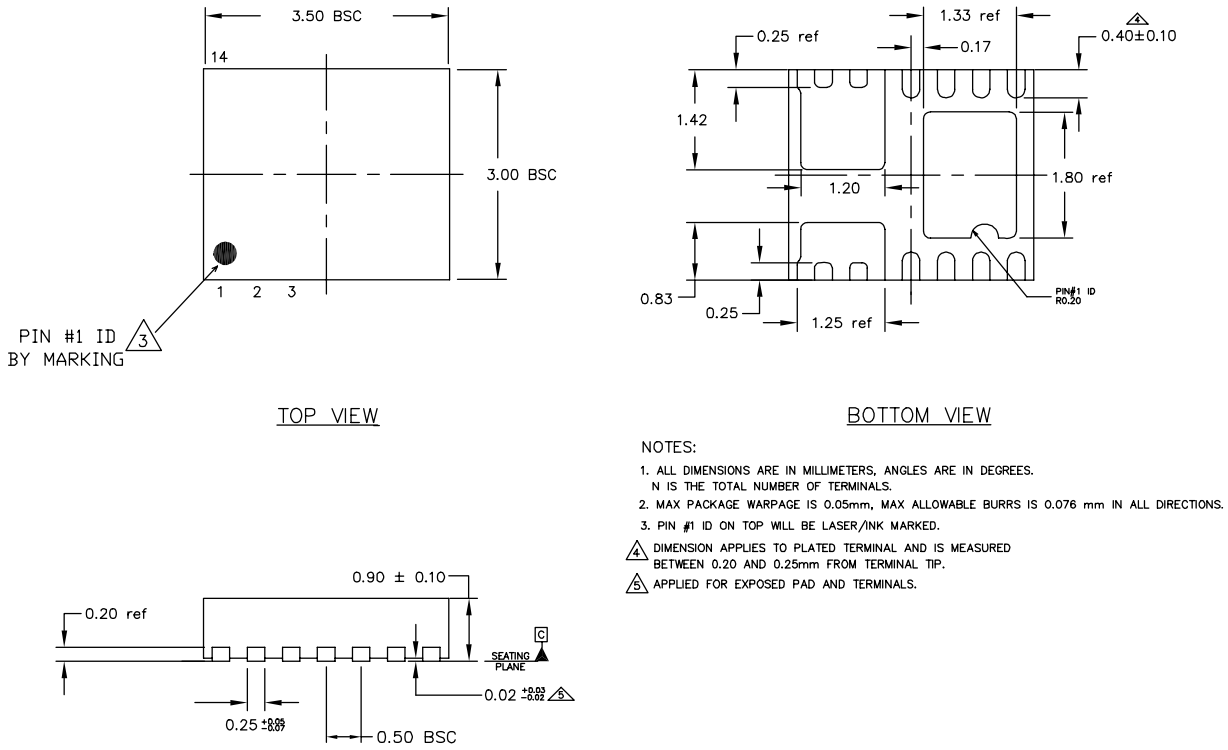
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C4	C1608X5R0J106K	TDK[1]	10µF Ceramic Capacitor X5R, 6.3V	2
	JMK107BJ106MA-T	Taiyo Yuden[2]		
	GRM188R60J106M	Murata[3]	10µF Ceramic Capacitor X7R, 6.3V	2
C2	C1005X5R0J104M	TDK[1]	1µF Ceramic Capacitor X5R, 6.3V	1
	04026D104MAT2A	AVX[4]		
	VJ0402Y104KXQPW1BC	Vishay[5]	1µF Ceramic Capacitor X7R, 6.3V	1
C3	C1005COG1H820J	TDK[1]	82pF Ceramic Capacitor COG, 50V	1
	VJ0402A80KXQPW1BC	Vishay[5]	82pF Ceramic Capacitor COG, 10V	1
R1	CRCW04021003FKEYE3	Vishay[5]	100K, 1% 0402, 1/16W (Optional)	1
R2	CRCW04021243FKEYE3	Vishay[5]	124K, 1% 0402, 1/16W (Optional)	1
R3	CRCW060320R0FKEYE3	Vishay[5]	20Ω, 1% 0603, 1/16W	1
R4, R5	CRCW06031002FKEYE3	Vishay[5]	10K, 1% 0603, 1/16W	1
U1	**MIC3385YHL**	**Micrel, Inc.[6]**	**8MHz Power System Module w/LDO Standby Mode**	**1**

Notes:

1. TDK: www.tdk.com
2. Taiyo Yuden, Inc.: www.t-yuden.com
3. Murata: www.murata.com
4. AVX: www.avxcorp.com
5. Vishay: www.website.com
6. **Micrel, Inc.: www.micrel.com**

Package Information



14-Pin 3mm x 3.5mm HMLF (HL)

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