MIC3832/3833

Current-Fed PWM Controllers

Not Recommended for New Designs

General Description

The MIC3832 and MIC3833 are unique PWM controllers designed for current-fed, multiple-output or push-pull, switched-mode power supply applications.

The MIC3832/3 features UVLO (undervoltage lockout) with hysteresis, soft start with a programmable time constant, cycle-by-cycle current limiting, a PWM latch to prevent multiple outputs due to noise or ringing, and front-edge blanking.

Current-fed topologies eliminate core saturation problems caused by shoot through (cross conduction) of push-pull circuits and reduce stress on the switching transistors.

The MIC3832/3 has one PWM stage capable of operating up to 500kHz and two output stages, Q and $\overline{Q}$, that operate at one-half of the system frequency at a fixed 50% duty cycle.

The MIC3832 UVLO circuit permits startup when the supply is above 15.9V and forces shutdown when the supply drops below 9.8V. The MIC3833 starts up above 8.3V and shuts down below 7.8V. An internal 22V zener diode provides low power overvoltage protection.

The three output stages are totem-pole drivers capable of 1A peak current to external power MOSFETs, BJTs, or IGBTs.

The Q and $\overline{Q}$ outputs have an intentional 50ns overlap (no dead time).

Features

- 15.9V startup, up to 21V operation (MIC3832)
  8.3V startup, up to 21V operation (MIC3833)
- 9.8V undervoltage lockout (MIC3832)
  7.8V undervoltage lockout (MIC3833)
- 0.5mA maximum startup current (40µA typical)
- 17mA typical operating current
- 50ns maximum rise and fall times
- 30kHz to 500kHz RC oscillator
- Voltage or current-mode control
- Cycle-by-cycle current limit
- Soft start function
- 5V 2% reference sources 20mA
- Totem-pole output drive stages
  1A peak output drive current
- 22V zener clamp on supply pin
- PWM latch eliminates false outputs from noise or ringing
- Adjustable maximum duty-cycle limit
- 5MHz bandwidth error amplifier

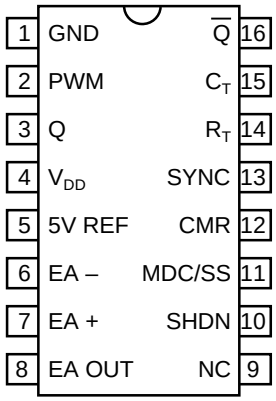
Applications

- High-power, multiple-output, switched-mode power supplies and dc-to-dc Converters
- Current-fed, push-pull, switched-mode power supplies or dc-to-dc converters
- Isolated high-voltage supplies

Ordering Information

Part Number	Temperature Range	Package
MIC3832BN	–40°C to +85°C	16-pin Plastic DIP
MIC3832BWM	–40°C to +85°C	16-pin Wide SOIC
MIC3833BN	–40°C to +85°C	16-pin Plastic DIP
MIC3833BWM	–40°C to +85°C	16-pin Wide SOIC

Pin Configuration



DIP (N) or Wide SOIC (WM)

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Pin Description

Pin Number	Pin Name	Pin Function
1	GND	Ground: Use as single-point ground tie point.
2	PWM	PWM Output: Variable duty-cycle totem pole output.
3	Q	Switch (Output): Totem pole output. Noninverting 50% duty cycle output (180° out-of-phase with $\overline{Q}$ with no dead time).
4	V_{DD}	Supply Voltage (Input): Clamped to 22V by internal zener diode.
5	5V REF	5V Bandgap Reference (Output)
6	EA –	Inverting Error Amplifier Input
7	EA +	Noninverting Error Amplifier Input
8	EA OUT	Error Amplifier Output: Connect to the appropriate feedback network to adjust the open loop gain or frequency response.
9	NC	No Connection: Do not use—leave open.
10	SHDN	Overcurrent Shutdown (Input): >1 V disables outputs, >1.25V initiates soft-start restart. For cycle-by-cycle current limiting, even in voltage-mode control applications, connect to current sensor. If current sense is not used, connect to GND.
11	MDC/SS	Maximum Duty Cycle/Soft Start (Input): Apply a dc voltage to adjust maximum duty cycle (see chart). Adjust soft start by adding capacitance to increase turn-on time during initial start up or restart after overcurrent shutdown.
12	CMR	Current Mode Ramp: Feed point for a sample of inductor current when using current mode control. For voltage-mode control, connect directly to the C_T pin.
13	SYNC	Synchronization (Input): AC coupled input from an external master clock (reference) signal. If not used, leave unconnected. A high (>1.5V) resets the C_T ramp.
14	R_T	Oscillator Timing Resistor: Connect 4kΩ minimum resistor to GND.
15	C_T	Oscillator Timing Capacitor: Connect capacitor to GND. See “Typical Characteristics: Discharge Time” graph for capacitor value. $\text{Maximum oscillator frequency} = \frac{1}{2 \times (\text{discharge time})}$
16	$\overline{Q}$	Switch (Output): Totem pole output. Inverting 50% duty cycle output (180° out-of-phase with Q with no deadtime).

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Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{DD} (continuous) 22V
Source/Sink Load Current (peak) 1A
Maximum Supply (Zener) Current 50mA
Junction Temperature ..... 150°C
Lead Temperature, Soldering ..... 260°C for 10s
θ_{JA} Plastic DIP ..... 130°C/W

Operating Ratings

Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range ..... –40°C to +85°C
Reference Load Current 25mA
Supply Voltage (V_{DD}): MIC3832 ..... 16V to 21V
Supply Voltage (V_{DD}): MIC3833 ..... 7.6V to 21V
Oscillator Frequency Range ..... 10kHz to 500kHz
Oscillator Timing Resistor ..... 3kΩ to 100kΩ
Oscillator Timing Capacitor ..... 1nF to 10nF

Electrical Characteristics (Notes 2, 3)

T_A = –40°C to +85°C, V_{DD} = 15V, f = 52kHz unless otherwise specified.

Parameter	Conditions	Min	Typical	Max	Units
Reference Section					
Output Voltage	I_o = 1mA, T_A = 25°C	4.90	5.0	5.10	V
Input Regulation	V_{CC} = 12V to 20V		5	20	mV
Output Regulation	I_O = 1mA to 20mA		6	25	mV
Temperature Stability			–0.2		mV/°C
Total Output Variation			50		mV
Output Noise Voltage	f = 10Hz to 10kHz, T_A = 25°C		50		µV
Long Term Stability	T_A = 125°C, 1000hrs.		5.0		mV
Output Short Circuit Current	V_{REF} = 0	25	60	160	mA
Oscillator Section					
Frequency	T_A = 25°C, R_T = 16kΩ, C_T = 2.2nF	47	52	57	kHz
Voltage Stability	V_{CC} = 12V to 20V		0.5		%
Amplitude (C_t)			1.7		V_{P-P}
Discharge Current	T_A = 25°C	1	2.3	5	mA
Synchronization	ac coupled		1.5		V
Error Amplifier Section					
Input Offset Voltage		–15	±2	15	mV
Input Bias Current			0.6	3.0	µA
Input Offset Current			0.1	1.0	µA
Open Loop Gain	1V < V_O < 4V	60	82		dB
CMRR	1.5V < V_{CM} < 4.5V	75	95		dB
PSRR	12V < V_{DD} < 20V	85	120		dB
Output Sink Current	$V_{EA\ OUT}$ = 1V	1.0	2.5		mA
Output Source Current	$V_{EA\ OUT}$ = 4V	–0.5	–1.3		mA
Output High Voltage	$I_{EA\ OUT}$ = –0.5mA	4.0	4.9	5.0	V
Output Low Voltage	$I_{EA\ OUT}$ = 1mA		0.6	1.0	V
Soft Start/Max Duty Cycle Section					
Bias Current			–0.05		µA
Discharge Current		1	3		mA
Duty Cycle Clamp Accuracy		40	50	60	%

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Parameter	Conditions	Min	Typical	Max	Units
Current Limit/Shutdown Section					
Bias Current			–0.02		µA
Current Limit Threshold		0.9	1.0	1.1	V
Shutdown Threshold		1.125	1.25	1.375	V
Delay to Output			400	600	ns
Front Edge Blanking Time			140		ns
PWM Comparator Section					
Bias Current	measured at CMR (pin 12)	–2	–0.05	2	µA
Duty Cycle Range	C = 2.2nF	0		85	%
Delay to Output			300	500	ns
Output Sections					
Output Low Level	I_{SINK} = 20mA		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.5	V
Output High Level	I_{SOURCE} = 20mA	12.5			V
	I_{SOURCE} = 200mA	12	13.1		V
Rise Time	C_L = 1000pF		50	150	ns
Fall Time	C_L = 1000pF		50	150	ns
UVLO Saturation	I_{SINK} = 1mA		0.7	1.1	V
Q to $\overline{Q}$ Overlap	Q rising, $\overline{Q}$ falling, 50%		50		ns
$\overline{Q}$ to Q Overlap	$\overline{Q}$ rising, Q falling, 50%		50		ns
Undervoltage Lockout Section					
Upper Threshold—Startup	MIC3832		15.9		V
	MIC3833		8.3		V
Lower Threshold—Operating	MIC3832		9.8		V
(Shutdown)	MIC3833		7.8		V
Total Standby Current					
Startup Current			0.04	0.2	mA
Operating Supply			17		mA
V_{CC} Zener Voltage	I_{CC} = 25mA		22		V

Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2 Minimum and maximum Electrical Characteristics are 100% tested at T_A = 25°C and T_A = 85°C, and 100% guaranteed over the entire range. Typicals are characterized at 25°C and represent the most likely parametric norm.

Note 3 All pins ESD protected to 2kV. Test conditions: Supply pin grounded; all other pins floating.

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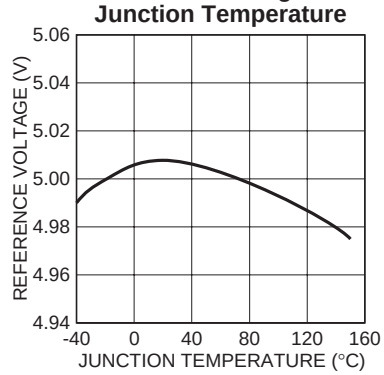
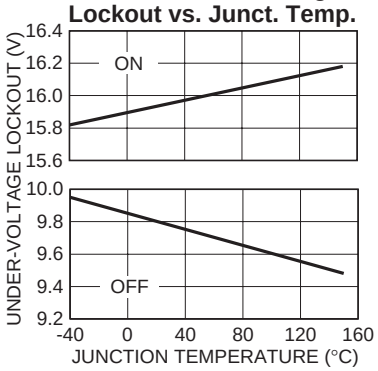
Typical Characteristics

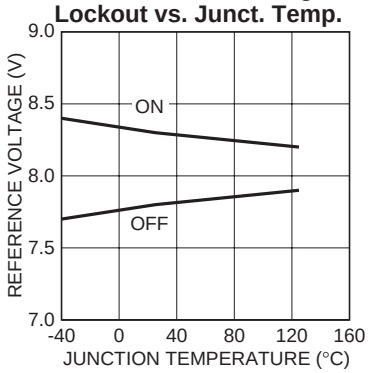
Reference Voltage vs. Junction Temperature



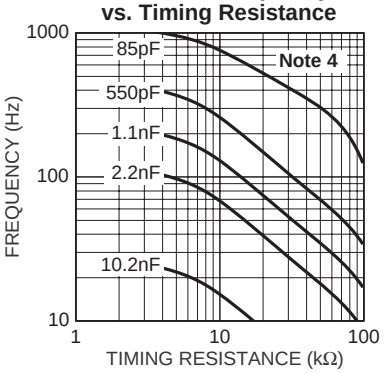
MIC3832 Undervoltage Lockout vs. Junct. Temp.



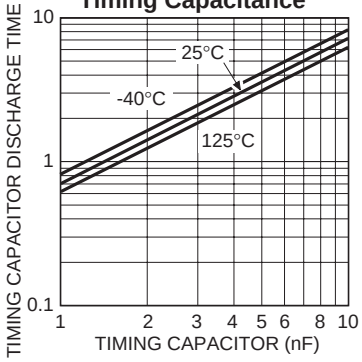
MIC3833 Undervoltage Lockout vs. Junct. Temp.



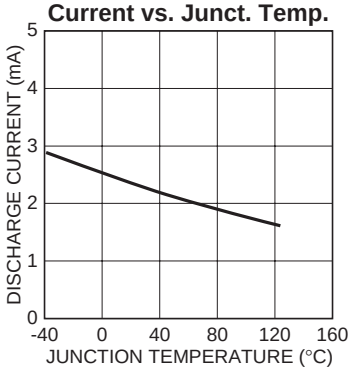
Oscillator Frequency vs. Timing Resistance



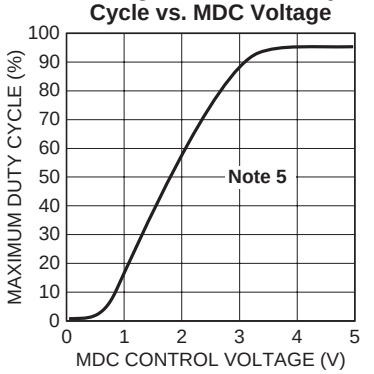
Discharge Time vs. Timing Capacitance



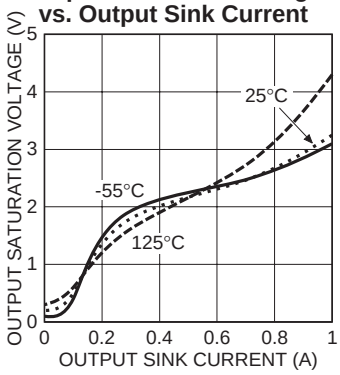
Oscillator Discharge Current vs. Junct. Temp.



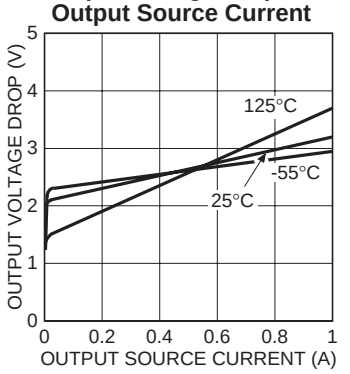
Voltage-Mode Max. Duty Cycle vs. MDC Voltage



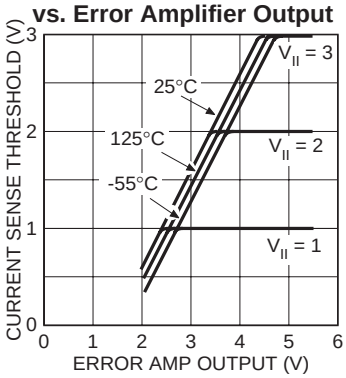
Output Saturation Voltage vs. Output Sink Current



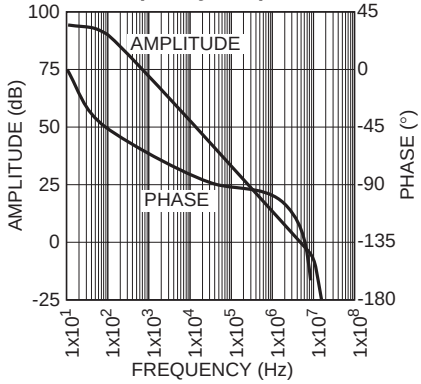
Output Voltage Drop vs. Output Source Current



Current Sense Threshold vs. Error Amplifier Output



Error Amplifier Open-Loop Frequency Response



Note 4: CMR (pin 12) connected to C_T (pin 15).

Note 5: CMR (pin 12) connected to C_T (pin 15). MDC voltage measured at MDC/SS (pin 11). C_T = 1nF, R_T = 10kΩ.

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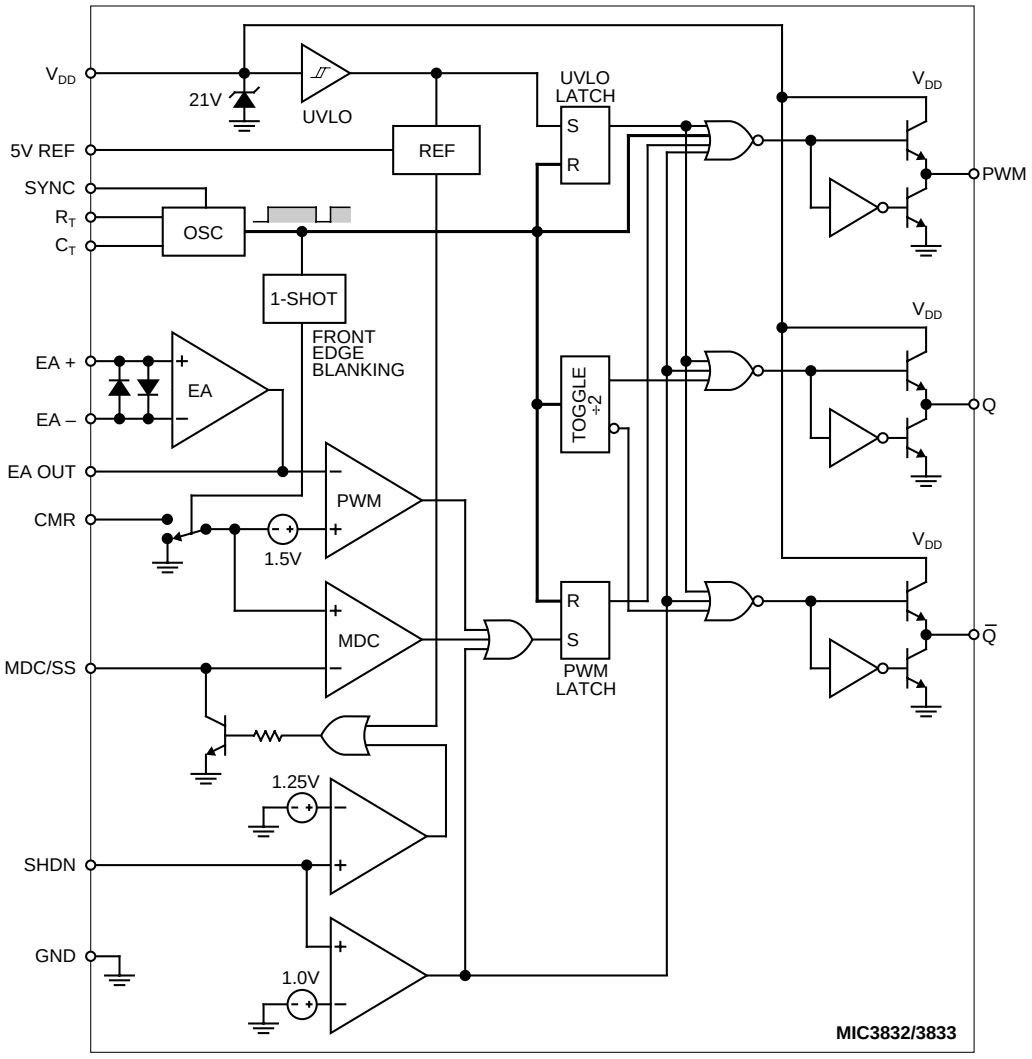
Block Diagram



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Functional Description

Refer to the block diagram and Figure 5.

The MIC3832 and MIC3833 are self-contained controllers, with a voltage reference, voltage-mode error amplifier; current-mode, maximum duty cycle, overcurrent, and shutdown comparators; and an undervoltage lockout circuit. Three control loops are provided: voltage-mode through the error amplifier, current-mode through the PWM comparator, and overcurrent through the shutdown comparator. Three totem-pole outputs provide up to 1A peak synchronized drive to external FETs for current-fed push-pull or bridge transformer applications.

Undervoltage Lockout (UVLO)

Undervoltage lockout (UVLO) requires that the input voltage rise above 15.9V (MIC3832) or 8.3V (MIC3833) before the startup circuit is energized. Once operating, the controller will not shut down until the supply drops to 9.8V (MIC3832) or 7.8V (MIC3833). There is an internal 22V zener between V_{DD} and ground for overvoltage clamping. Zener current should be limited to less than 20mA.

Voltage Reference (REF)

The reference consists of a 5V bandgap reference internally trimmed to 2% accuracy. It provides an internal reference and can be used to supply up to 25mA to external circuits.

Oscillator (R_T/C_T)

The oscillator stage performs two functions. First, it provides a linear sawtooth waveform which is fed to the PWM comparator in voltage-mode control. Second, it toggles the flip-flop which provides the Q and $\overline{Q}$ outputs. The oscillator frequency is configured using an external timing resistor and capacitor. A nominal voltage of 3.6V appears on the R_T pin; the resulting current is then mirrored through the C_T pin which charges the timing capacitor and generates the linear ramp.

It is important to select an appropriate capacitor. At high frequencies effective series resistance, effective series inductance, dielectric loss and dielectric absorption all affect frequency stability and accuracy. RF capacitors such as silver mica, glass, polystyrene, or COG ceramics are recommended. High K ceramics should not be used.

Front-Edge Blanking

This feature provides a fixed delay time prior to current sensing becoming active. This prevents the overcurrent sensing function from being falsely tripped by initial system transients. Timing is set to a nominal 140ns.

Error Amplifier (EA)

The error amplifier is an opamp with a low impedance output that is used to sense output conditions and provide a dc output based on those conditions to the PWM comparator. The output of this stage is brought out to allow tailoring of the closed loop gain or frequency response. The open loop gain of this stage is typically 95dB. The inputs are diode clamped to each other.

PWM Comparator

A sawtooth waveform is compared to the output of the error amplifier. The sawtooth is generally the oscillator waveform on C_T in voltage-mode control systems. In current-mode control systems, it is often the inductor current waveform. Both systems result in a square wave output which, after being NOR'ed with the MDC output (see below), is used to drive the main (PWM) output stage.

PWM Latch and Output

The PWM latch is reset by an oscillator rising cycle, turning the PWM output on if SHDN or UVLO are inactive. The PWM comparator trips when the CMR rising ramp voltage exceeds the error amplifier output voltage, setting the PWM latch and terminating the PWM output, after a minimum time set by the front edge blanking one-shot. If the output voltage is below the setpoint, the PWM cycle is terminated at a maximum duty cycle set by the voltage on the MDC/SS pin. If the output voltage is above the setpoint, the error amplifier output is low, and the PWM cycle terminates after the minimum set by the front edge blanking one-shot. The PWM output is designed to source and sink 1A peak into 1,000 pF loads. The output is disabled when SHDN is enabled.

Push-Pull Outputs (Q and $\overline{Q}$)

Two push-pull outputs are provided, with their leading edge synchronized to alternating PWM rising ramp initiation. The two outputs are 180° out of phase, with a slight (50ns typ.) overlap. The push-pull outputs are designed to source and sink 1A peak into 1,000 pF loads. This peak current was chosen to provide the designer with the option of using bipolar, MOSFET, or IGBT switching elements. To minimize ringing on the output waveform, the series inductance seen by the drivers should be as low as possible. This can be accomplished by keeping the distance between the MIC3832/3 and the switching elements as short as possible, or by using carbon composition resistors in series with the FET gates. The Q and $\overline{Q}$ outputs have a small overlap with no dead time. While advantageous to current-fed topologies, other topologies may require slight modification to accommodate this overlap. The outputs are disabled when SHDN is enabled.

Maximum Duty Cycle (MDC)

This feature, which uses the same pin as soft start (MDC/SS), provides another method of limiting duty cycle. The voltage seen by this pin determines the maximum duty cycle that can be obtained from the PWM output. As this feature can vary by as much as 15% over temperature, it is not recommended that it be used in place of a well designed feedback loop.

The voltage on MDC/SS, the inverting input of the MDC comparator, is compared to the voltage on CMR, with internal front edge blanking.

For voltage-mode operation, refer to the graph, "Typical Characteristics: Voltage-Mode Max. Duty Cycle vs. MDC Voltage." Voltage-mode operation requires the timing capacitor ramp, from C_T, be connected directly to CMR.

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If a voltage-divided portion of the timing capacitor ramp (from C_T) is fed to CMR (to slope compensate for current-mode subharmonic oscillation, for example), the corresponding maximum duty cycle control voltage must be proportionally reduced to achieve the same duty cycle control.

Soft Start

This feature prevents damage due to large inrush currents generated upon initial application of system power or when the device attempts to restart after an overcurrent shutdown by the current limit function. When soft start is activated, the PWM comparator output duty cycle will increase slowly, with a time constant determined by the size of the external capacitor connected to MDC/SS. (Timing is $R_{TH}C$, where R_{TH} is the Thevenin equivalent resistance seen by this pin.)

Overcurrent Sensing and Shutdown

Overcurrent sensing and shutdown is accomplished via a current sense transformer or an external sense resistor connected from the switching element (power transistor) to ground. The current ramp is fed into the noninverting input of two sensing comparators (SHDN). If the sensed voltage equals or exceeds 1.0V, the corresponding input to the logic gates is pulled low, and the PWM comparator output is overridden. This provides a current limited output. If 1.25V is exceeded, the other comparator is also tripped activating the soft start feature.

Application Information

Voltage Mode

Voltage mode control has a single feedback path, comparing the oscillator voltage ramp with the output of an error amplifier which is comparing a sample of the dc output voltage to a reference. The MIC3832/3 may be operated in voltage mode by connecting C_T directly to CMR. Excessive current may be controlled indirectly by driving SHDN. Input voltage changes are sensed as output voltage changes, with delayed response. The ESR (effective series resistance) of each output capacitor adds a pole, requiring a compensating zero or low-frequency roll-off in the error amplifier. Loop gain varies with input voltage.

Current Mode

Current-mode control samples the inductor current waveform. It provides feedback from the output stage, limits peak switching transistor current, removes one pole (the LC filter pole) from the output, provides input voltage feedforward with good rejection of input line transients, and reduces the problem of core saturation. The CMR pin monitors the inductor current.

Current-mode control uses a current sense resistor or transformer to provide a voltage ramp which is compared the output of an error amplifier/comparator which is comparing a sample of the dc output voltage to a reference.

The MIC3832/3 may be operated in current mode by connecting the current sample to the CMR pin. Input voltage variations affect the inductor current slope, providing fast response. Two feedback loops complicate circuit analysis. The error amplifier controls the output current, with a single pole from the output filter.

Multiple supplies may be connected in parallel without concern for current-hogging.

Slope Compensation

At duty cycles above 50% subharmonic oscillations may occur due to the negative resistance effect of the input, for example, current decreasing as input voltage increases. Slope compensation, adding a portion of the oscillator ramp to the CMR pin, is used to remove this error. Power circuit resonances may introduce instability due to output current variations. Internal front edge blanking reduces the effect of leading edge inductive current spikes.

Push-Pull Cross Conduction

Push-Pull power stages have a problem when both power switches are on simultaneously, creating a short-circuit path from rail to rail. In order to eliminate this cross-conduction, or shoot-through, a dead-time is usually added at each transition, allowing the energized switch to fully turn off before the opposite switch is energized. This dead time decreases efficiency as the available duty cycle time is reduced, making the input current larger than optimum for a given input voltage, with higher conduction losses.

In a push-pull (forward) converter, an output inductor operates like a buck converter to store and provide energy to the load and output capacitor during the deadtime. Both output rectifier diodes are pulled into conduction by the output inductor during the deadtime, draining the magnetic field from the output transformer. At the start of each power cycle the energized input switch sees a virtual short-circuit in the transformer, until the opposite diode is pulled out of conduction.

Current Fed

If a constant current source is added to the feedpoint of a push-pull power stage, no deadtime is needed between power cycles, since the switches may be designed to handle the limited cross-conduction current. No output inductor is needed to store energy during the deadtime, and the related problem of simultaneously conducting output rectifiers is eliminated.

Buck-Derived Current Fed

Refer to Figure 5.

If a supply is designed to operate from a widely varying input voltage, such as the power line, a PWM step-down (buck) regulator may be used as the constant current input to the push-pull stage by omitting the customary output capacitor from the buck circuit. A bifilar wound pulse transformer is used to provide high-side drive to the PWM switch. A slightly overlapping drive is provided to the push-pull switches, so the output side of the buck inductor will swing toward ground during cross-conduction, limiting dissipated power.

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The push-pull cycles are synchronized to run at half of the PWM frequency, so a soft or zero voltage switch transition may be obtained, reducing spikes and EMI. Feeding a sample of the PWM oscillator ramp to the current-mode comparator along with the input current sample allows slope compensation to be obtained for PWM duty cycles above 50%, preventing subharmonic oscillation at low input voltages.

Boost-Derived Current Fed

If a regulator is designed to run at higher push-pull voltage than the input line voltage, a step-up (boost) PWM regulator, with an inductor switched to ground, minus the normal output capacitor, will provide a current limited input to the push-pull stage. In this configuration all three power switches may be operated low-side, simplifying their drive circuitry. An input fuse is needed to guard against short-circuits since there is no high-side series switch.

Construction Hints

Careful prototyping techniques are required to prevent oscillations. Traditional solderless breadboards are a source of noise, and should be avoided. Use double-sided, copper-clad boards with a large area used as a single-point ground plane.

All timing and loop compensation capacitors and resistors should be star connected to GND (ground). Wire lengths along the high-current path should be kept as short as possible, with appropriate wire gauges being used. Do not socket the switching transistors as this can add to the voltage drop and power losses.

Current-Fed Push-Pull SMPS

Figure 3 illustrates this basic topology, a standard push-pull configuration where the center tap of the primary is fed with an inductor current instead of a voltage. This constant current reduces cross conduction and catastrophic transformer core saturation. Push-pull topologies are often used in 100W and larger power supplies as they allow more efficient use of the transformer. The entire range of the B-H curve is used in a push-pull supply, so a transformer that is one-half the size of a transformer used in a single-ended, forward-mode topology can be used. This topology can be extended to a full bridge where the two 50% duty cycle stages would be used to drive two MOSFETs each, one for each half of the bridge.

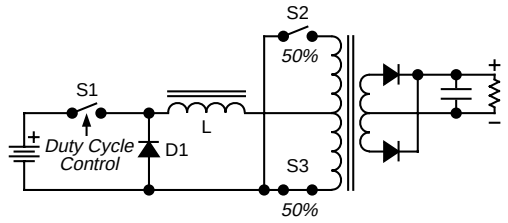

Figure 3: Current-Fed Push-Pull Topology

Current-Fed Multiple-Output SMPS

Figure 4 illustrates this topology. The absence of output inductors improves cross-regulation and simplifies the construction of isolated or high-voltage output supplies.

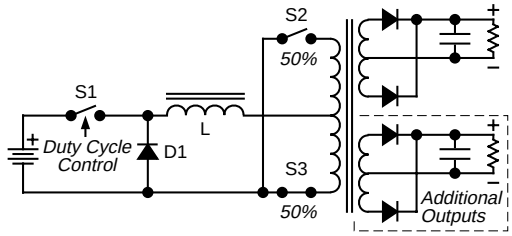

Figure 4: Current-Fed Multiple-Output Topology

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100kHz 100W Current-Fed Converter

Refer to Figure 5.

A 5V, 20A dc-to-dc converter uses the current-fed, push-pull configuration for increased safety and reduced size and transformer core area.

The input is an unregulated 14V to 32Vdc supply. An MIC2951 low-dropout regulator supplies 12V to the MIC3833.

The main PWM switching element is an IRF540, with gate drive provided by transformer T1. The two 50% duty cycle outputs each drive an IRF540 directly, which in turn drive respective sides of T2's center tapped primary. The 1N6291A transzorb is used to protect the MOSFETs from spikes.

Current-mode control simplifies the stability analysis, with the 0.2Ω, 5W resistor being used as the sensing element. As the maximum duty cycle at light loads is greater than 50%, the well characterized problem of subharmonic oscillations found when using current-mode control was evident. A ramp, introduced at the sensing element, provides slope compensation. The 10kΩ and 470kΩ divider from the oscillator (ramp source) to the sensing element provides the proper slope. A large resistor value from C_T to CMR makes buffering unnecessary.

Front-edge blanking eliminates the need for a filter network around the sensing element and decreases the possibility of turn-on transients that cause system instabilities.

Four inexpensive output capacitors in parallel reduce ESR to an acceptable level of 80mΩ without adding too much size or cost.

Error amplifier compensation uses a simple lead-lag network. With current-mode control there is no need to compensate for the LC filter pole.

Soft start is implemented to allow slow turn-on in the event of a short circuit.

All magnetics were chosen to minimize losses at 100 kHz. T2 and L1 are wound using Siemen's N87 material and T1 using Magnetics Inc.'s P-type material. T2 and L1 use Siemen's EFD core and bobbin assemblies which are designed to reduce the height/form factor of the finished supply. T1 is a bifilar-wound toroid used as a 200kHz pulse transformer. T2 is not gapped, since a push-pull transformer has a minimum dc current component, being a forward converter.

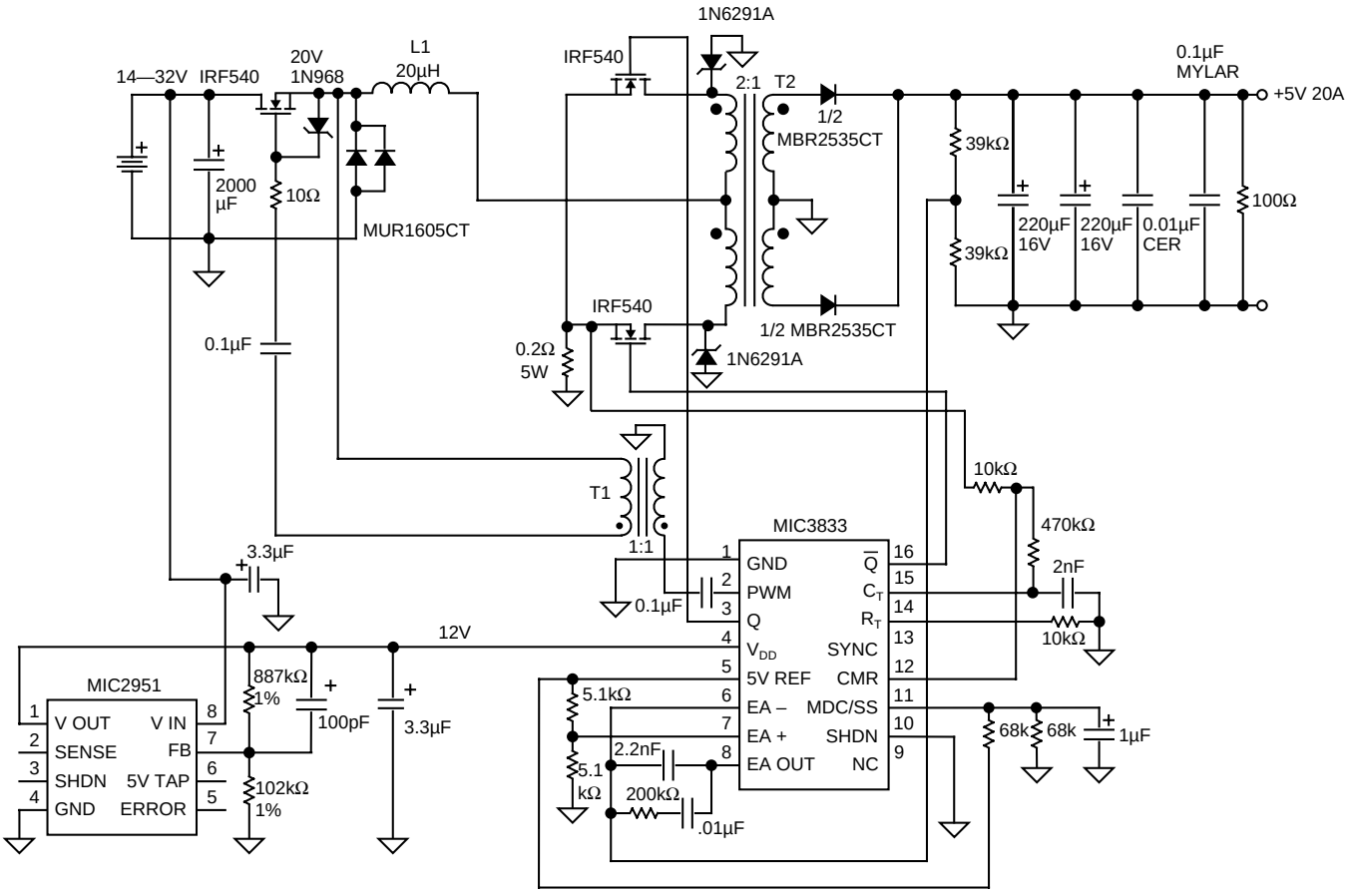

Figure 5: 100W Current-Fed, Push-Pull DC-to-DC Converter (Efficiency ~75%)

Magnetics Design

T1 : Magnetics Inc # 41303 – TC, P material, Primary = 26 turns 30 gauge wire, Secondary = 26 turns 30 gauge wire
T2: Seimen's EFD25, N87 material. Primary = 20 turns 20 gauge wire, Secondary = 10 turns trifilar wound 20 gauge wire. Both are center tapped.
L1: Seimen's EFD20, N87 material. 13 turns 20 gauge wire. Gap for 20µH

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