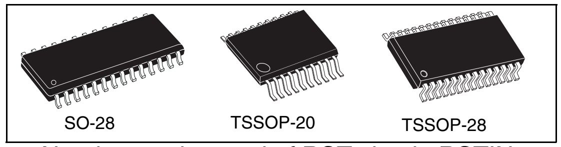
ST8024L

Smartcard interface

Features

- Designed to be compatible with the NDS conditional access system (ST8024LCDR and ST8024LCTR only)
- IC card interface
- 3 V or 5 V supply for the IC (V_{DD} and GND)
- Three specifically protected half-duplex bi-directional buffered I/O lines to card contacts C4, C7 and C8
- Step-up converter for V_{CC} generation separately powered from a 5 V ± 20% supply (V_{DDP} and PGND)
- 1.8 V ±6.5%, 3 V or 5 V ±5% regulated card supply voltage (V_{CC}) with appropriate decoupling has the following capabilities:
  - I_{CC} < 80 mA at V_{DDP} = 4.75 to 6.5 V
  - Handles current spikes of 40 nA up to 20 MHz
  - Controls rise and fall times
  - Filtered overload detection at ~120 mA
- Thermal and short-circuit protection on all card contacts
- Automatic activation and deactivation sequences; initiated by software or by hardware in the event of a short-circuit, card take-off, overheating, V_{DD} or V_{DDP} drop-out
- Enhanced ESD-protection on card side (>6 kV)
- 26 MHz integrated crystal oscillator
- Built-in debounce on card presence contacts
- One multiplexed status signal $\overline{OFF}$



- Non-inverted control of RST via pin RSTIN
- Clock generation for cards up to 20 MHz (divided by 1, 2, 4 or 8 through CLKDIV1 and CLKDIV2 signals) with synchronous frequency changes
- ISO 7816, GSM11.11 and EMV 4.0 (payment systems) compatibility
- Supply supervisor for spike-killing during power-on and power-off and power-on reset (threshold fixed internally or externally by a resistor bridge)

Applications

- Smartcard readers for set-top box
- IC card readers for banking
- Identification, pay TV

Description

The ST8024L is a complete low-cost analog interface for asynchronous Class A, B and C smartcards. It can be placed between the card and the microcontroller with few external components to perform all supply protection and control functions. ST8024LCDR and ST8024LCTR are compatible with ST8024 (with the exception of $V_{th(ext)rise/fall}$).

Table 1. Device summary

Order code	PORADJ/1.8V function	Temperature range	Package	Packaging
ST8024LCDR(1)	PORADJ	–25 to 85 °C	SO-28 (tape and reel)	1000 parts per reel
ST8024LCTR(1)	PORADJ	–25 to 85 °C	TSSOP-28 (tape and reel)	2500 parts per reel
ST8024LACDR	1.8 V	–25 to 85 °C	SO-28 (tape and reel)	1000 parts per reel
ST8024LTR	1.8 V	–25 to 85 °C	TSSOP-20 (tape and reel)	2500 parts per reel

1. Cerfified by NDS

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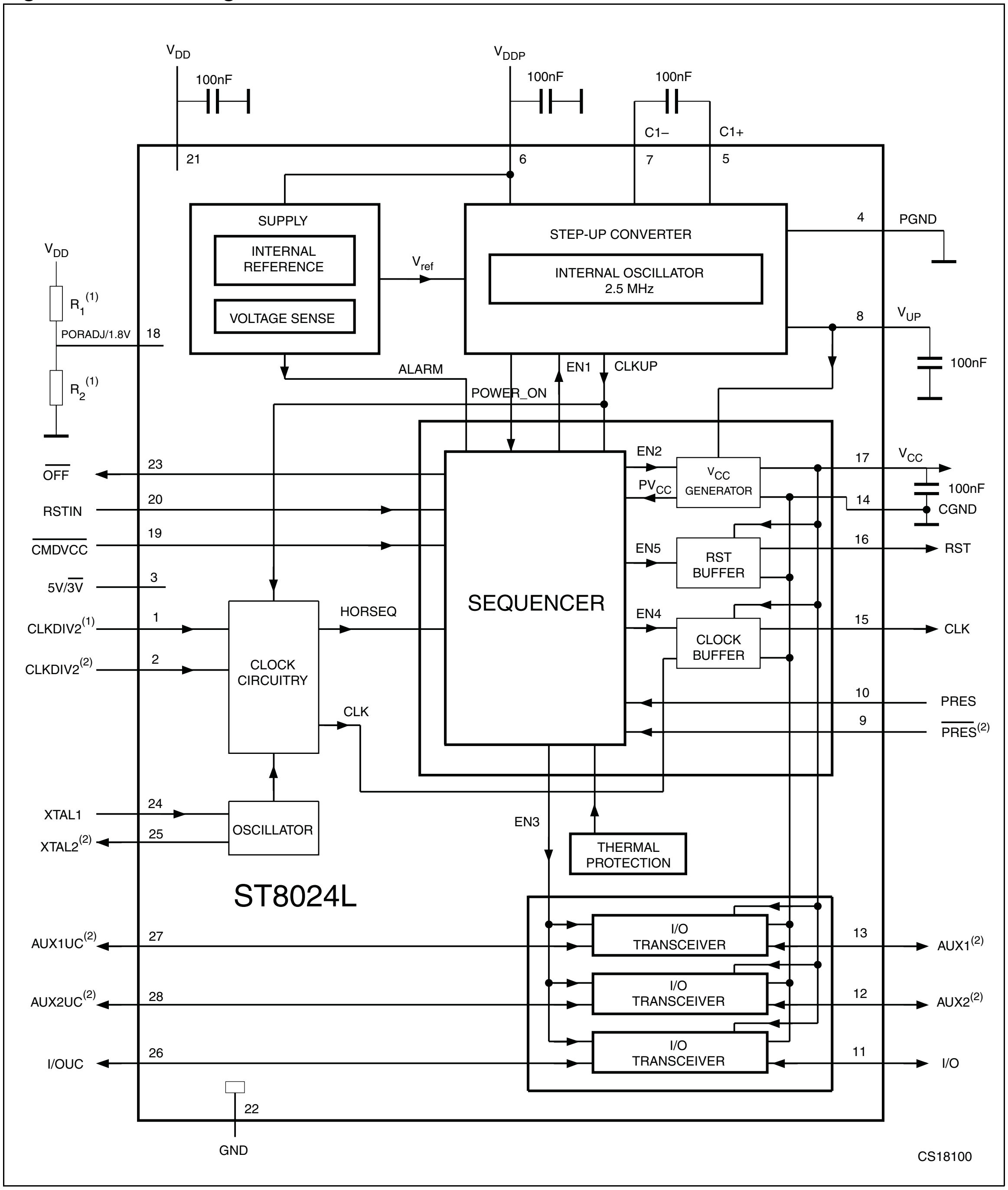
1 Diagram

Figure 1. Block diagram



1. To be used with the PORADJ pin if needed
2. Not available in the TSSOP-20L package

2 Pin configuration

Figure 2. Pin connections

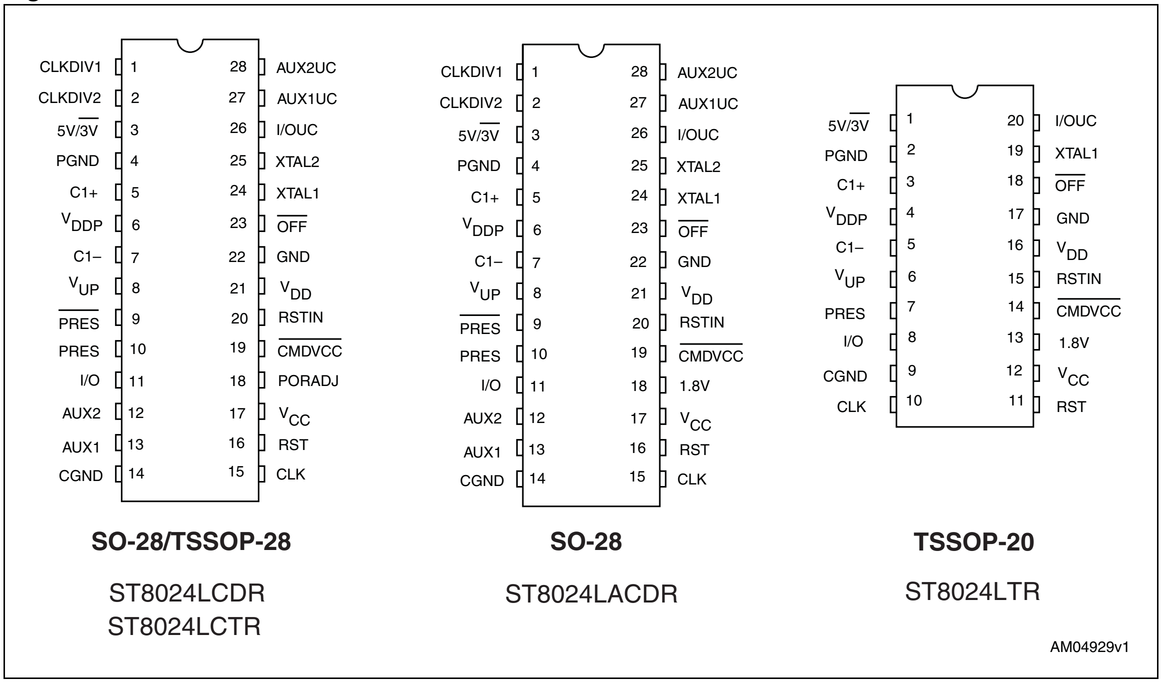


Table 2. Pin description

Symbol	Name and function	SO-28/ TSSOP-28	TSSOP-20
CLKDIV1	Control of CLK frequency (internal 11 kΩ pull-up resistor connected to V_{DD})	1	N.A
CLKDIV2	Control of CLK frequency (internal 11 kΩ pull-down resistor connected to V_{DD})	2	N.A
5V/$\overline{3V}$	5 V or 3 V V_{CC} selection for communication with the smartcard. Logic high selects 5 V operation and logic low selects 3 V operation. If the 1.8V pin is logic high, the 5V/$\overline{3V}$ pin is a “don't care” (see *Table 24* for a description of the V_{CC} selection settings.)	3	1
PGND	Power ground for step-up converter	4	2
C1+	External cap. step-up converter	5	3
V_{DDP}	Power supply for step-up converter	6	4
C1–	External cap. step-up converter	7	5
V_{UP}	Output of step-up converter	8	6
$\overline{PRES}$	Card presence input (active low) - bonding option	9	N.A
PRES	Card presence input (active high)	10	7

Table 2. Pin description (continued)

Symbol	Name and function	SO-28/ TSSOP-28	TSSOP-20
I/O	Data line to and from card (C7) (internal 11 kΩ pull-up resistor connected to V_{CC})	11	8
AUX2	Auxiliary line to and from card (C8) (internal 11 kΩ pull-up resistor connected to V_{CC})	12	N.A.
AUX1	Auxiliary line to and from card (C4) (internal 11 kΩ pull-up resistor to V_{CC})	13	N.A
CGND	Ground for card signal (C5)	14	9
CLK	Clock to card (C3)	15	10
RST	Card reset (C2)	16	11
V_{CC}	Supply voltage for the card (C1)	17	12
PORADJ	Power-on reset threshold adjustment input	18	N.A.
1.8V	1.8 V V_{CC} operation selection. Logic high selects 1.8 V operation and overrides any setting on the 5V/$\overline{3V}$ pin.	18/N.A.[1]	13
$\overline{CMDVCC}$	Start activation sequence input (active low)	19	14
RSTIN	Card reset input from MCU	20	15
V_{DD}	Supply voltage	21	16
GND	Ground	22	17
$\overline{OFF}$	Interrupt to MCU (active low)	23	18
XTAL1	Crystal or external clock input	24	19
XTAL2	Crystal connection (leave this pin open if external clock is used)	25	N.A
I/OUC	MCU data I/O line (internal 11 kΩ pull-up resistor connected to V_{DD})	26	20
AUX1UC	Non-inverting receiver input (internal 11 kΩ pull-up resistor connected to V_{DD})	27	N.A.
AUX2UC	Non-inverting receiver input (internal 11 kΩ pull-up resistor connected to V_{DD})	28	N.A.

1. Only available on the SO-8 package.

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}, V_{DDP}	Supply voltage	-0.3	7	V
V_{n1}	Voltage on pins XTAL1, XTAL2, 5V/$\overline{3V}$, RSTIN, AUX2UC, AUX1UC, I/OUC, CLKDIV1, CLKDIV2, PORADJ/1.8V, $\overline{CMDVCC}$, $\overline{PRES}$, PRES and $\overline{OFF}$	-0.3	V_{DD} + 0.3	V
V_{n2}	Voltage on card contact pins I/O, RST, AUX1, AUX2 and CLK	-0.3	V_{CC} + 0.3	V
V_{n3}	Voltage on pins V_{UP}, C1+, C1–		7	V
ESD1	MIL-STD-883 class 3 on card contact pins, $\overline{PRES}$ and PRES (*Note 1*, *Note 2*)	-6	6	kV
ESD2	MIL-STD-883 class 2 on µC contact pins and RSTIN (Note 1, 2)	-2	2	kV
$T_{J(MAX)}$	Maximum operating junction temperature		150	°C
T_{STG}	Storage temperature range	-40	150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Note: 1 All card contacts are protected against any short with any other card contact.

2 Method 3015 (HBM, 1500 Ω, 100 pF) 3 positive pulses and 3 negative pulses on each pin referenced to ground.

Table 4. Thermal data

Symbol	Parameter	Condition	SO-28	TSSOP-20 TSSOP-28	Unit
R_{thJA}	Thermal resistance junction-ambient temperature	Multilayer test board (Jedec standard)	56	50	°C/W

Table 5. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_A	Temperature range		–25		85	°C

4 Electrical characteristics

Table 6. Electrical characteristics over recommended operating condition

Symbol	Parameter[1]	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.7		6.5	V
V_{DDP}	Supply voltage for the step-up converter	V_{CC} = 5 V; $\lvert I_{CC}\rvert$ < 80 mA For NDS application	4.0	5	6.5	V
		V_{CC} = 3 V; $\lvert I_{CC}\rvert$ < 65 mA For NDS application	4.0	5	6.5	
		V_{CC} = 5 V; $\lvert I_{CC}\rvert$ < 20 mA	3.0		6.5	
		V_{CC} = 3 V; $\lvert I_{CC}\rvert$ < 20 mA	2.7		6.5	
		V_{CC} = 1.8 V; $\lvert I_{CC}\rvert$ < 20 mA	2.7		6.5	
I_{DD}	Supply current	Card inactive			1.2	mA
		Card active; $f_{CLK} = f_{XTAL}$; C_L = 30 pF			1.5	
I_{DDP}	Step-up converter supply current	Inactive mode			0.1	mA
		Active mode; $f_{CLK} = f_{XTAL}$; C_L = 30 pF; $\lvert I_{CC}\rvert$ = 0			10	
		V_{CC} = 5 V; $\lvert I_{CC}\rvert$ = 80 mA		50	200	
		V_{CC} = 3 V; $\lvert I_{CC}\rvert$ = 65 mA		50	100	
		V_{CC} = 1.8 V; $\lvert I_{CC}\rvert$ = 45 mA		30	60	
V_{th2}	Falling threshold voltage on V_{DD}	no external resistors at pin PORADJ; V_{DD} level falling	2.35	2.45	2.55	V
V_{HYS2}	Hysteresis of threshold voltage V_{th2}	no external resistors at pin PORADJ	50	100	150	mV
$V_{th(ext)rise}$	External rising threshold voltage on V_{DD}	external resistor bridge at pin PORADJ; V_{DD} level rising	1.17	1.20	1.23	V
$V_{th(ext)fall}$	External falling threshold voltage on V_{DD}	external resistor bridge at pin PORADJ; V_{DD} level falling	1.11	1.14	1.17	V
$V_{HYS(ext)}$	Hysteresis of threshold voltage $V_{th(ext)}$	external resistor bridge at pin PORADJ	30	60	90	mV
$\Delta V_{HYS(ext)}$	Hysteresis of threshold voltage $V_{th(ext)}$ variation with temperature	external resistor bridge at pin PORADJ			0.25	mV/K
t_W	Width of internal power-on reset pulse	no external resistor bridge at pin PORADJ	4	8	12	ms
		external resistor bridge at pin PORADJ	8	16	24	
I_L	Leakage current on pin PORADJ	V_{PORADJ} < 0.5 V	–0.1	4	10	µA
		V_{PORADJ} > 1.0 V	–1		1	
P_{TOT}	Total power dissipation	Continuous operation; T_A = –25 to 85 °C			0.56	W

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 7. Step-up converter

Symbol	Parameter(1)	Test conditions	Min.	Typ.	Max.	Unit
f_{CLK}	Clock frequency	Card active	2.2		3.2	MHz
$V_{th(vd-vf)}$	Threshold voltage for step-up converter to change to voltage follower	5 V card	5.2	5.8	6.2	V
		3 V card	3.8	4.1	4.4	
		1.8 V card	3.8	4.1	4.4	
V_{UP}	Output voltage on pin V_{UP} (average value)	5 V card	5.2	5.7	6.2	V
		3 V card	3.5	3.9	4.3	
		1.8 V card	3.5	3.9	4.3	

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 8. Card supply voltage characteristics

Symbol	Parameter(1)	Test conditions		Min.	Typ.	Max.	Unit
C_{VCC}	External capacitance on pin V_{CC}	*Note 2* and *Note 3*		80		400	nF
V_{CC}	Card supply voltage (including ripple voltage)	Card inactive; $\|I_{CC}\|$ = 0 mA	5 V, 3 V and 1.8 V card	-0.1	0	0.1	V
		Card inactive; $\|I_{CC}\|$ = 1 mA	5 V, 3 V and 1.8 V card	-0.1	0	0.3	
		Card active; $\|I_{CC}\|$ < 80 mA	5 V card	4.75	5	5.25	
		Card active; $\|I_{CC}\|$ < 65 mA	3 V card	2.85	3	3.15	
		Card active; $\|I_{CC}\|$ < 45 mA	1.8 V card	1.68	1.8	1.92	
		Card active; single current pulse I_P = –100 mA; t_p = 2 µs	5 V card	4.65	5	5.25	
		Card active; single current pulse I_P = –100 mA; t_p = 2 µs	3 V card	2.76	3	3.20	
		Card active; single current pulse I_P = –100 mA; t_p = 2 µs	1.8 V card	1.62	1.8	1.98	
		Card active; current pulses, Q_P = 40 nAs	5 V card	4.65	5	5.25	
			3 V card	2.76	3	3.20	
			1.8 V card	1.62	1.8	1.98	
		Card active; current pulses Q_P = 40 nAs with $\|I_{CC}\|$ < 200 mA, t_p < 400 ns	5 V card	4.65	5	5.25	
			3 V card	2.76	3	3.20	
			1.8 V card	1.62	1.8	1.98	
V_{CC} (RIPPLE) (P-P)	Ripple voltage on V_{CC} (peak-to-peak value)	f_{RIPPLE} = 20 KHz to 200 MHz				350	mV

Table 8. Card supply voltage characteristics (continued)

Symbol	Parameter[(1)]	Test conditions	Min.	Typ.	Max.	Unit
$\|I_{CC}\|$	Card supply current	V_{CC} = 0 to 5 V			80	mA
		V_{CC} = 0 to 3 V			65	
		V_{CC} = 0 to 1.8 V			45	
		V_{CC} short circuit to GND	90		120	
S_R	Slew rate	Slew up or down, V_{CC} = 5 V; 3 V; 1.8 V; $\|I_{CC}\|$ < 30 mA	0.08	0.15	0.22	V/µs

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C. *Note 1*

Table 9. Crystal connection (pins XTAL1 and XTAL2)

Symbol	Parameter[(1)]	Test conditions	Min.	Typ.	Max.	Unit
$C_{XTAL1,2}$	External capacitance on pins XTAL1, XTAL2	Depends on type of crystal or resonator used		-	15	pF
f_{XTAL}	Crystal frequency		2	-	26	MHz
f_{XTAL1}	Frequency applied on pin XTAL1		0	-	26	MHz
V_{IH}	High level input voltage on pin XTAL1		0.7 V_{DD}	-	V_{DD}+0.3	V
V_{IL}	Low level input voltage on pin XTAL1		-0.3	-	+0.3V_{DD}	V

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 10. Data lines (pins I/O, I/OUC, AUX1, AUX2, AUX1UC AND AUX2UC)

Symbol	Parameter[(1)]	Test conditions	Min.	Typ.	Max.	Unit
$t_{D(I/O-I/OUC)}$, $t_{D(I/OUC-I/O)}$	I/O to I/OUC, I/OUC to I/O falling edge delay		-	-	200	ns
t_{PU}	Active pull-up pulse width		-	-	100	ns
$f_{I/O(MAX)}$	Maximum frequency on data lines		-	-	1	MHz
C_I	Input capacitance on data lines		-	-	10	pF

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 11. Data lines to card reader (pins I/O, AUX1 AND AUX2 with integrated 11 kΩ pull-up resistor to V_{CC}

Symbol	Parameter[(1)]	Test conditions		Min.	Typ.	Max.	Unit
$V_{O(inactive)}$	Output voltage	Inactive mode	No load	0		0.1	V
			$I_{O(inactive)}$=1 mA			0.3	
$I_{O(inactive)}$	Output current	Inactive mode; pin grounded				-1	mA
V_{OH}	High level output voltage	No DC load		0.9 V_{CC}		V_{CC}+0.1	V
		5 V and 3 V cards; I_{OH} < –40 µA		0.75 V_{CC}		V_{CC}+0.1	
		1.8 V card I_{OH} < –40 µA		0.75 V_{CC}			
		$\lvert I_{OH}\rvert \geq$ 10 mA		0		0.4	
V_{OL}	Low level output voltage	I_{OL} = 1 mA		0		0.2	V
		$I_{OL} \geq$ 15 mA		V_{CC}–0.4		V_{CC}	
V_{IH}	High level input voltage	5 V and 3 V cards		1.5		V_{CC}+0.3	V
		1.8 V card		0.6 V_{CC}			
V_{IL}	Low level input voltage	5 V and 3 V cards		0.3		1.0	V
		1.8 V card		0		0.2	
$\lvert I_{LIH}\rvert$	High level input leakage current	V_{IH} = V_{CC}				10	µA
$\lvert I_{IL}\rvert$	Low level input current	V_{IL} = 0 V				600	µA
R_{PU}	Integrated pull-up resistor	Pull-up resistor to V_{CC}		9	11	13	kΩ
$t_{T(DI)}$	Data input transition time	V_{IL} max to V_{IH} min				1.2	µs
$t_{T(DO)}$	Data output transition time	V_O = 0 to V_{CC}; $C_L \leq$ 80 pF; 10% to 90%				0.1	µs
I_{PU}	Current when pull-up active	V_{OH} = 0.9V_{CC}; C_L = 80 pF		-2			mA

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 12. Data lines to microcontroller (pins I/OUC, AUX1UC and AUX2UC with integrated 11 kΩ pull-up resistor to V_{DD}

Symbol	Parameter[(1)]	Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	High level output voltage	5 V, 3 V and 1.8 V cards; $I_{OH} < -40$ µA	0.75 V_{DD}		V_{DD}+0.1	V
		No DC load	0.9 V_{DD}		V_{DD}+0.1	
V_{OL}	Low level output voltage	I_{OL} = 1 mA	0		0.3	V
V_{IH}	High level input voltage		0.7 V_{DD}		V_{DD}+0.3	V
V_{IL}	Low level input voltage		-0.3		0.3 V_{DD}	V
$\|I_{LIH}\|$	High level input leakage current	$V_{IH} = V_{DD}$			10	µA
$\|I_{IL}\|$	Low level input current	V_{IL} = 0 V			600	µA
R_{PU}	Internal pull-up resistance to V_{DD}	Pull-up resistor to V_{DD}	9	11	13	kΩ
$t_{T(DI)}$	Data input transition time	$V_{IL(max)}$ to $V_{IH(min)}$			1.2	µs
$t_{T(DO)}$	Data output transition time	V_O = 0 to V_{DD}; C_L < 30 pF; 10% to 90%			0.1	µs
I_{PU}	Current when pull-up active	$V_{OH} = 0.9V_{DD}$; C_L = 30 pF	-1			mA

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 13. Internal oscillator

Symbol	Parameter[(1)]	Test conditions	Min.	Typ.	Max.	Unit
$f_{OSC(INT)}$	Frequency of internal oscillator	Inactive mode	55	140	200	kHz
		Active mode	2.2	2.7	3.2	MHz

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted.Typical values are at T_A = 25 °C.

Table 14. Reset output to card reader (pin RST)

Symbol	Parameter[(1)]	Test conditions	Min.	Typ.	Max.	Unit
$V_{O(inactive)}$	Output voltage in inactive mode	$I_{O(inactive)}$ = 1 mA	0	-	0.3	V
		No load	0	-	0.1	
$I_{O(inactive)}$	Output current	Inactive mode; pin grounded	0	-	-1	mA
$t_{D(RSTIN-RST)}$	RSTN to RST delay	RST enable		-	2	µs
V_{OL}	Low level output voltage	I_{OL} = 200 µA	0	-	0.2	V
		I_{OL} = 20 mA (current limit)	V_{CC}-0.4	-	V_{CC}	
V_{OH}	High level output voltage	I_{OH} = –200 µA	0.9V_{CC}	-	V_{CC}	V
		I_{OH} = –20 mA (current limit)	0	-	0.4	
t_R, t_F	Rise and fall time	C_L = 100 pF		-	0.1	µs

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 15. Clock output to card reader (pin CLK)

Symbol	Parameter(1)	Test conditions	Min.	Typ.	Max.	Unit
$V_{O(inactive)}$	Output voltage in inactive mode	$I_{O(inactive)}$ = 1 mA	0	-	0.3	V
		No load	0	-	0.1	
$I_{O(inactive)}$	Output current	CLK inactive mode; pin grounded	0	-	–1	mA
V_{OL}	Low level output voltage	I_{OL} = 200 µA	0	-	0.3	V
		I_{OL} = 70 mA (current limit)	V_{CC}-0.4	-	V_{CC}	
V_{OH}	High level output voltage	I_{OH} = –200 µA	0.9V_{CC}	-	V_{CC}	V
		I_{OH} = –70 mA (current limit)	0	-	0.4	
t_R, t_F	Rise and fall time	C_L = 30 pF (*Note 4*)		-	16	ns
δ	Duty factor (except for f_{XTALS})	C_L = 30 pF (*Note 4*)	45	-	55	%
S_R	Slew rate	Slew up or down; C_L = 30 pF	0.2	-		V/ns

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 16. Control inputs (pins CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, RSTIN, 5V/$\overline{3V}$ and PORADJ/1.8V)

Symbol	Parameter(1)	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input voltage low		–0.3		0.3V_{DD}	V
V_{IH}	Input voltage high		0.7V_{DD}		V_{DD}	V
$\|I_{LIH}\|$	Input leakage current high	V_{IH} = V_{DD}			1	µA
$\|I_{LIL}\|$	Input leakage current low	V_{IL} = 0			1	µA

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C. (*Note 5*)

Table 17. Card presence inputs (pins PRES and $\overline{PRES}$)

Symbol	Parameter(1)	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input voltage low		-0.3	-	0.3 V_{DD}	V
V_{IH}	Input voltage high		0.7 V_{DD}	-	V_{DD}+0.3	V
$\|I_{LIH}\|$	Input leakage current high	V_{IH} = V_{DD}		-	5	µA
$\|I_{LIL}\|$	Input leakage current low	V_{IL} = 0		-	5	µA

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C. (*Note 6*)

Table 18. Interrupt output (pin $\overline{OFF}$ NMOS drain with integrated 20 kΩ pull-up resistor to V_{DD})

Symbol	Parameter(1)	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	I_{OL} = 2 mA	0		0.3	V
V_{OH}	High level output voltage	I_{OH} = –15 µA	0.75 V_{DD}			V
R_{PU}	Integrated pull-up resistor	20 kΩ pull-up resistor to V_{DD}	16	20	24	kΩ

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 19. Protection and limitation

Symbol	Parameter(1)	Test conditions	Min.	Typ.	Max.	Unit
$\|I_{CC(SD)}\|$	Shutdown and limitation current pin V_{CC}		90		120	mA
$I_{I/O(lim)}$	limitation current pins I/O, AUX1 and AUX2		–15		15	mA
$I_{CLK(lim)}$	limitation current pin CLK		–70		70	mA
$I_{RST(lim)}$	limitation current pin RST		–20		20	mA
T_{SD}	Shutdown temperature			150		°C

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

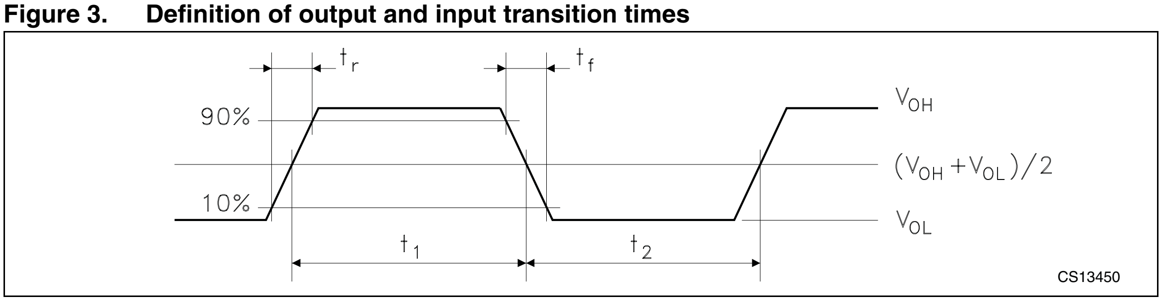
Table 20. Timing

Symbol	Parameter(1)	Test conditions	Min.	Typ.	Max.	Unit
t_{ACT}	Activation time	(See *Figure 5*) for V_{CC} = 5 V	50		220	µs
t_{DE}	Deactivation time	(See *Figure 7*)	50	80	100	µs
t_3	Start of the window for sending CLK to card	(See *Figure 6*)			130	µs
t_5	End of the window for sending CLK to card	(See *Figure 6*)	140			µs
$t_{debounce}$	Debounce time pins PRES and $\overline{PRES}$	(See *Figure 8*)	5	8	11	ms

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Note:
1. *All parameters remain within limits but are tested only statistically for the temperature range. When a parameter is specified as a function of V_{DD} or V_{CC} it means their actual value at the moment of measurement.*
2. *To meet these specifications, pin V_{CC} should be decoupled to CGND using two ceramic multilayer capacitors of 350 mΩ ESR both with values of 100 nF and 100 nF (see Figure 10).*
3. *Permitted capacitor values are 100 nF, 220 nF or 400 nF.*
4. *Transition time and duty factor definitions are shown in Figure 3; $\delta = t_1/(t_1 + t_2)$.*
5. *Pin $\overline{CMDVCC}$ is active low; pin RSTIN is active high; for CLKDIV1 and CLKDIV2 functions (see Table 20).*
6. *Pin $\overline{PRES}$ is active low; pin PRES is active high see Figure 8 and Figure 9; PRES has an integrated 1.25 µA current source to GND. ($\overline{PRES}$ to V_{DD}); the card is considered present if at least one of the inputs $\overline{PRES}$ or PRES is active.*

Figure 3. Definition of output and input transition times



5 Functional description

Throughout this document it is assumed that the reader is familiar with ISO7816 terminology.

5.1 Power supply

The supply pins for the IC are V_{DD} and GND. V_{DD} should be in the range of 2.7 to 6.5 V. All signals interfacing with the system controller are referred to V_{DD}, therefore V_{DD} should also supply the system controller. All card reader contacts remain inactive during power-on or power-off.

The internal circuits are maintained in the reset state until V_{DD} reaches V_{th2} +V_{hys2} and for the duration of the internal Power-on reset pulse, t_W (see *Figure 4*). When V_{DD} falls below V_{th2}, an automatic deactivation of the contacts is performed.

A step-up converter is incorporated to generate the 1.8 V (for those devices with the 1.8V pin), 3 V or 5 V card supply voltage (V_{CC}). The step-up converter should be supplied separately by V_{DDP} and PGND. Due to the possibility of large transient currents, the two 100 nF capacitors of the step-up converter should be located as near as possible to the IC and have an ESR less than 350 mΩ.

Supply voltages V_{DD} and V_{DDP} may be applied to the IC in any sequence.

After powering the device, $\overline{\text{OFF}}$ remains low until $\overline{\text{CMDVCC}}$ is set high.

During power-off, $\overline{\text{OFF}}$ falls low when V_{DD} is below the falling threshold voltage.

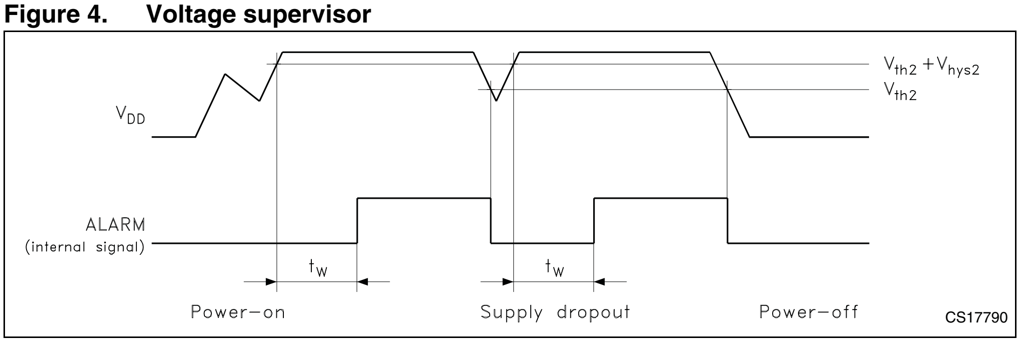
5.2 Voltage supervisor

5.2.1 Without external divider on pin PORADJ

The voltage supervisor surveys the V_{DD} supply. A defined reset pulse of approximately 8 ms (t_W) is used internally to keep the IC inactive during power-on or power-off of the V_{DD} supply (see *Figure 4*).

As long as V_{DD} is less than V_{th2} + V_{hys2}, the IC remains inactive whatever the levels on the command lines. This state also lasts for the duration of t_W after V_{DD} has reached a level higher than V_{th2} + V_{hys2}. When V_{DD} falls below V_{th2}, a deactivation sequence of the contacts is performed.

Figure 4. Voltage supervisor



5.2.2 With an external divider on pin PORADJ

In this case, a resistor bridge is applied to the PORADJ pin (see *Figure 1*). $V_{TH(ext)\ rise}$ and $V_{TH(ext)\ fall}$ are the external rising threshold voltage and the external falling threshold voltage on V_{DD}, respectively. They are the voltages on pin PORADJ that switch the device on and off. By knowing these values and using the formula:

$$V_{PORADJ} = (R_2/R_1 + R_2) \times V_{DD}$$

it is possible to set R_1 and R_2 in order to get suitable values for V_{DD} in order to turn the device on and off ($R_1 + R_2 = 100\ k\Omega$ typ).

In particular, R_1 and R_2 have to be set so that, when V_{DD} is getting low, before turning the microcontroller off, the smartcard has to be switched off properly as well. The same is true for the microcontroller startup in that the smartcard has to be turned on after the microcontroller. The reset pulse width t_W is doubled to approximately 16 ms.

Input PORADJ is biased internally with a pull-down current source of 4 µA which is removed when the voltage on pin PORADJ exceeds 1 V.

This ensures that after detection of the external bridge by the IC during power-on, the input current on pin PORADJ does not cause inaccuracy of the bridge voltage.

Note: The V_{th} threshold of the ST8024L is slightly lower (80 mV typ.) than the ST8024 device. If for example, the microcontroller is shut down at 2.5 V, appropriate external resistor values must be chosen to ensure proper deactivation of the ST8024L device.

5.2.3 Application examples

The voltage supervisor is used as power-on reset and as supply dropout detection during a card session. Supply dropout detection is to ensure that a proper deactivation sequence is followed before the voltage is too low. For the internal voltage supervisor to function, the system microcontroller should operate down to 2.35 V to ensure a proper deactivation sequence. If this is not possible, external resistor values can be chosen to overcome the problem.

5.3 Clock circuitry (only on SO-28 and TSSOP-28 packages)

The card clock signal (CLK) is derived from a clock signal input to pin XTAL1 or from a crystal operating at up to 26 MHz connected between pins XTAL1 and XTAL2.

The clock frequency can be f_{XTAL}, 1/2 x f_{XTAL}, 1/4 x f_{XTAL} or 1/8 x f_{XTAL}. Frequency selection is made via inputs CLKDIV1 and CLKDIV2 (see *Table 21*).

Table 21. Clock frequency selection (1)

CLKDIV1	CLKDIV2	f_{CLK}
0	0	$f_{XTAL}/8$
0	1	$f_{XTAL}/4$
1	1	$f_{XTAL}/2$
1	0	f_{XTAL}

1. The status of pins CLKDIV1 and CLKDIV2 must not be changed simultaneously; a delay of 10 ns minimum between changes is needed. The minimum duration of any state of CLK is eight periods of XTAL1.

The frequency change is synchronous, which means that during transition no pulse is shorter than 45 % of the smallest period, and that the first and last clock pulses about the instant of change have the correct width.

When changing the frequency dynamically, the change is effective for only eight periods of XTAL1 after the command. The duty factor of f_{XTAL} depends on the signal present at pin XTAL1. In order to reach a 45 to 55 % duty factor on pin CLK, the input signal on pin XTAL1 should have a duty factor of 48 to 52 % and transition times of less than 5 % of the input signal period.

If a crystal is used, the duty factor on pin CLK may be 45 to 55 % depending on the circuit layout and on the crystal characteristics and frequency. In other cases, the duty factor on pin CLK is guaranteed between 45 and 55 % of the clock period.

The crystal oscillator runs as soon as the IC is powered up. If the crystal oscillator is used, or if the clock pulse on pin XTAL1 is permanent, the clock pulse is applied to the card as shown in the activation sequences shown in *Figure 5* and *Figure 6*

If the signal applied to XTAL1 is controlled by the system microcontroller, the clock pulse will be applied to the card when it is sent by the system microcontroller (after completion of the activation sequence).

5.4 I/O transceivers

The three data lines I/O, AUX1 and AUX2 are identical.The idle state is realized by both I/O and I/OUC lines being pulled high via a 11 kΩ resistor (I/O to V_{CC} and I/OUC to V_{DD}). Pin I/O is referenced to V_{CC}, and pin I/OUC to V_{DD}, thus allowing operation when V_{CC} is not equal to V_{DD}. The first side of the transceiver to receive a falling edge becomes the master. An anti-latch circuit disables the detection of falling edges on the line of the other side, which then becomes a slave. After a time delay $t_{d(edge)}$, an N transistor on the slave side is turned on, thus transmitting the logic 0 present on the master side. When the master side returns to logic 1, a P transistor on the slave side is turned on during the time delay t_{pu} and then both sides return to their idle states. This active pull-up feature ensures fast low-to-high transitions; it is able to deliver more than 1 mA at an output voltage of up to 0.9 V_{CC} into an 80 pF load. At the end of the active pull-up pulse, the output voltage depends only on the internal pull-up resistor and the load current. The current to and from the card I/O lines is limited internally to 15 mA and the maximum frequency on these lines is 1 MHz.

5.5 Inactive mode

After a power-on reset, the circuit enters the inactive mode. A minimum number of circuits are active while waiting for the microcontroller to start a session:

- All card contacts are inactive (approximately 200 Ω to GND)
- Pins I/OUC, AUX1UC and AUX2UC are in the high-impedance state (11 kΩ pull-up resistor to V_{DD}). Applies only to SO-28 and TSSOP-28 packages.
- Voltage generators are stopped
- XTAL oscillator is running
- Voltage supervisor is active
- The internal oscillator is running at its low frequency.

5.6 Activation sequence

After power-on and after the internal pulse width delay, the system microcontroller can check the presence of a card using the signals $\overline{\text{OFF}}$ and $\overline{\text{CMDVCC}}$ as shown in Table 22.

If the card is in the reader (this is the case if $\overline{\text{PRES}}$ or PRES is active), the system microcontroller can start a card session by pulling $\overline{\text{CMDVCC}}$ low. The following sequence then occurs (see Figure 6):

1. $\overline{\text{CMDVCC}}$ is pulled low and the internal oscillator changes to its high frequency (t_0).
2. The step-up converter is started (between t_0 and t_1).
3. V_{CC} rises from 0 to 5 V (or 1.8 V, 3 V) with a controlled slope ($t_2 = t_1 + 1.5 \times T$) where T is 64 times the period of the internal oscillator (approximately 25 µs).
4. I/O, AUX1 and AUX2 are enabled ($t_3 = t_1 + 4T$) (these were pulled low until this moment).
5. CLK is applied to the C3 contact of the card reader (t_4).
6. RST is enabled ($t_5 = t_1 + 7T$).

The clock may be applied to the card using the following sequence (see Figure 5):

1. Set RSTIN high.
2. Set $\overline{\text{CMDVCC}}$ low.
3. Reset RSTIN low between t_3 and t_5; CLK will start at this moment.
4. RST remains low until t_5, when RST is enabled to be the copy of RSTIN.
5. After t_5, RSTIN has no further affect on CLK; this allows a precise count of CLK pulses before toggling RST.

If the applied clock is not needed, then $\overline{\text{CMDVCC}}$ may be set low with RSTIN low. In this case, CLK will start at t_3 (minimum 200 ns after the transition on I/O), and after t_5, RSTIN may be set high in order to obtain an Answer To Request (ATR) from the card.

Activation should not be performed with RSTIN held permanently high.

Note: It is recommended that no control smartcard signals are to be shared with any other devices. Sharing could result in inadvertent activation or deactivation of the smartcard.

Table 22. Card presence indicator

$\overline{\text{OFF}}$	$\overline{\text{CMDVCC}}$	Indication
H	H	card present
L	H	card not present

Figure 5. Activation sequence using RSTIN and $\overline{CMDVCC}$

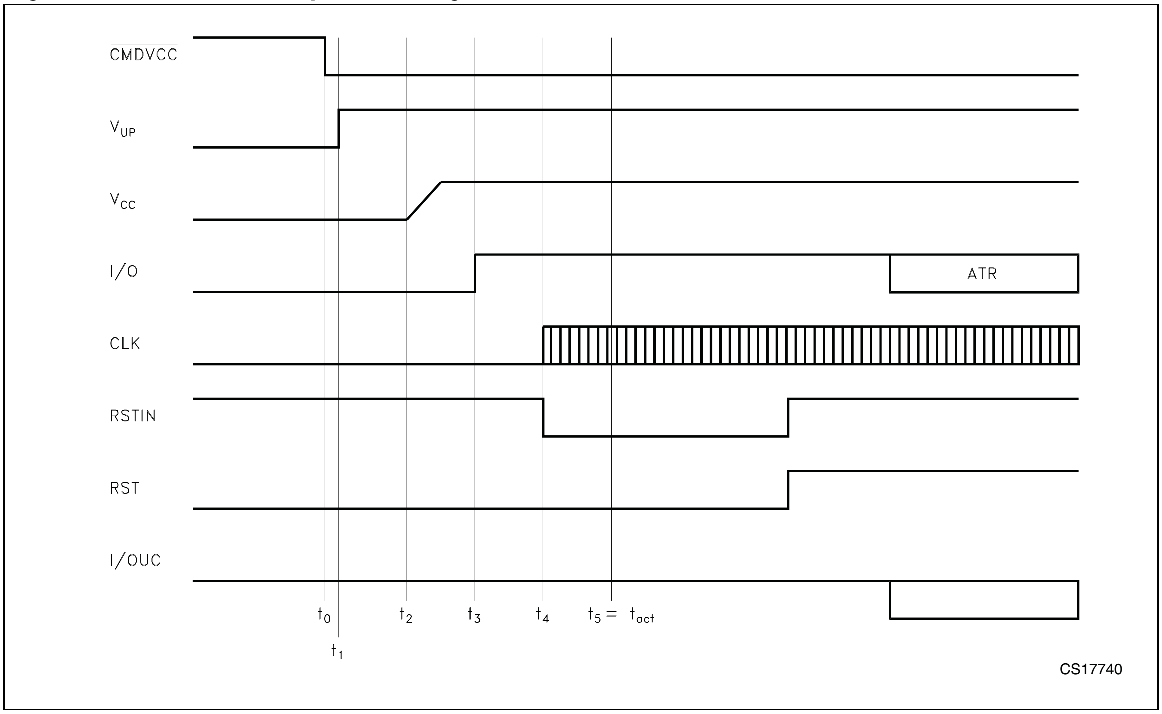
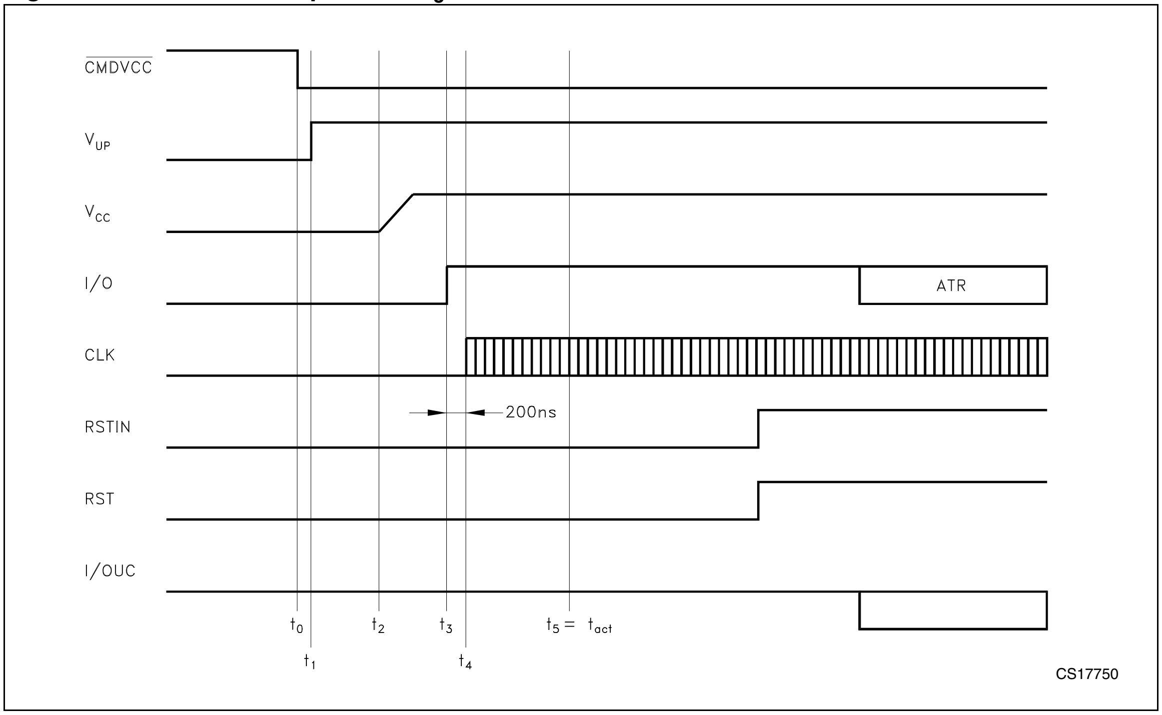


Figure 6. Activation sequence at t_3



5.7 Active mode

When the activation sequence is completed, the ST8024L will be in its active mode. Data are exchanged between the card and the microcontroller via the I/O lines.

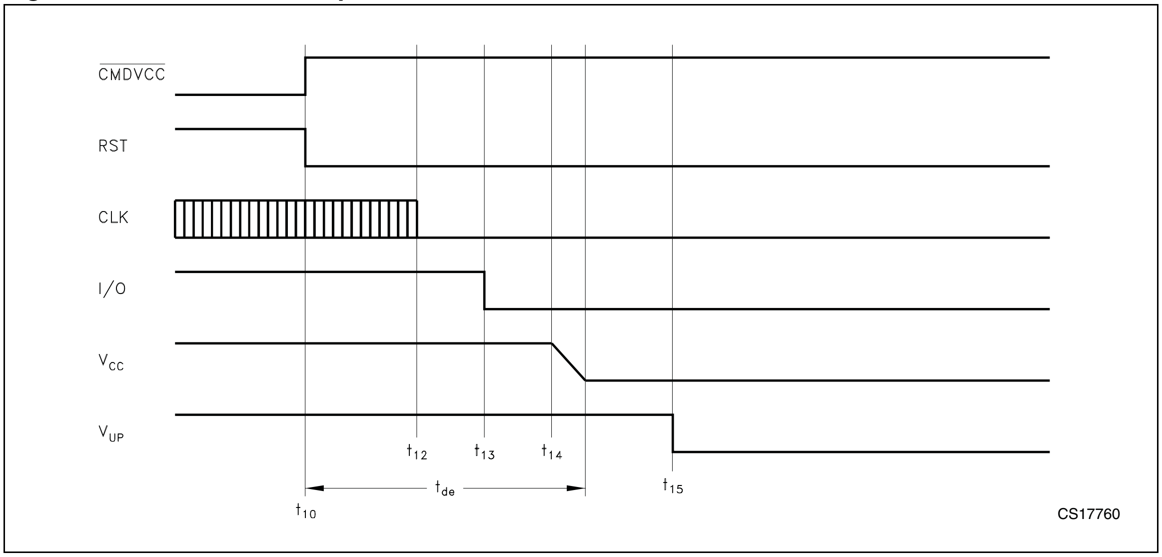
The ST8024L is designed for cards without V_{PP} (the voltage required to program or erase the internal non-volatile memory).

5.8 Deactivation sequence

When a session is completed, the microcontroller sets the $\overline{\text{CMDVCC}}$ line HIGH. The circuit then executes an automatic deactivation sequence by counting the sequencer back and finishing in the inactive mode (see *Figure 7*):

1. RST goes low (t_{10}).
2. CLK is held low ($t_{12} = t_{10} + 0.5 \times T$) where T is 64 times the period of the internal oscillator (approximately 25 µs).
3. I/O, AUX1 and AUX2 are pulled low ($t_{13} = t_{10} + T$).
4. V_{CC} starts to fall towards zero ($t_{14} = t_{10} + 1.5 \times T$).
5. The deactivation sequence is complete at t_{de}, when V_{CC} reaches its inactive state.
6. All card contacts become low-impedance to GND; I/OUC, AUX1UC and AUX2UC remain at V_{DD} (pulled-up via a 11 kΩ resistor).
7. The internal oscillator returns to its lower frequency.

Figure 7. Deactivation sequence



5.9 V_{CC} generator

The V_{CC} generator has a capacity to supply up to 80 mA (max) continuously at 5 V, 65 mA (max) at 3 V, and 45 mA (max) at 1.8 V. An internal overload detector operates at approximately 120 mA. Current samples to the detector are internally filtered, allowing spurious current pulses up to 200 mA with a duration in the order of µs to be drawn by the card without causing deactivation. The average current must stay below the specified maximum current value. For reasons of V_{CC} voltage accuracy, a 100 nF capacitor with an ESR < 350 mΩ should be tied to CGND near to pin V_{CC}, and 100 nF capacitor with the same ESR should be tied to CGND near card reader contact C1.

5.10 Fault detection

The following fault conditions are monitored:

- Short-circuit or high current on V_{CC}
- Removal of a card during a transaction
- V_{DD} dropping
- Step-up converter operating out of the specified values (V_{DDP} too low or current from V_{UP} too high)
- Overheating
- There are two different cases (see *Figure 8*):
- $\overline{\text{CMDVCC}}$ high outside a card session. Output $\overline{\text{OFF}}$ is low if a card is not in the card reader, and high if a card is in the reader. A voltage drop on the V_{DD} supply is detected by the supply supervisor, this generates an internal power-on reset pulse but does not act upon $\overline{\text{OFF}}$. No short-circuit or overheating is detected because the card is not powered-up.
- $\overline{\text{CMDVCC}}$ low within a card session. Output $\overline{\text{OFF}}$ goes low when a fault condition is detected. As soon as this occurs, an emergency deactivation is performed automatically (see *Figure 9*). When the system controller resets $\overline{\text{CMDVCC}}$ to high it may sense the $\overline{\text{OFF}}$ level again after completing the deactivation sequence. This distinguishes between a hardware problem or a card extraction ($\overline{\text{OFF}}$ goes high again if a card is present).

Depending on the type of card-present switch within the connector (normally closed or normally open) and on the mechanical characteristics of the switch, bouncing may occur on the PRES signals at card insertion or withdrawal.

There is a debounce feature in the device with an 8 ms typical duration (see *Figure 8*). When a card is inserted, output $\overline{\text{OFF}}$ goes high only at the end of the debounce time.

When the card is extracted, an automatic deactivation sequence of the card is performed on the first true/false transition on PRES or $\overline{\text{PRES}}$ and output $\overline{\text{OFF}}$ goes low.

Figure 8. Behavior of $\overline{OFF}$, $\overline{CMDVCC}$, PRES and V_{CC}

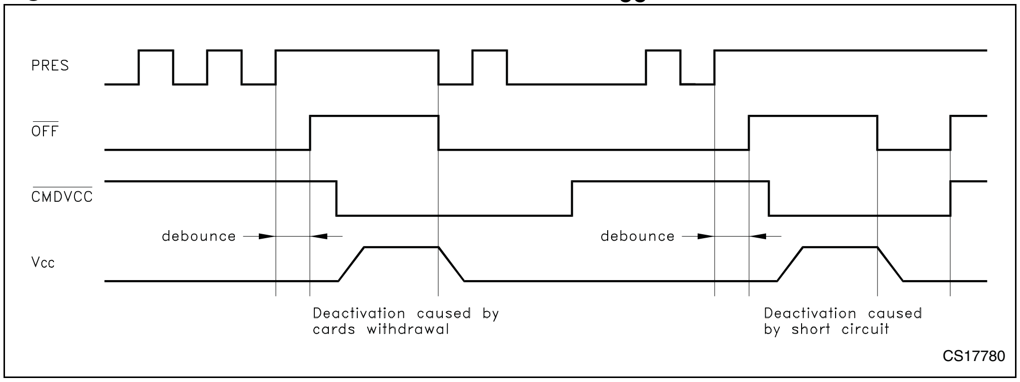
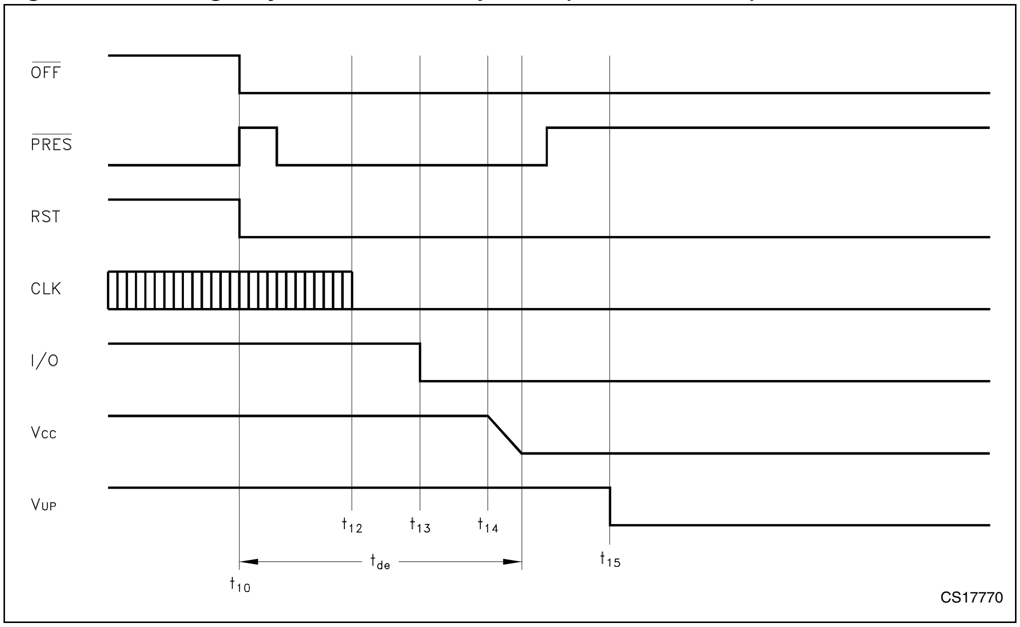


Figure 9. Emergency deactivation sequence (card extraction)



5.11 V_{CC} selection settings

The ST8024L supports three smartcard V_{CC} voltages: 1.8 V, 3 V and 5 V. The V_{CC} selection is controlled by the 1.8V and 5V/$\overline{3V}$ signals as shown in *Table 23*. The 1.8V signal has priority over the 5V/$\overline{3V}$. When the 1.8V pin is taken high, V_{CC} is 1.8V and it overrides any setting on the 5V/$\overline{3V}$ pin.

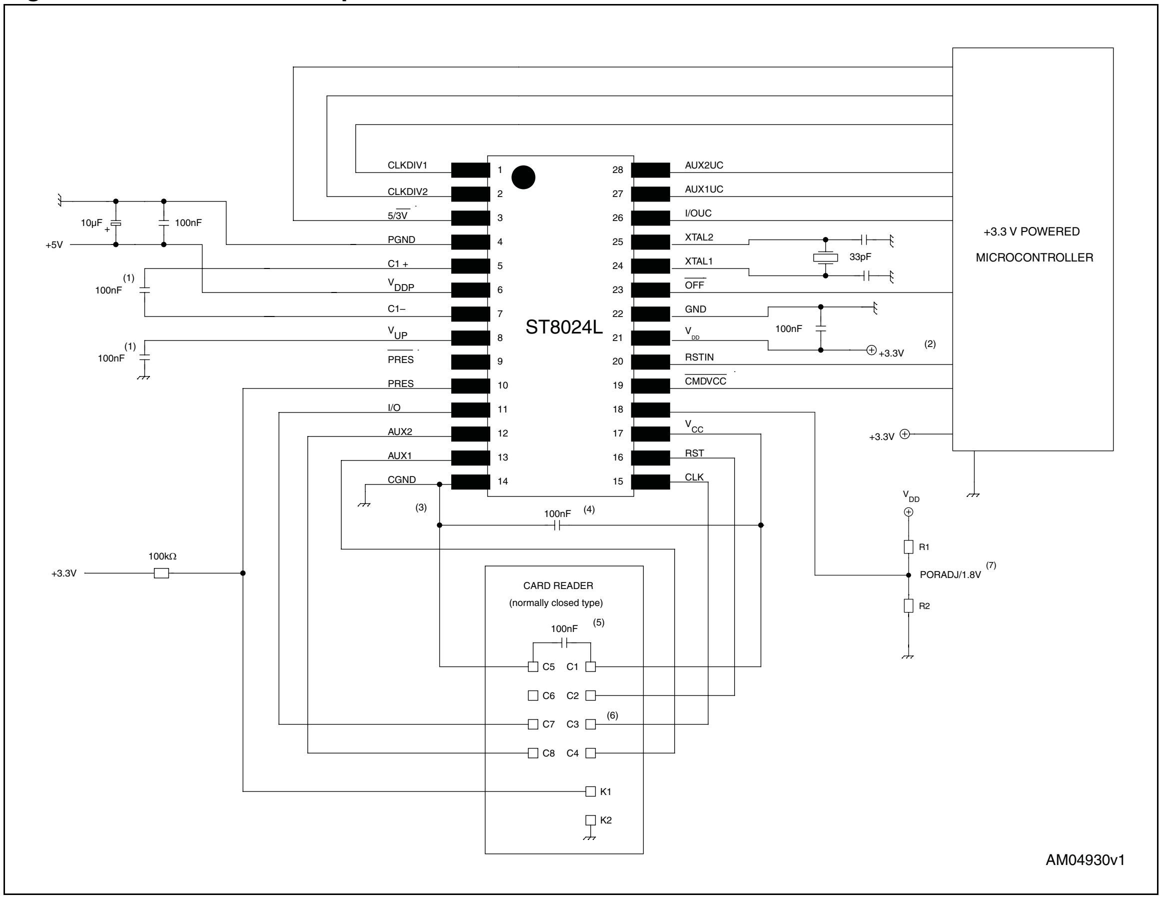
When the 1.8V pin is taken low, the 5V/$\overline{3V}$ pin selects the 5 V or 3 V V_{CC}. If the 5V/$\overline{3V}$ pin is taken high, then V_{CC} is 5 V and if the 5V/$\overline{3V}$ pin is taken low then V_{CC} is 3 V.

Table 23. V_{CC} selection settings

5V/$\overline{3V}$ pin	1.8V pin	V_{CC} output
0	0	3 V
1	0	5 V
x	1	1.8 V

6 Applications

Figure 10. Hardware hookup



1. These capacitors must be < 350 mΩ ESR and be placed near the IC (within 10 mm).
2. ST8024L and the microcontroller must use the same V_{DD} supply.
3. Make short, straight connections between CGND, C5 and the ground connection to the capacitor.
4. Mount one ESR-type (< 350 mΩ) 100 nF capacitor close to pin V_{CC}.
5. Mount one ESR-type (< 350 mΩ) 100 nF capacitor close to C1 contact.
6. The connection to C3 should be routed as far from C2, C7, C4 and C8 and, if possible, surrounded by grounded tracks.
7. This is the optional resistor bridge for changing the threshold of V_{DD} when using the PORADJ function. If this bridge is not required, pin 18 should be connected to ground.

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 11. SO-28 small outline, package mechanical drawing

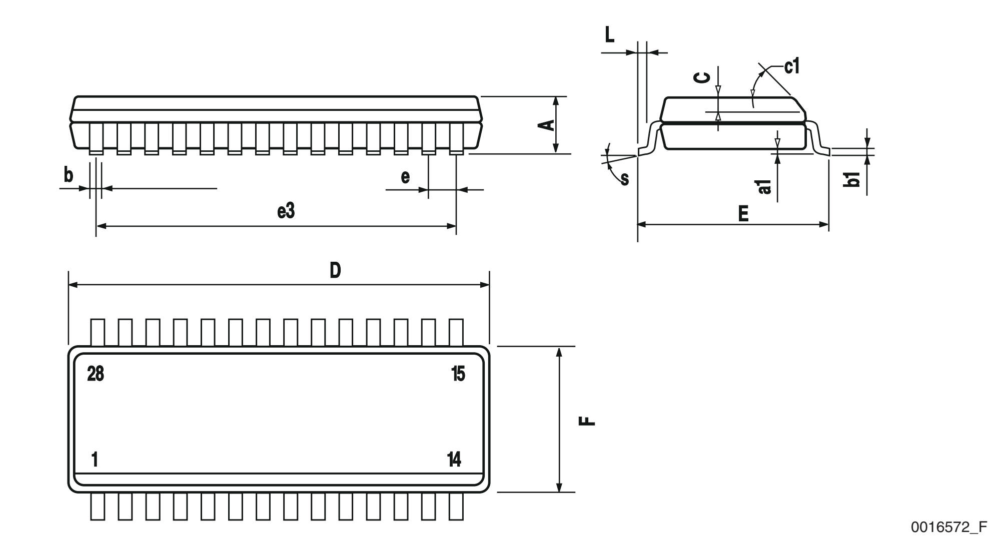


Table 24. SO-28 small outline, package mechanical data

Dimension	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ)					
D	17.70		18.10	0.697		0.713
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		16.51			0.650	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	8° (max)					

Figure 12. TSSOP-20 package mechanical drawing

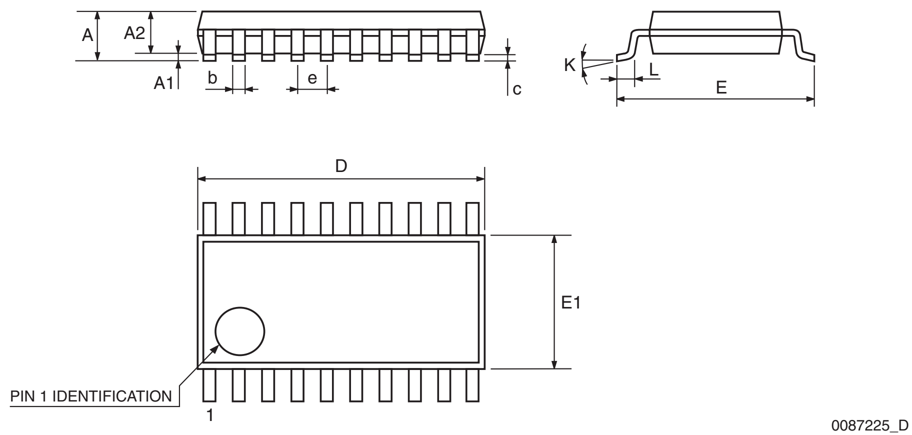


Table 25. TSSOP-20 package mechanical data

Dimension	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 13. TSSOP-28 package mechanical drawing

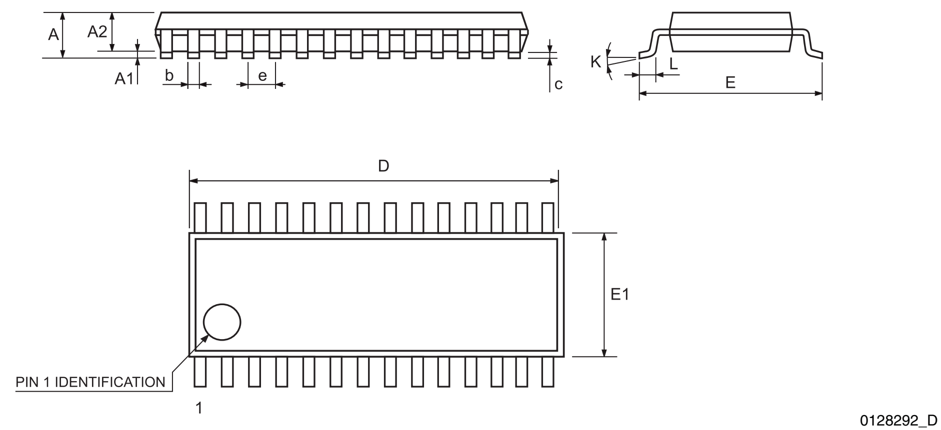


Table 26. TSSOP-28 package mechanical data

Dimension	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	9.6	9.7	9.8	0.378	0.382	0.386
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 14. SO-28 tape and reel schematic

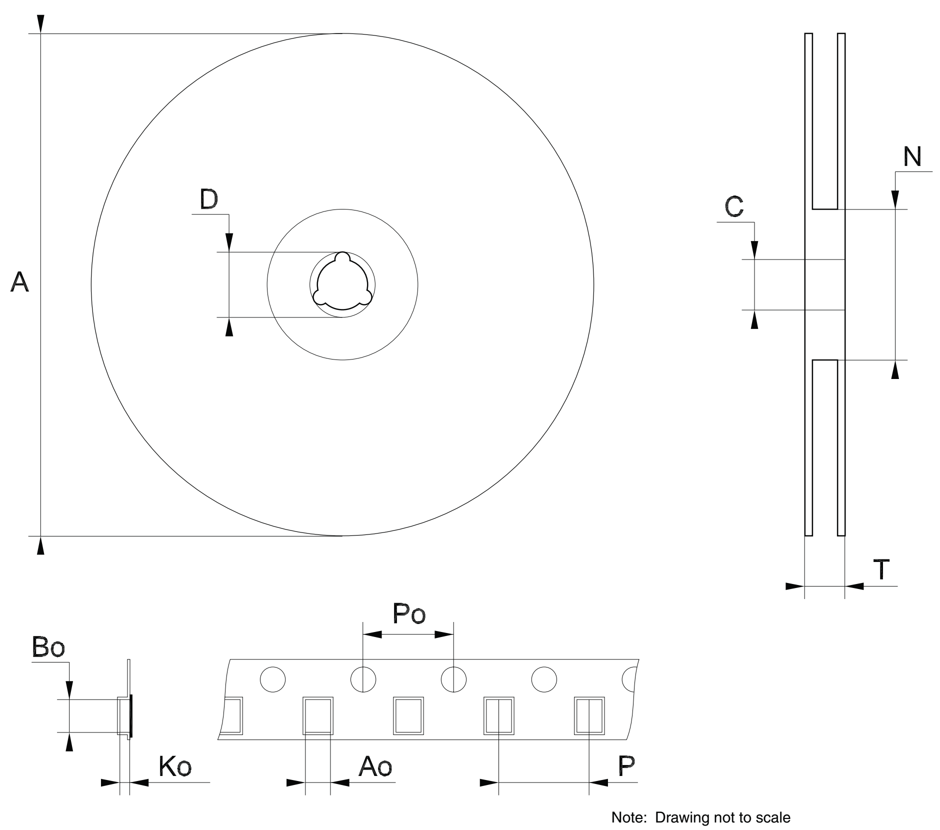


Table 27. SO-28 tape and reel mechanical data

Dimension	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
A_O	10.8		11.0	0.425		0.433
B_O	18.2		18.4	0.716		0.724
K_O	2.9		3.1	0.114		0.122
P_O	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 15. TSSOP-20 tape and reel schematic

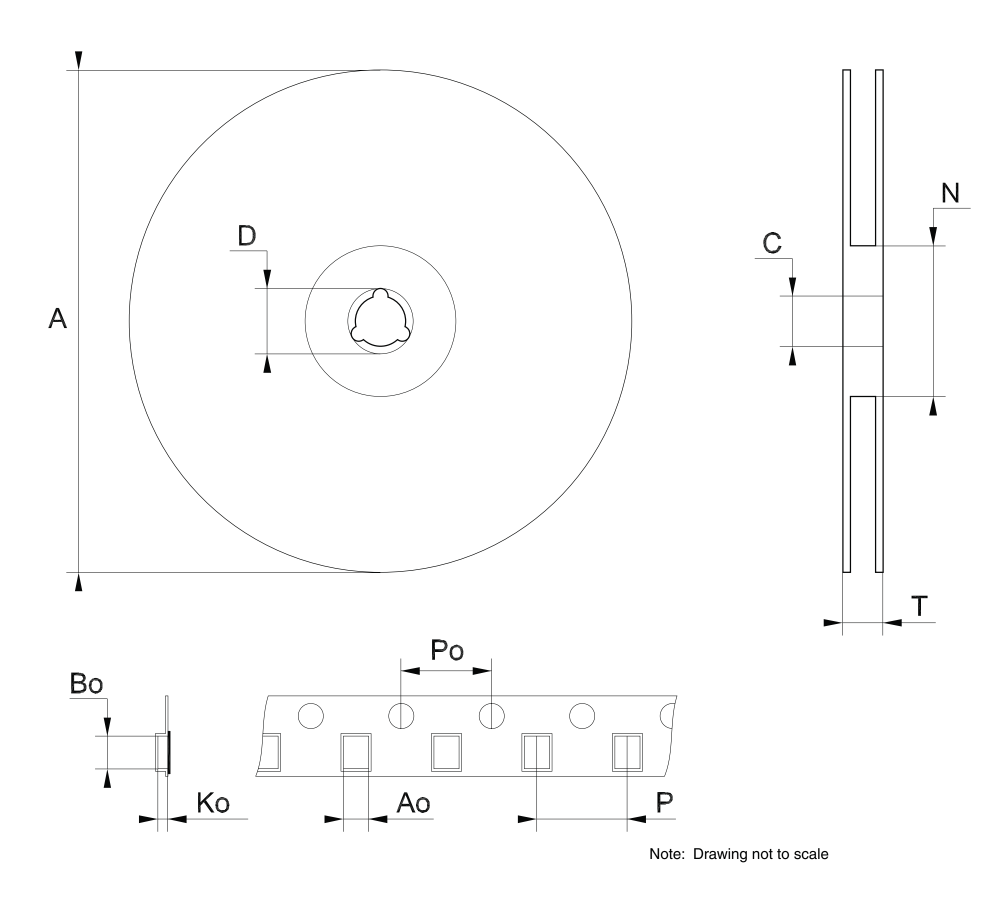


Table 28. TSSOP-20 tape and reel mechanical data

Dimension	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
A_O	6.8		7	0.268		0.276
B_O	6.9		7.1	0.272		0.280
K_O	1.7		1.9	0.067		0.075
P_O	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 16. TSSOP-28 tape and reel schematic

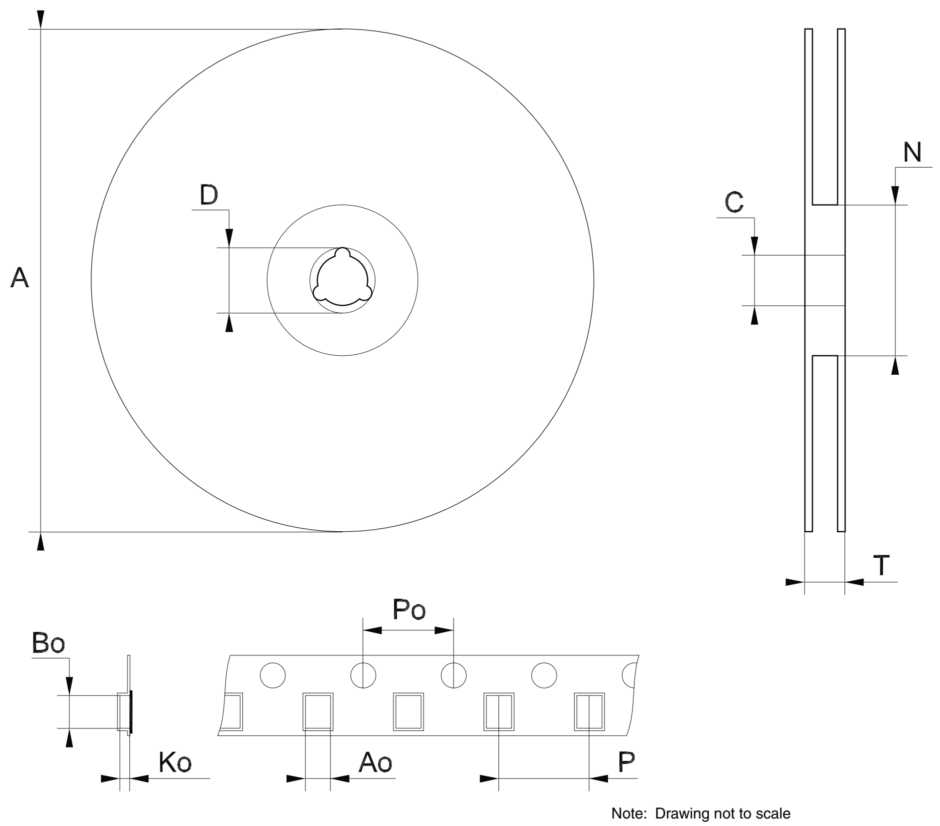


Table 29. TSSOP-28 tape and reel mechanical data

Dimension	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
A_O	6.8		7	0.268		0.276
B_O	10.1		10.3	0.398		0.406
K_O	1.7		1.9	0.067		0.075
P_O	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

8 Revision history

Table 30. Document revision history

Date	Revision	Changes
19-Jul-2010	1	Initial release.
30-Jul-2010	2	Updated *Description*, *Table 6*.
27-Sep-2010	3	Updated *Features*, *Table 1*, *6*, *8*, *19*, *20*, *Section 5.1*, *Section 5.2.2*, *Section 5.6*, *Section 5.9*, footnotes of *Figure 10*.

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