FAIRCHILD SEMICONDUCTOR™

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74VCX32500
Low Voltage 36-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs

General Description

The VCX32500 is an 36-bit universal bus transceiver which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if $\overline{\text{CLKAB}}$ is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{\text{CLKAB}}$. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in a high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active HIGH and $\overline{\text{OEBA}}$ is active LOW).

The VCX32500 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The 74VCX32500 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.4V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (A to B, B to A)
  2.9 ns max for 3.0V to 3.6V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
  ±24 mA @ 3.0V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
  Human body model > 2000V
  Machine model >200V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pull-up resistor and OEAB should be tied to GND through a pull-down resistors; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

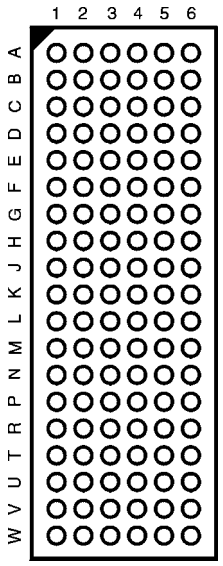
Ordering Code:

Order Number	Package Number	Package Description
74VCX32500G (Note 2)(Note 3)	BGA114A	114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

Note 2: Ordering Code "G" indicates Trays.

Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



(Top Thru View)

FBGA Pin Assignments

	1	2	3	4	5	6
A	$1A_2$	$1A_1$	$LEAB_1$	$\overline{CLKAB}_1$	$1B_1$	$1B_2$
B	$1A_4$	$1A_3$	$OEAB_1$	GND	$1B_3$	$1B_4$
C	$1A_6$	$1A_5$	GND	GND	$1B_5$	$1B_6$
D	$1A_8$	$1A_7$	V_{CC}	V_{CC}	$1B_7$	$1B_8$
E	$1A_{10}$	$1A_9$	GND	GND	$1B_9$	$1B_{10}$
F	$1A_{12}$	$1A_{11}$	GND	GND	$1B_{11}$	$1B_{12}$
G	$1A_{14}$	$1A_{13}$	V_{CC}	V_{CC}	$1B_{13}$	$1B_{14}$
H	$1A_{15}$	$1A_{16}$	GND	GND	$1B_{16}$	$1B_{15}$
J	$1A_{17}$	$1A_{18}$	$\overline{OEBA}_1$	$\overline{CLKBA}_1$	$1B_{18}$	$1B_{17}$
K	NC	$LEAB_2$	$LEBA_1$	GND	$\overline{CLKAB}_2$	NC
L	$2A_2$	$2A_1$	$OEAB_2$	GND	$2B_1$	$2B_2$
M	$2A_4$	$2A_3$	GND	GND	$2B_3$	$2B_4$
N	$2A_6$	$2A_5$	V_{CC}	V_{CC}	$2B_5$	$2B_6$
P	$2A_8$	$2A_7$	GND	GND	$2B_7$	$2B_8$
R	$2A_{10}$	$2A_9$	GND	GND	$2B_9$	$2B_{10}$
T	$2A_{12}$	$2A_{11}$	V_{CC}	V_{CC}	$2B_{11}$	$2B_{12}$
U	$2A_{14}$	$2A_{13}$	GND	GND	$2B_{13}$	$2B_{14}$
V	$2A_{15}$	$2A_{16}$	$\overline{OEBA}_2$	$\overline{CLKBA}_2$	$2B_{16}$	$2B_{15}$
W	$2A_{17}$	$2A_{18}$	$LEBA_2$	GND	$2B_{18}$	$2B_{17}$

Pin Descriptions

Pin Names	Description
$OEAB_n$	Output Enable Input for A to B Direction (Active HIGH)
$\overline{OEBA}_n$	Output Enable Input for B to A Direction (Active LOW)
$LEAB_n$, $LEBA_n$	Latch Enable Inputs
$\overline{CLKAB}_n$, $\overline{CLKBA}_n$	Clock Inputs
$1A_1$–$1A_{18}$ $2A_1$–$2A_{18}$	Side A Inputs or 3-STATE Outputs
$1B_1$–$1B_{18}$ $2B_1$–$2B_{18}$	Side B Inputs or 3-STATE Outputs

Function Table (Note 4)

Inputs				Outputs
$OEAB_n$	$LEAB_n$	$\overline{CLKAB}_n$	A_n	B_n
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0 (Note 5)
H	L	L	X	B_0 (Note 6)

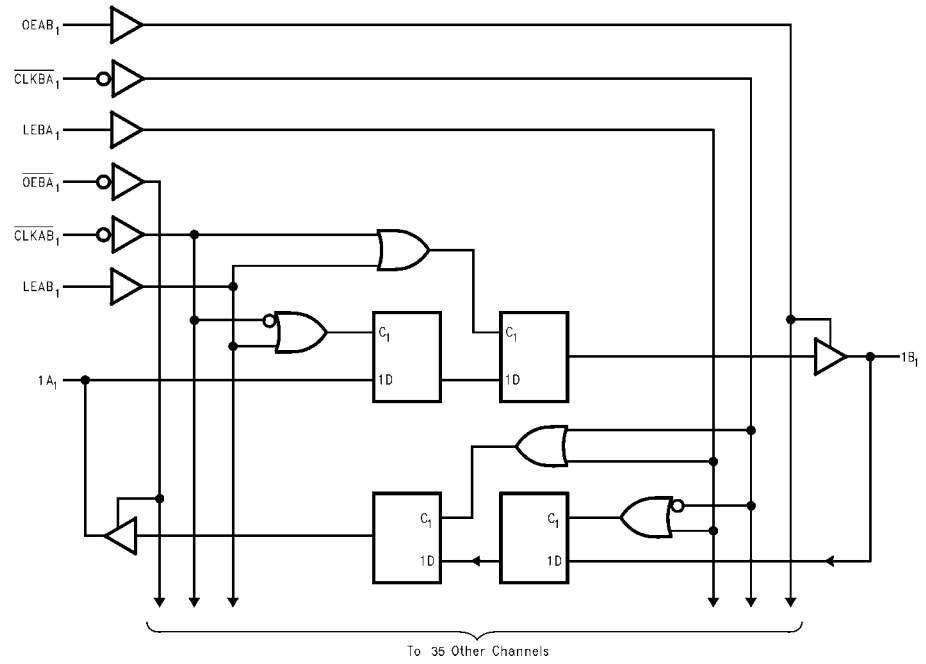
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

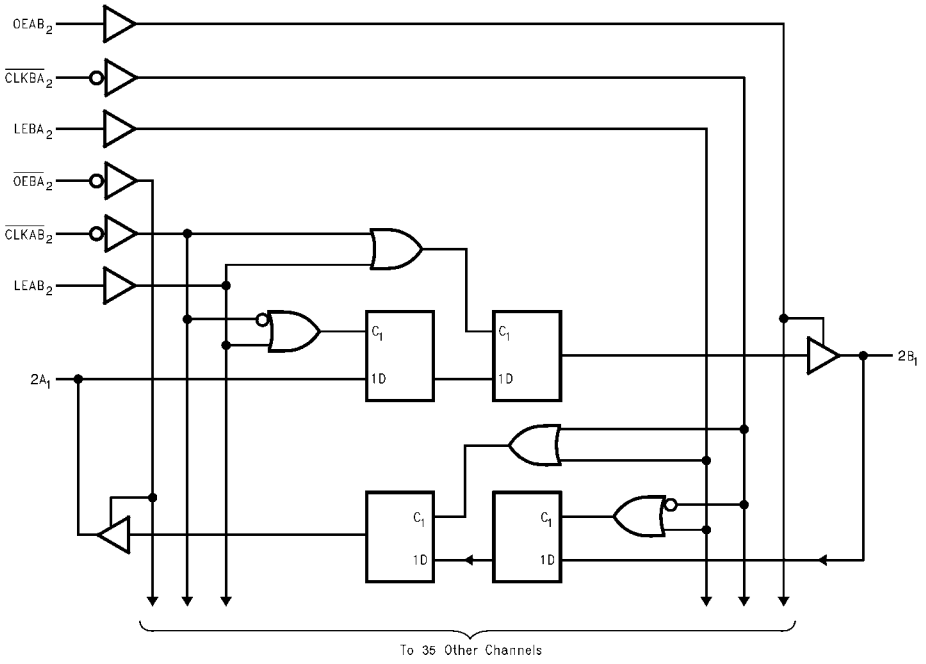
Note 4: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA and $\overline{CLKBA}$. $\overline{OEBA}$ is active LOW.

Note 5: Output level before the indicated steady-state input conditions were established.

Note 6: Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was LOW before LEAB went LOW.

Logic Diagrams





Absolute Maximum Ratings (Note 7)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +4.6V
Outputs Active (Note 8)	−0.5 to V_{CC} + 0.5V
DC Input Diode Current (I_{IK}) V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 9)

Power Supply	
Operating	1.4V to 3.6V
Input Voltage	−0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0V to 3.6V
Output Current in I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±24 mA
V_{CC} = 2.3V to 2.7V	±18 mA
V_{CC} = 1.65V to 2.3V	±6 mA
V_{CC} = 1.4V to 1.6V	±2 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 7: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 8: I_O Absolute Maximum Rating must be observed.

Note 9: Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	0.65 x V_{CC}		
			1.4 - 1.6	0.65 x V_{CC}		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		0.35 x V_{CC}	
			1.4 - 1.6		0.35 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.7 - 3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
		I_{OH} = −100 µA	2.3 - 2.7	V_{CC} − 0.2		
		I_{OH} = −6 mA	2.3	2.0		
		I_{OH} = −12 mA	2.3	1.8		
		I_{OH} = −18 mA	2.3	1.7		
		I_{OH} = −100 µA	1.65 -2.3	V_{CC} − 0.2		
		I_{OH} = −6 mA	1.65	1.25		
		I_{OH} = −100 µA	1.4 - 1.6	V_{CC} − 0.2		
		I_{OH} = −2 mA	1.4	1.05		

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7 - 3.6		0.2	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 18 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
		I_{OL} = 100 μA	2.3 - 2.7		0.2	
		I_{OL} = 12 mA	2.3		0.4	V
		I_{OL} = 18 mA	2.3		0.6	
		I_{OL} = 100 μA	1.65 - 2.3		0.2	
		I_{OL} = 6 mA	1.65		0.3	
		I_{OL} = 100 μA	1.4 - 1.6		0.2	
		I_{OL} = 2 mA	1.4		0.35	
I_I	Input Leakage Current	0V ≤ V_I ≤ 3.6V	1.4 - 3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage	0V ≤ V_O ≤ 3.6V V_I = V_{IH} or V_{IL}	1.4 - 3.6		±10.0	μA
I_{OFF}	Power Off Leakage Current	0V ≤ (V_I, V_O) ≤ 3.6V	0		10.0	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	1.4 - 3.6		40.0	μA
		V_{CC} ≤ (V_I, V_O) ≤ 3.6V (Note 10)	1.4 - 3.6		±40.0	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7 - 3.6		750	μA

Note 10: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 11)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units	Figure Number
				Min	Max		
f_{MAX}	Setup Time	C_L = 30 pF	3.3 ± 0.3	250		MHz	
			2.5 ± 0.2	200			
			1.8 ± 0.15	100			
		C_L = 15 pF	1.5 ± 0.1	80.0			
t_{PHL} t_{PLH}	Propagation Delay Bus-to-Bus	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.6	2.7	ns	Figures 1, 2
			2.5 ± 0.2	0.8	3.5		
			1.8 ± 0.15	1.5	7.0		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	14.0		Figures 7, 8
t_{PHL} t_{PLH}	Propagation Delay Clock-to-Bus	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.6	4.2	ns	Figures 1, 2
			2.5 ± 0.2	0.8	5.3		
			1.8 ± 0.15	1.5	9.8		
		C_L = 15 pF, R_L = 500Ω	1.5 ± 0.1	1.0	19.6		Figures 7, 8
t_{PHL} t_{PLH}	Propagation Delay LE-to-Bus	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.6	3.8	ns	Figures 1, 2
			2.5 ± 0.2	0.8	4.9		
			1.8 ± 0.15	1.5	9.8		
		C_L = 15 pF, R_L = 500Ω	1.5 ± 0.1	1.0	19.6		Figures 7, 8
t_{PZL} t_{PZH}	Output Enable Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.6	3.8	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	4.9		
			1.8 ± 0.15	1.5	9.8		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 7, 9, 10
t_{PLZ} t_{PHZ}	Output Disable Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.6	3.7	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	4.2		
			1.8 ± 0.15	1.5	7.6		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	15.2		Figures 7, 9, 10

AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units	Figure Number
				Min	Max		
t_S	Setup Time	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	1.5		ns	Figures 1, 6
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	2.5			
		$C_L = 15$ pF, $R_L = 500\Omega$	1.5 ± 0.1	3.0			Figures 7, 8
t_H	Hold Time	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	1.0		ns	Figures 1, 6
			2.5 ± 0.2	1.0			
			1.8 ± 0.15	1.0			
		$C_L = 15$ pF, $R_L = 500\Omega$	1.5 ± 0.1	2.0			Figures 7, 6
t_W	Pulse Width	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	1.5		ns	Figures 1, 5
			2.5 ± 1.2	1.5			
			1.8 ± 0.15	4.0			
		$C_L = 15$ pF, $R_L = 500\Omega$	1.5 ± 0.1	4.0			Figures 5, 7

Note 11: For $C_L = 50$pF, add approximately 300ps to the AC maximum specification.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	–0.25	V
			2.5	–0.6	
			3.3	–0.8	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$	Units
C_{IN}	Input Capacitance	$V_I = 0V$ or V_{CC} $V_{CC} = 1.8V$, 2.5V, or 3.3V,	6.0	pF
$C_{I/O}$	Output Capacitance	$V_I = 0V$, or V_{CC}, $V_{CC} = 1.8V$, 2.5V or 3.3V	7.0	pF
C_{PD}	Power Dissipation Capacitance	$V_I = 0V$ or V_{CC}, f = 10 MHz $V_{CC} = 1.8V$, 2.5V or 3.3V	20.0	pF

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.15V)

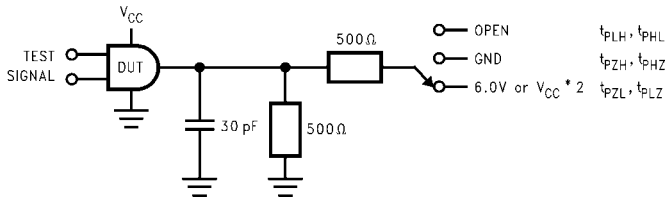


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V; V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V; 1.8 ± 0.15V
t_{PZH}, t_{PHZ}	GND

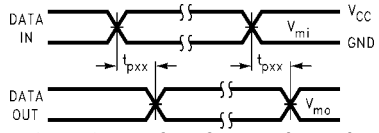


FIGURE 2. Waveform for Inverting and Non-inverting Functions

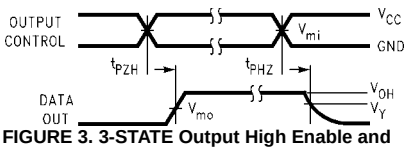


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

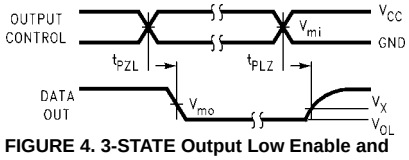


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

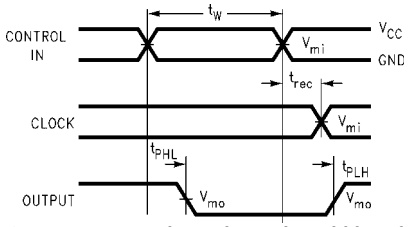


FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms

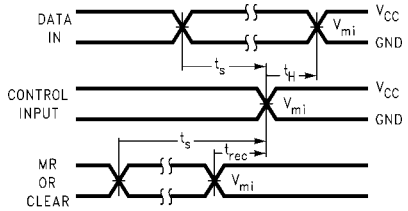
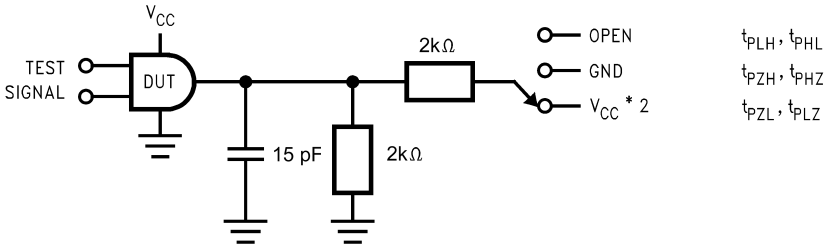


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8 ± 0.15V
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V

AC Loading and Waveforms (V_{CC} 1.5V ± 0.1V)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC} x 2 at V_{CC} = 1.5V ± 0.1V
t_{PZH}, t_{PHZ}	GND

FIGURE 7. AC Test Circuit

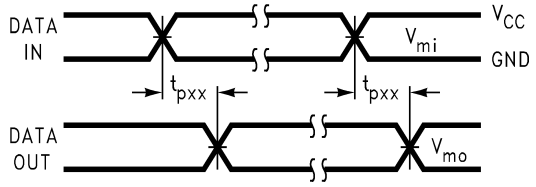


FIGURE 8. Waveform for Inverting and Non-Inverting Functions

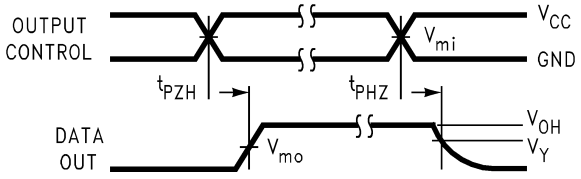


FIGURE 9. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

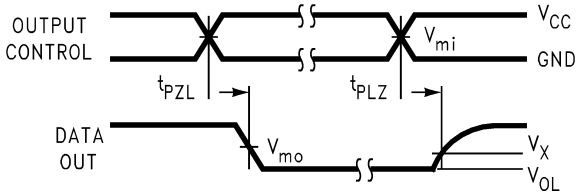
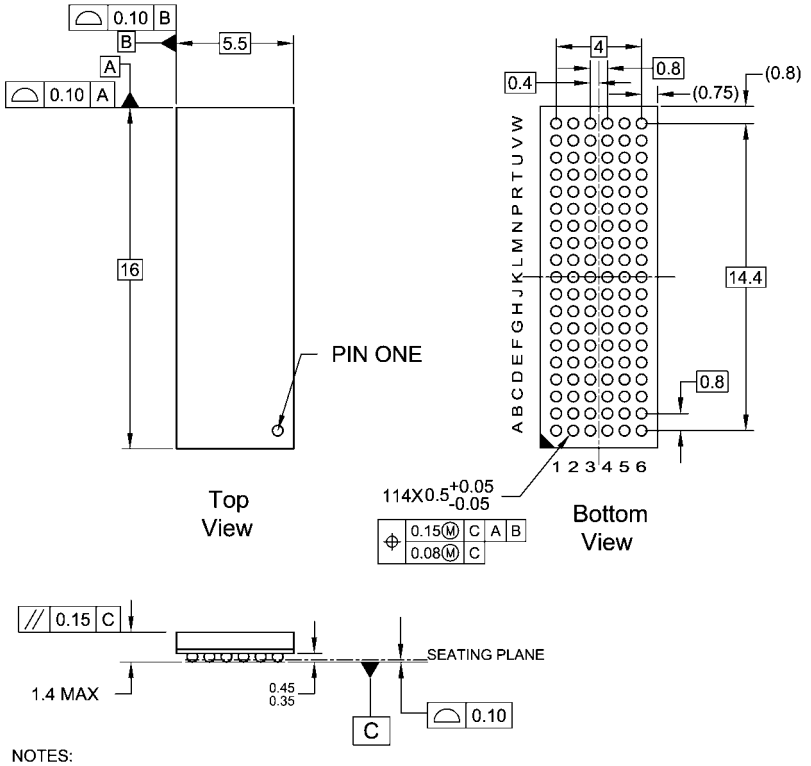


FIGURE 10. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}
	1.5V ± 0.1V
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_x	V_{OL} + 0.1V
V_y	V_{OH} − 0.1V

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA114ArevE

114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA114A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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