±15 kV ESD-Protected, 3.3 V,12 Mbps, EIA RS-485/RS-422 Transceiver

ADM3485E

FEATURES

TIA/EIA RS-485/RS-422 compliant
±15 kV ESD protection on RS-485 input/output pins
12 Mbps data rate
Half-duplex transceiver
Up to 32 nodes on the bus
Receiver open-circuit, fail-safe design
Low power shutdown current
Outputs high-Z when disabled or powered off
Common-mode input range: −7 V to +12 V
Thermal shutdown and short-circuit protection
Industry-standard 75176 pinout
8-lead narrow SOIC package

APPLICATIONS

Power/energy metering
Telecommunications
EMI-sensitive systems
Industrial control
Local area networks

FUNCTIONAL BLOCK DIAGRAM

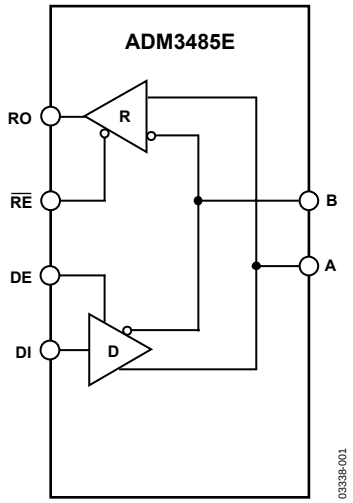

Figure 1.

GENERAL DESCRIPTION

The ADM3485E is a 3.3 V, low power data transceiver with ±15 kV ESD protection, suitable for half-duplex communication on multipoint bus transmission lines. The ADM3485E is designed for balanced data transmission and complies with TIA/EIA standards RS-485 and RS-422. The ADM3485E is a half-duplex transceiver that shares differential lines and has separate enable inputs for the driver and the receiver.

The devices have a 12 kΩ receiver input impedance, which allows up to 32 transceivers on a bus. Because only one driver should be enabled at any time, the output of a disabled or powered-down driver is tristated to avoid overloading the bus.

The receiver has a fail-safe feature that ensures a logic high output when the inputs are floating. Excessive power dissipation caused by bus contention or by output shorting is prevented with a thermal shutdown circuit.

The part is fully specified over the industrial temperature range and is available in an 8-lead narrow SOIC package.

Rev. C

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SPECIFICATIONS

V_{CC} = +3.3 V ± 0.3 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Differential Outputs						
Differential Output Voltage	V_{OD}	2.0			V	R_L = 100 Ω (RS-422) (see Figure 3)
		1.5			V	R_L = 54 Ω (RS-485) (see Figure 3)
		1.5			V	R_L = 60 Ω (RS-485) (see Figure 4)
Δ|V_{OD}| for Complementary Output States[1]	ΔV_{OD}			0.2	V	R_L = 54 Ω or 100 Ω (see Figure 3)
Common-Mode Output Voltage	V_{OC}			3	V	R_L = 54 Ω or 100 Ω (see Figure 3)
Δ|V_{OC}| for Complementary Output States[1]	ΔV_{OC}			0.2	V	R_L = 54 Ω or 100 Ω (see Figure 3)
Short-Circuit Output Current	I_{OSD}	−250			mA	V_{OUT} = −7 V
				250	mA	V_{OUT} = 12 V
Logic Inputs						
Input High Voltage	V_{IH}			0.8	V	DE, DI, $\overline{RE}$
Input Low Voltage	V_{IL}	2.0			V	DE, DI, $\overline{RE}$
Logic Input Current	I_{IN1}			±2	μA	DE, DI, $\overline{RE}$
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage	V_{TH}	−0.2		+0.2	V	−7 V < V_{CM} < +12 V
Input Voltage Hysteresis	ΔV_{TH}		50		mV	V_{CM} = 0 V
Input Resistance (A, B)	R_{IN}	12			kΩ	−7 V < V_{CM} < +12 V
Input Current (A, B)	I_{IN2}			1.0	mA	DE = 0 V, V_{CC} = 0 V or 3.6 V, V_{IN} = 12 V
		−0.8			mA	DE = 0 V, V_{CC} = 0 V or 3.6 V, V_{IN} = −7 V
RO Logic Output						
Output Voltage High	V_{OH}	V_{CC} − 0.4 V			V	I_{OUT} = −1.5 mA, V_{ID} = 200 mV (see Figure 5)
Output Voltage Low	V_{OL}			0.4	V	I_{OUT} = 2.5 mA, V_{ID} = 200 mV (see Figure 5)
Short-Circuit Output Current	I_{OSR}	±8		±60	mA	0 V < V_{RO} < V_{CC}
Tristate Output Leakage Current	I_{OZR}			±1	μA	V_{CC} = 3.6 V, 0 V < V_{OUT} < V_{CC}
POWER SUPPLY CURRENT						
Voltage Range	V_{CC}	3.0		3.6	V	
Supply Current	I_{CC}		1.1	2.2	mA	No load, DI = 0 V or V_{CC}, DE = V_{CC}, $\overline{RE}$ = 0 V or V_{CC}
			0.95	1.9	mA	No load, DI = 0 V or V_{CC}, DE = 0 V, $\overline{RE}$ = 0 V
Shutdown Current	I_{SHDN}		0.002	1	μA	DE = 0 V, $\overline{RE}$ = V_{CC}, DI = 0 V or V_{CC}
ESD PROTECTION						
A, B Pins			±15		kV	Human body model
All Pins Except A, B			±4		kV	Human body model

[1] Δ|V_{OD}| and Δ|V_{OC}| are the changes in V_{OD} and V_{OC}, respectively, when DI input changes state.

TIMING SPECIFICATIONS

V_{CC} = 3.3 V, T_A = 25°C.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate		12	15			
Differential Output Delay	t_{DD}	1	22	35	ns	R_L = 60 Ω, C_{L1} = C_{L2} = 15 pF (see Figure 6)
Differential Output Transition Time	t_{TD}	3	11	25	ns	R_L = 60 Ω, C_{L1} = C_{L2} = 15 pF (see Figure 6)
Propagation Delay						
From Low to High Level	t_{PLH}	7	23	35	ns	R_L = 27 Ω (see Figure 7)
From High to Low Level	t_{PHL}	7	23	35	ns	R_L = 27 Ω (see Figure 7)
$\lvert t_{PLH} - t_{PHL} \rvert$ Propagation Delay Skew	t_{PDS}		–1.4	±8	ns	R_L = 27 Ω (see Figure 7)
Enable/Disable Timing						
Enable Time to Low Level	t_{PZL}		42	90	ns	R_L = 110 Ω (see Figure 9)
Enable Time to High Level	t_{PZH}		42	90	ns	R_L = 110 Ω (see Figure 8)
Disable Time from Low Level	t_{PLZ}		35	80	ns	R_L = 110 Ω (see Figure 9)
Disable Time from High Level	t_{PHZ}		35	80	ns	R_L = 110 Ω (see Figure 8)
Enable Time from Shutdown to Low Level	t_{PSL}		650	900	ns	R_L = 110 Ω (see Figure 9)
Enable Time from Shutdown to High Level	t_{PSH}		650	900	ns	R_L = 110 Ω (see Figure 8)
RECEIVER						
Propagation Delay						
From Low to High Level	t_{RPLH}	25	62	90	ns	V_{ID} = 0 V to 3.0 V, C_L = 15 pF (see Figure 10)
From High to Low Level	t_{RPHL}	25	62	90	ns	V_{ID} = 0 V to 3.0 V, C_L = 15 pF (see Figure 10)
$\lvert t_{RPLH} - t_{RPHL} \rvert$ Propagation Delay Skew	t_{RPDS}		6	±10	ns	V_{ID} = 0 V to 3.0 V, C_L = 15 pF (see Figure 10)
Enable/Disable Timing						
Enable Time to Low Level	t_{RPZL}		25	50	ns	C_L = 15 pF (see Figure 11)
Enable Time to High Level	t_{RPZH}		25	50	ns	C_L = 15 pF (see Figure 11)
Disable Time from Low Level	t_{RPLZ}		25	45	ns	C_L = 15 pF (see Figure 11)
Disable Time from High Level	t_{RPHZ}		25	45	ns	C_L = 15 pF (see Figure 11)
Enable Time from Shutdown to Low Level	t_{RPSL}		720	1400	ns	C_L = 15 pF (see Figure 11)
Enable Time from Shutdown to High Level	t_{RPSH}		720	1400	ns	C_L = 15 pF (see Figure 11)
Time to Shutdown[1]	t_{SHDN}	80	190	300	ns	

[1] The transceivers are put into shutdown mode by bringing the $\overline{RE}$ high and the DE low. If the inputs are in this state for less than 80 ns, the parts are guaranteed not to enter shutdown. If the parts are in this state for 300 ns or more, the parts are guaranteed to enter shutdown.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Values
V_{CC} to GND	−0.3 V to +6 V
Digital Input/Output Voltage (DE, $\overline{RE}$, DI)	−0.3 V to +6 V
Receiver Output Voltage (RO)	−0.3 V to (V_{CC} + 0.3 V)
Driver Output (A, B)/ Receiver Input (A, B) Voltage	−8 V to +13 V
Driver Output Current	±250 mA
Power Dissipation (8-Lead SOIC_N)	650 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD Rating	
Human Body Model (A, B)	±15 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead SOIC_N	158	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

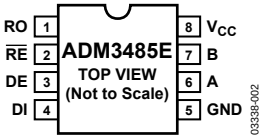


Figure 2. SOIC_N Pin Configuration (R-8)

Table 5. Pin Function Descriptions

Mnemonic	Pin Number	Description
RO	1	Receiver Output. When enabled, if A > B by 200 mV, then RO = high. If A < B by 200 mV, then RO = low.
$\overline{RE}$	2	Receiver Output Enable. With $\overline{RE}$ low, the receiver output (RO) is enabled. With $\overline{RE}$ high, the output goes into a high impedance state. If $\overline{RE}$ is high and DE is low, the ADM3485E enters a shutdown state.
DE	3	Driver Output Enable. A high level enables the driver differential outputs A and B. A low level places it in a high impedance state.
DI	4	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high, while a logic high on DI forces A high and B low.
GND	5	Ground Connection, 0 V.
A	6	Noninverting Receiver Input A/Driver Output A.
B	7	Inverting Receiver Input B/Driver Output B.
V_{CC}	8	Power Supply, 3.3 V ± 0.3 V.

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

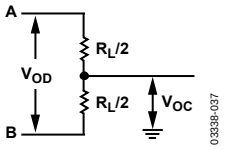


Figure 3. Driver Differential Output Voltage and Common-Mode Output Voltage

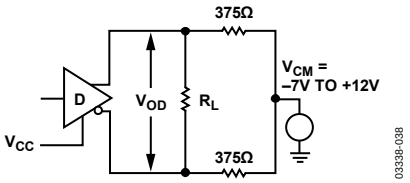


Figure 4. Driver Differential Output Voltage with Varying Common-Mode Voltage

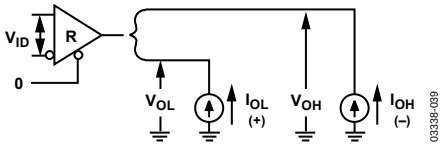
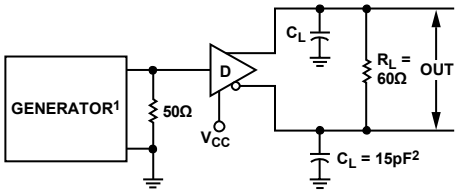


Figure 5. Receiver Output Voltage High and Output Voltage Low



[1]PPR = 250kHz, 50% DUTY CYCLE, $t_R \le 6.0$ns, $Z_O = 50\Omega$.
[2]C_L INCLUDES PROBE AND STRAY CAPACITANCE.

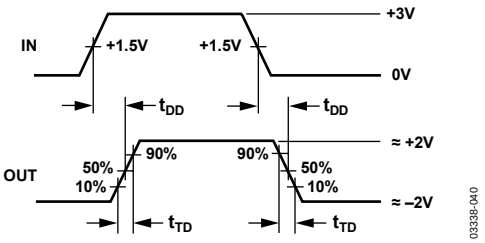
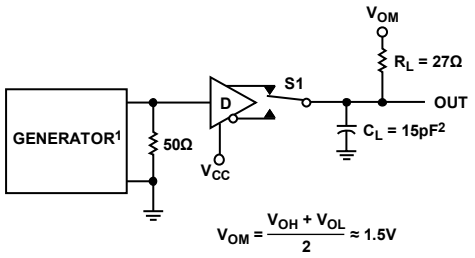


Figure 6. Driver Differential Output Delay and Transition Times



[1]PPR = 250kHz, 50% DUTY CYCLE, $t_R \le 6.0$ns, $Z_O = 50\Omega$.
[2]C_L INCLUDES PROBE AND STRAY CAPACITANCE.

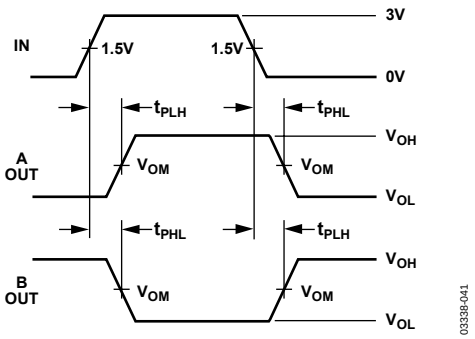
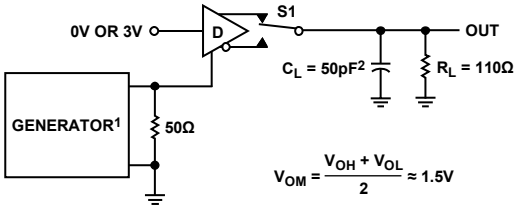


Figure 7. Driver Propagation Delays



[1]PPR = 250kHz, 50% DUTY CYCLE, $t_R \le 6.0$ns, $Z_O = 50\Omega$.
[2]C_L INCLUDES PROBE AND STRAY CAPACITANCE.

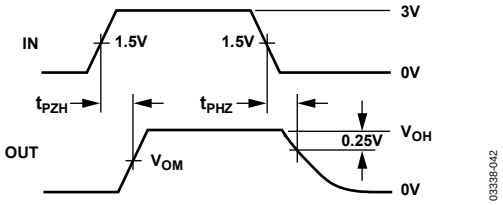
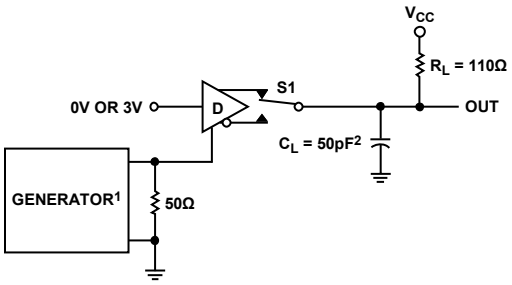


Figure 8. Driver Enable and Disable Times (t_{PZH}, t_{PSH}, t_{PHZ})



1PPR = 250kHz, 50% DUTY CYCLE, $t_R \le 6.0$ns, $Z_O = 50\Omega$.
2C_L INCLUDES PROBE AND STRAY CAPACITANCE.

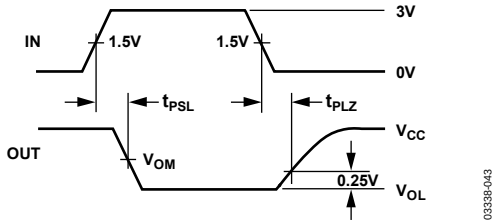
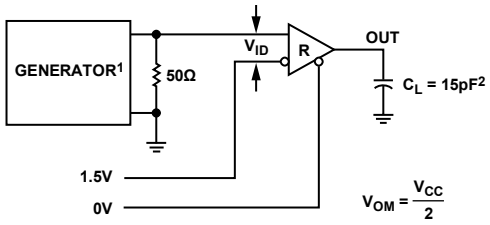


Figure 9. Driver Enable and Disable Times (t_{PZL}, t_{PSL}, t_{PLZ})



1PPR = 250kHz, 50% DUTY CYCLE, $t_R \le 6.0$ns, $Z_O = 50\Omega$.
2C_L INCLUDES PROBE AND STRAY CAPACITANCE.

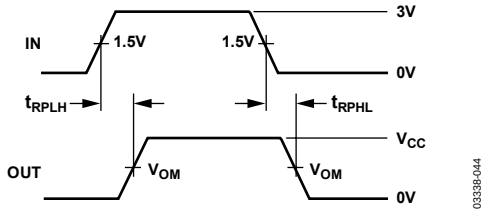
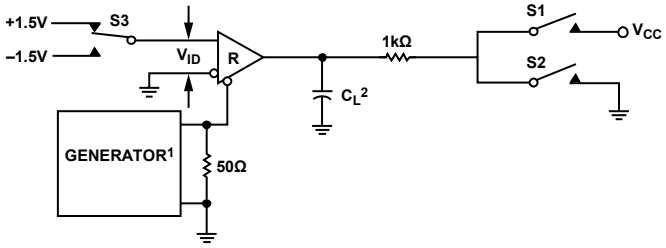


Figure 10. Receiver Propagation Delays



1PPR = 250kHz, 50% DUTY CYCLE, $t_R \le 6.0$ns, $Z_O = 50\Omega$.
2C_L INCLUDES PROBE AND STRAY CAPACITANCE.

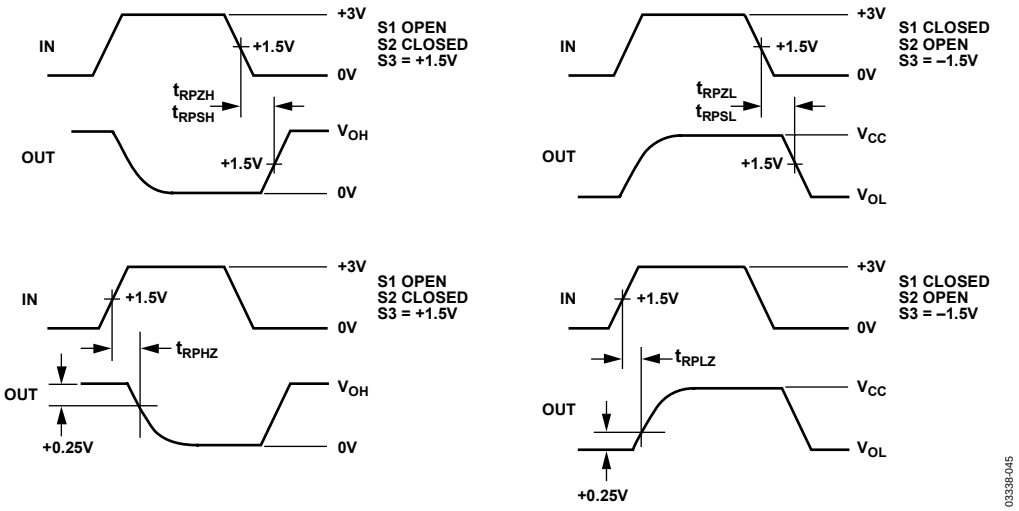


Figure 11. Receiver Enable and Disable Times

TYPICAL PERFORMANCE CHARACTERISTICS

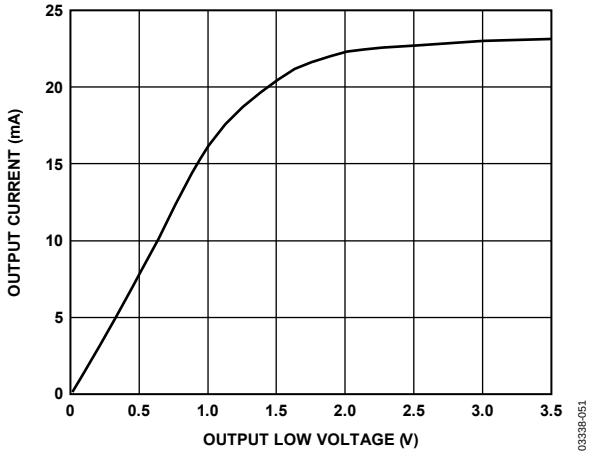


Figure 12. Output Current vs. Receiver Output Low Voltage

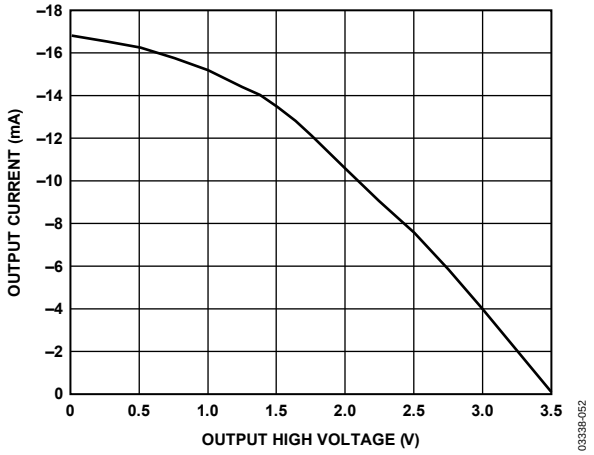


Figure 13. Output Current vs. Receiver Output High Voltage

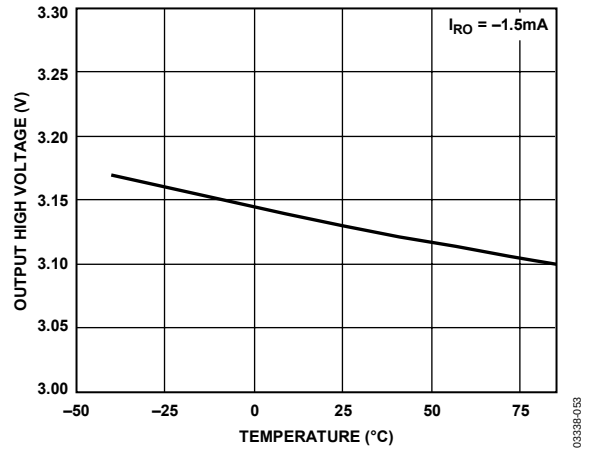


Figure 14. Receiver Output High Voltage vs. Temperature

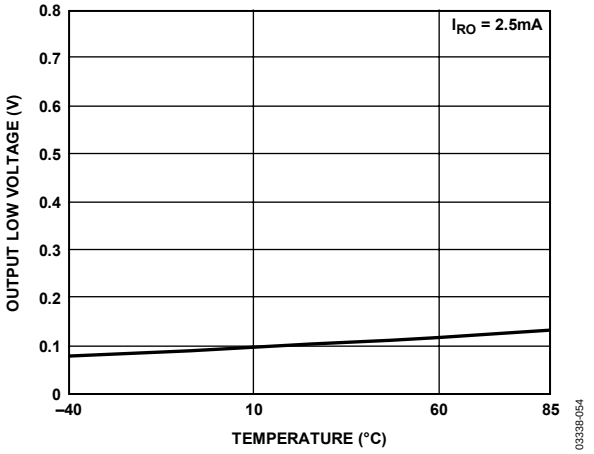


Figure 15. Receiver Output Low Voltage vs. Temperature

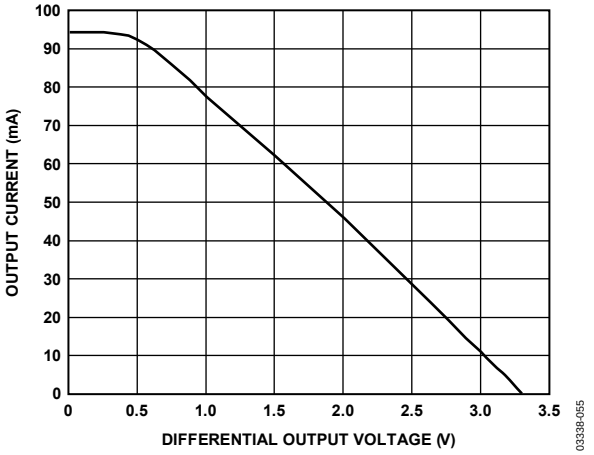


Figure 16. Driver Output Current vs. Differential Output Voltage

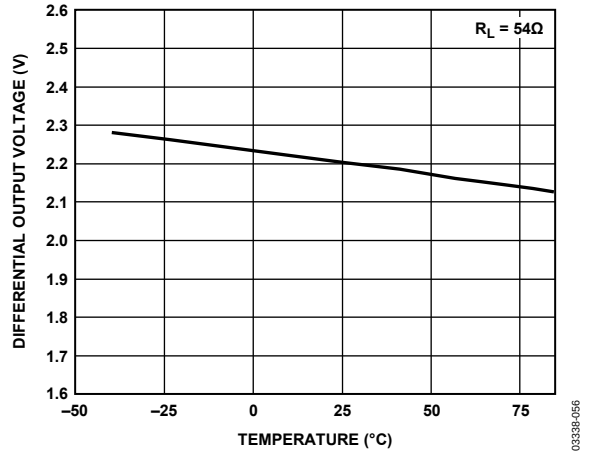


Figure 17. Driver Differential Output Voltage vs. Temperature

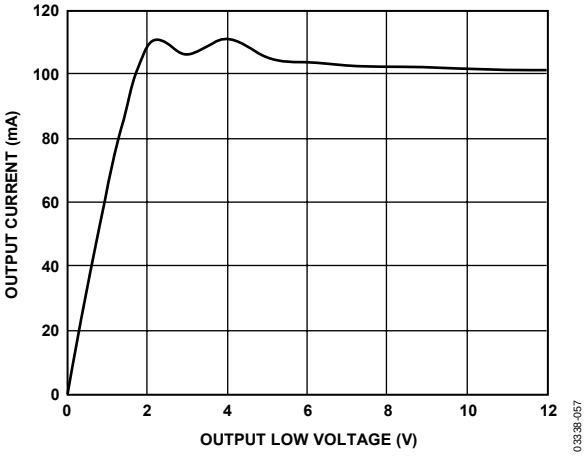


Figure 18. Output Current vs. Driver Output Low Voltage

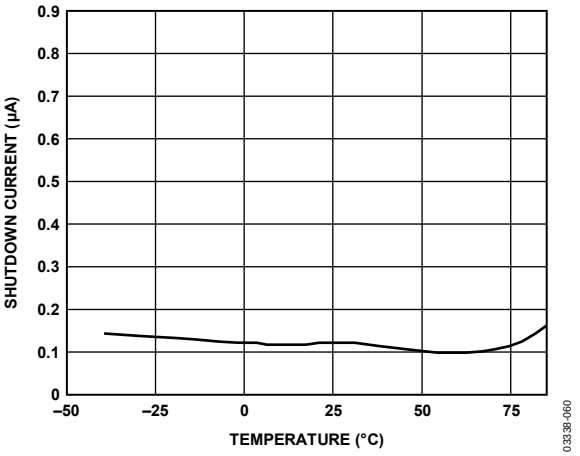


Figure 21. Shutdown Current vs. Temperature

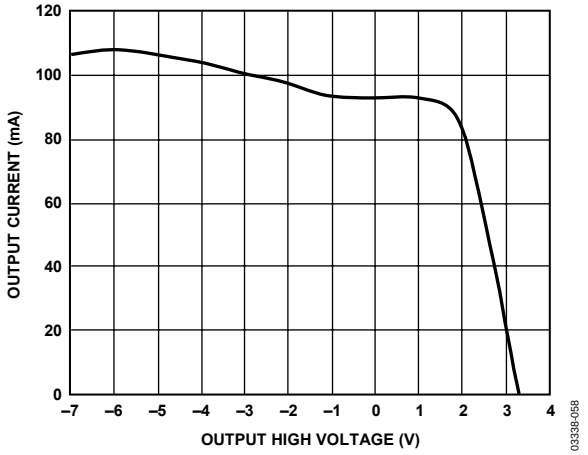


Figure 19. Output Current vs. Driver Output High Voltage

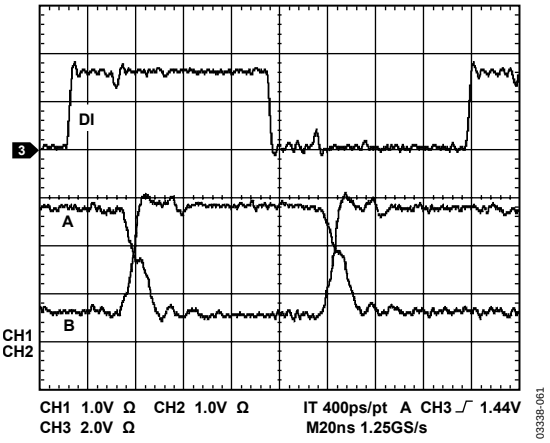


Figure 22. Driver Propagation Delay

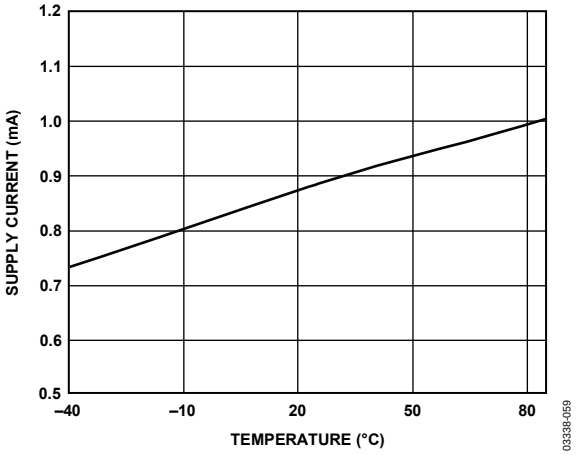


Figure 20. Supply Current vs. Temperature

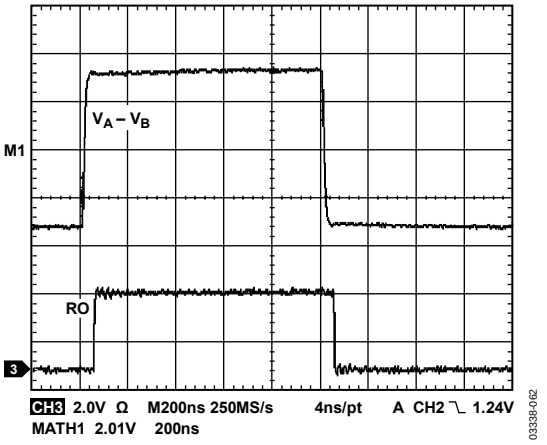


Figure 23. Receiver Propagation Delay, Driven by External RS-485 Device

STANDARDS AND TESTING

Table 6 compares RS-422 and RS-485 interface standards, and Table 7 and Table 8 show transmitting and receiving truth tables.

Table 6.

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Data Rate	10 Mbps	10 Mbps
Maximum Cable Length	4000 ft	4000 ft
Minimum Driver Output Voltage	±2 V	±1.5 V
Driver Load Impedance	100 Ω	54 Ω
Receiver Input Resistance	4 kΩ min	12 kΩ min
Receiver Input Sensitivity	±200 mV	±200 mV
Receiver Input Voltage Range	−7 V to +7 V	−7 V to +12 V
Number of Drivers/Receivers per Line	1/10	32/32

Table 7. Transmitting Truth Table

Transmitting Inputs			Transmitting Outputs	
$\overline{RE}$	DE	DI	B	A
X[1]	1	1	0	1
X[1]	1	0	1	0
0	0	X[1]	High-Z[2]	High-Z[2]
1	0	X[1]	High-Z[2]	High-Z[2]

[1] X = don't care.
[2] High-Z = high impedance.

Table 8. Receiving Truth Table

Receiving Inputs		Receiving Outputs	
$\overline{RE}$	DE	A – B	RO
0	X[1]	> +0.2 V	1
0	X[1]	< –0.2 V	0
0	X[1]	Inputs open	1
1	X[1]	X[1]	High-Z[2]

[1] X = don't care.
[2] High-Z = high impedance.

ESD TESTING

Two coupling methods are used for ESD testing, contact discharge and air-gap discharge. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage but does not make direct contact with the unit under test. With air-gap discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap, hence the term air-gap discharge. This method is influenced by humidity, temperature, barometric pressure, distance, and rate of closure of the discharge gun. The contact discharge method, while less realistic, is more repeatable and is gaining acceptance and preference over the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time, coupled with high voltages, can cause failures in unprotected semiconductors. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device can suffer from parametric degradation, which can result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

I/O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I/O cable can result in a static discharge that can damage or completely destroy the interface product connected to the I/O port. It is extremely important, therefore, to have high levels of ESD protection on the I/O lines.

The ESD discharge could induce latch-up in the device under test, so it is important that ESD testing on the I/O pins be carried out while device power is applied. This type of testing is more representative of a real-world I/O discharge, where the equipment is operating normally when the discharge occurs.

Table 9. ESD Test Results

ESD Test Method	I/O Pins
Human Body Model	±15 kV

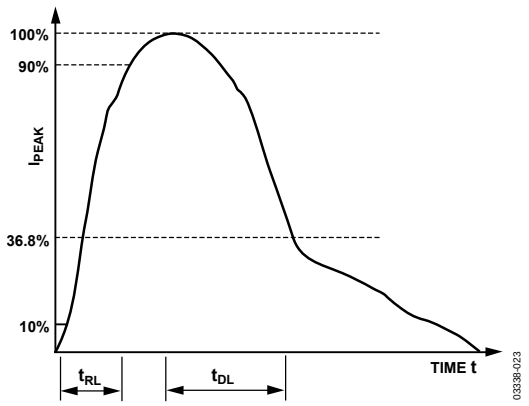


Figure 24. Human Body Model Current Waveform

APPLICATIONS INFORMATION

DIFFERENTIAL DATA TRANSMISSION

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals that appear as common-mode voltages on the line.

Two main standards that specify the electrical characteristics of transceivers used in differential data transmission are approved by the Electronics Industries Association (EIA). The RS-422 standard specifies data rates up to 10 Mbps and line lengths up to 4000 feet. A single driver can drive a transmission line with up to 10 receivers. The RS-485 standard was defined to cater to true multipoint communications. This standard meets or exceeds all the requirements of RS-422 but also allows multiple drivers and receivers to be connected to a single bus. An extended common-mode range of −7 V to +12 V is defined.

The most significant difference between RS-422 and RS-485 is the fact that under the RS-485 standard the drivers may be disabled, thereby allowing more than one to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

CABLE AND DATA RATE

The transmission line of choice for RS-485 communications is a twisted pair. Twisted-pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

The ADM3485E is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 25. Only one driver can transmit at a particular time, but multiple receivers may be enabled simultaneously.

As with any transmission line, it is important that reflections are minimized. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths off the main line must also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

RECEIVER OPEN-CIRCUIT FAIL-SAFE

The receiver input includes a fail-safe feature that guarantees a logic high on the receiver when the inputs are open circuit or floating.

Table 10. RS-422 and RS-485 Interface Standards

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Cable Length	4000 ft	4000 ft
Minimum Driver Output Voltage	±2 V	±1.5 V
Driver Load Impedance	100 Ω	54 Ω
Receiver Input Resistance	4 kΩ min	12 kΩ min
Receiver Input Sensitivity	±200 mV	±200 mV
Receiver Input Voltage Range	−7 V to +7 V	−7 V to +12 V

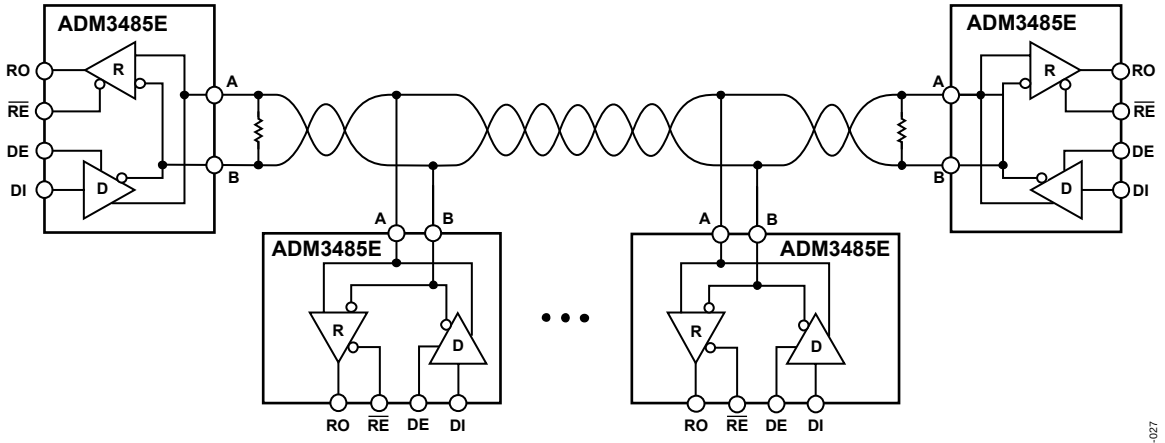


Figure 25. Multipoint Transmission Network

OUTLINE DIMENSIONS

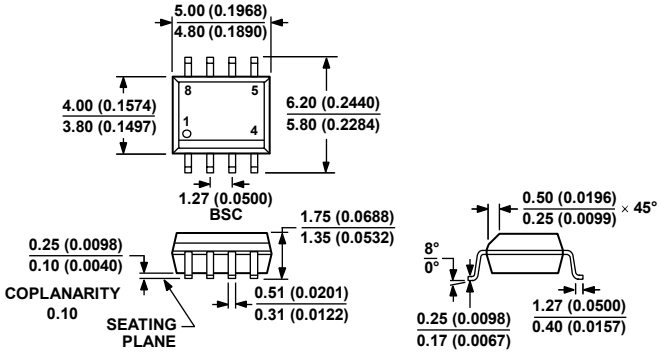


Figure 26. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM3485EAR	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM3485EAR-REEL7	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM3485EAR-REEL	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM3485EARZ[1]	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM3485EARZ-REEL7[1]	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM3485EARZ-REEL[1]	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = Pb-free part.

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