Isolated 15kV ESD Protected RS-485 Transceiver with Integrated Isolated DC/DC Converter

Preliminary Technical Data

ADM2582E/ADM2587E

FEATURES

Isolated RS-485/RS-422 transceiver, configurable as half or full duplex
***iso*Power™ integrated isolated DC/DC converter**
±15 kV ESD protection on RS485 input/output pins
Complies with ANSI/TIA/EIA-485-A-98 and ISO 8482:1987(E)
Data rate: 500kbps/16 Mbps
5 V or 3.3V operation
Short Circuit to
256 nodes on bus
True fail-safe receiver inputs
High common-mode transient immunity: >25 kV/µs
Thermal shutdown protection
Safety and regulatory approvals (targeted)
UL recognition: 2500 V_{RMS} for 1 minute per UL 1577
VDE Certificates of Conformity
DIN VVDE V 0884-10 (VDE V 0884-10):2006-12
V_{IORM} = 560 V peak
Operating temperature range: –40° to +85°C
Wide-body, 20-lead SOIC package

APPLICATIONS

Isolated RS-485/RS-422 interfaces
Industrial field networks
Multipoint data transmission systems

FUNCTIONAL BLOCK DIAGRAM

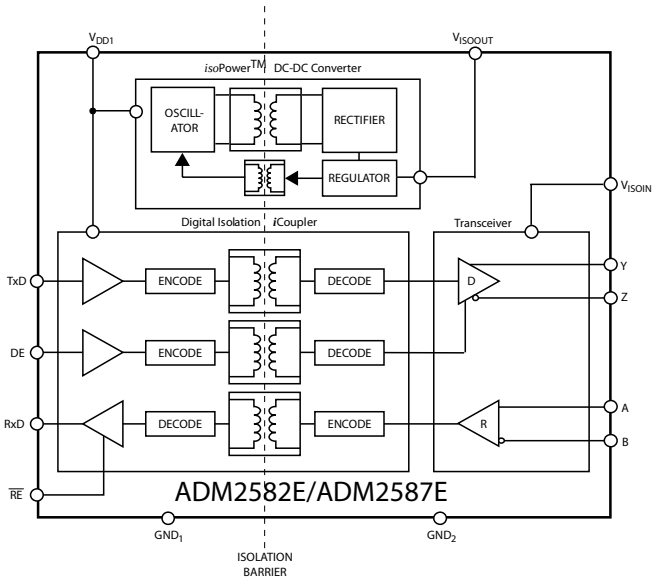

Figure 1.

GENERAL DESCRIPTION

The ADM2582E/ADM2587E are fully integrated isolated data transceivers with ±15 kV ESD protection and is suitable for high speed communication on multipoint transmission lines. The ADM2582E/ADM2587E includes an integrated Isolated DC-DC Power supply, which eliminates the need for an external DC-DC Isolation block.

It is designed for balanced transmission lines and complies with ANSI/TIA/EIA RS-485-A-98 and ISO 8482:1987(E).

The device employs Analog Devices, Inc., *i*Coupler® technology to combine a 3-channel isolator, a three-state differential line driver, a differential input receiver and an *iso*Power™ DC-DC converter into a single package. The device is powered by a single 5V or 3.3V supply realizing a fully isolated RS-485 solution.

The ADM2582E/ADM2587E driver has an active high enable. Also provided is an active high receiver disable that causes the receive output to enter a high impedance state.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where bus contention might cause excessive power dissipation. The part is fully specified over the industrial temperature range and is available in a 20-lead, wide-body SOIC package.

The ADM2582E/ADM2587E contains *iso*Power technology that uses high frequency switching elements to transfer power through its transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. Refer to Application Note AN-0971 for details on board layout considerations.

Rev. PrH

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REVISION HISTORY

02/09—Revision PrH: Initial Version

SPECIFICATIONS

All voltages are relative to their respective ground; 3.0 ≤ V_{CC} ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{CC} = 5 V unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
ADM2587E TxD/RxD Data Rate ≤ 500kbps	I_{CC}		90		mA	V_{CC} = 3.3V, 100Ω Load between Y and Z
ADM2587E TxD/RxD Data Rate ≤ 500kbps	I_{CC}		72		mA	V_{CC} = 5V, 100Ω Load between Y and Z
ADM2587E TxD/RxD Data Rate ≤ 500kbps	I_{CC}		125		mA	V_{CC} = 3.3V, 54Ω Load between Y and Z
ADM2587E TxD/RxD Data Rate ≤ 500kbps	I_{CC}		98		mA	V_{CC} = 5V, 54Ω Load between Y and Z
TxD/RxD Data Rate ≤ 500kbps	I_{CC}			120	mA	100Ω Load between Y and Z
TxD/RxD Data Rate = 16Mbps	I_{CC}			150	mA	100Ω Load between Y and Z
TxD/RxD Data Rate = 16 Mbps	I_{CC}			200	mA	54Ω Load between Y and Z
DRIVER						
Differential Outputs						
Differential Output Voltage, Loaded	$\|V_{OD2}\|$	2.0		5.0	V	R_L = 100 Ω (RS-422), see Figure 3
		1.5		5.0	V	R_L = 54 Ω (RS-485), see Figure 3
	$\|V_{OD3}\|$	1.5		5.0	V	−7 V ≤ V_{TEST1} ≤ 12 V, see Figure 4
Δ$\|V_{OD}\|$ for Complementary Output States	Δ$\|V_{OD}\|$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 3
Common-Mode Output Voltage	V_{OC}			3.0	V	R_L = 54 Ω or 100 Ω, see Figure 3
Δ$\|V_{OC}\|$ for Complementary Output States	Δ$\|V_{OC}\|$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 3
Short-Circuit Output Current	I_{OS}			250	mA	
Output Leakage Current (Y, Z)	Io			125	µA	DE = 0 V, $\overline{RE}$ = 0 V, V_{CC} = 0 V or 3.6 V, V_{IN} = 12 V
		-100			µA	DE = 0 V, $\overline{RE}$ = 0 V, V_{CC} = 0 V or 3.6 V, V_{IN} = -7 V
Logic Inputs DE, $\overline{RE}$, TxD						
Input Threshold Low	V_{ILTxD}	0.3 × V_{DD}			V	DE, $\overline{RE}$, TxD
Input Threshold High	V_{IHTRxD}			0.7 × V_{DD}	V	DE, $\overline{RE}$, TxD
Input Current	I_{TxD}	−10	0.01	10	µA	DE, $\overline{RE}$, TxD
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage	V_{TH}	−200	-125	-30	mV	-7 V < V_{CM} < 12 V
Input Voltage Hysteresis	V_{HYS}		15		mV	V_{OC} = 0 V
Input Current (A, B)	I_I			125	µA	DE = 0 V, V_{DD} = 0 V or 3.6 V, V_{IN} = 12 V
		-100			µA	DE = 0 V, V_{DD} = 0 V or 3.6 V, V_{IN} = -7 V
Line Input Resistance	R_{IN}	96			kΩ	-7 V < V_{CM} < 12 V
Logic Outputs						
Output Voltage Low	V_{OLRxD}		0.2	0.4	V	I_{OrxD} = 1.5 mA, V_A − V_B = −0.2 V
Output Voltage High	V_{OHRxD}	V_{DD1} − 0.3	V_{DD1} − 0.2		V	I_{OrxD} = −1.5 mA, V_A − V_B = 0.2 V
Short Circuit Current				100	mA	

SPECIFICATIONS (CONTINUED)

All voltages are relative to their respective ground; 3.0 ≤ V_{CC} ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{CC} = 5 V unless otherwise noted.

Table 1 (Continued).

COMMON-MODE TRANSIENT IMMUNITY[1]		**25**			**kV/µs**	**V_{CM} = 1 kV, transient magnitude = 800 V**

[1] CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common-mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS – ADM2582E

T_A = −40°C to +85°C

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DRIVER						
Maximum Data Rate		16			Mbps	
Propagation Delay	t_{PLH}, t_{PHL}			100	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 5 and Figure 9
Output Skew	t_{SKEW}			8	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 5 and Figure 9
Rise Time/Fall Time	t_R, t_F			15	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 5 and Figure 9
Enable Time				120	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 11
Disable Time				150	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 11
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL}			110	ns	C_L = 15 pF, see Figure 7 and Figure 10
Output Skew	t_{SKEW}			8	ns	C_L = 15 pF, see Figure 7 and Figure 10
Enable Time				15	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 8 and Figure 12
Disable Time				15	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 8 and Figure 12

TIMING SPECIFICATIONS – ADM2587E

T_A = −40°C to +85°C

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DRIVER						
Maximum Data Rate		500			kbps	
Propagation Delay	t_{PLH}, t_{PHL}	250		700	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 5 and Figure 9
Output Skew	t_{SKEW}			100	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 5 and Figure 9
Rise Time/Fall Time	t_R, t_F	200		1100	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 5 and Figure 9
Enable Time				2.5	µs	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 11
Disable Time				200	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 11
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL}			200	ns	C_L = 15 pF, see Figure 7 and Figure 10
Output Skew	t_{SKEW}			30	ns	C_L = 15 pF, see Figure 7 and Figure 10
Enable Time				15	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 8 and Figure 12
Disable Time				15	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 8 and Figure 12

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

Table 3.

Parameter	Rating
V_{CC}	−0.5 V to +7 V
Digital Input Voltage (DE, $\overline{RE}$, TxD)	−0.5 V to V_{DD} + 0.5 V
Digital Output Voltage	
RxD	−0.5 V to V_{DD} + 0.5 V
Driver Output/Receiver Input Voltage	−9 V to +14 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +150°C
Average Output Current per Pin	−35 mA to +35 mA
ESD (Human Body Model) on A, B, Y and Z pins	±15 kV
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Reference Standard
AC Voltage			
Bipolar Waveform	424	V peak	50-year minimum lifetime
Unipolar Waveform			
Basic Insulation	600	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Basic Insulation	600	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADM2582E/ADM2587E CHARACTERISTICS

PACKAGE CHARACTERISTICS

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-Output)[1]	C_{I-O}		3		pF	f = 1 MHz
Input Capacitance[2]	C_I		4		pF	
Input IC Junction-to-Case Thermal Resistance	θ_{JCI}		33		°C/W	Thermocouple located at center of package underside
Output IC Junction-to-Case Thermal Resistance	θ_{JCO}		28		°C/W	Thermocouple located at center of package underside

[1] Device considered a 2-terminal device: Pin 1 to Pin 8 shorted together and Pin 9 to Pin 16 shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

Table 6. Pending ADM2582E/ADM2587E Approvals(TARGETED)

Organization	Approval Type	Notes
UL	To be recognized under the Component Recognition Program of Underwriters Laboratories, Inc.	In accordance with UL 1577, each ADM2582E/ADM2587E is proof tested by applying an insulation test voltage ≥2500 V rms for 1 second.
VDE	To be certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12	In accordance with VDE 0884-10, each ADM2582E/ADM2587E is proof tested by applying an insulation test voltage ≥1050 V_{PEAK} for 1 second.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 7.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	5.15 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	5.5 min	mm	Measured from input terminals to output terminals, shortest distance along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303-1
Isolation Group		IIIa		Material Group (DIN VDE 0110: 1989-01, Table 1).

VDE 0884 INSULATION CHARACTERISTICS (TARGETED)

This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

An asterisk (*) on a package denotes VDE 0884 approval for 560 V peak working voltage.

Table 8.

Description	Conditions	Symbol	Characteristic	Unit
CLASSIFICATIONS				
Installation Classification per DIN VDE 0110 for Rated Mains Voltage				
≤150 V rms			I to IV	
≤300 V rms			I to III	
≤400 V rms			I to II	
Climatic Classification			40/85/21	
Pollution Degree	DIN VDE 0110, see Table 1		2	
VOLTAGE				
Maximum Working Insulation Voltage		V_{IORM}	560	V_{PEAK}
Input-to-Output Test Voltage		V_{PR}		
Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production tested, t_m = 1 sec, partial discharge < 5 pC		1050	V_{PEAK}
Method a				
After Environmental Tests, Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		896	V_{PEAK}
After Input and/or Safety Test, Subgroup 2/Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		672	V_{PEAK}
Highest Allowable Overvoltage	(Transient overvoltage, t_{TR} = 10 sec)	V_{TR}	4000	V_{PEAK}
SAFETY-LIMITING VALUES	Maximum value allowed in the event of a failure.			
Case Temperature		T_S	150	°C
Input Current		$I_{S, INPUT}$	265	mA
Output Current		$I_{S, OUTPUT}$	335	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

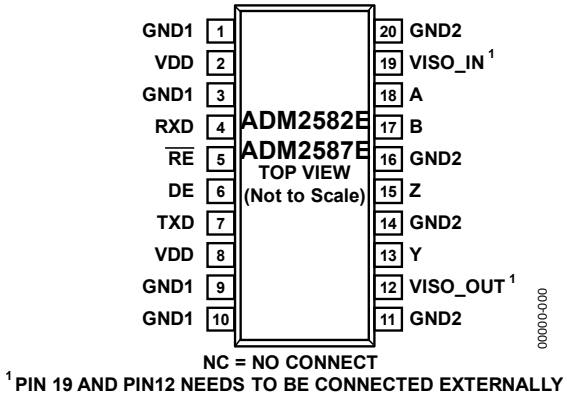


Figure 2. Pin Configuration

Table 9.

Pin	Mnemonic	Function
1	GND_1	Ground, Logic Side.
2	V_{DD}	Power Supply. Decoupling capacitor to GND_1 required; capacitor value should be between 0.01 µF and 0.1 µF.
3	GND_1	Ground, Logic Side.
4	RxD	Receiver Output Data. This output is high when (A – B) > 200 mV and low when (A – B) < –200 mV. The output is tristated when the receiver is disabled, that is, when $\overline{RE}$ is driven high.
5	$\overline{RE}$	Receiver Enable Input. This is an active-low input. Driving this input low enables the receiver; driving it high disables the receiver.
6	DE	Driver Enable Input. Driving this input high enables the driver; driving it low disables the driver.
7	TxD	Driver Input. Data to be transmitted by the driver is applied to this input.
8	V_{DD}	Power Supply. Decoupling capacitor to GND_1 required; capacitor value should be between 0.01 µF and 0.1 µF.
9	GND_1	Ground, Logic Side.
10	GND_1	Ground, Logic Side.
11	GND_2	Ground, Bus Side.
12	V_{ISOOUT}	Isolated Power Supply Output. This pin must be connected externally to V_{ISOIN}
13	Y	Driver Non-inverting output
14	GND_2	Ground (bus side).
15	Z	Driver Inverting output
16	GND_2	Ground (bus side).
17	B	Receiver Inverting Input.
18	A	Receiver Non-inverting Input.
19	V_{ISOIN}	Isolated Power Supply Input. This pin must be connected externally to V_{ISOOUT}
20	GND_2	Ground (bus side).

TEST CIRCUITS

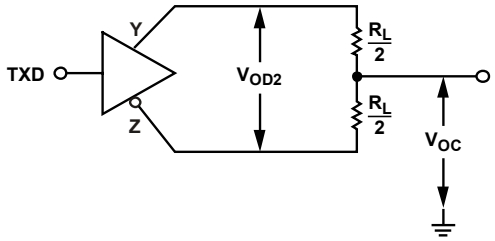


Figure 3. Driver Voltage Measurement

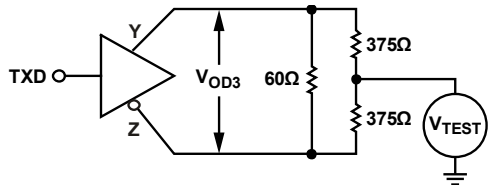


Figure 4. Driver Voltage Measurement

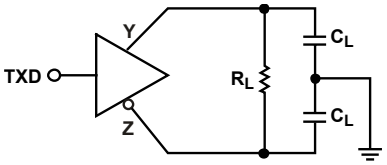


Figure 5. Driver Propagation Delay

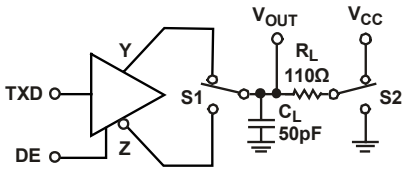


Figure 6. Driver Enable/Disable

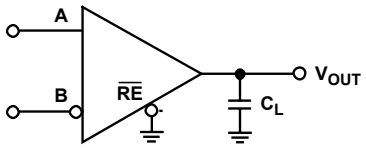


Figure 7. Receiver Propagation Delay

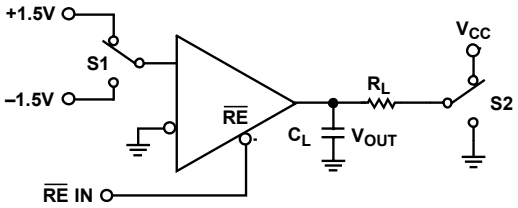


Figure 8. Receiver Enable/Disable

SWITCHING CHARACTERISTICS

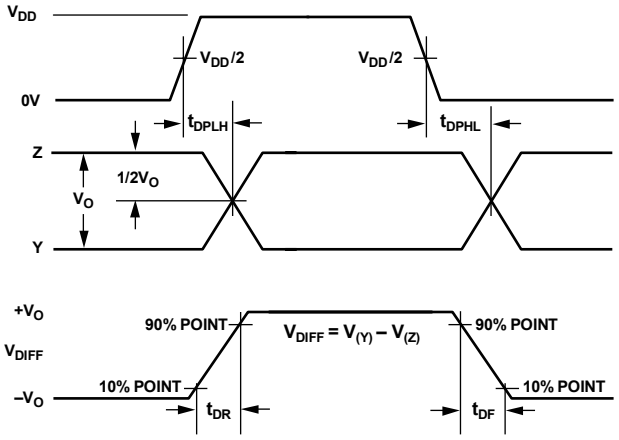


Figure 9. Driver Propagation Delay, Rise/Fall Timing

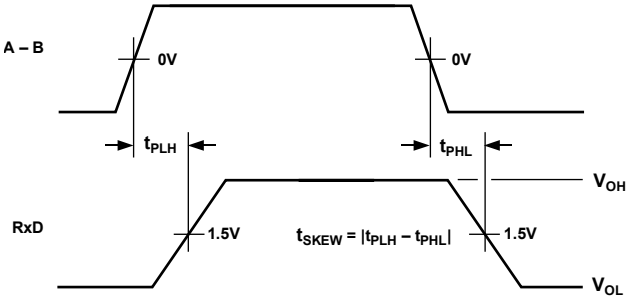


Figure 10. Receiver Propagation Delay

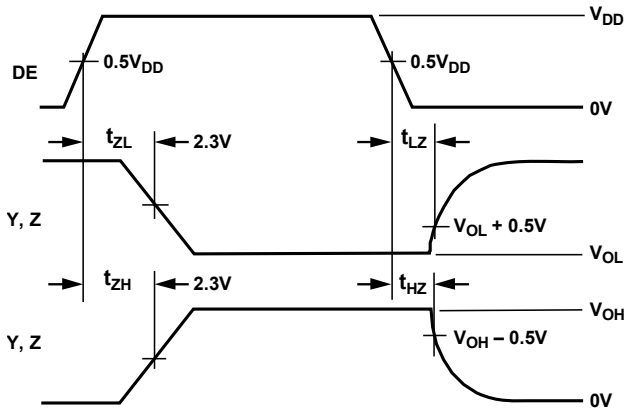


Figure 11. Driver Enable/Disable Timing

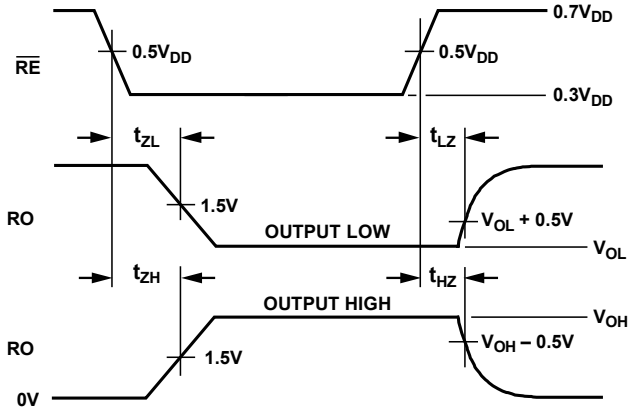


Figure 12. Receiver Enable/Disable Timing

CIRCUIT DESCRIPTION

SIGNAL ISOLATION

The ADM2582E/ADM2587E signal isolation is implemented on the logic side of the interface. The part achieves signal isolation by having a digital isolation section and a transceiver section. (see Figure 1). Driver input and data applied to the TXD and DE pins, respectively, and referenced to logic ground (GND_1) are coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground (GND_2). Similarly, the receiver output, referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RXD pin referenced to logic ground.

POWER ISOLATION

The ADM2582E/ADM2587E power isolation is implemented with using an *iso*Power™ integrated isolated DC/DC converter.

TRUTH TABLES

The truth tables in this section use the abbreviations found in Table 10.

Table 10. Truth Table Abbreviations

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Irrelevant
Z	High impedance (off)
NC	Disconnected

Table 11. Transmitting

Supply Status		Inputs		Outputs	
V_{DD1}	V_{DD2}	DE	TxD	Y	Z
On	On	H	H	H	L
On	On	H	L	L	H
On	On	L	X	Z	Z
On	Off	X	X	Z	Z
Off	On	L	X	Z	Z
Off	Off	X	X	Z	Z

Table 12. Receiving

Supply Status		Inputs		Outputs
V_{DD1}	V_{DD2}	A – B	$\overline{RE}$	RxD
On	On	>−0.05 V	L or NC	H
On	On	<−0.2 V	L or NC	L
On	On	−0.2 V < A – B < −0.05 V	L or NC	I
On	On	Inputs open	L or NC	H
On	On	X	H	Z
On	Off	X	L or NC	H
Off	Off	X	L or NC	L

THERMAL SHUTDOWN

The ADM2582E/ADM2587E contain thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

TRUE FAIL-SAFE RECEIVER INPUTS

The receiver inputs have a true fail-safe feature that ensures that the receiver output is high when the inputs are open or shorted. During line-idle conditions, when no driver on the bus is enabled, the voltage across a terminating resistance at the receiver input decays to 0 V. With traditional transceivers, receiver input thresholds specified between −200 mV and +200 mV mean that external bias resistors are required on the A and B pins to ensure that the receiver outputs are in a known state. The true fail-safe receiver input feature eliminates the need for bias resistors by specifying the receiver input threshold between −50 mV and −200 mV. The guaranteed negative threshold means that when the voltage between A and B decays to 0 V, the receiver output is guaranteed to be high.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

The digital signals transmit across the isolation barrier using *i*Coupler technology. This technique uses chip scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1 µs, periodic sets of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than approximately 5 µs, the input side is assumed to be unpowered or non-functional, in which case the isolator output is forced to a default state (see Table 3) by the watchdog timer circuit.

This situation should occur in the ADM2582E/ADM2587E devices only during power-up and power-down operations. The limitation on the ADM2582E/ADM2587E magnetic field

immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur.

The 3.3 V operating condition of the ADM2582E/ADM2587E is examined because it represents the most susceptible mode of operation. The pulses at the transformer output have an amplitude of >1.0 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$V = (-d\beta/dt)\Sigma\pi r_{n2}; n = 1, 2, \ldots, N$

where:

β is magnetic flux density (gauss).

N is the number of turns in the receiving coil.

r_n is the radius of the n_{th} turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADM2582E/ADM2587E, and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in **Error! Reference source not found.**.

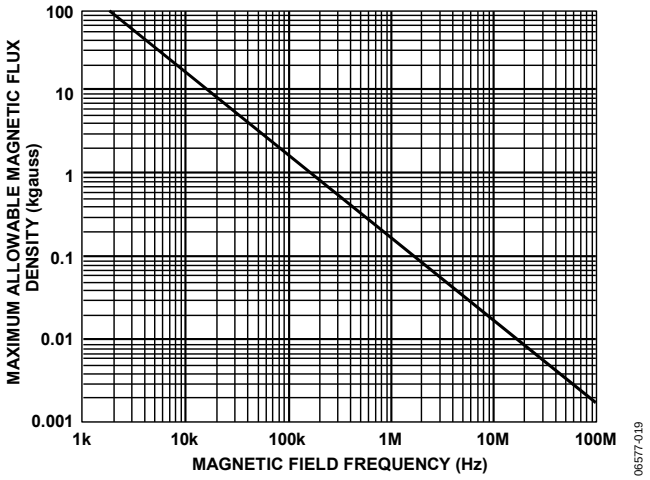


Figure 13. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADM2582E/ADM2587E transformers. Figure 26 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 26, the ADM2582E/ADM2587E are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example, a 0.5 kA current would need to be placed 5 mm away from the ADM2582E/ADM2587E to affect component operation.

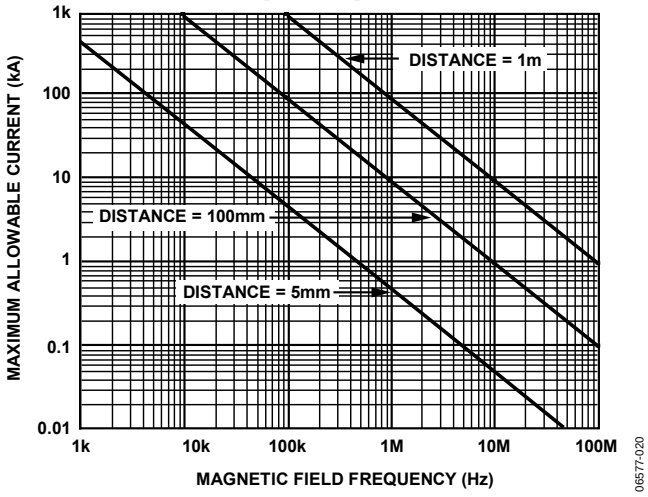


Figure 14. Maximum Allowable Current for Various Current-to-ADM2582E/ADM2587E Spacings

Note that in combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

EMI CONSIDERATIONS

The dc-to-dc converter section of the ADM2582E/ADM2587E components must, of necessity, operate at very high frequency to allow efficient power transfer through the small transformers. This creates high frequency currents that can propagate in circuit board ground and power planes, causing edge and dipole radiation. Grounded enclosures are recommended for applications that use these devices. If grounded enclosures are not possible, good RF design practices should be followed in layout of the PCB. See application Note AN-0971 for more information on the Control of Radiated Emissions with *iso*Power Devices.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADM2582E/ADM2587E.

Accelerated life testing is performed using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined, allowing calculation of the time to failure at the working voltage of interest. The values shown in Table 4 summarize the peak voltages for 50 years of service life in several operating conditions. In many cases, the working voltage approved by agency testing is higher than the 50-year service life voltage. Operation at working voltages higher than the service life voltage listed leads to premature insulation failure.

The insulation lifetime of the ADM2582E/ADM2587E depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 15, Figure 16, and Figure 17 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. A 50-year operating lifetime under the bipolar ac condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 4 can be applied while maintaining the 50-year minimum lifetime, provided the voltage conform to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 16 or Figure 17 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 4.

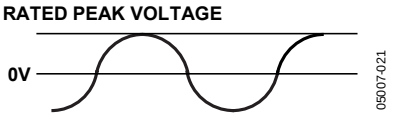


Figure 15. Bipolar AC Waveform

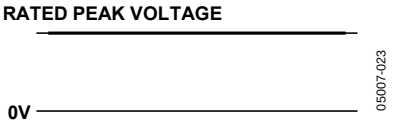
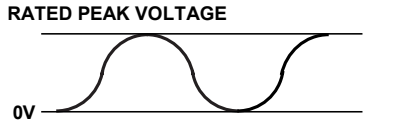


Figure 16. DC Waveform



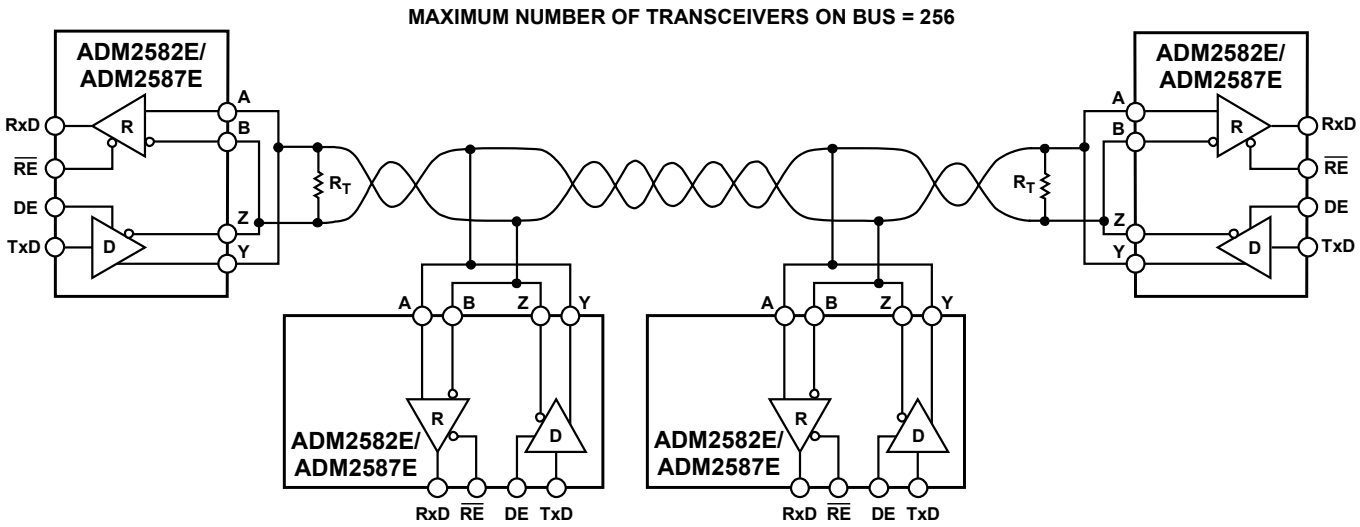
NOTES:
1. THE VOLTAGE IS SHOWN AS SINUSOIDAL FOR ILLUSTRATION PURPOSES ONLY. IT IS MEANT TO REPRESENT ANY VOLTAGE WAVEFORM VARYING BETWEEN 0 AND SOME LIMITING VALUE. THE LIMITING VALUE CAN BE POSITIVE OR NEGATIVE, BUT THE VOLTAGE CANNOT CROSS 0V.

05007-022

Figure 17. Unipolar AC Waveform

TYPICAL APPLICATIONS

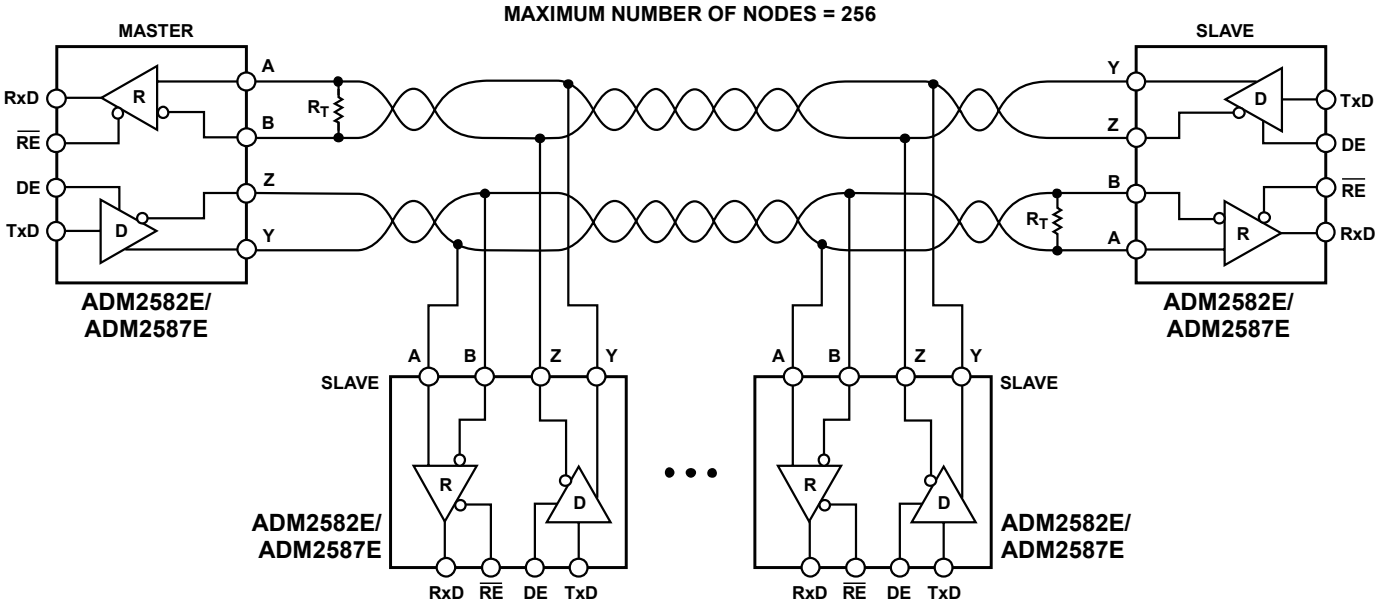
Figure 18 and Figure 19 show typical applications of the ADM2582E/ADM2587E in half-duplex and full-duplex RS-485 network configurations. Up to 256 transceivers can be connected to the RS-485 bus. To minimize reflections, the line must be terminated at the receiving end in its characteristic impedance, and stub lengths off the main line must be kept as short as possible. For half-duplex operation, this means that both ends of the line must be terminated, because either end can be the receiving end.



NOTES
1. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.
2. ISOLATION NOT SHOWN.

07379-027

Figure 18. ADM2582E/ADM2587E Typical Half-Duplex RS-485 Network

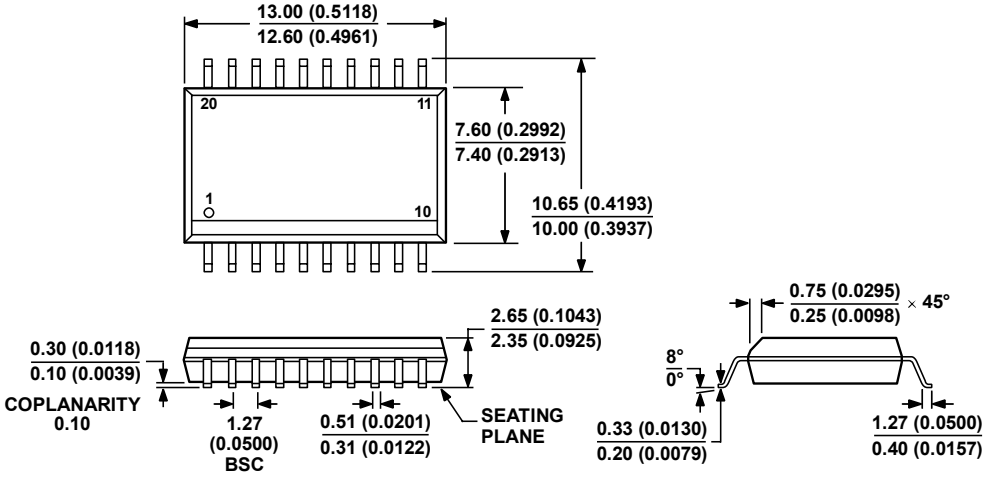


NOTES
1. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.
2. ISOLATION NOT SHOWN.

07379-028

Figure 19. ADM2582E/ADM2587E Typical Full-Duplex RS-485 Network

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060706-A

Figure 20. 20-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-20)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Data Rate (Mbps)	Temperature Range	Package Description	Package Option
ADM2582EBRWZ[1]	16	−40°C to +85°C	20-Lead SOIC_W	RW-20
ADM2582EBRWZ-REEL7[1]	16	−40°C to +85°C	20-Lead SOIC_W	RW-20
ADM2587EBRWZ[1]	0.5	−40°C to +85°C	20-Lead SOIC_W	RW-20
ADM2587EBRWZ-REEL7[1]	0.5	−40°C to +85°C	20-Lead SOIC_W	RW-20

[1] Z = RoHS Compliant part.