DATA SHEET

SAB9075H
Picture-in-Picture (PIP) controller for NTSC

Preliminary specification
File under Integrated Circuits, IC02

February 1995

Philips Semiconductors

PHILIPS

Picture-in-Picture (PIP) controller for NTSC SAB9075H

FEATURES

Display

- One or two live pictures can be displayed simultaneously
- Wide range of multi-Picture-In-Picture (PIP) modes available
- Six 6-bit Analog-to-Digital Converters (ADC) with clamping circuit
- Enhanced vertical resolution at most modes for live pictures
- Two Phase-Locked-Loops (PLL) with Voltage Controlled Oscillator (VCO) to generate the line-locked clocks
- Three 7-bit Digital-to-Analog Converters (DAC)
- 4 : 1 : 1 data format
- Data reduction factors 1 to 4, 1 to 9 and 1 to 16.

I^2C-bus programmable

- Different single, double and multi-PIP modes can be set
- Several aspect ratios can be handled
- Reduction factors can be set automatically and manually
- Selection of vertical filtering type
- Freeze of live pictures
- Single-PIP display position, four corners on-screen
- Multi-PIP display position, left or right on-screen
- Fine tuned display position, H (6-bit), V (6-bit)
- Fine tuned acquisition area, H (4-bit), V (4-bit)
- Channel-border and live PIP selectable
- Eight main-border, sub-border, channel-border and background colours selectable
- Border and background brightness adjustable, 30%, 50%, 70% and 100% IRE
- Several types of decoder input signals can be set
- 6-bit HUE and SAT signals (0 to 5 V) adjustable by I^2C-bus
- Main and sub-audio mute controllable by I^2C-bus.

GENERAL DESCRIPTION

The SAB9075H is a picture-in-picture controller for the NTSC environment in combination with the Integrated NTSC decoder and sync processor TDA8315.

The device inserts one or two live video channels with reduced sizes into a live video signal. All video signals are expected to be analog baseband signals. The conversion into the digital environment and back to the analog environment is carried out on-chip. Internal clocks are generated by two PLLs.

Due to the two PIP channels and a large external memory, a wide range of PIP modes are offered. The emphasis is put on double-PIP and multi-PIP modes. In combination with the different border colours and some external software the IC concept can be used as an excellent channel selection tool.

Some of the I^2C-bus registers are for controlling the saturation and HUE of the colours. There are also outputs for the mute function of main and sub-channel.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAB9075H	QFP100[1]	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	all positive supply pins	4.5	5.0	5.5	V
I_{tot}	total supply current	note 1	tbf	220	tbf	mA
f_{sys}	system frequency	note 2	–	27	30	MHz
f_{loop}	loop bandwidth frequency		4	–	–	kHz
t_{jitter}	short term stability time	jitter during 1 line (64 μs)	–	–	4	ns
ς	damping factor		–	0.7	–	–

Notes

1. Digital clocks are silent and analog bias current is zero.
2. The internal system frequencies are 1728 times the input frequency. For more detailed information about the clock generation see Section "PLLs and clock generation".

BLOCK DIAGRAM

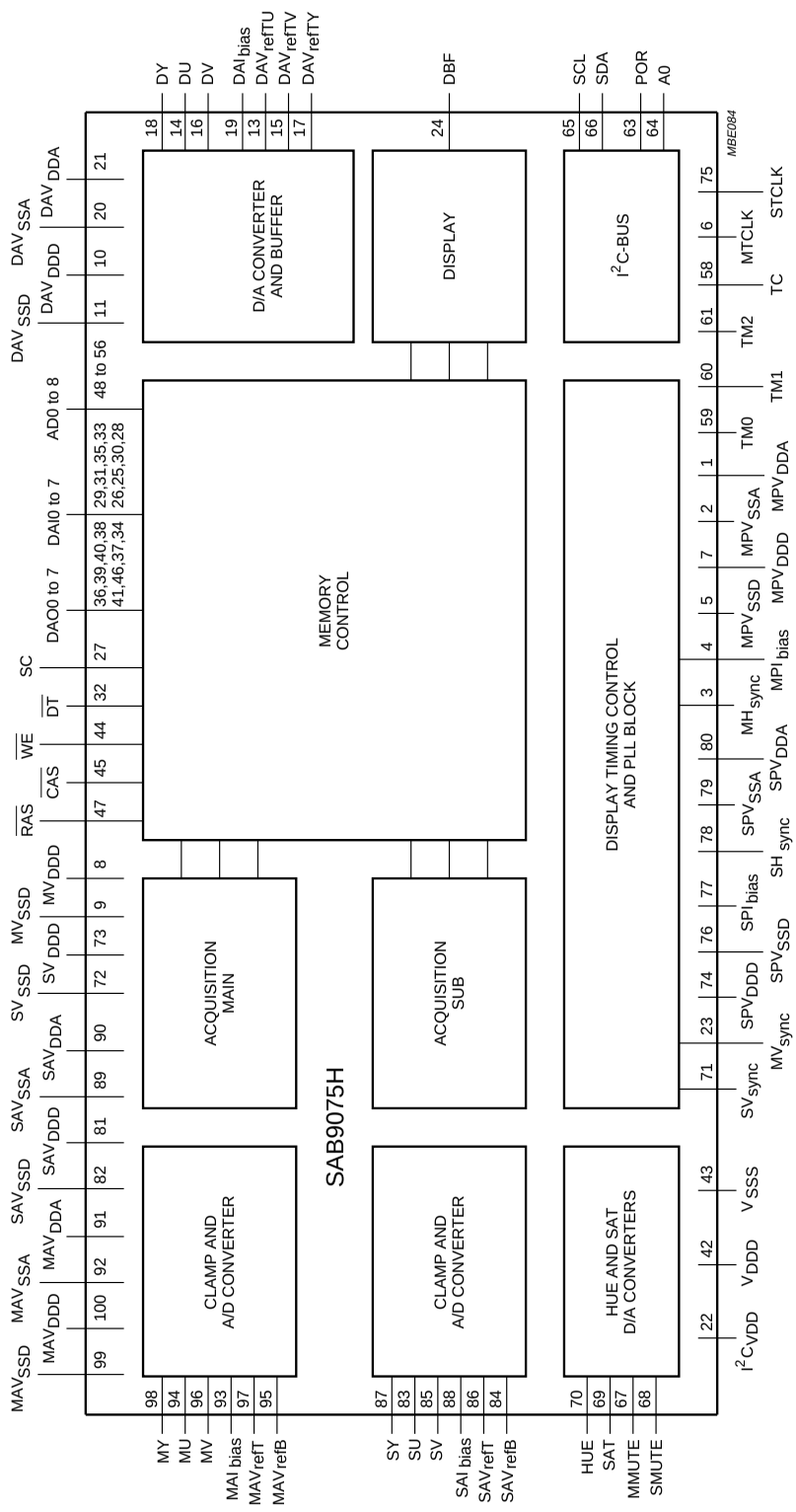


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
MPV_{DDA}	1	I/O	E030	analog positive power supply for PLL main-channel
MPV_{SSA}	2	I/O	E009	analog negative power supply for PLL main-channel
MH_{sync}	3	I	E027	horizontal synchronization for main-channel
MPI_{bias}	4	I	E027	analog bias reference current for PLL main-channel
MPV_{SSD}	5	I/O	E009	digital negative power supply for PLL main-channel
MTCLK	6	I	HPP01	test clock for main-channel
MPV_{DDD}	7	I/O	E030	digital positive power supply for PLL main-channel
MV_{DDD}	8	I/O	E030	digital positive power supply for main-channel core
MV_{SSD}	9	I/O	E009	digital negative power supply for main-channel core
DAV_{DDD}	10	I/O	E030	digital positive power supply for DACs
DAV_{SSD}	11	I/O	E009	digital negative power supply for DACs
n.c.	12	–	–	not connected
DAV_{refTU}	13	I/O	E027	analog reference voltage for top U DAC
DU	14	O	E027	analog U output
DAV_{refTV}	15	I/O	E027	analog reference voltage for top V DAC
DV	16	O	E027	analog V output
DAV_{refTY}	17	I/O	E027	analog reference voltage for top Y DAC
DY	18	O	E027	analog Y output
DAI_{bias}	19	I	E027	analog bias reference current for DACs
DAV_{SSA}	20	I/O	E009	analog negative power supply for DACs
DAV_{DDA}	21	I/O	E030	analog positive power supply for DACs
I^2CV_{DD}	22	I/O	E030	positive supply for HUE and SAT decoders
MV_{sync}	23	I	HPP01	vertical synchronization for main-channel
DBF	24	O	SPF20	fast blanking control output signal
DAI5	25	I	HPP01	data bus input from memory; bit 5
DAI4	26	I	HPP01	data bus input from memory; bit 4
SC	27	O	OPF20	memory shift clock
DAI7	28	I	HPP01	data bus input from memory; bit 7
DAI0	29	I	HPP01	data bus input from memory; bit 0
DAI6	30	I	HPP01	data bus input from memory; bit 6
DAI1	31	I	HPP01	data bus input from memory; bit 1
$\overline{DT}$	32	O	OPF20	memory data transfer; active LOW
DAI3	33	I	HPP01	data bus input from memory; bit 3
DAO7	34	O	OPF20	data bus output to memory; bit 7
DAI2	35	I	HPP01	data bus input from memory; bit 2
DAO0	36	O	OPF20	data bus output to memory; bit 0
DAO6	37	O	OPF20	data bus output to memory; bit 6
DAO3	38	O	OPF20	data bus output to memory; bit 3
DAO1	39	O	OPF20	data bus output to memory; bit 1
DAO2	40	O	OPF20	data bus output to memory; bit 2

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
DAO4	41	O	OPF20	data bus output to memory; bit 4
V_{DDD}	42	I/O	E030	digital positive power supply for peripherals
V_{SSS}	43	I/O	E009	digital negative power supply for peripherals
$\overline{WE}$	44	O	OPF20	memory write enable; active LOW
$\overline{CAS}$	45	O	OPF20	memory column address strobe; active LOW
DAO5	46	O	OPF20	data bus output to memory; bit 5
$\overline{RAS}$	47	O	OPF20	memory row address strobe; active LOW
AD0	48	O	OPF20	memory address bus; bit 0
AD8	49	O	OPF20	memory address bus; bit 8
AD1	50	O	OPF20	memory address bus; bit 1
AD6	51	O	OPF20	memory address bus; bit 6
AD2	52	O	OPF20	memory address bus; bit 2
AD5	53	O	OPF20	memory address bus; bit 5
AD3	54	O	OPF20	memory address bus; bit 3
AD4	55	O	OPF20	memory address bus; bit 4
AD7	56	O	OPF20	memory address bus; bit 7
n.c.	57	–	–	not connected
TC	58	I	HPP01	test control
TM0	59	I	HPP01	test mode 0
TM1	60	I	HPP01	test mode 1
TM2	61	I	HPP01	test mode 2
n.c.	62	–	–	not connected
POR	63	I	HUP07	power-on reset
A0	64	I	HPF01	I^2C-bus address 0 selection pin
SCL	65	I	HPF01	shift clock for I^2C-bus
SDA	66	I/O	IOI41	shift I^2C-bus input data; acknowledge I^2C-bus output data
MMUTE	67	O	SPF20	mute output for main-channel
SMUTE	68	O	SPF20	mute output for sub-channel
SAT	69	O	E027	analog output for SAT decoder
HUE	70	O	E027	analog output for HUE decoder
SV_{sync}	71	I	HPP01	vertical synchronization for sub-channel
SV_{SSD}	72	I/O	E009	digital negative power supply for sub-channel core
SV_{DDD}	73	I/O	E030	digital positive power supply for sub-channel core
SPV_{DDD}	74	I/O	E030	digital positive power supply for PLL sub-channel
STCLK	75	I	HPP01	test clock for sub-channel
SPV_{SSD}	76	I/O	E009	digital negative power supply for PLL sub-channel
SPI_{bias}	77	I	E027	analog bias reference current for PLL sub-channel
SH_{sync}	78	I	E027	horizontal synchronization for sub-channel
SPV_{SSA}	79	I/O	E009	analog negative power supply for PLL sub-channel
SPV_{DDA}	80	I/O	E030	analog positive power supply for PLL sub-channel
SAV_{DDD}	81	I/O	E030	digital positive power supply for ADC sub-channel

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
SAV_{SSD}	82	I/O	E009	digital negative power supply for ADC sub-channel
SU	83	I	E027	analog U input for sub-channel
SAV_{refB}	84	I/O	E027	analog reference voltage for bottom ADC sub-channel
SV	85	I	E027	analog V input for sub-channel
SAV_{refT}	86	I/O	E027	analog reference voltage for top ADC sub-channel
SY	87	I	E027	analog Y input for sub-channel
SAI_{bias}	88	I	E027	analog bias reference current for ADC sub-channel
SAV_{SSA}	89	I/O	E009	analog negative power supply for ADC sub-channel
SAV_{DDA}	90	I/O	E030	analog positive power supply for ADC sub-channel
MAV_{DDA}	91	I/O	E030	analog positive power supply for ADC main-channel
MAV_{SSA}	92	I/O	E009	analog negative power supply for ADC main-channel
MAI_{bias}	93	I	E027	analog bias reference current for ADC main-channel
MU	94	I	E027	analog U input for main-channel
MAV_{refB}	95	I/O	E027	analog reference voltage for bottom ADC main-channel
MV	96	I	E027	analog V input for main-channel
MAV_{refT}	97	I/O	E027	analog reference voltage for top ADC main-channel
MY	98	I	E027	analog Y input for main-channel
MAV_{SSD}	99	I/O	E009	digital negative power supply for ADC main-channel
MAV_{DDD}	100	I/O	E030	digital positive power supply for ADC main-channel

Table 1 Pin type explanation

PIN TYPE	DESCRIPTION
E030	V_{DD} pin; diode to V_{SS}
E009	V_{SS} pin; diode to V_{DD}
E027	analog input pin; diode to V_{DD} and V_{SS}
HPF01	digital input pin; CMOS levels, diode to V_{SS}
HPP01	digital input pin; CMOS levels, diode to V_{DD} and V_{SS}
HUP07	digital input pin; CMOS levels with hysteresis, pull up resistor to V_{DD}, diode to V_{DD} and V_{SS}
IOI41	I^2C-bus pull-down output stage; CMOS input levels
OPF20	digital output pin
SPF20	digital output pin; slew rate controlled

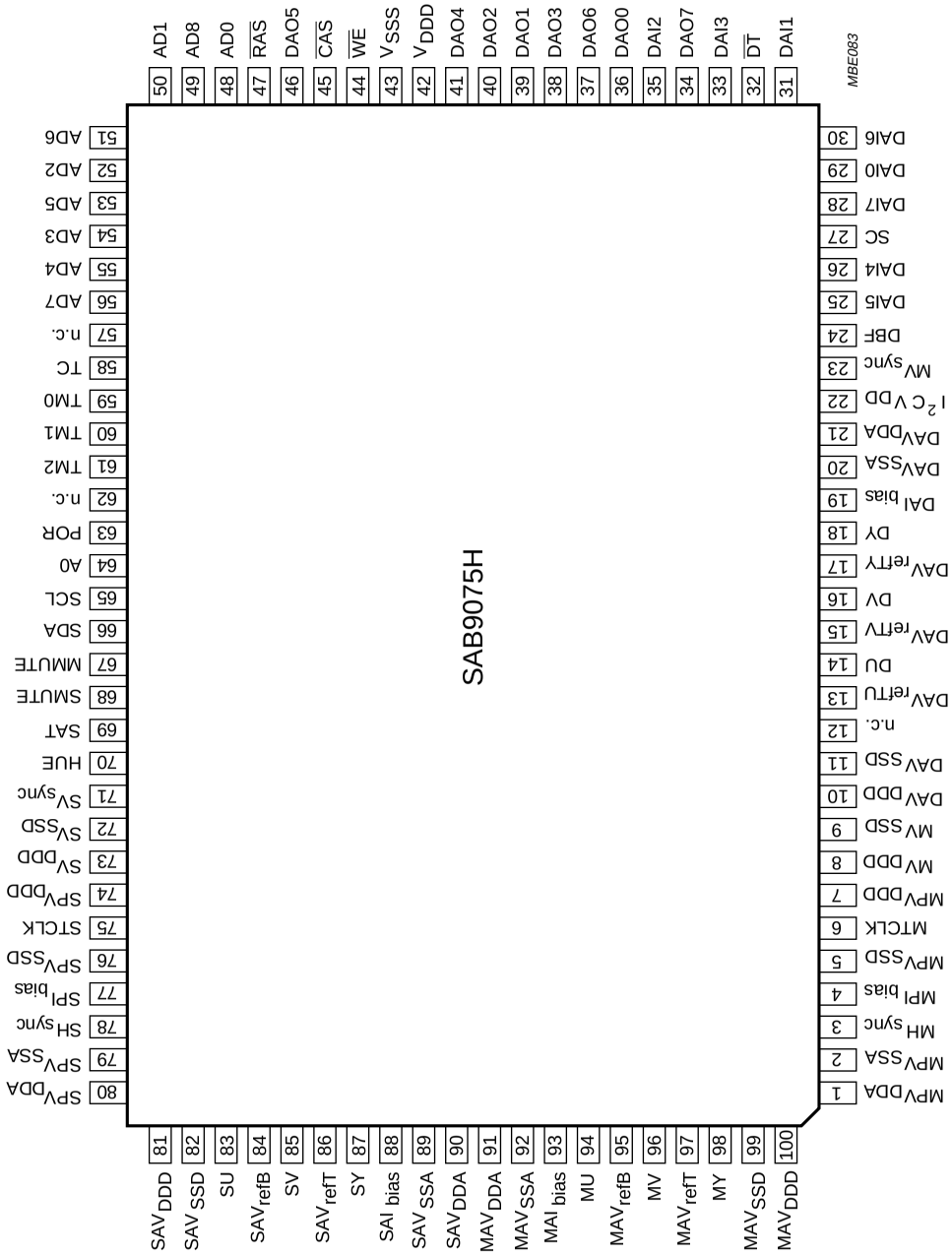


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Acquisition area

The acquisition area is in the centre of the visible screen area. Vertically 228 lines are sampled. Horizontally 672 Y-pixels are processed. The exact active processing area can be fine tuned in horizontal (2 pixels/steps, 16 steps) and vertical (1 line/step, 16 steps) direction for both main and sub-channel by the I²C-bus (see Fig.3). The given numbers are pixel numbers at a 13.5 MHz data rate. The signals, which are dependent on the I²C-bus registers, can also be related to the H_{sync}, in which event they are delayed by 68 pixels.

Chrominance format

The chrominance format is 4 : 1 : 1.

The YUV signals are sampled at a rate of 27 MHz and then filtered and subsampled to a data rate of 13.5 MHz.

It is expected that the input signals do not contain frequencies outside the video bandwidth (Y_{BW} = 4.5 MHz; U_{BW} and V_{BW} = 1.125 MHz).

Display area

The display area is shown in Fig.4. The given numbers are pixels at a data rate of 13.5 MHz. The signals are related to the burstkey and the V_{sync}. Dependent on the I²C-bus registers the signals can also be related to the H_{sync}.

The internal 13.5 MHz data rate is upsampled to the double frequency (27 MHz) and then fed to the DACs.

The display output can be fine positioned by the I²C-bus in 64 steps of 4 pixels in horizontal direction and 64 steps of 1 line/field in vertical direction.

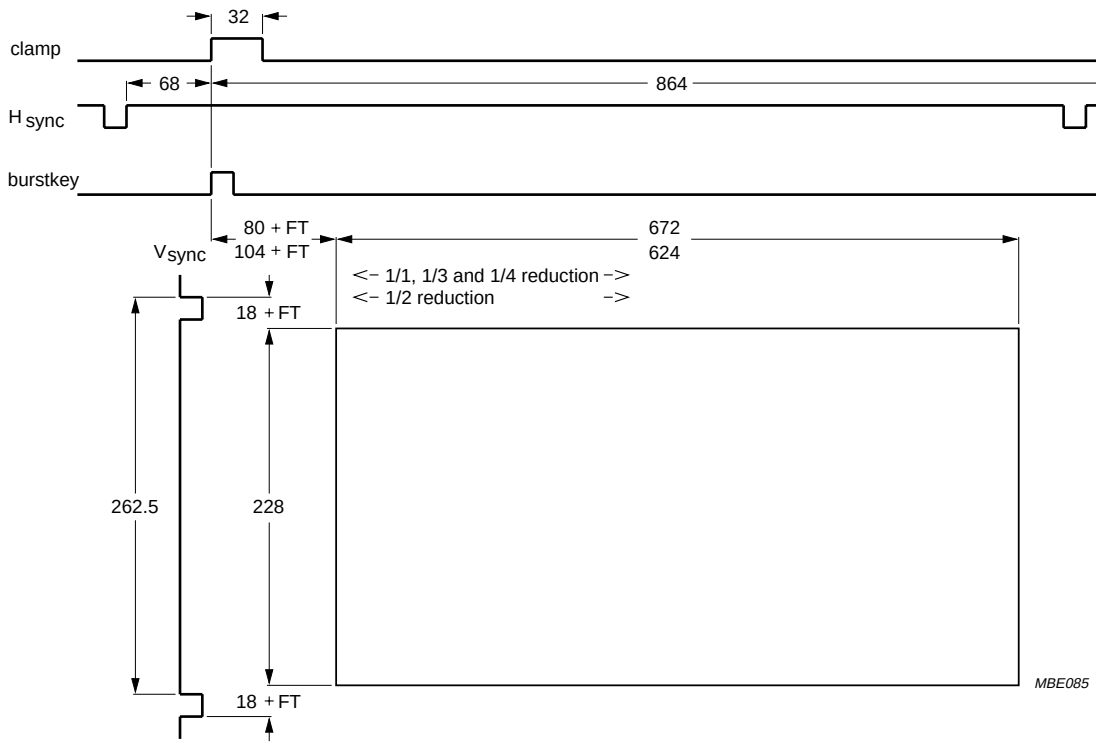


Fig.3 Acquisition area.

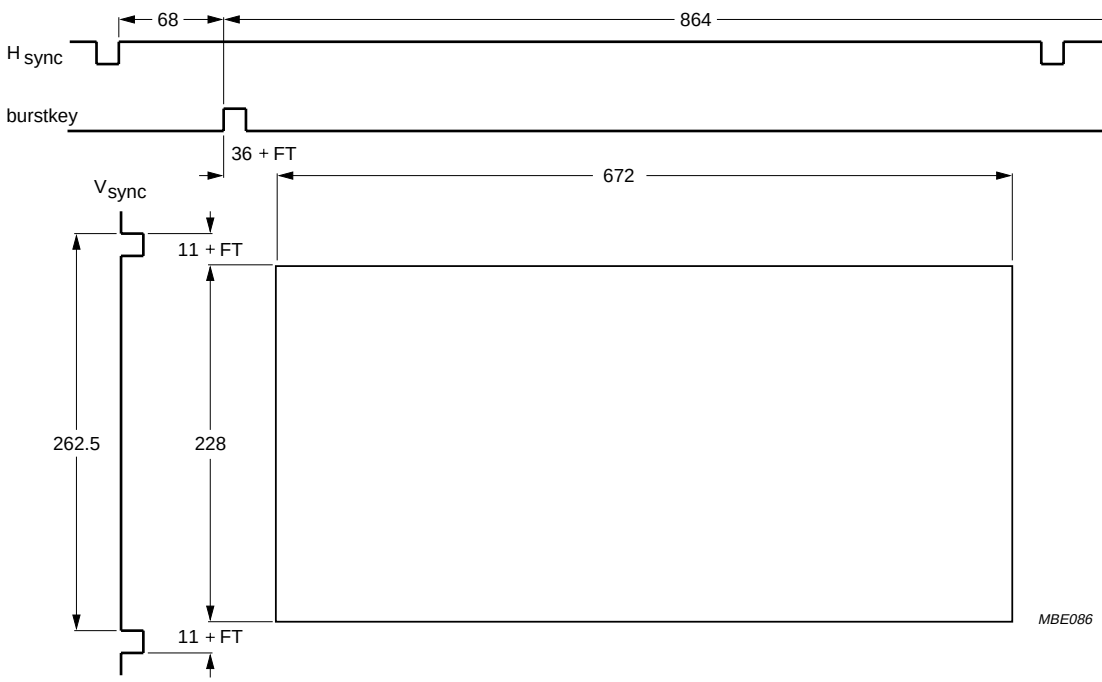


Fig.4 Display area.

PIP modes

The controller contains two independent acquisition-channels which provide the scaling factors to support the range of different modes. With the external memory of 2 Mbit it is possible to select between single, double and multi-PIP modes.

Table 2 gives an overview of the different PIP modes.

Table 2 PIP modes

MODE		SUB	MAIN	SUB SIZE(1)		MAIN SIZE(1)	
				PIXELS	REDUCTION(2)	PIXELS	REDUCTION(2)
4 : 3 main + 4 : 3 sub to 4 : 3 screen or 16 : 9 main + 16 : 9 sub to 16 : 9 screen							
1.1	SPS	$1/16$	–	160P, 53L	$1/4$H, $1/4$V	–	–
1.2	SPL	$1/9$	–	216P, 72L	$1/3$H, $1/3$V	–	–
1.3	DP	$1/4$	$1/4$	304P, 108L	$1/2$H, $1/2$V	304P, 108L	$1/2$H, $1/2$V
1.4	MP3	$3 \times 1/16$	–	160P, 53L	$1/4$H, $1/4$V	–	–
1.5	MP4	$3 \times 1/16$	$1/4$	160P, 53L	$1/4$H, $1/4$V	304P, 108L	$1/2$H, $1/2$V
1.6	MP7	$7 \times 1/16$	–	160P, 53L	$1/4$H, $1/4$V	–	–
1.7	MP8	$7 \times 1/16$	$1/4$	160P, 53L	$1/4$H, $1/4$V	304P, 108L	$1/2$H, $1/2$V
1.8	MP9	$8 \times 1/9$	$1/9$	216P, 72L	$1/3$H, $1/3$V	216P, 72L	$1/3$H, $1/3$V
16 : 9 sub + 4 : 3 main to 4 : 3 screen							
2.1	SPS	$1/16$	–	216P, 53L	$1/3$H, $1/4$V	–	–
2.2	SPL	$1/9$	–	304P, 72L	$1/2$H, $1/3$V	–	–
4 : 3 sub + 16 : 9 main to 16 : 9 screen							
3.1	SPS	$1/16$	–	160P, 72L	$1/4$H, $1/3$V		
3.2	DP	$1/4$	$1/4$	216P, 108L	$1/3$H, $1/2$V	304P, 108L	$1/2$H, $1/2$V

Notes

1. The given sub/main sizes are visible PIP sizes, a border is drawn around these PIPs and does not influence these sizes. The size of the border is 4 pixels wide and 2 lines/fields high.
2. The SAB9075H can be set in automatic mode in which the reduction factors are automatically set by the mode select and aspect ratio select bits of the I^2C-bus. If the automatic mode is switched OFF the reduction factors can be set manually. This will give more flexibility to adjust the aspect ratios of incoming signals.

PIP positions

The positions are graphically depicted in Figs 5 to 17.

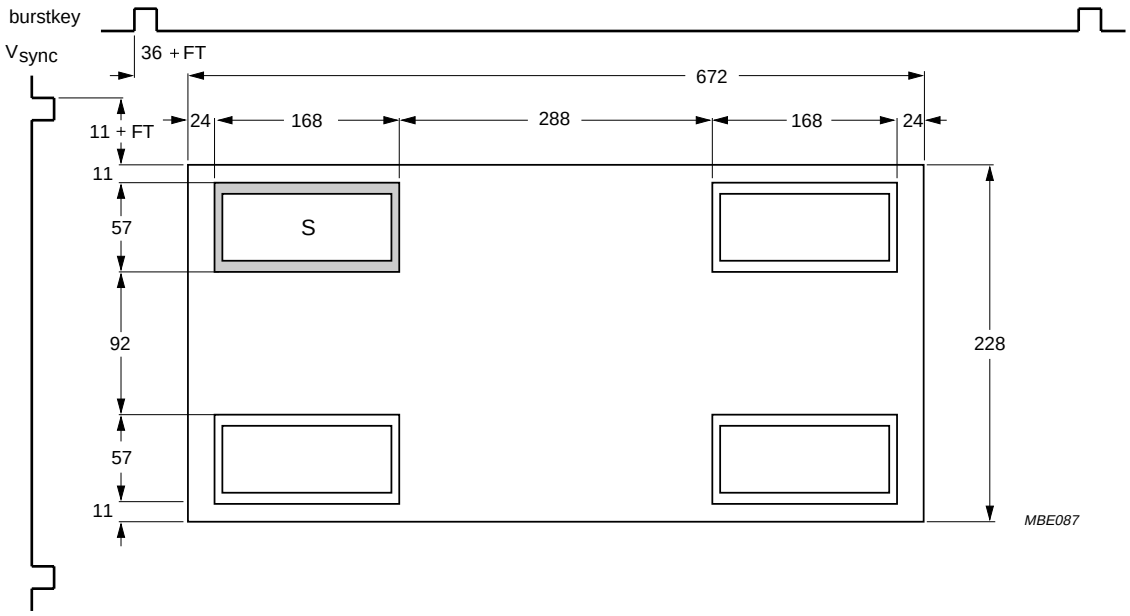


Fig.5 Single-PIP, size $\frac{1}{16}$ (mode SPS).

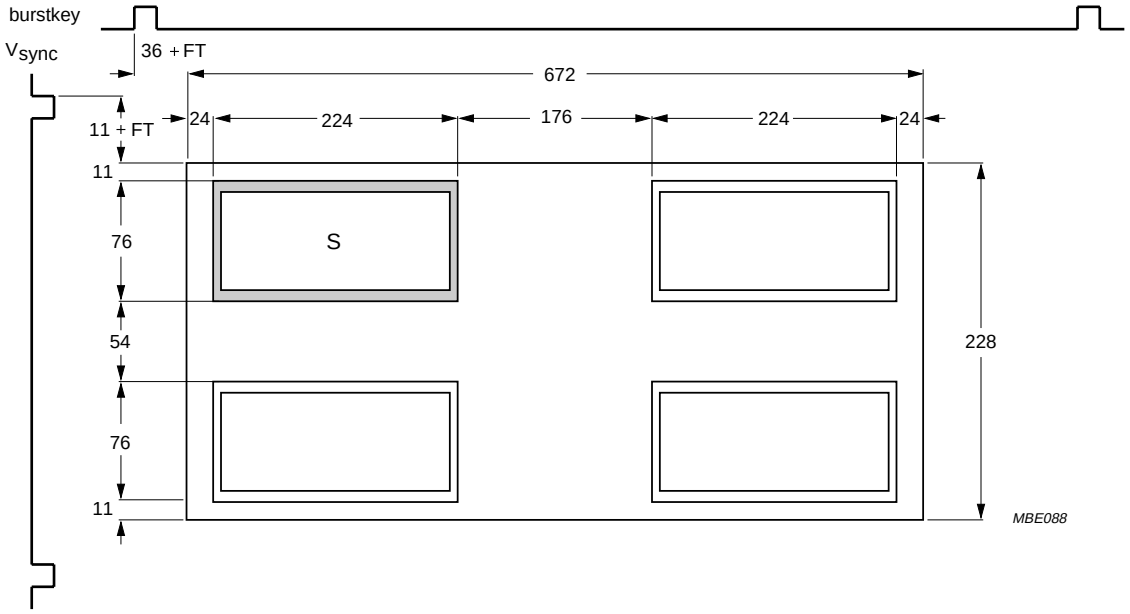


Fig.6 Single-PIP, size $\frac{1}{9}$ (mode SPL).

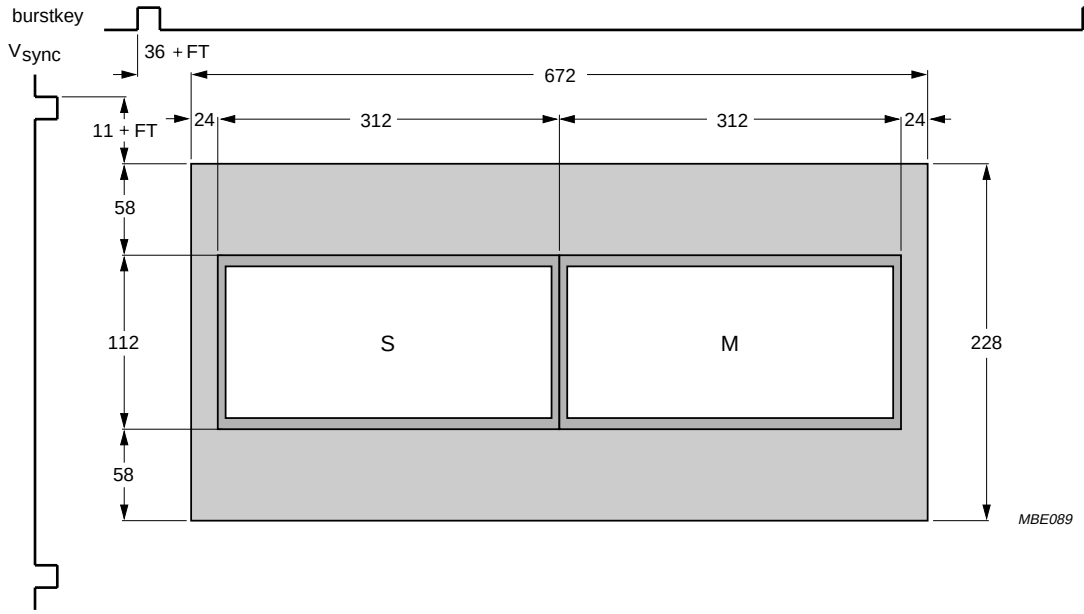


Fig.7 Double-PIP, size $^{1}/_{16}$ (mode DP).

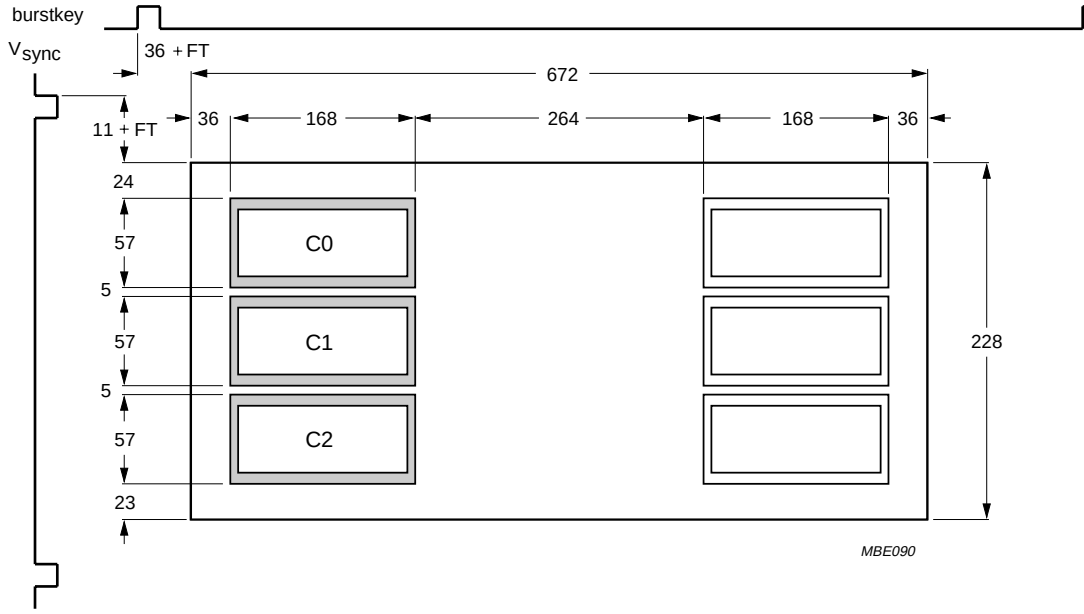


Fig.8 Multi PIP, 3 × sub $^{1}/_{16}$ (mode MP3).

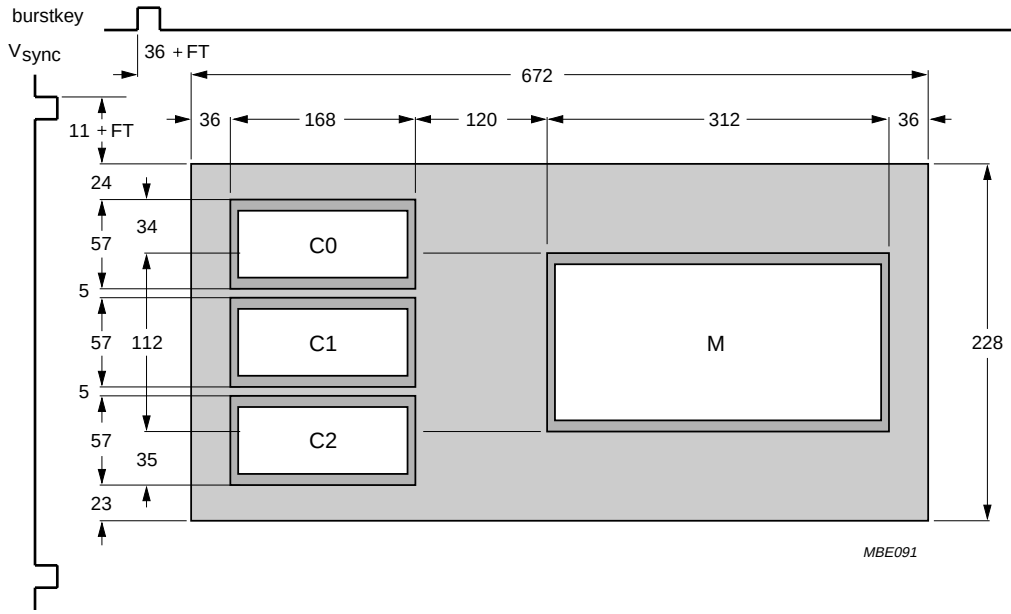


Fig.9 Multi-PIP, 3 × sub 1/16, 1 × main 1/4 (mode MP4).

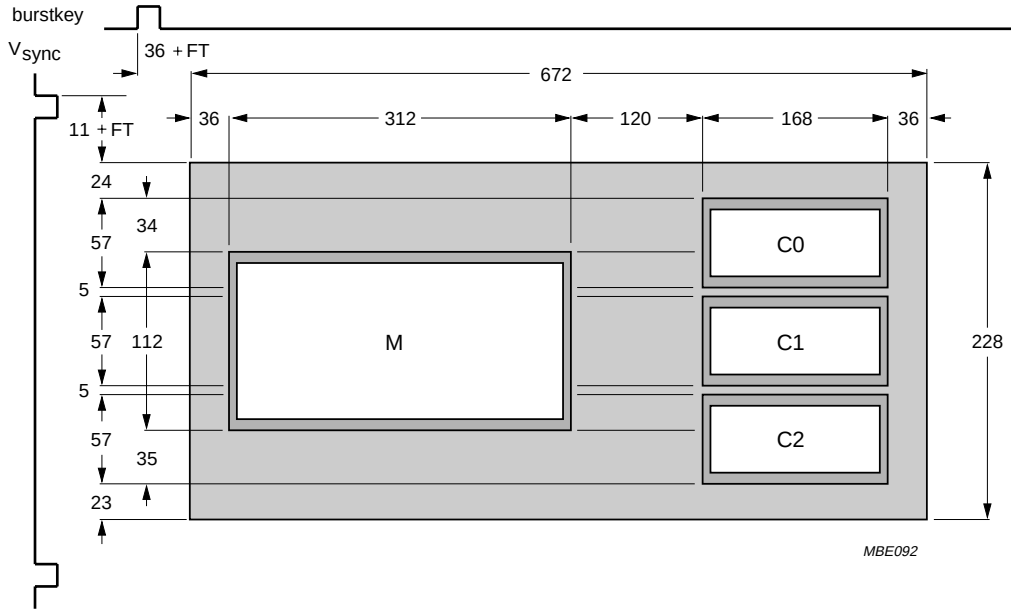


Fig.10 Multi-PIP, 3 × sub 1/16, 1 × main 1/4 (mode MP4, Right).

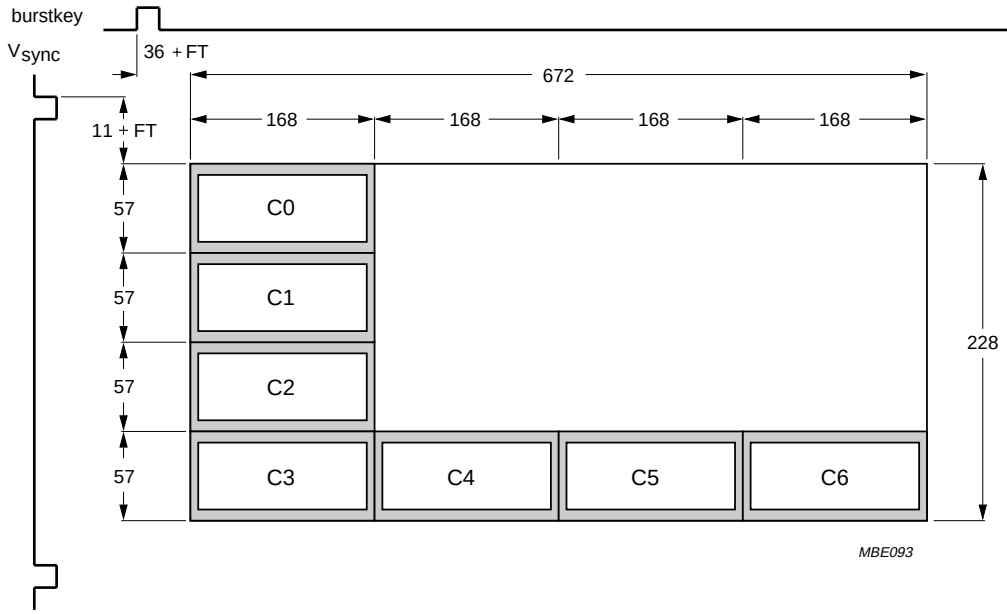


Fig.11 Multi-PIP, 7 × sub $^{1}/_{16}$, main life (mode MP7).

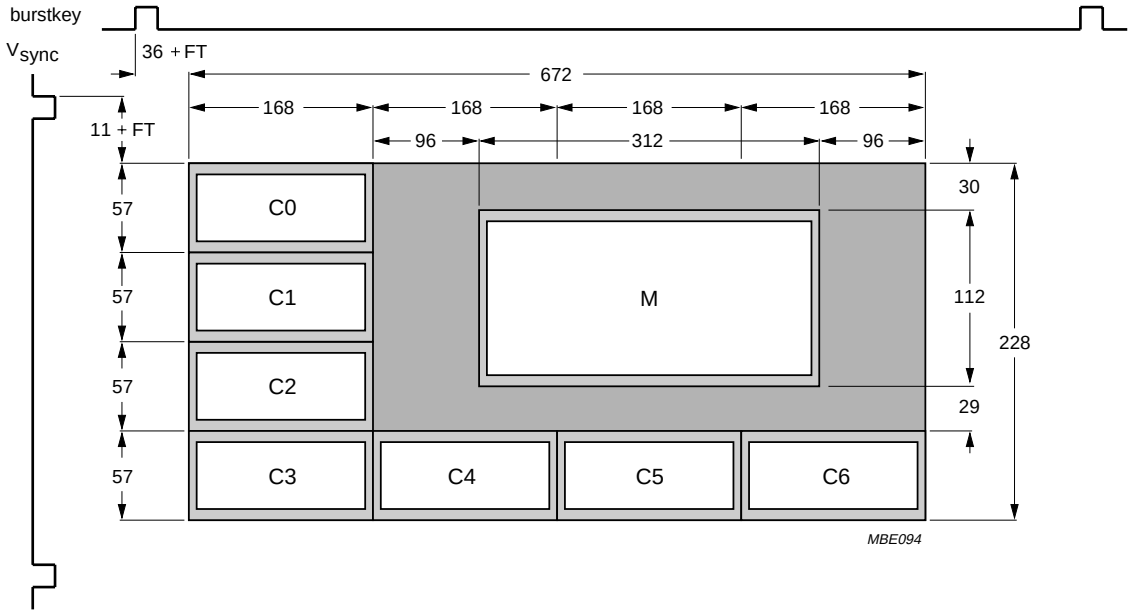


Fig.12 Multi-PIP, 7 × sub $^{1}/_{16}$, 1 × main $^{1}/_{4}$ (mode MP8).

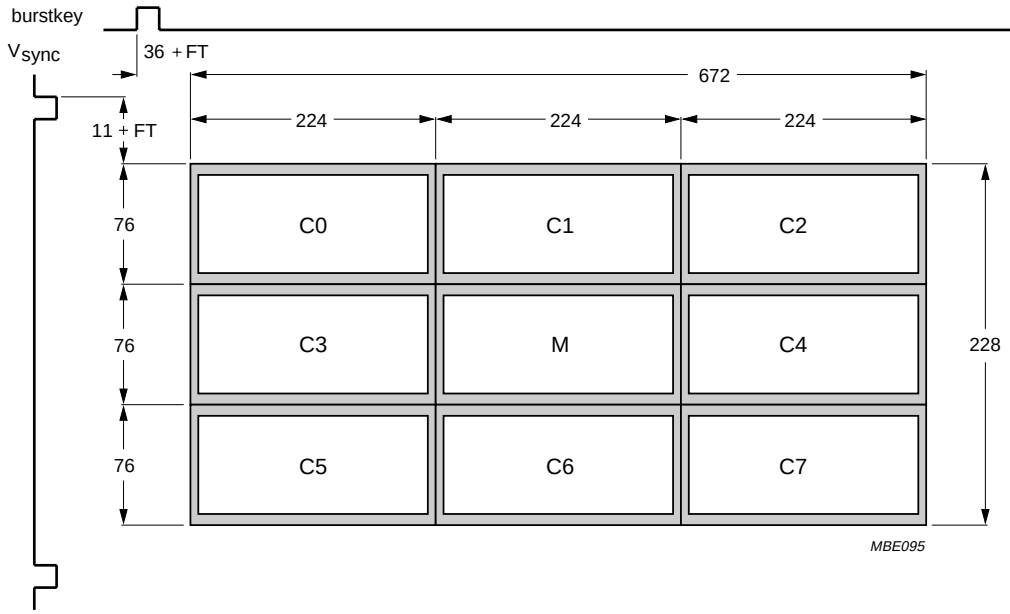


Fig.13 Multi-PIP, 8 × sub 1/9, 1 × main 1/9 (mode MP9).

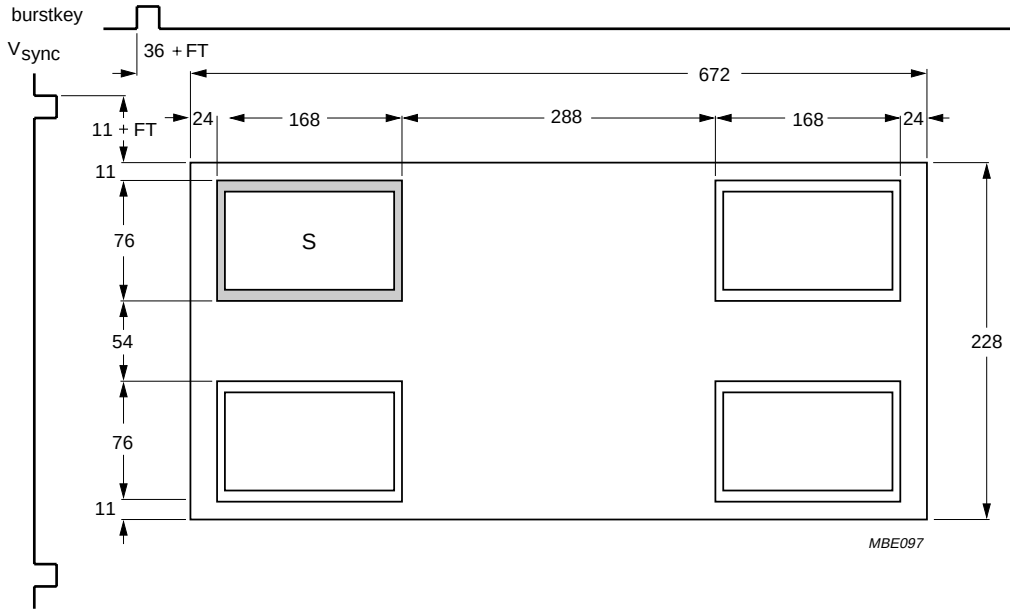


Fig.14 Single-PIP, 4 : 3 sub to 16 : 9 screen (mode SPS).

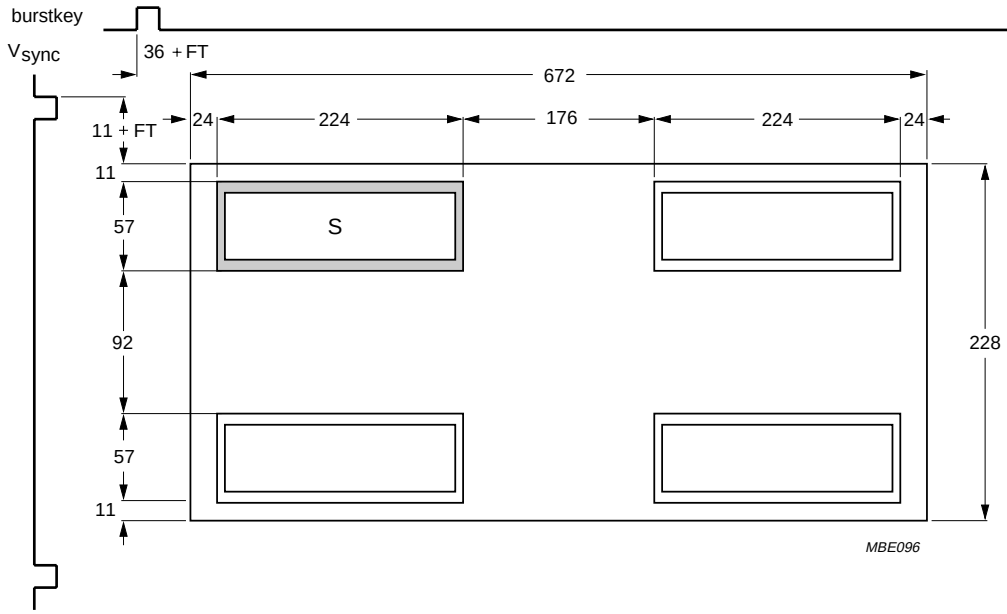


Fig.15 Single-PIP, 16 : 9 sub to 4 : 3 screen (mode SPS).

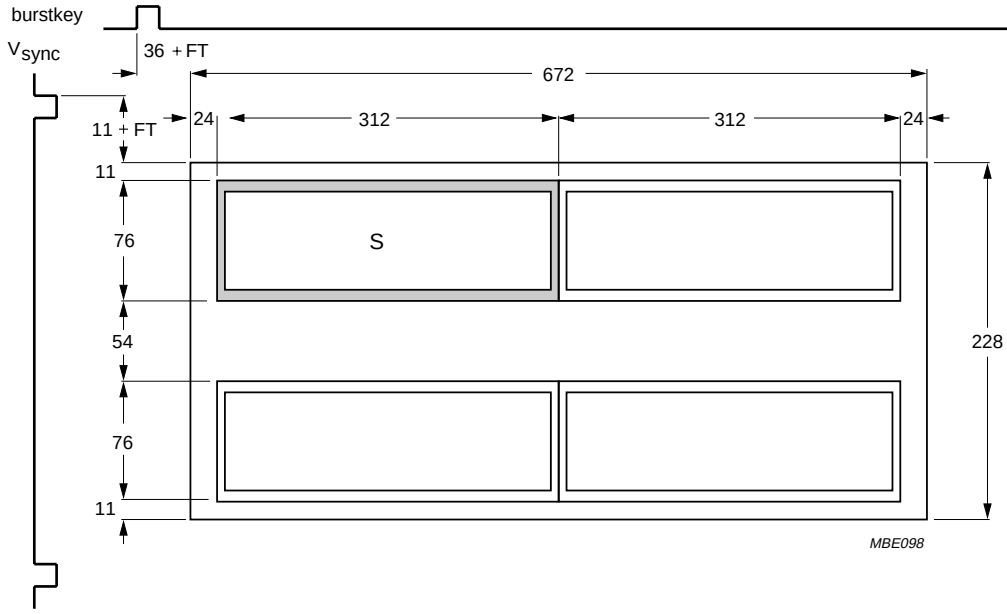


Fig.16 Single-PIP, 16 : 9 sub to 4 : 3 screen (mode SPL).

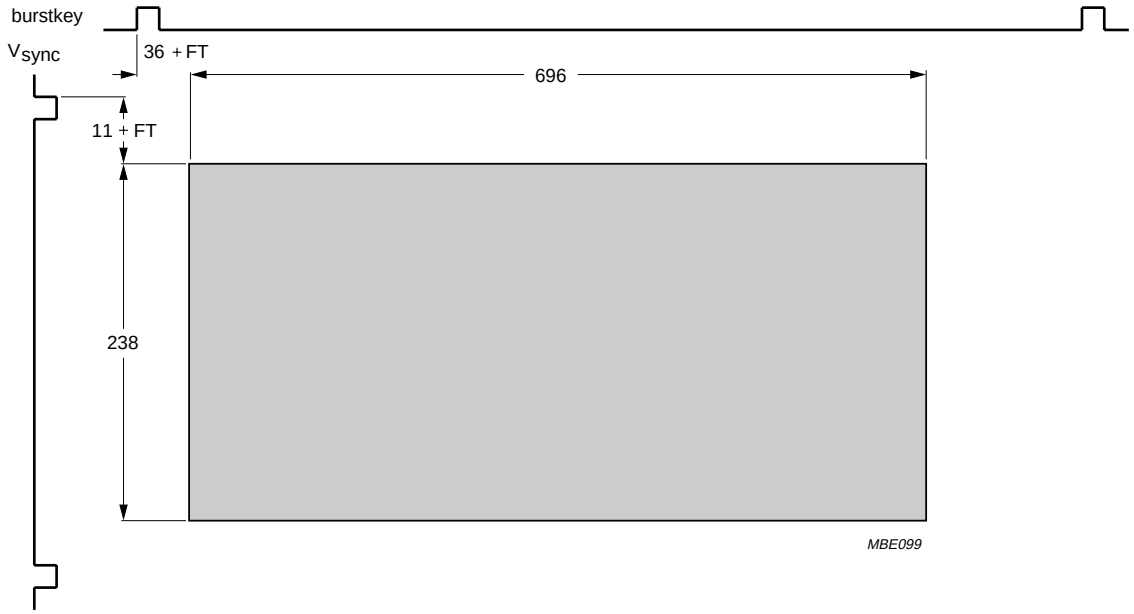


Fig.17 Factory mode.

I²C-bus

The I²C-bus provides bi-directional 2-line communication between different ICs. The SDA line is the Serial Data line and the SCL serves as Serial Clock Line. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

The SAB9075H has the I²C-bus addresses 2C and 2E, switchable by the pin A0. Valid subaddresses are 00H to 0FH.

I²C-bus control is in accordance with the I²C-bus protocol.

First a start sequence must be put on the I²C-bus, then the I²C-bus address 2C or 2E, followed by a subaddress 00 to 0F. After this sequence, the data of the subaddress must be sent. An auto-increment function then gives the option ‘send data’ of the incremented subaddresses until a stop sequence has been given.

Table 3 Overview of I²C-bus addresses (note 1)

	Data Bytes							
SA	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
00	PIPON	MANRED	MASPECT	SASPECT	MODE3	MODE2	MODE1	MODE0
01	HPOS	VPOS	MFREEZE	SFREEZE	note 2	BCOLPOL	MVFILT	SVFILT
02	note 2	note 2	DHFP5	DHFP4	DHFP3	DHFP2	DHFP1	DHFP0
03	note 2	note 2	DVFP5	DVFP4	DVFP3	DVFP2	DVFP1	DVFP0
04	MREDH1	MREDH0	MREDV1	MREDV0	SREDH1	SREDH0	SREDV1	SREDV0
05	note 2	CBSEL2	CBSEL1	CBSEL0	note 2	SLSEL2	SLSEL1	SLSEL0
06	note 2	MBON	MBBRT1	MBBRT0	note 2	MBCOL2	MBCOL1	MBCOL0
07	note 2	SBON	SBBRT1	SBBRT0	note 2	SBCOL2	SBCOL1	SBCOL0
08	note 2	CBON	CBBRT1	CBBRT0	note 2	CBCOL2	CBCOL1	CBCOL0
09	FACMODE	BGON	BGBRT1	BGBRT0	note 2	BGCOL2	BGCOL1	BGCOL0
0A	MCOLPOL	MVSPOL	MHSYNC	MFPOL	SCOLPOL	SVSPOL	SHSYNC	SFPOL
0B	MAAHFP3	MAAHFP3	MAAHFP3	MAAHFP3	MAAVFP3	MAAVFP3	MAAVFP3	MAAVFP3
0C	SAAHFP3	SAAHFP3	SAAHFP3	SAAHFP3	SAAVFP3	SAAVFP3	SAAVFP3	SAAVFP3
0D	note 2	note 2	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
0E	note 2	note 2	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
0F	MMUTE	SMUTE	note 2	note 2	note 2	note 2	note 2	note 2

Notes

1. Table 3 gives an overview of the I²C-bus addresses. They will be explained in more detail in the following pages.
2. Some address spaces are unused but already implemented for future functionality.

Table 4 PIP mode control (note 1)

PIP MODE		ASPECT RATIO		MAIN-REDUCTION(2)		SUB-REDUCTION(2)	
NAME	**MODE(3)**	**MAIN(4)**	**SUB(4)**	**HOR**	**VER**	**HOR**	**VER**
SPS	0000	0	0	–	–	1/4	1/4
SPS	0000	0	1	–	–	1/3	1/4
SPS	0000	1	0	–	–	1/4	1/3
SPS	0000	1	1	–	–	1/4	1/4
SPL	0001	0	0	–	–	1/3	1/3
SPL	0001	0	1	–	–	1/2	1/3
SPL	0001	1	X	–	–	1/3	1/3
DP	1010	0	X	1/2	1/2	1/2	1/2
DP	1010	1	0	1/2	1/2	1/3	1/2
DP	1010	1	1	1/2	1/2	1/2	1/2
MP3	0110	X	X	–	–	1/4	1/4
MP4	1110	X	X	1/2	1/2	1/4	1/4
MP7	0100	X	X	–	–	1/4	1/4
MP8	1100	X	X	1/2	1/2	1/4	1/4
MP9	1001	X	X	1/3	1/3	1/3	1/3

Notes

1. Table 4 gives an overview of the possible PIP modes and how to set them via the I^2C-bus.
2. The columns main and sub-reduction indicate how the PIP pictures appear on the screen.
3. The column mode corresponds to the lower 4 bits of I^2C-bus Register 0.
4. The main and sub-aspect ratios correspond to the bits 5 and 6 of I^2C-bus Register 0.

Table 5 Register 0; PIP mode control register

BIT	MODE	RESULT
7	PIPON	logic 0 = PIP function is OFF[1]; logic 1 = PIP function is ON
6	MANRED	logic 0 = automatic reduction factors[2]; logic 1 = manual reduction factors[3]
5	MASPECT[4]	main-aspect ratio; 0 = 4 : 3; 1 = 16 : 9
4	SASPECT[4]	sub-aspect ratio; 0 = 4 : 3; 1 = 16 : 9
3	MODE(3)[5]	PIP mode
2	MODE(2)[5]	PIP mode
1	MODE(1)[5]	PIP mode
0	MODE(0)[5]	PIP mode

Notes

1. With PIPON in OFF mode the fast blanking signal is made inactive. All other functions will operate as if the circuit were in operational mode.
2. With MANRED set to logic 0 the reduction factors will be set automatically, dependent on the PIP mode and the aspect ratio bits of main and sub (bits 5 and 4). Table 4 indicates which bits should be set to obtain a certain PIP mode.
3. With MANRED set to logic 1 the calculation of the reduction factors is not carried out and should be set by Register 4 (see Table 9). Only combinations with MANRED set to logic 0 are guaranteed.
4. MASPECT and SASPECT are used in automatic mode (MANRED) to indicate the type of input signals, together with MODE the PIP mode can be set (see Table 4). In manual mode these bits are ignored.
5. The MODE bits set the PIP mode. For the multi-PIP modes the frozen PIPs are set to the 30% grey colour. Once a PIP has been made live it will always display the last video data.

Table 6 Register 1; general control register

BIT	MODE	RESULT
7	HPOS[1]	logic 0 = left; logic 1 = right
6	VPOS[1]	logic 0 = top; logic 1 = bottom
5	MFREEZE[2]	logic 0 = main-freeze is OFF; logic 1 = main-freeze is ON
4	SFREEZE[2]	logic 0 = sub-freeze is OFF; logic 1 = sub-freeze is ON
3	–	not used
2	BCOLPOL[3]	border UV polarity; logic 0 = +(B–Y), +(R–Y); logic 1 = –(B–Y), –(R–Y)
1	MVFILT[4]	main-vertical filter mode; logic 0 = Mode 0; logic 1 = Mode 1
0	SVFILT[4]	sub-vertical filter mode; logic 0 = Mode 0; logic 1 = Mode 1

Notes

1. HPOS and VPOS determine the general location of the sub-PIP on the screen. HPOS only operates in modes SPS, SPL, DP, MP3 and MP4. VPOS only operates in modes SPS and SPL. The default location of the sub-pictures will be left top.
2. MFREEZE will freeze the main-picture, and SFREEZE will freeze the sub-picture selected by the live select bits as in Register 8 (see Table 13).
3. BCOLPOL can invert the border polarity of U and V.
4. MVFILT and SVFILT set the type of vertical filtering for the main and sub-channel. Mode 1 means that diagonal lines are linearized, in Mode 0 this option is switched OFF. This filtering mode only operates with vertical reduction factors $\frac{1}{3}$ and $\frac{1}{4}$.

Table 7 Register 2; display horizontal fine position register

BIT	MODE	DESCRIPTION(1)
7	–	not used
6	–	not used
5	DHFP(5)	horizontal fine position (64 steps)
4	DHFP(4)	horizontal fine position
3	DHFP(3)	horizontal fine position
2	DHFP(2)	horizontal fine position
1	DHFP(1)	horizontal fine position
0	DHFP(0)	horizontal fine position

Note

1. The display position can be set in steps of 4 pixels/lines and 1 line/field. The offsets on the display position are depicted in Fig.4.

Table 8 Register 3; display vertical fine position register

BIT	MODE	DESCRIPTION(1)
7	–	not used
6	–	not used
5	DVFP(5)	vertical fine position (64 steps)
4	DVFP(4)	vertical fine position
3	DVFP(3)	vertical fine position
2	DVFP(2)	vertical fine position
1	DVFP(1)	vertical fine position
0	DVFP(0)	vertical fine position

Note

1. The display position can be set in steps of 4 pixels/lines and 1 line/field. The offsets on the display position are depicted in Fig.4.

Table 9 Register 4; reduction factor register

BIT	MODE	DESCRIPTION(1)
7	MREDH(1)	main-horizontal reduction factor
6	MREDH(0)	main-horizontal reduction factor
5	MREDV(1)	main-vertical reduction factor
4	MREDV(0)	main-vertical reduction factor
3	SREDH(1)	sub-horizontal reduction factor
2	SREDH(2)	sub-horizontal reduction factor
1	SREDV(1)	sub-vertical reduction factor
0	SREDV(0)	sub-vertical reduction factor

Note

1. 01 = $^1/_1$; 10 = $^1/_2$; 11 = $^1/_3$; 00 = $^1/_4$.

Table 10 Register 5; channel select register

BIT	MODE	DESCRIPTION
7	–	not used
6	CBSEL(2)[1]	channel-border select (maximum 8 channels)
5	CBSEL(1)[1]	channel-border select
4	CBSEL(0)[1]	channel-border select
3	–	not used
2	SLSEL(2)[2]	sub-live select (maximum 8 channels)
1	SLSEL(1)[2]	sub-live select
0	SLSEL(0)[2]	sub-live select

Notes

1. With CBSEL one border of the displayed sub-borders can be selected independently of the SLSEL. This only operates when the channel select-border is ON as in Register 8 (see Table 13) and when the selected channel number is displayed.
2. With SLSEL the active sub-live picture can be selected. This only operates when the SFREEZE is OFF as in Register 1 (see Table 6) and when the selected channel is displayed.

Background and main, sub and channel-border colour and brightness handling

Registers 6 to 9 (see Tables 11 to 14) handle background and main, sub and channel-border colour and brightness. The borders and background can be set ON and OFF.

Background, main and sub-borders are black when they are OFF. The channel-border gets the current sub-border colour when it is switched OFF. The brightness can be set in 4 steps (30%, 50%, 70% and 100%). Eight different colours can be set in accordance with Table 15.

Table 11 Register 6; main-border control register

BIT	MODE	DESCRIPTION
7	–	not used
6	MB0N	logic 0 = MB is OFF; logic 1 =MB is ON
5	MBBRT(1)	main-border brightness (4 steps)
4	MBBRT(0)	main-border brightness
3	–	not used
2	MBCOL(2)	main-border colour (8 colours)
1	MBCOL(1)	main-border colour
0	MBCOL(0)	main-border colour

Table 12 Register 7; sub-border control register

BIT	MODE	DESCRIPTION
7	–	not used
6	SBON	logic 0 = SB is OFF; logic 1 = SB is ON
5	SBBRT(1)	sub-border brightness (4 steps)
4	SBBRT(0)	sub-border brightness
3	–	not used
2	SBCOL(2)	sub-border colour (8 colours)
1	SBCOL(1)	sub-border colour
0	SBCOL(0)	sub-border colour

Table 13 Register 8; channel-border control register

BIT	MODE	DESCRIPTION
7	–	not used
6	CBON	logic 0 = CB is OFF; logic 1 = CB is ON
5	CBBRT(1)	channel-border brightness (4 steps)
4	CBBRT(0)	channel-border brightness
3	–	not used
2	CBCOL(2)	channel-border colour (8 colours)
1	CBCOL(1)	channel-border colour
0	CBCOL(0)	channel-border colour

Table 14 Register 9; background control register

BIT	MODE	DESCRIPTION
7	FACMODE[1]	logic 0 = FM is OFF; logic 1 = FM is ON
6	BGON	logic 0 = BG is OFF; logic 1 = BG is ON
5	BGBRT(1)	background brightness (4 steps)
4	BGBRT(0)	background brightness
3	–	not used
2	BGCOL(2)	background colour (8 colours)
1	BGCOL(1)	background colour
0	BGCOL(0)	background colour

Note

1. The FACMODE bit controls the factory mode which shows an enlarged background colour as depicted in Fig.17 (BGON must be set).

Table 15 Colour table

COLOUR TYPE	BRIGHTNESS (%)(1)							
	0	**10**	**30**	**50**	**60**	**70**	**80**	**100**
Black/white	40H	50H	60H	70H	47H	57H	67H	77H
Blue	–	–	41H	51H	–	61H	–	71H
Red	–	–	42H	52H	–	62H	–	72H
Magenta	–	–	43H	53H	–	63H	–	73H
Green	–	–	44H	54H	–	64H	–	74H
Cyan	–	–	45H	55H	–	65H	–	75H
Yellow	–	–	46H	56H	–	66H	–	76H

Note

1. The values in are the I²C-bus register values for the Colour Control Registers 6 to 9 (see Tables 11 to 14). The values are hexadecimal values of which the left part indicates the brightness and the right part the colour value.

Table 16 Border display

PIP MODES	MBON	BGON(1)	SBON	CBON	MAIN-BORDER DISPLAY(2)	BACK-GROUND DISPLAY	SUB-BORDER DISPLAY(2)	CHANNEL BORDER DISPLAY
MP4 MP8 MP9 FFS	OFF	OFF	–	–	live BG(3)	live BG(3)	–	–
	OFF	ON	–	–	BGCOL	BGCOL	–	–
	ON	OFF	–	–	MBCOL	live BG(3)	–	–
	ON	ON	–	–	MBCOL	BGCOL	–	–
SPS SPL	–	–	OFF	–	–	–	live BG(3)	–
	–	–	ON	–	–	–	SBCOL	–
DP	OFF	OFF	OFF	–	live BG(3)	live BG(3)	live BG(3)	–
	OFF	ON	OFF	–	BGCOL	BGCOL	BGCOL	–
	ON	OFF	ON	–	MBCOL	live BG(3)	SBCOL	–
	ON	ON	ON	–	MBCOL	BGCOL	SBCOL	–
MP3 MP4 MP7 MP8 MP9	–	OFF	OFF	ON	–	live BG(3)	live BG(3)	CBCOL
	–	ON	OFF	ON	–	BGCOL	BGCOL	CBCOL
	–	OFF	ON	ON	–	live BG(3)	SBCOL	CBCOL
	–	ON	ON	ON	–	BGCOL	SBCOL	CBCOL

Notes

1. The BGON I²C-bus bit controls the display area outside the PIP and border area, set to ON means that the background gets the BGCOL colour value.
2. The main and sub-border displays are dependent on the I²C-bus switches.
3. ‘Live BG’ means that the original picture is shown.

Table 17 Register A; decoder format register

BIT	MODE	RESULT
7	MCOLPOL(1)	main-UV polarity; logic 0 = original; logic 1 = inverted
6	MVSPOL(2)	main-vertical sync polarity; logic 0 = positive pulse; logic 1 = negative pulse
5	MHSYNC(3)	main-horizontal sync selection; logic 0 = burst edge; logic 1 = H – sync
4	MFPOL	main-field polarity; inverts field identification window
3	SCOLPOL(1)	sub-UV polarity; logic 0 = original; logic 1 = inverted
2	SVSPOL(2)	sub-vertical sync polarity; logic 0 = positive pulse; logic 1 = negative pulse
1	SHSYNC(3)	sub-horizontal sync selection; logic 0 = burst edge; logic 1 = H – sync
0	SFPOL	sub-field polarity, inverts field identification window

Notes

1. MCOLPOL and SCOPOL invert the UV video data.
2. MVSPOL and SVSPOL determine the active edge of the V_{sync}. If VSPOL is logic 0, the positive edge of the V_{sync} will be taken; if VSPOL is logic 1, the negative edge of the V_{sync} will be taken.
3. MHSYNC and SHSYNC determine whether the H_{sync} signal or the burstkey is used as internal horizontal synchronization.

The exact timing of the V_{sync} in relation to the H_{sync} reference pulse is depicted in Fig.18. A field identification window determines whether a V_{sync} is being handled as a 1st field or a 2nd field. This field identification window can be inverted by the FPOL bit. If FPOL is logic 0 and an active edge of the V_{sync} occurs when the F-ID signal is logic 0, it will be regarded as the 1st field. If FPOL is logic 0 and an active edge of the V_{sync} occurs when the F-ID signal is logic 1, it will be regarded as the 2nd field. If FPOL is logic 1 the 1st and 2nd field IDs are changed over.

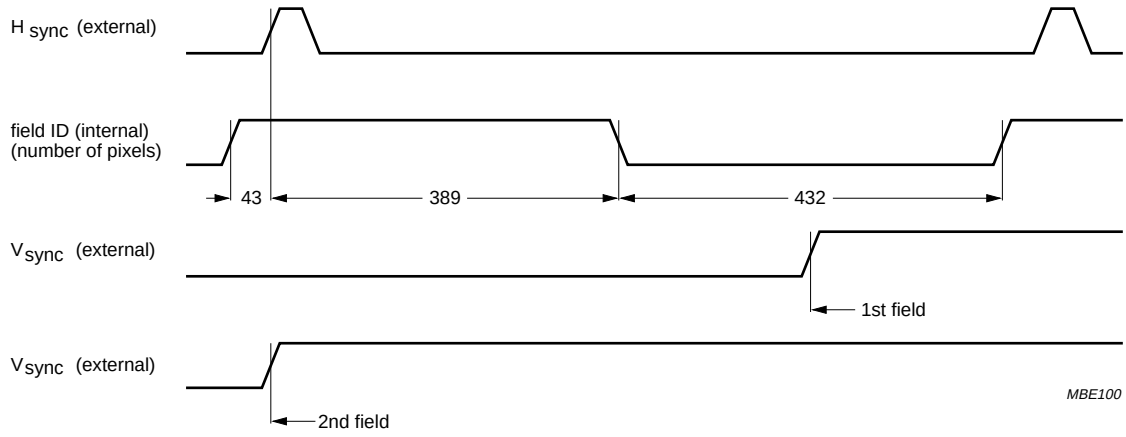


Fig.18 V_{sync} timing and field identification.

Table 18 Register B; main-acquisition area fine position

BIT	MODE	DESCRIPTION(1)
7	MAAHFP(3)	main-acquisition area horizontal fine position
6	MAAHFP(2)	main-acquisition area horizontal fine position
5	MAAHFP(1)	main-acquisition area horizontal fine position
4	MAAHFP(0)	main-acquisition area horizontal fine position
3	MAAVFP(3)(2)	main-acquisition area vertical fine position
2	MAAVFP(2)(2)	main-acquisition area vertical fine position
1	MAAVFP(1)(2)	main-acquisition area vertical fine position
0	MAAVFP(0)(2)	main-acquisition area vertical fine position

Notes

1. The acquisition area can be adjusted in 16 steps of 2 pixels horizontally and 1 line/field vertically.
2. With MAAVFP a complete field must have been processed before the next V_{sync} occurs. This is relevant for non-standard signals.

Table 19 Register C; sub-acquisition area fine position

BIT	MODE	DESCRIPTION (1)
7	SAAHFP(3)	sub-acquisition area horizontal fine position
6	SAAHFP(2)	sub-acquisition area horizontal fine position
5	SAAHFP(1)	sub-acquisition area horizontal fine position
4	SAAHFP(0)	sub-acquisition area horizontal fine position
3	SAAVFP(3)(2)	sub-acquisition area vertical fine position
2	SAAVFP(2)(2)	sub-acquisition area vertical fine position
1	SAAVFP(1)(2)	sub-acquisition area vertical fine position
0	SAAVFP(0)(2)	sub-acquisition area vertical fine position

Notes

1. The acquisition area can be adjusted in 16 steps of 2 pixels horizontally and 1 line/field vertically.
2. With SAAVFP a complete field must have been processed before the next V_{sync} occurs. This is relevant for non-standard signals.

Auxiliary registers

The Auxiliary Registers D to F (see Tables 20 to 22) are implemented to generate I^2C-bus controlled signals for circuits which do not have an on-board I^2C-bus.

Table 20 Register D; Auxiliary Control Register 1

BIT	MODE	DESCRIPTION
7	–	not used
6	–	not used
5	HUE(5)	hue control (output pin HUE)
4	HUE(4)	hue control
3	HUE(3)	hue control
2	HUE(2)	hue control
1	HUE(1)	hue control
0	HUE(0)	hue control

Table 21 Register E; Auxiliary Control Register 2

BIT	MODE	DESCRIPTION
7	–	not used
6	–	not used
5	SAT(5)	saturation control (output pin SAT)
4	SAT(4)	saturation control
3	SAT(3)	saturation control
2	SAT(2)	saturation control
1	SAT(1)	saturation control
0	SAT(0)	saturation control

Table 22 Register F; Auxiliary Control Register 3

BIT	MODE	DESCRIPTION
7	MMUTE	data bit directly to output pin MMUTE
6	SMUTE	data bit directly to output pin SMUTE
5	–	not used
4	–	not used
3	–	not used
2	–	not used
1	–	not used
0	–	not used

External memory

For the external memory two VDRAMS of type Mitsubishi M5442256 are used. They have a storage capacity of 262144 words of 4-bit each and will be used in parallel.

An overview of the timing to the VDRAM is depicted in Fig.19. Three different timing modes are shown. If the SAB9075 is not in one of these three modes, it is in idle mode in which all the control signals are HIGH. An idle mode takes at least 4 clock periods. Switching from one mode to another is always carried out via this idle mode.

The clock signal shown is an internal clock derived from the PLLs and is approximately 27 MHz.

Main and sub-ADCs

Both main and sub-channels convert the analog input signals to digital signals by three ADCs for each channel.

The input levels of the ADCs are equal and can set by the MAV_{refT}, SAV_{refT}, MAV_{refB}, and SAV_{refB} pins.The reference levels are made internally by a resistor network which divides the analog V_{DD} to a default set of preferred signal levels of 1.5 V. If the application requires a different set of levels the internal resistors can be shunted. External capacitors are required to filter AC components on the reference levels.

The resolution of the ADCs is 6-bit and the sampling is carried out at the system frequency of 27 MHz. The bias current I_{bias} is made internally but can be increased or decreased.

The inputs should be AC-coupled and an internal clamping circuit will clamp the input to MAV_{refB} and SAV_{refB} for the luminance channels and to

$$\frac{MAV_{refT} + MAV_{refB}}{2} + \frac{LSB}{2}$$

$$\frac{SAV_{refT} + SAV_{refB}}{2} + \frac{LSB}{2}$$

for the chrominance channels. The clamping starts at the active edge of the burstkey.

For more information see chapter “Test and application information”.

Output DACs

The digital processed signals are converted to analog signals by means of three DACs. The output voltages of these DACs are default set by the DAV_{refTU}, DAV_{refTV} and DAV_{refTY} pins for the TOP-levels. Default signal levels are 1.5 V. The output buffer after each DAC is a PMOS source follower.

For more information see chapter “Test and application information”.

HUE and SAT DACs

The HUE and SAT DACs are resistor DACs based on a R2R network. They have a direct control from their I^2C-bus register and therefore their sample frequency is limited by the I^2C-bus frequency. The output voltage is linear with the I^2CV_{DD}. Therefore the V_{DD} of this block is a separate pin.

PLLs and clock generation

The SAB9075H has two PLLs on-board, one for the sub-channel and one for the main-channel and the display part. The PLLs lock to the input signals MH_{sync} and SH_{sync}. The internal clock frequency is 1728 times higher which is approximately 27 MHz in a standard NTSC system.

The positive edges of the H_{sync} signals are the driving timing points. For good short term stability they have to be noise/jitter free.

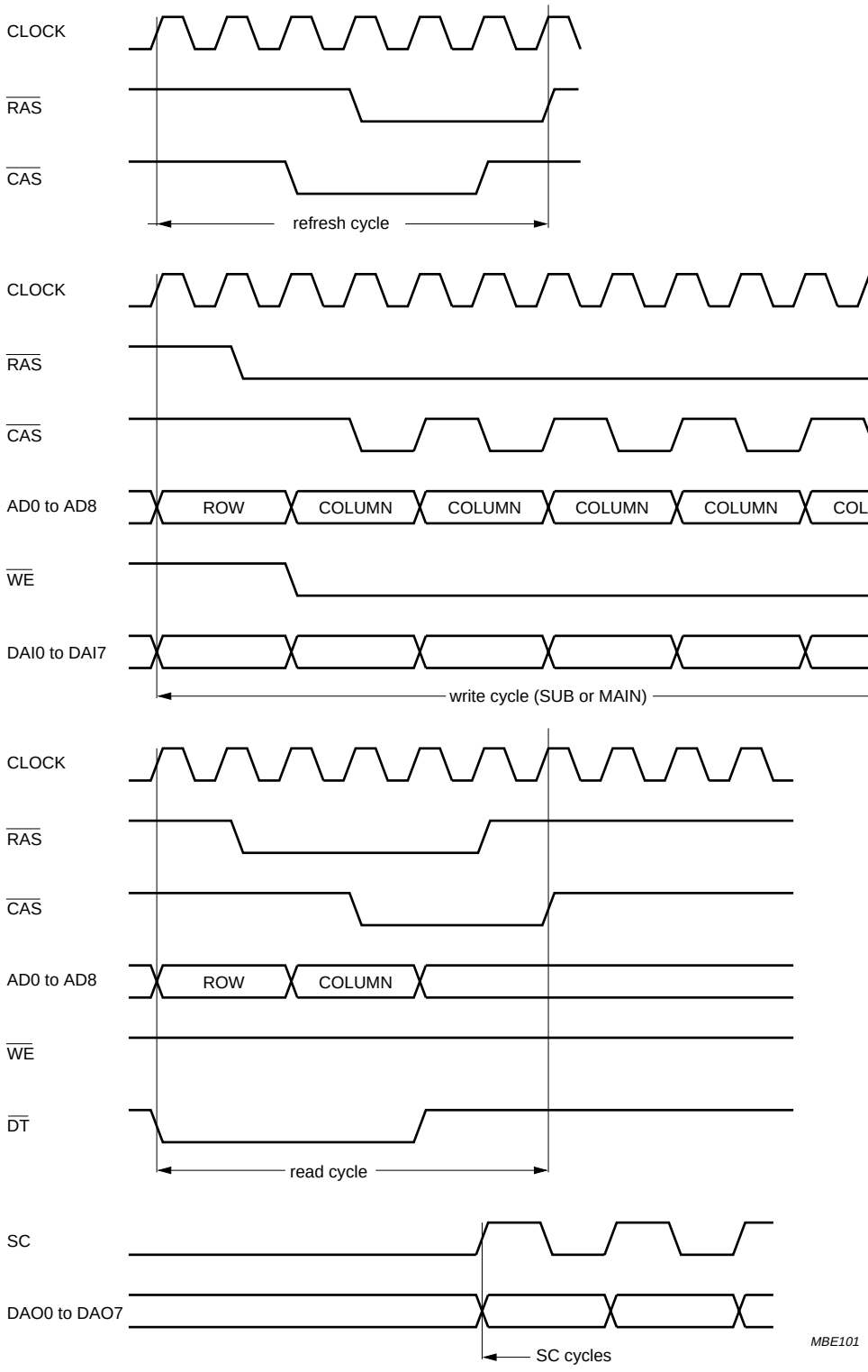


Fig.19 VDRAM timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+6.5	V
ΔV_{DD}	supply voltage variation	–	0.2	V
T_{stg}	storage temperature	–25	+150	°C
T_{amb}	operating ambient temperature	0	70	°C
V_{esd}	electrostatic discharge handling	–	–	V
P_{tot}	total power dissipation	–	1.5	W

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R_{thj-a}	thermal resistance from junction to ambient in free air	38	K/W

QUALITY SPECIFICATION

In accordance with SNW-FQ-611, Part E, dated 14 December 1992.

CHARACTERISTICS

V_{DD} = 5.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	positive supply voltage		4.5	5.0	5.5	V
V_{SS}	negative supply voltage		–	0	–	V
ΔV_{DD}	maximum voltage difference between all positive supply pins		–	0	100	mV
ΔV_{SS}	maximum voltage difference between all negative supply pins		–	0	100	mV
I_{DDQ}	quiescent current digital positive supply pins	note 1	–	2	tbf	μA
$MPIV_{DDA}$	supply current PLL main		–	2.5	tbf	mA
$SPIV_{DDA}$	supply current PLL sub		–	2.5	tbf	mA
$MAIV_{DDA}$	supply current 3 main-ADCs		–	36	tbf	mA
$SAIV_{DDA}$	supply current 3 sub-ADCs		–	36	tbf	mA
DIV_{DDA}	supply current 3 display DACs		–	18	tbf	mA
I^2CV_{DD}	supply current HUE and SAT DACs	note 2	–	2.5	5	mA
I_{tot}	total supply current		tbf	220	tbf	mA
Converter and clamping						
AV_{refT}	top reference voltage	note 3	1.0	1.9	2.0	V
AV_{refB}	bottom reference voltage	note 3	0	0.4	1.0	V
Rin_{ref}	input resistance V_{refT} to V_{refB}	note 3; 1 ADC	tbf	860	tbf	Ω
V_I	DC input voltage		V_{refB}	–	V_{refT}	V
V_i	AC input voltage (peak-to-peak value)		1.0	1.5	–	V
R_i	input resistance	clamping OFF	1	–	–	MΩ
R_{iY}	input resistance for Y channel	clamping ON	–	200	–	Ω
R_{iV}	input resistance for V channel	clamping ON	–	800	–	Ω
R_{iU}	input resistance for U channel	clamping ON	–	800	–	Ω
C_i	input capacitance		–	15	–	pF
Res	resolution		–	6	–	bit
f_s	sample frequency rate	note 4	–	27	–	MHz
DNL	differential non-linearity		–1.0	–	+1.0	LSB
INL	integral non-linearity		–1.0	–	+1.0	LSB
V_{os}	input offset voltage		–1.0	–	+1.0	LSB
α_{cs}	channel separation	within channel	tbf	40	–	dB
		to other channel	tbf	40	–	dB
PSRR	power supply rejection ratio		tbf	40	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TD_{clamp}	delay burstkey edge to clamping start		–	0	–	µs
T_{clamp}	duration of clamping		–	2.33	–	µs
V_{clampY}	clamping voltage level Y	AD_{out} = 0H	–	V_s	–	V
V_{clampU}	clamping voltage level U	AD_{out} = 20H	–	0.5 V_{T+B}	–	V
V_{clampV}	clamping voltage level V	AD_{out} = 20H	–	0.5 V_{T+B}	–	V
Digital-to-analog converter						
V_{refT}	top reference voltage (Y, U and V)	note 3	1.0	1.5	2.0	V
Rin_{ref}	input resistance V_{refT} to V_{refB}	note 3; 1 DAC	tbf	1.0	tbf	kΩ
$V_{o(max)}$	maximum output voltage		V_{refB}	–	V_{refT}	V
$R_{L(min)}$	minimum load resistance		10	–	–	kΩ
$C_{L(max)}$	maximum load capacitance		–	50	–	pF
Res	resolution		–	7	–	bit
f_s	sample frequency rate	note 4	–	27	–	MHz
DNL	differential non-linearity		–0.5	–	+0.5	LSB
INL	integral non-linearity		–1.0	–	+1.0	LSB
α_{cs}	channel separation		tbf	40	–	dB
PSRR	power supply rejection ratio		tbf	40	–	dB
Digital-to-analog converter HUE/SAT						
V_o	output voltage		V_{SS}	–	V_{DD}	V
$R_{L(min)}$	minimum load resistance	note 2	100	–	–	kΩ
$C_{L(max)}$	maximum load capacitance		–	50	–	pF
Res	resolution		–	6	–	bit
DNL	differential non-linearity		–1.0	–	+1.0	LSB
INL	integral non-linearity		–1.0	–	+1.0	LSB
PSRR	power supply rejection ratio	note 2	–	0	–	dB
PLL and clock generation; note 4						
V_{TOP}	TOP-level input voltage		2.5	–	PV_{DD}	V
V_{LOW}	LOW-level input voltage		–	–	0.5	V
V_{slice}	slicing voltage level below TOP		0.45	1.0	2.0	V
f_{PLL}	input frequency		14750	15734	17250	Hz

Notes

1. Digital clocks are silent and analog bias current is zero.
2. The HUE and SAT DACs are based on a R2R ladder network as describe in the section “HUE and SAT DACs”. The maximum output sample frequency is determined by the I^2C-bus.
3. The input configuration of the ADCs is depicted in Fig.20. The minimum difference $AV_{refT} - AV_{refB}$ should be larger than 1.0 V. The reference voltages can be calculated as follows:

$$V_{refT} = AV_{DD} \times \left(\frac{1.9}{5.0}\right) V \; ; \; V_{refB} = AV_{DD} \times \left(\frac{0.4}{5.0}\right) V$$

4. The internal system frequencies are 1728 times the input frequency. For more detailed information about the clock generation see section “PLLs and clock generation”.

DC CHARACTERISTICS FOR DIGITAL PART

All V_{DD} pins = 4.5 to 5.5 V; T_{amb} = −20 to +75 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH level input voltage	HPF01	70	–	–	$\%V_{DD}$
		HPP01	70	–	–	$\%V_{DD}$
		HUP07	80	–	–	$\%V_{DD}$
V_{IL}	LOW level input voltage	IOI41	70	–	–	$\%V_{DD}$
		HPF01	–	–	30	$\%V_{DD}$
		HPP01	–	–	30	$\%V_{DD}$
		HUP07	–	–	20	$\%V_{DD}$
		IOI41	–	–	30	$\%V_{DD}$
V_{hys}	hysteresis voltage	HUP07	–	33	–	$\%V_{DD}$
V_{OH}	HIGH level output voltage	OPF20; I_{OL} = −2 mA; V_{DD} = 4.5 V	4.4	–	–	V
		SPF20; I_{OL} = −2 mA; V_{DD} = 4.5 V	4.4	–	–	V
V_{OL}	LOW level output voltage	IOI41; I_{OL} = +2 mA; V_{DD} = 4.5 V	–	–	0.15	V
		OPF20; I_{OL} = +2 mA; V_{DD} = 4.5 V	–	–	0.15	V
		SPF20; I_{OL} = +2 mA; V_{DD} = 4.5 V	–	–	0.15	V
I_{LI}	input leakage current	HPF01	–	0.1	1	µA
		HPP01	–	0.1	1	µA
I_{LOZ}	three-state output leakage current	IOI41; V_{DD} = 5.5 V	–	0.2	5.0	µA
R_{pu}	internal pull up resistor	HUP07	17	–	134	kΩ

AC CHARACTERISTICS FOR DIGITAL PART

V_{DD} = 4.5 5.5 V; T_{amb} = −20 to +75 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{sys}	system frequency	note 1	–	27	30	MHz
t_r	rise time	V_{DD} = 4.5 V	–	6	25	ns
t_f	fall time	V_{DD} = 4.5 V	–	6	25	ns

Note

1. The internal system frequencies are 1728 times the input frequency. For more detailed information about the clock generation see section “PLLs and clock generation”.

TEST AND APPLICATION INFORMATION

Fig.20 shows how the ADCs and the DACs can be connected in the application.

The generation of the reference voltages is carried out internally and they have to be externally decoupled for AC signals.

For all ADCs and DACs the internal resistor division is such that a maximum signal voltage level of 1.5 V is obtained. For the ADCs there is a DC offset voltage of 0.4 V.

A modification of these reference voltages can be achieved by external shunting.

The ADC reference voltages are the same for all Y/U/V channels which means that their input levels need to be the same. The DAC voltage references can be set separately for Y/U/V channels. These reference voltages can be modified by shunting.

The output buffers of the DACS are PMOS source followers with a minimum output load of 10 kΩ.

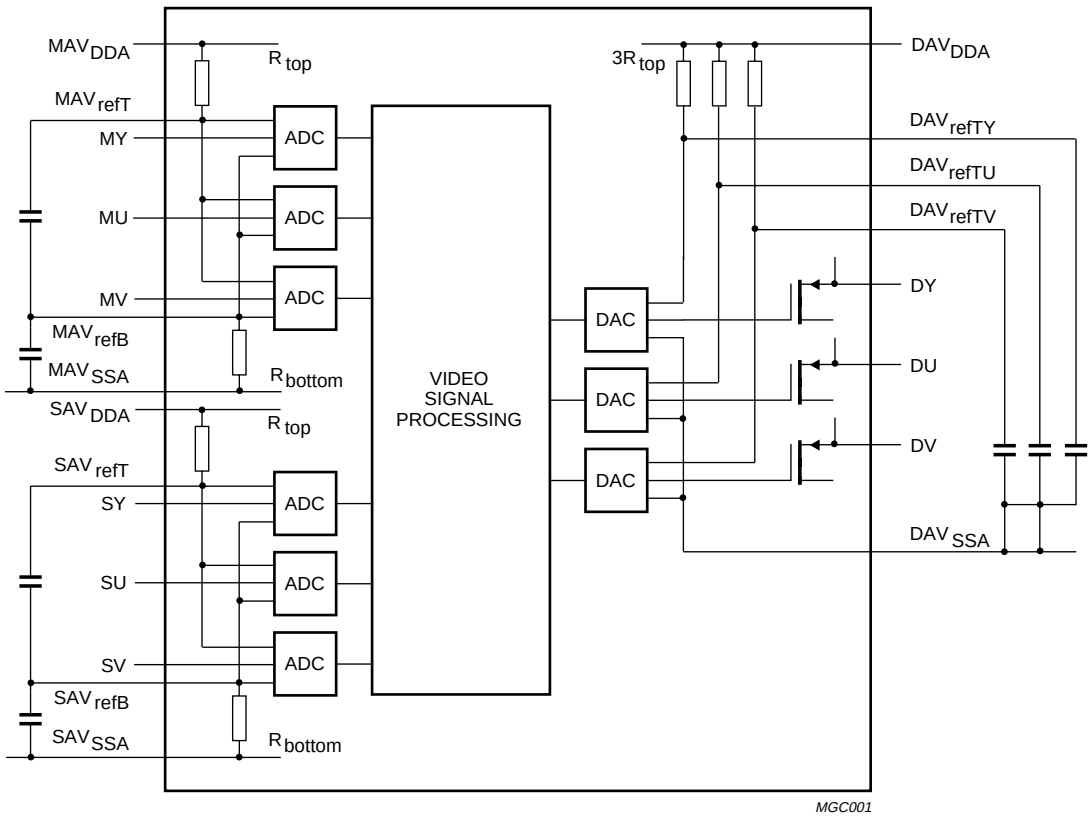


Fig.20 Analog application diagram ADCs and DACs.

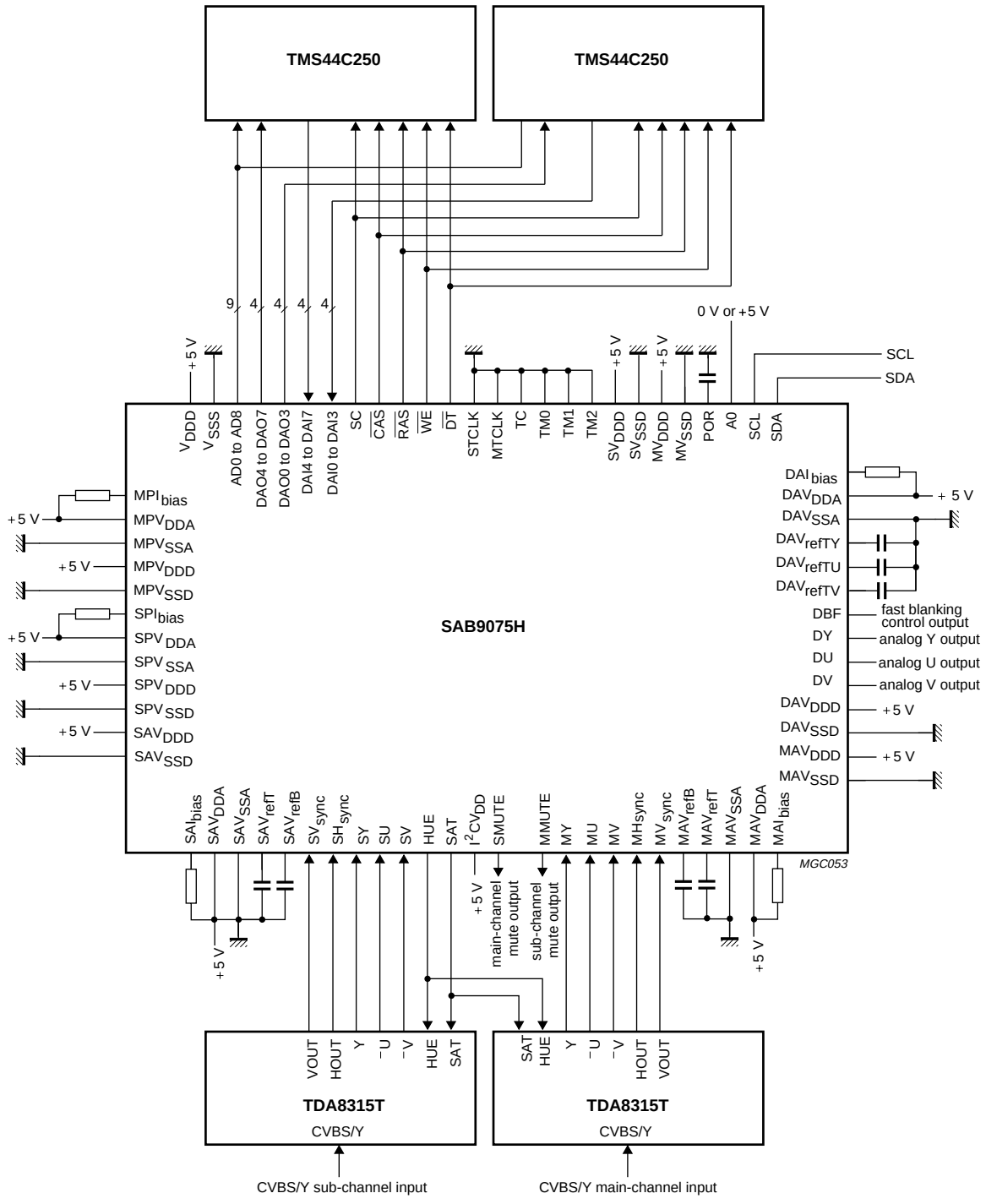
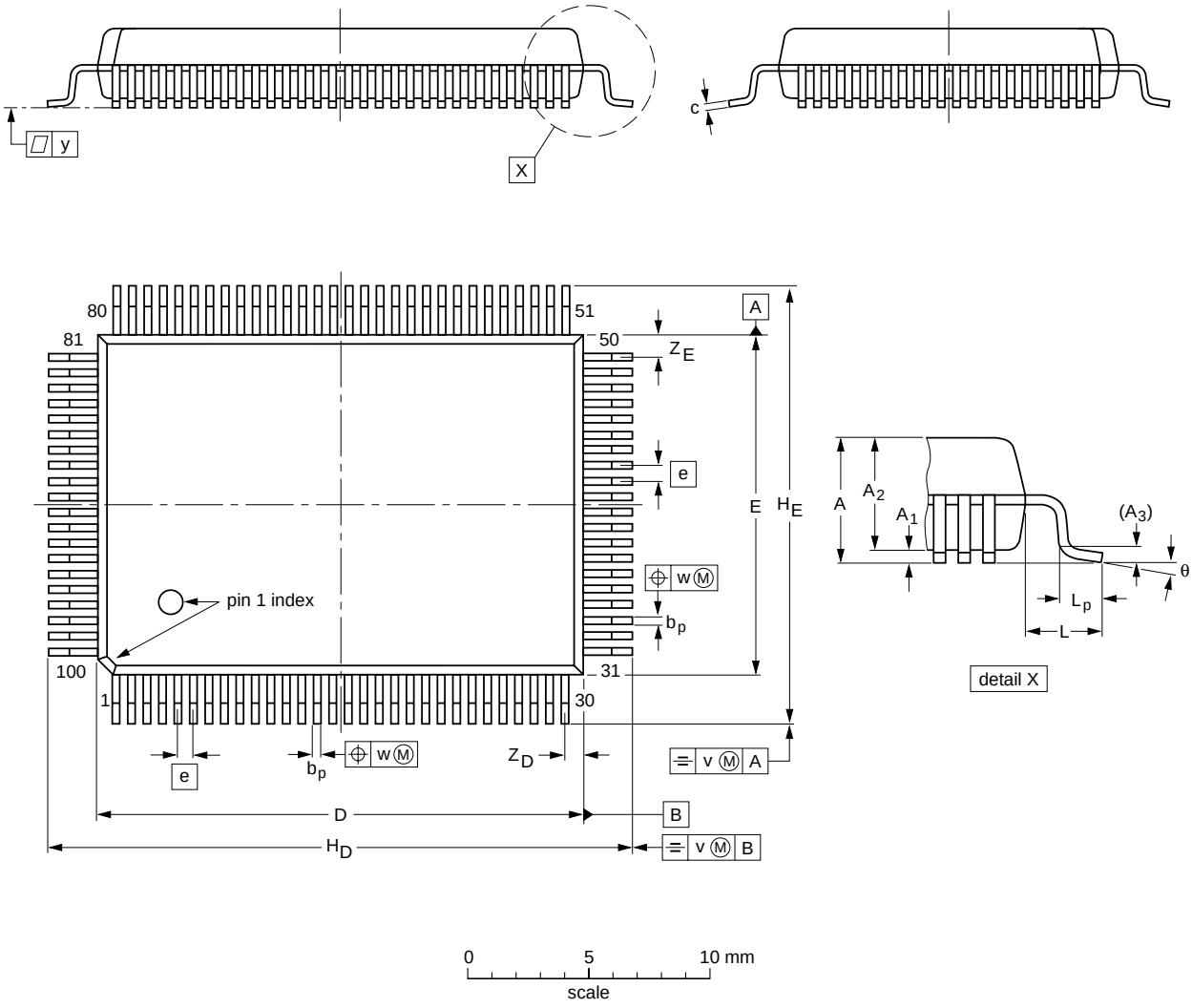


Fig.21 Application diagram.

PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						~~95-02-04~~ 97-08-01

SOLDERING

Plastic quad flat-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

Philips Semiconductors – a worldwide company

Argentina: IEROD, Av. Juramento 1992 - 14.b, (1428)
BUENOS AIRES, Tel. (541)786 7633, Fax. (541)786 9367

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. (02)805 4455, Fax. (02)805 4466

Austria: Triester Str. 64, A-1101 WIEN, P.O. Box 213,
Tel. (01)60 101-1236, Fax. (01)60 101-1211

Belgium: Postbus 90050, 5600 PB EINDHOVEN, The Netherlands,
Tel. (31)40 783 749, Fax. (31)40 788 399

Brazil: Rua do Rocio 220 - 5th floor, Suite 51,
CEP: 04552-903-SÃO PAULO-SP, Brazil.
P.O. Box 7383 (01064-970).
Tel. (011)821-2333, Fax. (011)829-1849

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS:
Tel. (800) 234-7381, Fax. (708) 296-8556

Chile: Av. Santa Maria 0760, SANTIAGO,
Tel. (02)773 816, Fax. (02)777 6730

Colombia: IPRELENSO LTDA, Carrera 21 No. 56-17,
77621 BOGOTA, Tel. (571)249 7624/(571)217 4609,
Fax. (571)217 4549

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. (032)88 2636, Fax. (031)57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. (9)0-50261, Fax. (9)0-520971

France: 4 Rue du Port-aux-Vins, BP317,
92156 SURESNES Cedex,
Tel. (01)4099 6161, Fax. (01)4099 6427

Germany: P.O. Box 10 63 23, 20043 HAMBURG,
Tel. (040)3296-0, Fax. (040)3296 213.

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. (01)4894 339/4894 911, Fax. (01)4814 240

Hong Kong: PHILIPS HONG KONG Ltd., 6/F Philips Ind. Bldg.,
24-28 Kung Yip St., KWAI CHUNG, N.T.,
Tel. (852)424 5121, Fax. (852)428 6729

India: Philips INDIA Ltd, Shivsagar Estate, A Block ,
Dr. Annie Besant Rd. Worli, Bombay 400 018
Tel. (022)4938 541, Fax. (022)4938 722

Indonesia: Philips House, Jalan H.R. Rasuna Said Kav. 3-4,
P.O. Box 4252, JAKARTA 12950,
Tel. (021)5201 122, Fax. (021)5205 189

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. (01)640 000, Fax. (01)640 200

Italy: PHILIPS SEMICONDUCTORS S.r.l.,
Piazza IV Novembre 3, 20124 MILANO,
Tel. (0039)2 6752 2531, Fax. (0039)2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. (03)3740 5028, Fax. (03)3740 0580

Korea: (Republic of) Philips House, 260-199 Itaewon-dong,
Yongsan-ku, SEOUL, Tel. (02)794-5011, Fax. (02)798-8022

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA,
SELANGOR, Tel. (03)750 5214, Fax. (03)757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TX 79905,
Tel. 9-5(800)234-7381, Fax. (708)296-8556

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB
Tel. (040)783749, Fax. (040)788399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. (09)849-4160, Fax. (09)849-7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. (022)74 8000, Fax. (022)74 8341

Pakistan: Philips Electrical Industries of Pakistan Ltd.,
Exchange Bldg. ST-2/A, Block 9, KDA Scheme 5, Clifton,
KARACHI 75600, Tel. (021)587 4641-49,
Fax. (021)577035/5874546.

Philippines: PHILIPS SEMICONDUCTORS PHILIPPINES Inc,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. (02)810 0161, Fax. (02)817 3474

Portugal: PHILIPS PORTUGUESA, S.A.,
Rua dr. António Loureiro Borges 5, Arquiparque - Miraflores,
Apartado 300, 2795 LINDA-A-VELHA,
Tel. (01)4163160/4163333, Fax. (01)4163174/4163366.

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. (65)350 2000, Fax. (65)251 6500

South Africa: S.A. PHILIPS Pty Ltd.,
195-215 Main Road Martindale, 2092 JOHANNESBURG,
P.O. Box 7430 Johannesburg 2000,
Tel. (011)470-5911, Fax. (011)470-5494.

Spain: Balmes 22, 08007 BARCELONA,
Tel. (03)301 6312, Fax. (03)301 42 43

Sweden: Kottbygatan 7, Akalla. S-164 85 STOCKHOLM,
Tel. (0)8-632 2000, Fax. (0)8-632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. (01)488 2211, Fax. (01)481 77 30

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66, Chung Hsiao West
Road, Sec. 1. Taipeh, Taiwan ROC, P.O. Box 22978,
TAIPEI 100, Tel. (02)388 7666, Fax. (02)382 4382.

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong,
Bangkok 10260, THAILAND,
Tel. (662)398-0141, Fax. (662)398-3319.

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. (0212)279 2770, Fax. (0212)269 3094

United Kingdom: Philips Semiconductors LTD.,
276 Bath Road, Hayes, MIDDLESEX UB3 5BX,
Tel. (081)730-5000, Fax. (081)754-8421

United States: 811 East Arques Avenue, SUNNYVALE,
CA 94088-3409, Tel. (800)234-7381, Fax. (708)296-8556

Uruguay: Coronel Mora 433, MONTEVIDEO,
Tel. (02)70-4044, Fax. (02)92 0601

For all other countries apply to: Philips Semiconductors,
International Marketing and Sales, Building BE-p,
P.O. Box 218, 5600 MD, EINDHOVEN, The Netherlands,
Telex 35000 phtcnl, Fax. +31-40-724825

Printed in The Netherlands

533061/1500/01/pp40 Date of release: February 1995

Document order number: 9397 745 30011

Philips Semiconductors

PHILIPS

PHILIPS