

# M66255FP

## 8192 × 10-Bit Line Memory (FIFO)

REJ03F0249-0200  
Rev.2.00  
Sep 14, 2007

### Description

The M66255FP is a high-speed line memory with a FIFO (First In First Out) structure of 8192-word × 10-bit configuration which uses high-performance silicon gate CMOS process technology.

It has separate clock, enable and reset signals for write and read, and is most suitable as a buffer memory between devices with different data processing throughput.

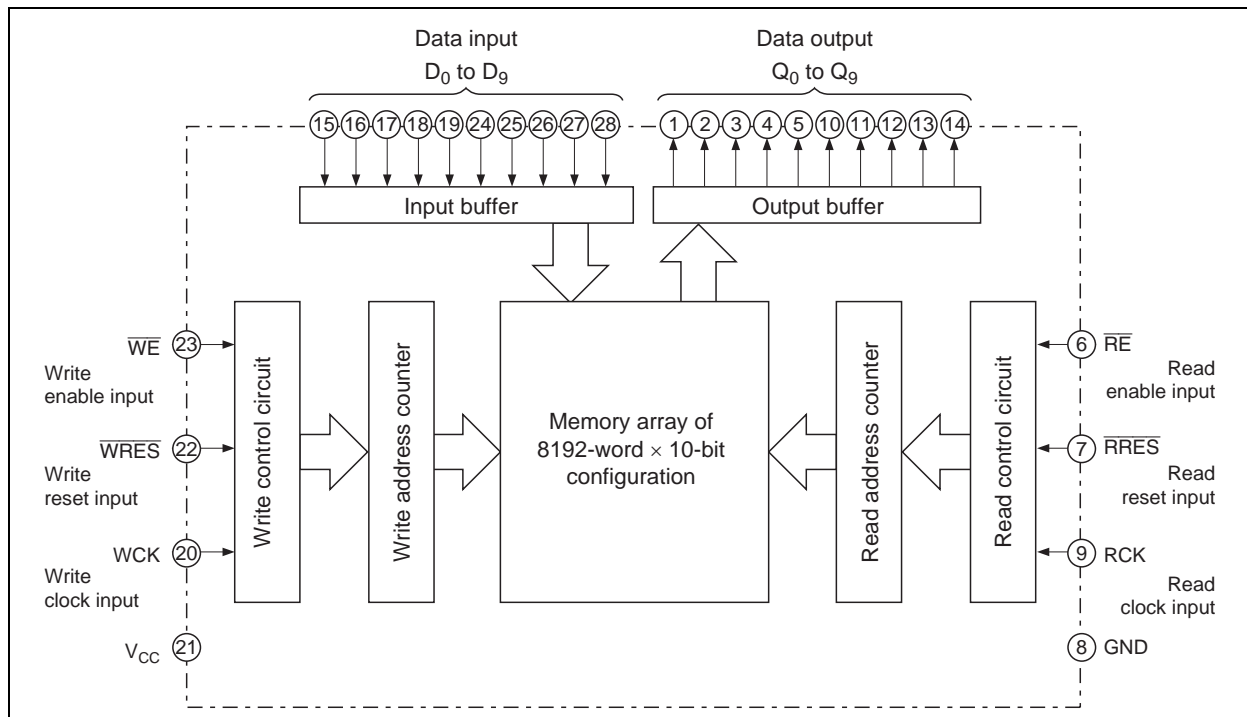
### Features

- Memory configuration: 8192 words × 10 bits (dynamic memory)
- High-speed cycle: 30 ns (Min)
- High-speed access: 25 ns (Max)
- Output hold: 5 ns (Min)
- Fully independent, asynchronous write and read operations
- Variable length delay bit
- Output: 3 states

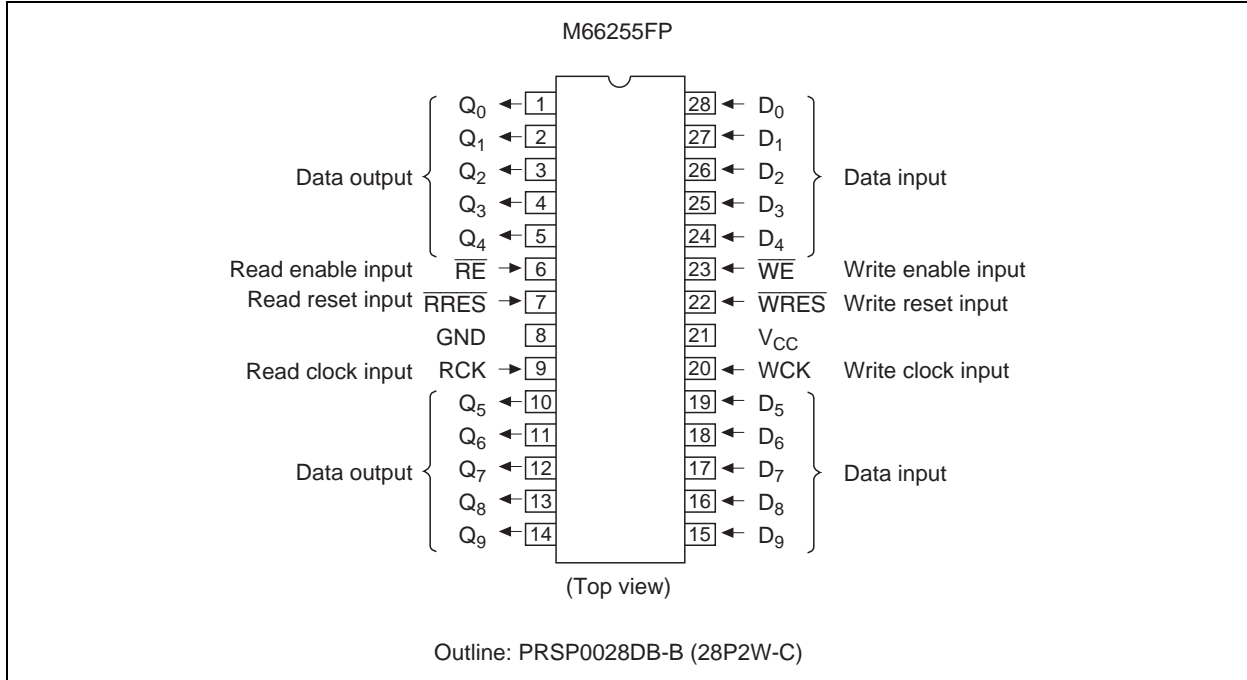
### Application

Digital photocopiers, high-speed facsimile, laser beam printers.

### Block Diagram



Pin Arrangement



## Absolute Maximum Ratings

(Ta = 0 to 70°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	-0.5 to +7.0	V	A value based on GND pin
Input voltage	V <sub>I</sub>	-0.5 to V <sub>CC</sub> + 0.5	V	
Output voltage	V <sub>O</sub>	-0.5 to V <sub>CC</sub> + 0.5	V	
Power dissipation	P <sub>d</sub>	825*	mW	Ta = 25°C
Storage temperature	T <sub>stg</sub>	-65 to 150	°C	

Note: \* Ta ≥ 40°C are derated at -9.7 mW / °C

## Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5	5.5	V
Supply voltage	GND	—	0	—	V
Operating ambient temperature	T <sub>opr</sub>	0	—	70	°C

## Electrical Characteristics

(Ta = 0 to 70°C, V<sub>CC</sub> = 5 V ± 10%, GND = 0 V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
"H" input voltage	V <sub>IH</sub>	2.0	—	—	V	
"L" input voltage	V <sub>IL</sub>	—	—	0.8	V	
"H" output voltage	V <sub>OH</sub>	V <sub>CC</sub> - 0.8	—	—	V	I <sub>OH</sub> = -4 mA
"L" output voltage	V <sub>OL</sub>	—	—	0.55	V	I <sub>OL</sub> = 4 mA
"H" input current	I <sub>IH</sub>	—	—	1.0	μA	V <sub>I</sub> = V <sub>CC</sub> WE, WRES, WCK, RE, RRES, RCK, D <sub>0</sub> to D <sub>9</sub>
"L" input current	I <sub>IL</sub>	—	—	-1.0	μA	V <sub>I</sub> = GND WE, WRES, WCK, RE, RRES, RCK, D <sub>0</sub> to D <sub>9</sub>
Off state "H" output current	I <sub>OZH</sub>	—	—	5.0	μA	V <sub>O</sub> = V <sub>CC</sub>
Off state "L" output current	I <sub>OZL</sub>	—	—	-5.0	μA	V <sub>O</sub> = GND
Operating mean current dissipation	I <sub>CC</sub>	—	—	150	mA	V <sub>I</sub> = V <sub>CC</sub> , GND, Output open t <sub>WCK</sub> , t <sub>RCK</sub> = 30 ns
Input capacitance	C <sub>I</sub>	—	—	10	pF	f = 1 MHz
Off state output capacitance	C <sub>O</sub>	—	—	15	pF	f = 1 MHz

## Function

When write enable input  $\overline{WE}$  is "L", the contents of data inputs D<sub>0</sub> to D<sub>9</sub> are written into memory in synchronization with rise edge of write clock input WCK. At this time, the write address counter is also incremented simultaneously.

The write functions given below are also performed in synchronization with rise edge of WCK.

When  $\overline{WE}$  is "H", a write operation to memory is inhibited and the write address counter is stopped.

When write reset input  $\overline{WRES}$  is "L", the write address counter is initialized.

When read enable input  $\overline{RE}$  is "L", the contents of memory are output to data outputs Q<sub>0</sub> to Q<sub>9</sub> in synchronization with rise edge of read clock input RCK. At this time, the read address counter is also incremented simultaneously.

The read functions given below are also performed in synchronization with rise edge of RCK.

When  $\overline{RE}$  is "H", a read operation from memory is inhibited and the read address counter is stopped. The outputs are in the high impedance state.

When read reset input  $\overline{RRES}$  is "L", the read address counter is initialized.

## Switching Characteristics

(Ta = 0 to 70°C, V<sub>CC</sub> = 5 V ± 10%, GND = 0 V)

Item	Symbol	Min	Typ	Max	Unit
Access time	t <sub>AC</sub>	—	—	25	ns
Output hold time	t <sub>OH</sub>	5	—	—	ns
Output enable time	t <sub>OEN</sub>	5	—	25	ns
Output disable time	t <sub>ODIS</sub>	5	—	25	ns

## Timing Conditions

(Ta = 0 to 70°C, V<sub>CC</sub> = 5 V ± 10%, GND = 0 V, unless otherwise noted)

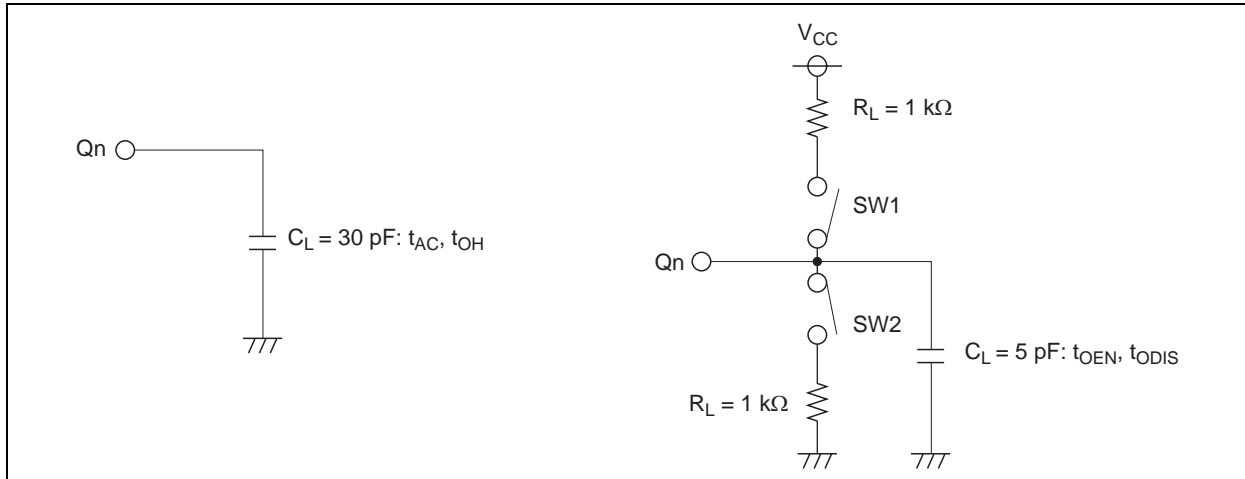
Item	Symbol	Min	Typ	Max	Unit
Write clock (WCK) cycle	t <sub>WCK</sub>	30	—	—	ns
Write clock (WCK) "H" pulse width	t <sub>WCKH</sub>	12	—	—	ns
Write clock (WCK) "L" pulse width	t <sub>WCKL</sub>	12	—	—	ns
Read clock (RCK) cycle	t <sub>RCK</sub>	30	—	—	ns
Read clock (RCK) "H" pulse width	t <sub>RCKH</sub>	12	—	—	ns
Read clock (RCK) "L" pulse width	t <sub>RCKL</sub>	12	—	—	ns
Input data setup time to WCK	t <sub>DS</sub>	5	—	—	ns
Input data hold time to WCK	t <sub>DH</sub>	5	—	—	ns
Reset setup time to WCK or RCK	t <sub>RESS</sub>	5	—	—	ns
Reset hold time to WCK or RCK	t <sub>RESH</sub>	5	—	—	ns
Reset nonselect setup time to WCK or RCK	t <sub>NRESS</sub>	5	—	—	ns
Reset nonselect hold time to WCK or RCK	t <sub>NRESH</sub>	5	—	—	ns
$\overline{WE}$ setup time to WCK	t <sub>WES</sub>	5	—	—	ns
$\overline{WE}$ hold time to WCK	t <sub>WEH</sub>	5	—	—	ns
$\overline{WE}$ nonselect setup time to WCK	t <sub>NWES</sub>	5	—	—	ns
$\overline{WE}$ nonselect hold time to WCK	t <sub>NWEH</sub>	5	—	—	ns
$\overline{RE}$ setup time to RCK	t <sub>RES</sub>	5	—	—	ns
$\overline{RE}$ hold time to RCK	t <sub>REH</sub>	5	—	—	ns
$\overline{RE}$ nonselect setup time to RCK	t <sub>NRES</sub>	5	—	—	ns
$\overline{RE}$ nonselect hold time to RCK	t <sub>NREH</sub>	5	—	—	ns
Input pulse rise/fall time	t <sub>r</sub> , t <sub>f</sub>	—	—	20	ns
Data hold time*	t <sub>H</sub>	—	—	20	ms

Notes: Perform reset operation after turning on power supply.

\* For 1-line access, the following should be satisfied:

 $\overline{WE}$  "H" level period ≤ 20 ms – 8192 t<sub>WCK</sub> –  $\overline{WRES}$  "L" level period $\overline{RE}$  "H" level period ≤ 20 ms – 8192 t<sub>RCK</sub> –  $\overline{RRES}$  "L" level period

## Test Circuit



Input pulse level: 0 to 3 V

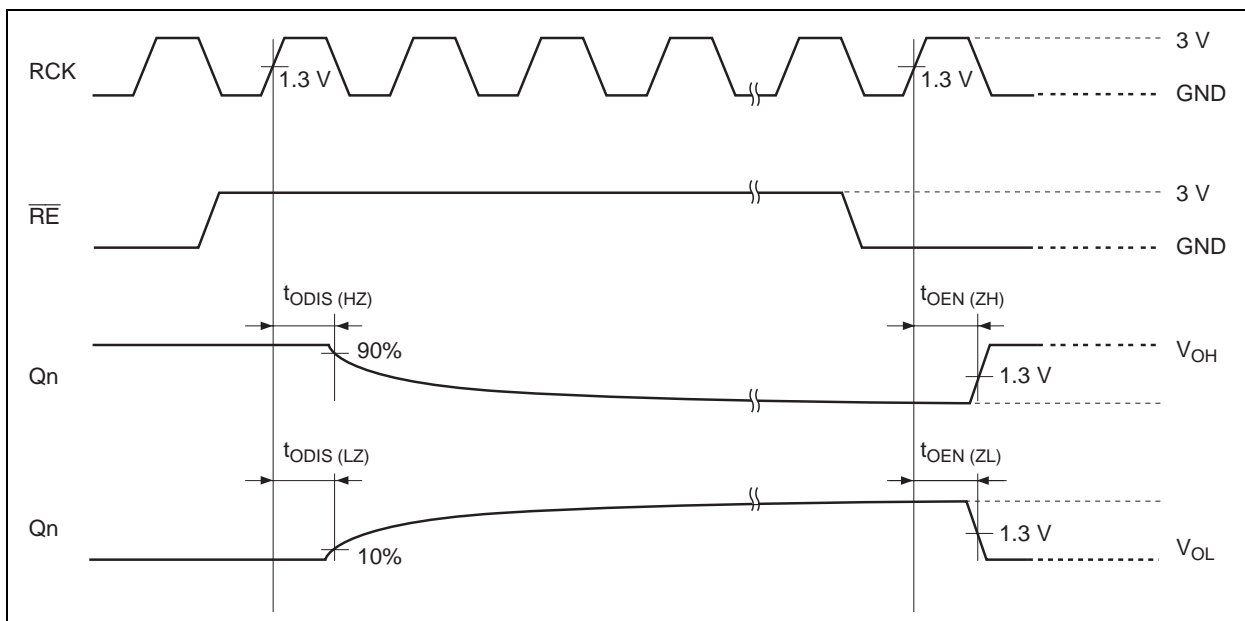
Input pulse rise/fall time: 3 ns

Decision voltage input: 1.3 V

Decision voltage output: 1.3 V (However,  $t_{ODIS(LZ)}$  is 10% of output amplitude and  $t_{ODIS(HZ)}$  is 90% of that for decision)

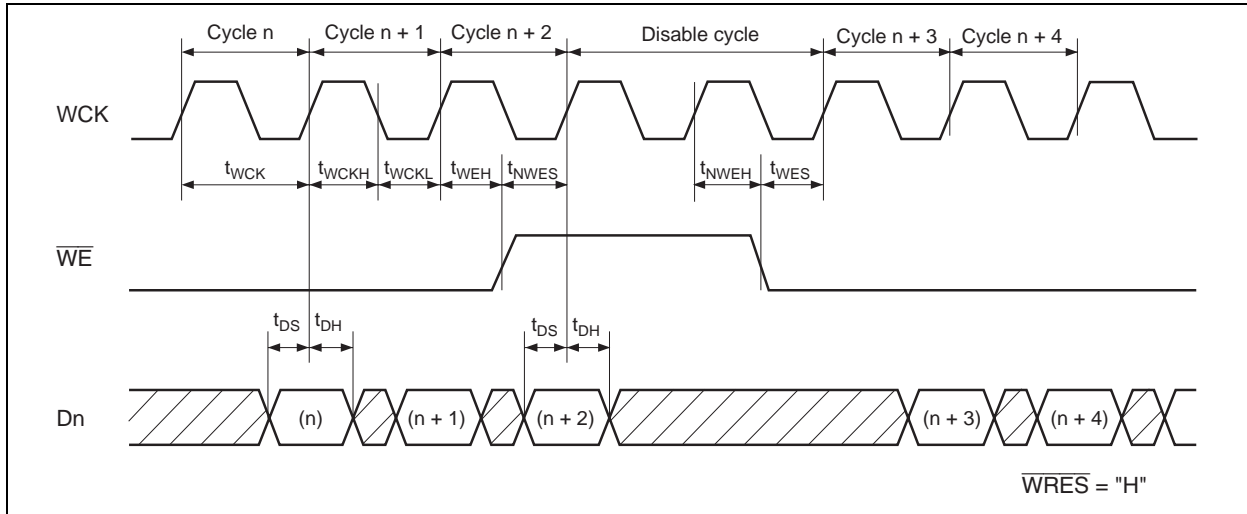
The load capacitance  $C_L$  includes the floating capacitance of connection and the input capacitance of probe.

Parameter	SW1	SW2
$t_{ODIS(LZ)}$	Closed	Open
$t_{ODIS(HZ)}$	Open	Closed
$t_{OEN(ZL)}$	Closed	Open
$t_{OEN(ZH)}$	Open	Closed

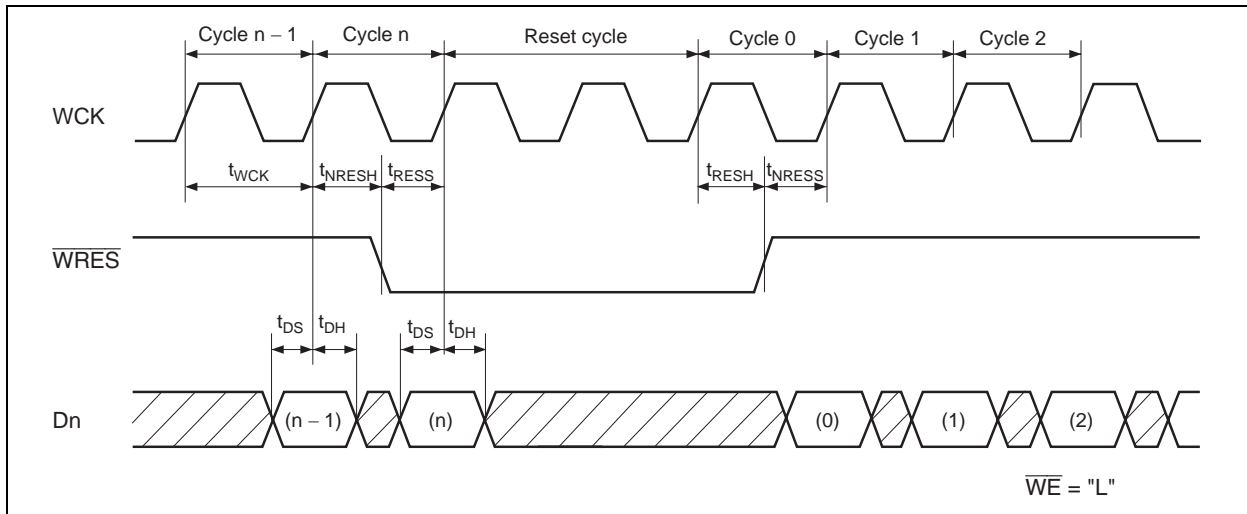
 $t_{ODIS}/t_{OEN}$  Test Condition

## Operating Timing

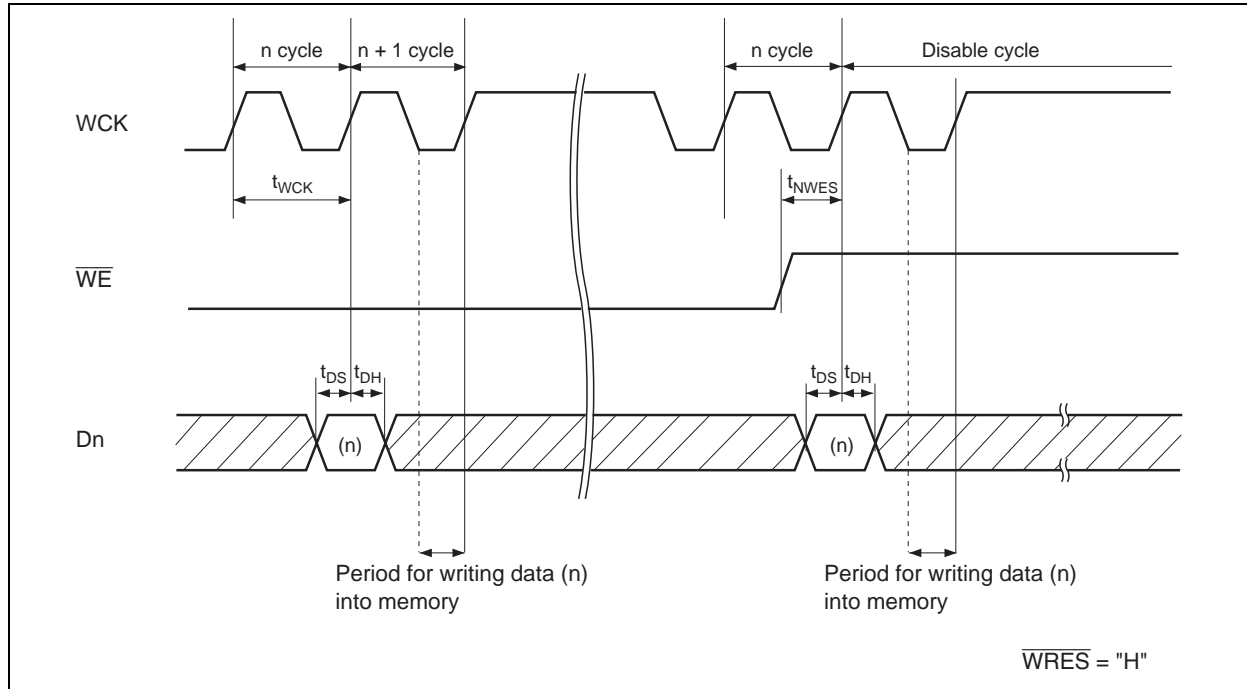
### Write Cycle



### Write Reset Cycle



## Matters that Needs Attention when WCK Stops

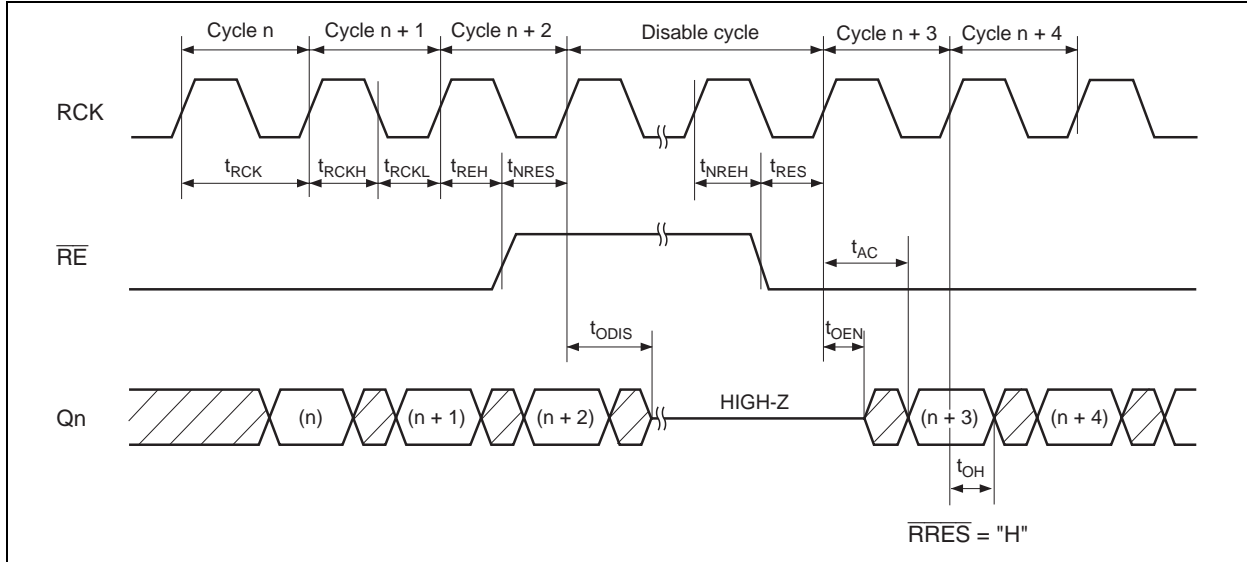


Input data of n cycle is read at the rising edge after WCK of n cycle and writing operation starts in the WCK low-level period of n + 1 cycle. The writing operation is complete at the falling edge after n + 1 cycle.

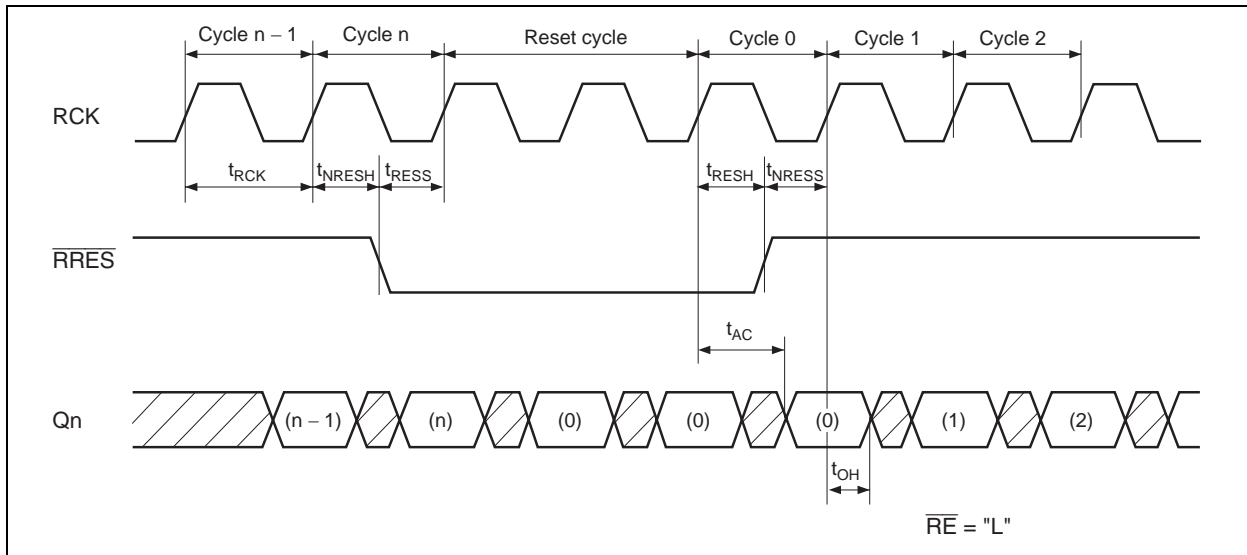
To stop reading write data at n cycle, enter WCK before the rising edge after n + 1 cycle.

When the cycle next to n cycle is a disable cycle, WCK for a cycle requires to be entered after the disable cycle as well.

Read Cycle



Read Reset Cycle

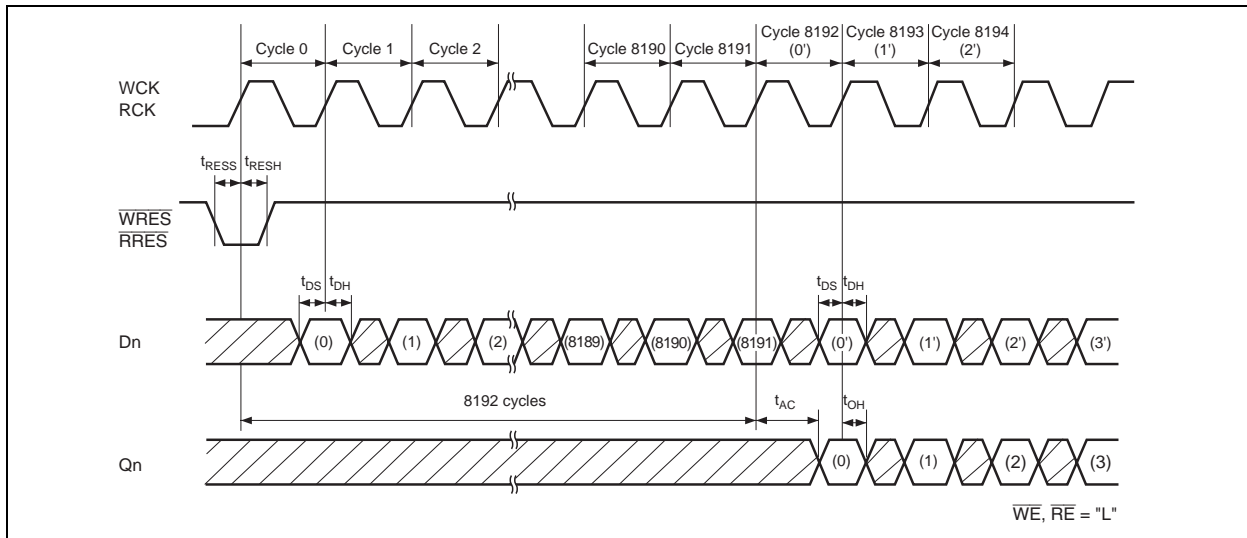




## Variable Length Delay Bits

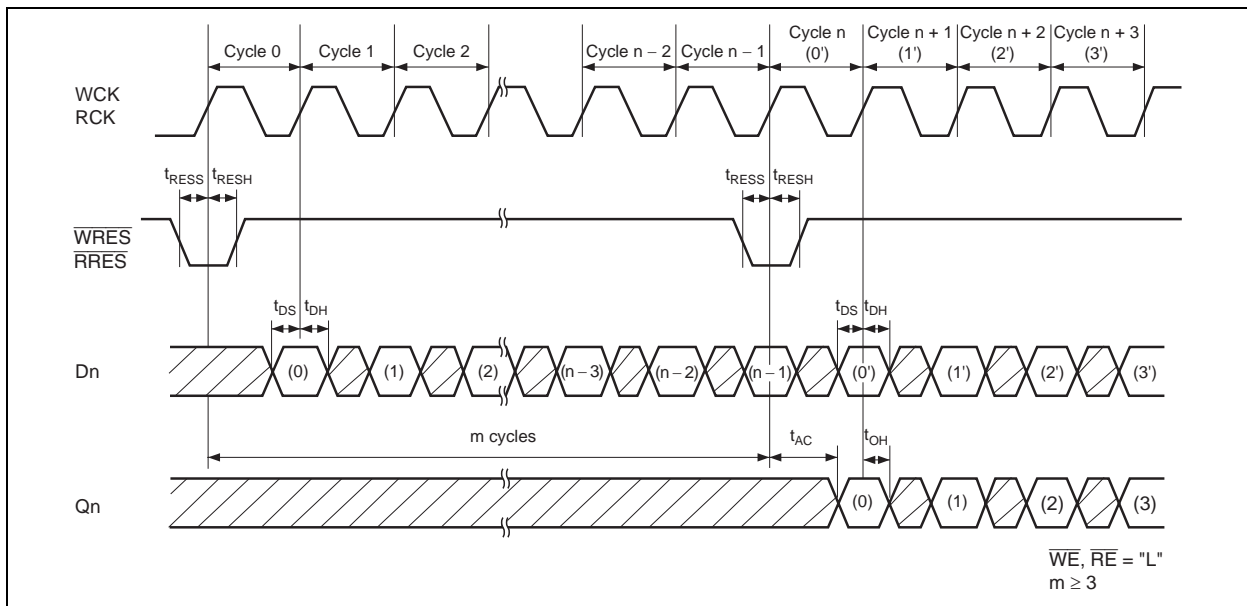
### 1-line (8192 Bits) Delay

A write input data is written into memory at the second rise edge of WCK in the cycle, and a read output data is output from memory at the first rise edge of RCK in the cycle, so that 1-line delay can be made easily.



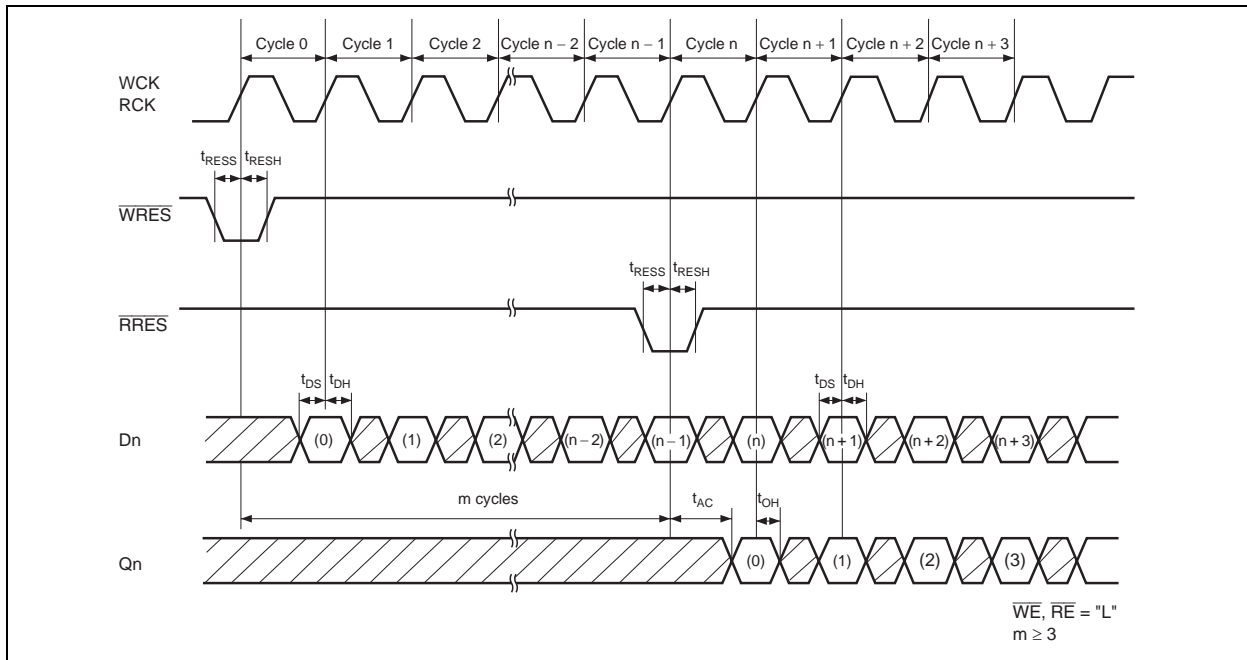
### N-bit Delay Bit

(Making a reset at a cycle corresponding to delay length)



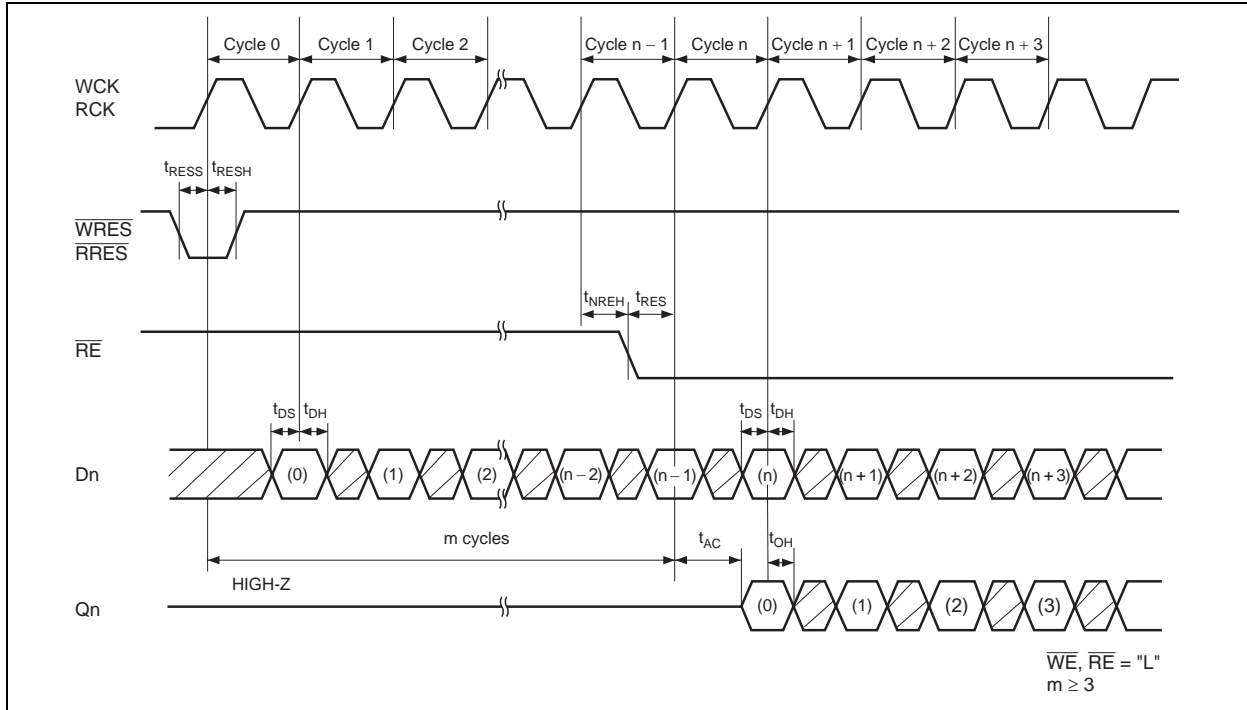
### N-bit Delay 2

(Sliding  $\overline{WRES}$  and  $\overline{RRES}$  at a cycle corresponding to delay length)



### N-bit Delay 3

(Disabling  $\overline{RE}$  at a cycle corresponding to delay length)

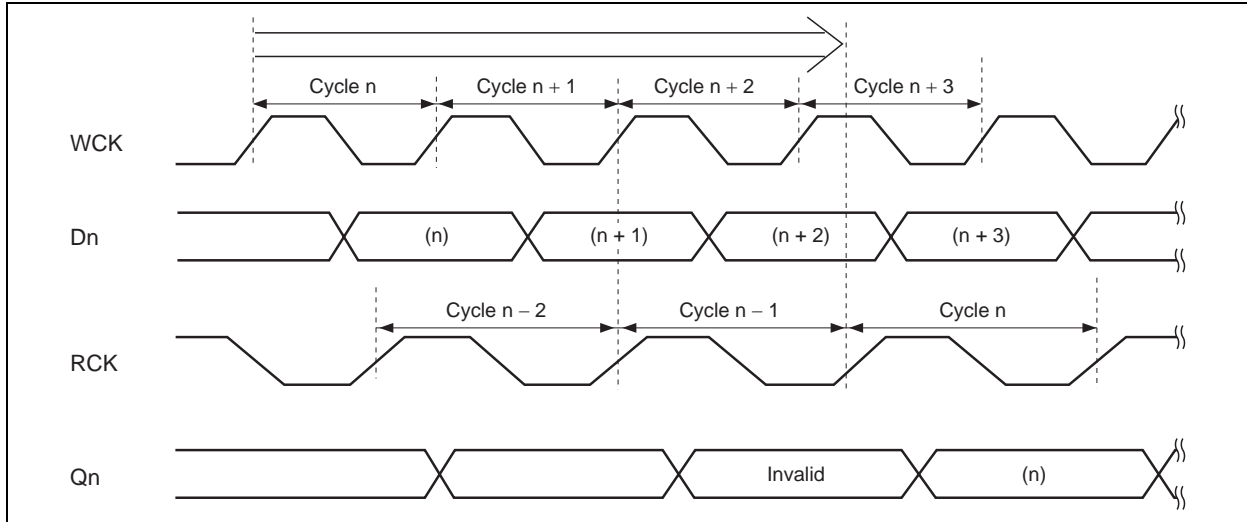


### Shortest Read of Data "n" Written in Cycle n

(Cycle  $n - 1$  on read side should be started after end of cycle  $n + 1$  on write side)

When the start of cycle  $n - 1$  on read side is earlier than the end of cycle  $n + 1$  on write side, output  $Q_n$  of cycle  $n$  becomes invalid.

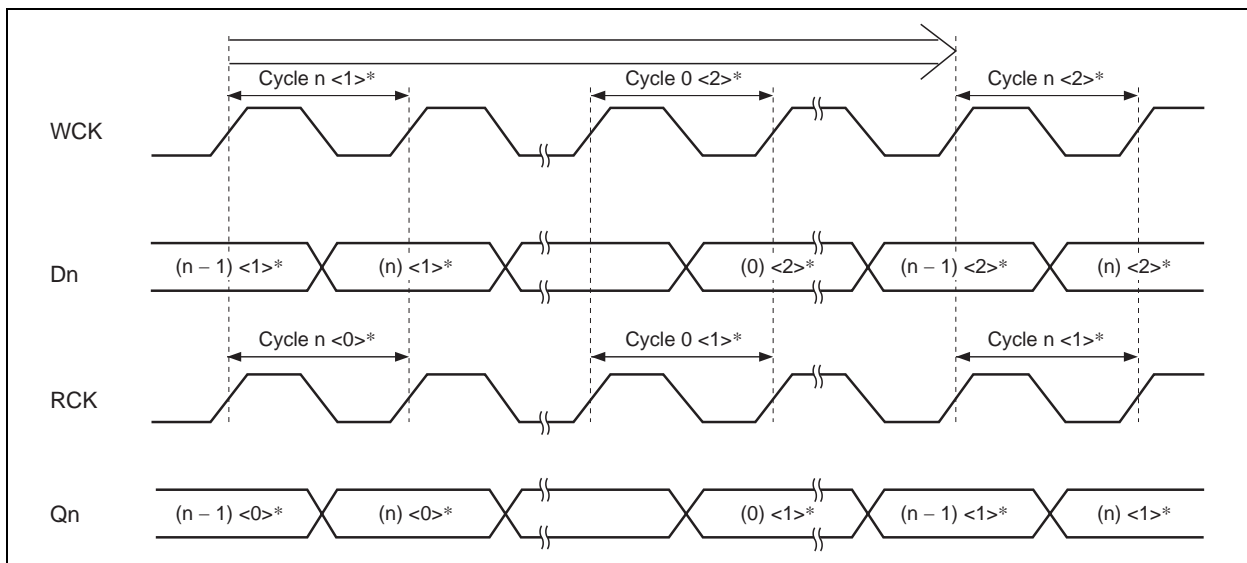
In the figure shown below, the read of cycle  $n - 1$  is invalid.



### Longest Read of Data "n" Written in Cycle n: 1-line Delay

(Cycle  $n <1>^*$  on read side should be started when cycle  $n <2>^*$  on write is started)

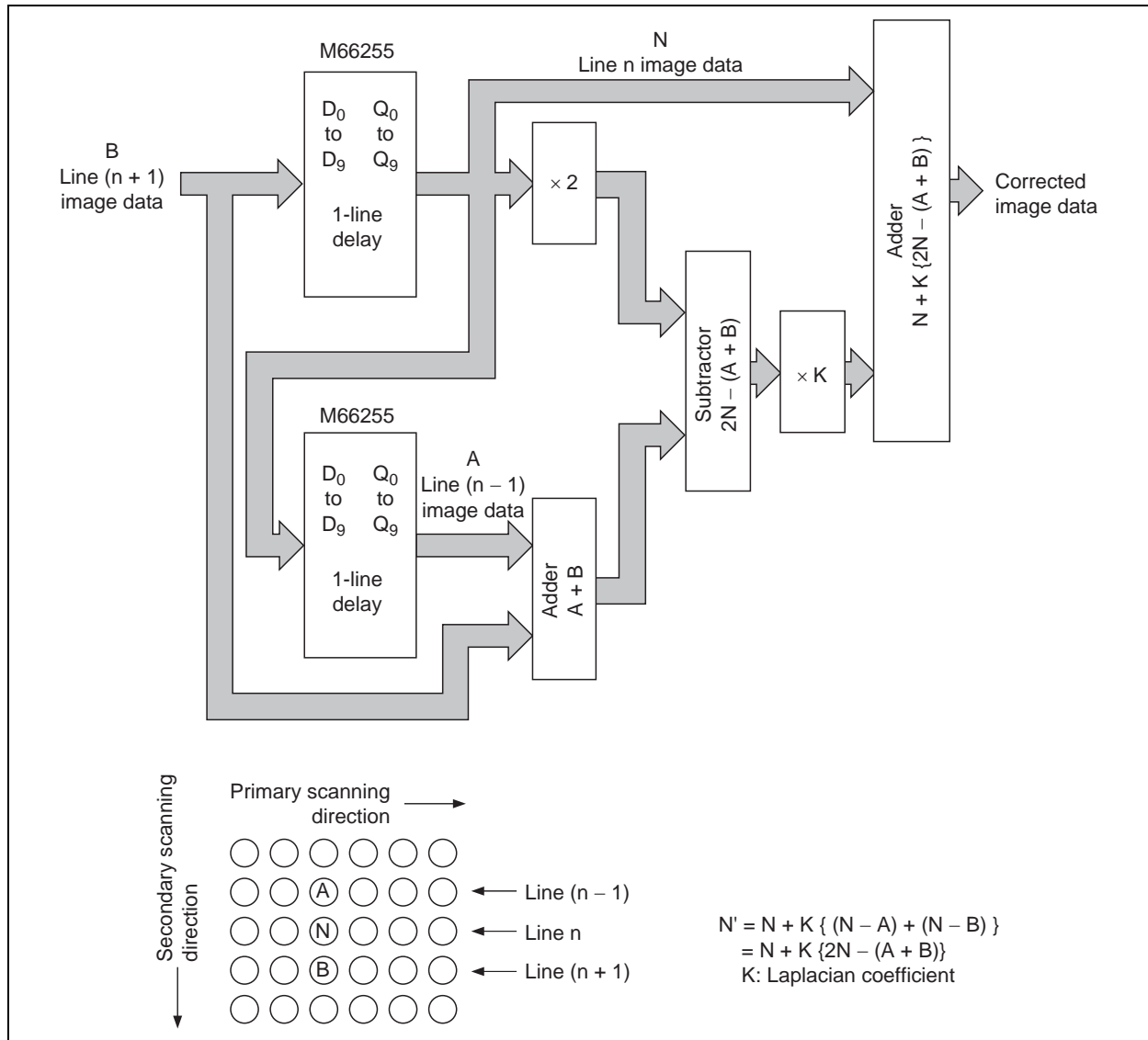
Output  $Q_n$  of  $n$  cycle  $<1>^*$  can be read until the start of reading side  $n$  cycle  $<1>^*$  and the start of writing side  $n$  cycle  $<2>^*$  overlap each other.



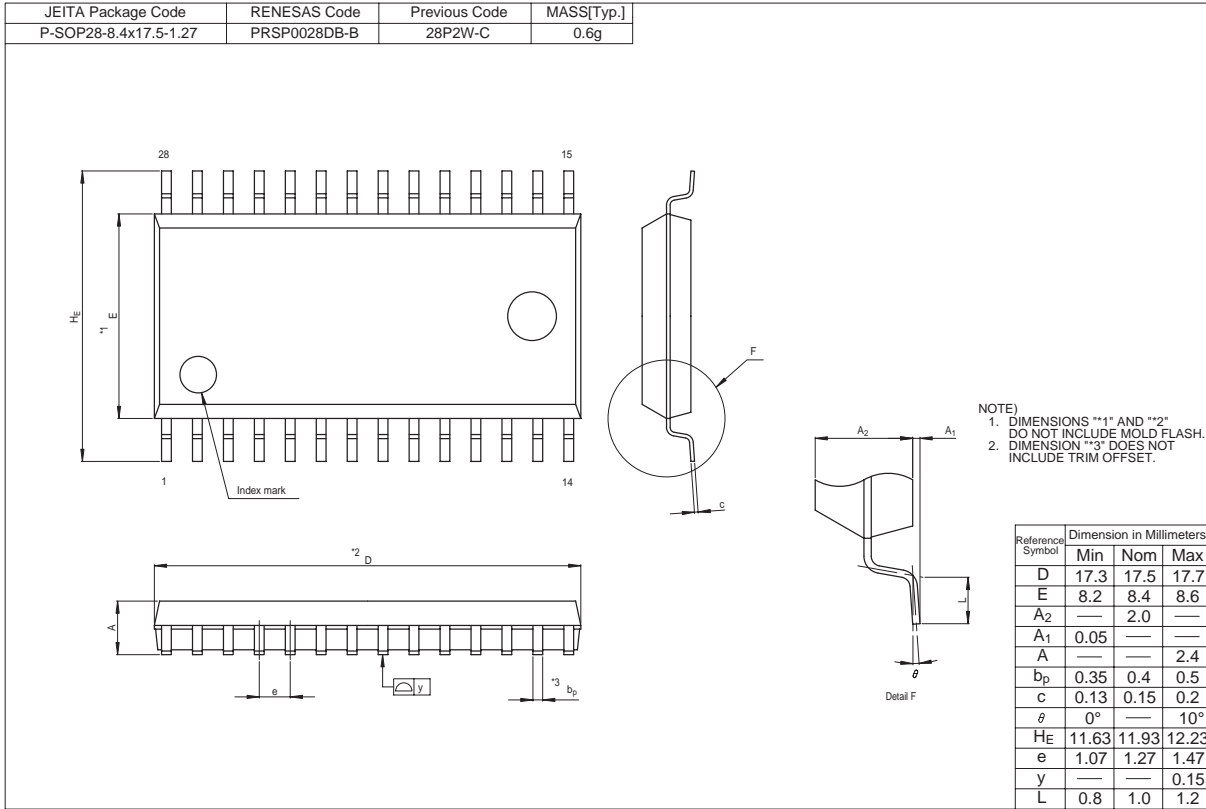
Note:  $<0>^*$ ,  $<1>^*$  and  $<2>^*$  indicates a line value.

## Application Example

### Laplacian Filter Circuit for Correction of Resolution in the Secondary Scanning Direction



Package Dimensions



Notes:

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