M66257FP

5120 × 8-Bit × 2 Line Memory (FIFO)

REJ03F0251-0200
Rev.2.00
Sep 14, 2007

Description

The M66257FP is a high-speed line memory with a FIFO (First In First Out) structure of 5120-word × 8-bit double configuration which uses high-performance silicon gate CMOS process technology.

It allows simultaneous output of 1-line delay data and 2-line delay data, and is most suitable for data correction over multiple lines.

It has separate clock, enable and reset signals for write and read, and is most suitable as a buffer memory between devices with different data processing throughput.

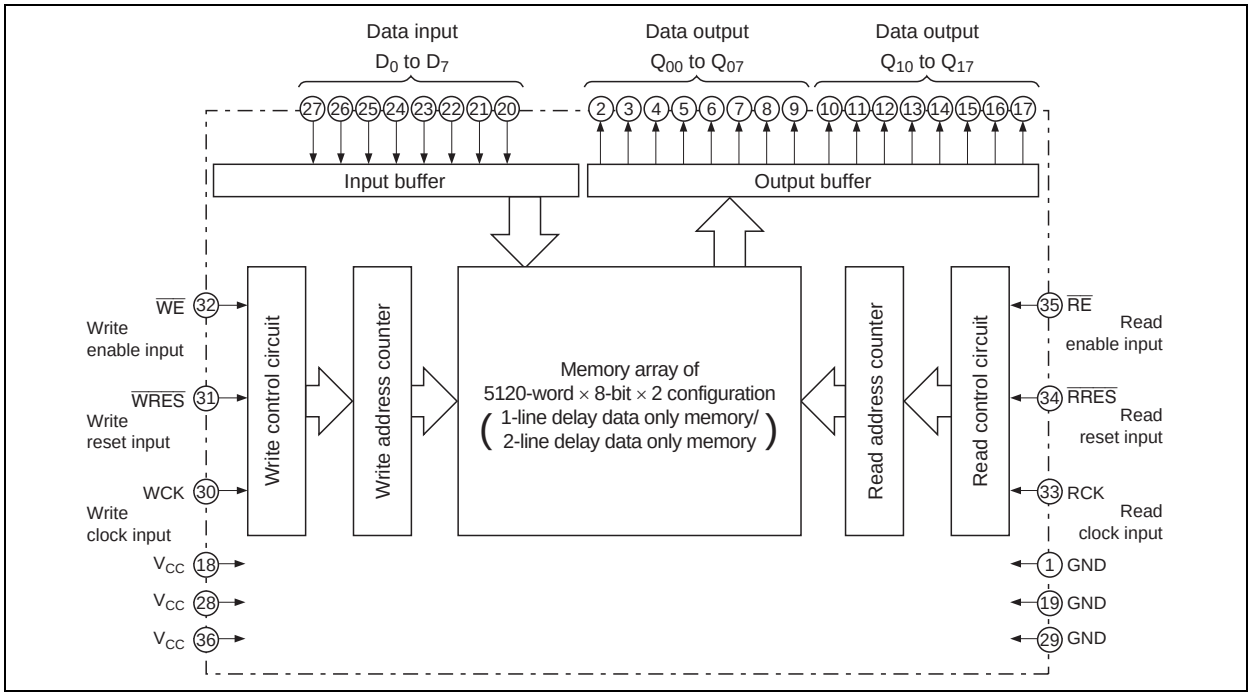
Features

- Memory configuration: 5120 words × 8 bits × 2 (dynamic memory)
- High-speed cycle: 25 ns (Min)
- High-speed access: 18 ns (Max)
- Output hold: 3 ns (Min)
- Fully independent, asynchronous write and read operations
- Output: 3 states
- Q_{00} to Q_{07}: 1-line delay
- Q_{10} to Q_{17}: 2-line delay

Application

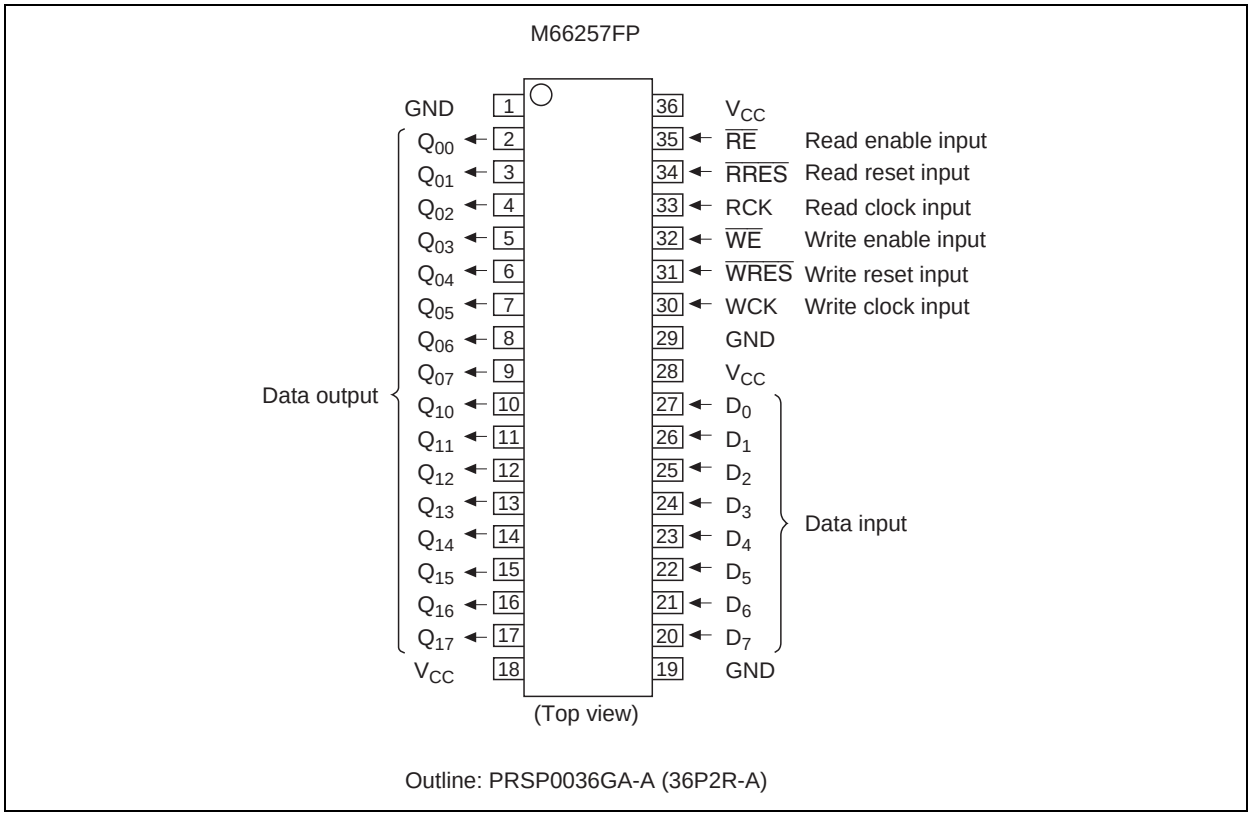
Digital photocopiers, high-speed facsimile, laser beam printers.

Block Diagram



Downloaded from Elcodis.com electronic components distributor

Pin Arrangement



Outline: PRSP0036GA-A (36P2R-A)

Downloaded from Elcodis.com electronic components distributor

Absolute Maximum Ratings

(Ta = 0 to 70°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to +7.0	V	A value based on GND pin
Input voltage	V_I	–0.5 to V_{CC} + 0.5	V	
Output voltage	V_O	–0.5 to V_{CC} + 0.5	V	
Power dissipation	Pd	660	mW	Ta = 25°C
Storage temperature	Tstg	–65 to 150	°C	

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5	5.5	V
Supply voltage	GND	—	0	—	V
Operating ambient temperature	Topr	0	—	70	°C

Electrical Characteristics

(Ta = 0 to 70°C, V_{CC} = 5 V ± 10%, GND = 0 V, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
"H" input voltage	V_{IH}	2.0	—	—	V		
"L" input voltage	V_{IL}	—	—	0.8	V		
"H" output voltage	V_{OH}	V_{CC} – 0.8	—	—	V	I_{OH} = –4 mA	
"L" output voltage	V_{OL}	—	—	0.55	V	I_{OL} = 4 mA	
"H" input current	I_{IH}	—	—	1.0	µA	$V_I = V_{CC}$	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK, D_0 to D_7
"L" input current	I_{IL}	—	—	–1.0	µA	V_I = GND	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK, D_0 to D_7
Off state "H" output current	I_{OZH}	—	—	5.0	µA	$V_O = V_{CC}$	
Off state "L" output current	I_{OZL}	—	—	–5.0	µA	V_O = GND	
Operating mean current dissipation	I_{CC}	—	—	120	mA	$V_I = V_{CC}$, GND, Output open t_{WCK}, t_{RCK} = 25 ns	
Input capacitance	C_I	—	—	10	pF	f = 1 MHz	
Off state output capacitance	C_O	—	—	15	pF	f = 1 MHz	

Downloaded from Elcodis.com electronic components distributor

Function

When write enable input $\overline{WE}$ is "L", the contents of data inputs D_0 to D_7 are written into 1-line delay data only memory in synchronization with rise edge of write clock input WCK. At this time, the write address counter of 1-line delay data only memory is also incremented simultaneously.

The write functions given below are also performed in synchronization with rise edge of WCK.

When $\overline{WE}$ is "H", a write operation to 1-line delay data only memory is inhibited and the write address counter of 1-line delay data only memory is stopped.

When write reset input $\overline{WRES}$ is "L", the write address counter of 1-line delay data only memory is initialized.

When read enable input $\overline{RE}$ is "L", the contents of 1-line delay data only memory are output to data outputs Q_{00} to Q_{07} and those of 2-line delay data only memory to data outputs Q_{10} to Q_{17} in synchronization with the rise of read clock input RCK. At this time, the read address counters of 1-line and 2-line delay data only memories is also incremented simultaneously.

Moreover, data of Q_{00} to Q_{07} are written into 2-line delay data only memory in synchronization with rise edge of RCK. At this time, the write address of 2-line delay data only memory is incremented.

The read functions given below are also performed in synchronization with rise edge of RCK.

When $\overline{RE}$ is "H", a read operation from both of 1-line delay data only memory and 2-line delay data only memory is inhibited and the read address counter of each memory is stopped. The outputs of Q_{00} to Q_{07} and Q_{10} to Q_{17} are in the high impedance state.

Moreover, a write operation to 2-line delay data only memory is inhibited and the write address counter of 2-line delay data only memory is stopped.

When read reset input $\overline{RRES}$ is "L", the read address counter of 1-line delay data only memory, and the write address counter and read address counter of 2-line delay data only memory are initialized.

Downloaded from Elcodis.com electronic components distributor

Switching Characteristics

(Ta = 0 to 70°C, V_{CC} = 5 V ± 10%, GND = 0 V, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit
Access time	t_{AC}	—	—	18	ns
Output hold time	t_{OH}	3	—	—	ns
Output enable time	t_{OEN}	3	—	18	ns
Output disable time	t_{ODIS}	3	—	18	ns

Timing Conditions

(Ta = 0 to 70°C, V_{CC} = 5 V ± 10%, GND = 0 V, unless otherwise noted)

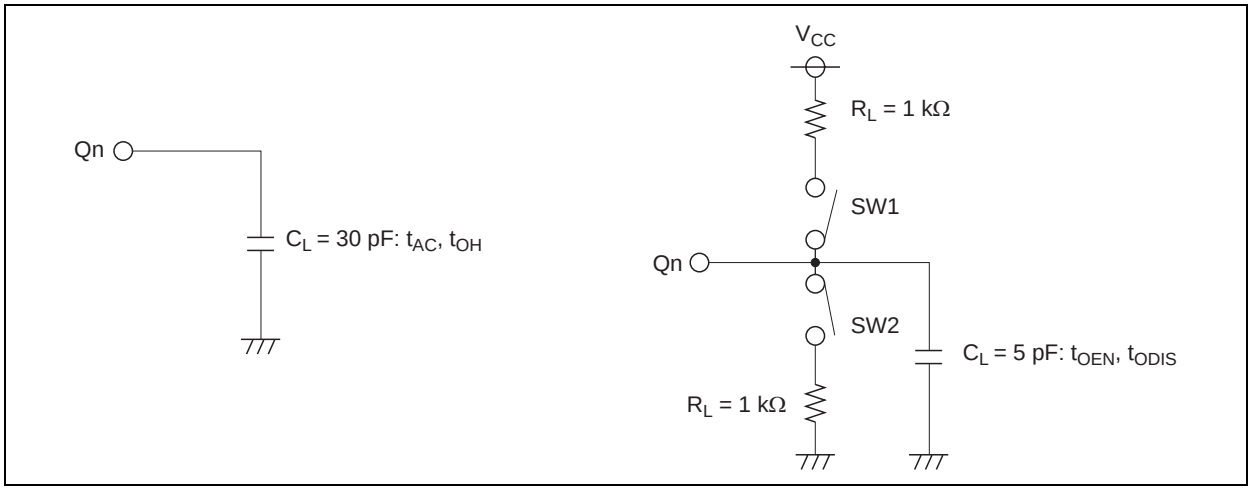
Item	Symbol	Min	Typ	Max	Unit
Write clock (WCK) cycle	t_{WCK}	25	—	—	ns
Write clock (WCK) "H" pulse width	t_{WCKH}	11	—	—	ns
Write clock (WCK) "L" pulse width	t_{WCKL}	11	—	—	ns
Read clock (RCK) cycle	t_{RCK}	25	—	—	ns
Read clock (RCK) "H" pulse width	t_{RCKH}	11	—	—	ns
Read clock (RCK) "L" pulse width	t_{RCKL}	11	—	—	ns
Input data setup time to WCK	t_{DS}	7	—	—	ns
Input data hold time to WCK	t_{DH}	3	—	—	ns
Reset setup time to WCK or RCK	t_{RESS}	7	—	—	ns
Reset hold time to WCK or RCK	t_{RESH}	3	—	—	ns
Reset nonselect setup time to WCK or RCK	t_{NRESS}	7	—	—	ns
Reset nonselect hold time to WCK or RCK	t_{NRESH}	3	—	—	ns
$\overline{WE}$ setup time to WCK	t_{WES}	7	—	—	ns
$\overline{WE}$ hold time to WCK	t_{WEH}	3	—	—	ns
$\overline{WE}$ nonselect setup time to WCK	t_{NWES}	7	—	—	ns
$\overline{WE}$ nonselect hold time to WCK	t_{NWEH}	3	—	—	ns
$\overline{RE}$ setup time to RCK	t_{RES}	7	—	—	ns
$\overline{RE}$ hold time to RCK	t_{REH}	3	—	—	ns
$\overline{RE}$ nonselect setup time to RCK	t_{NRES}	7	—	—	ns
$\overline{RE}$ nonselect hold time to RCK	t_{NREH}	3	—	—	ns
Input pulse rise/fall time	tr, tf	—	—	20	ns
Data hold time*	t_H	—	—	20	ms

Notes: Reset the IC after power is turned on.

* For 1-line access, the following should be satisfied:
$\overline{WE}$ "H" level period < 20 ms − 5120 t_{WCK} − $\overline{WRES}$ "L" level period
$\overline{RE}$ "H" level period < 20 ms − 5120 t_{RCK} − $\overline{RRES}$ "L" level period

Downloaded from Elcodis.com electronic components distributor

Test Circuit



Input pulse level: 0 to 3 V

Input pulse rise/fall time: 3 ns

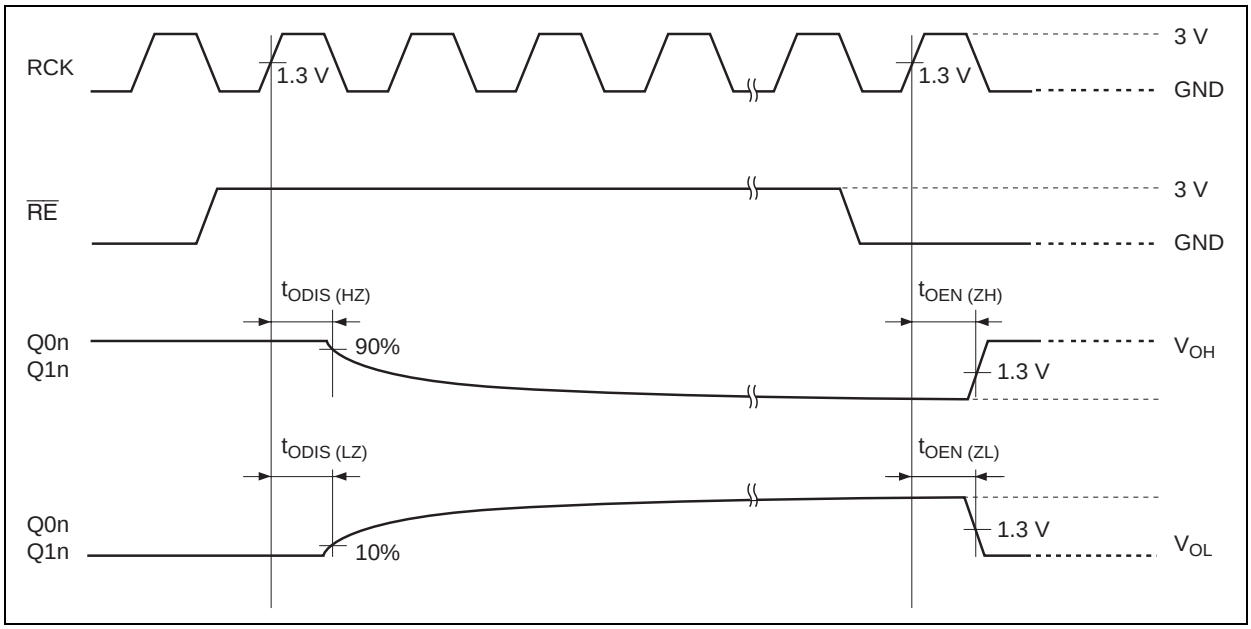
Decision voltage input: 1.3 V

Decision voltage output: 1.3 V (However, $t_{ODIS\ (LZ)}$ is 10% of output amplitude and $t_{ODIS\ (HZ)}$ is 90% of that for decision)

The load capacitance C_L includes the floating capacitance of connection and the input capacitance of probe.

Parameter	SW1	SW2
$t_{ODIS\ (LZ)}$	Closed	Open
$t_{ODIS\ (HZ)}$	Open	Closed
$t_{OEN\ (ZL)}$	Closed	Open
$t_{OEN\ (ZH)}$	Open	Closed

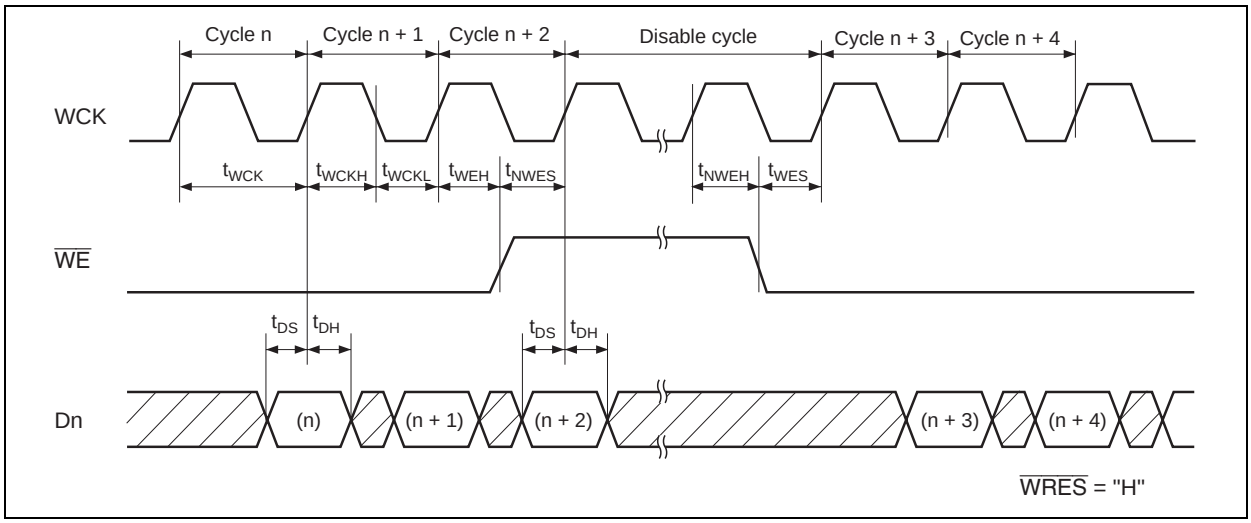
t_{ODIS}/t_{OEN} Test Condition



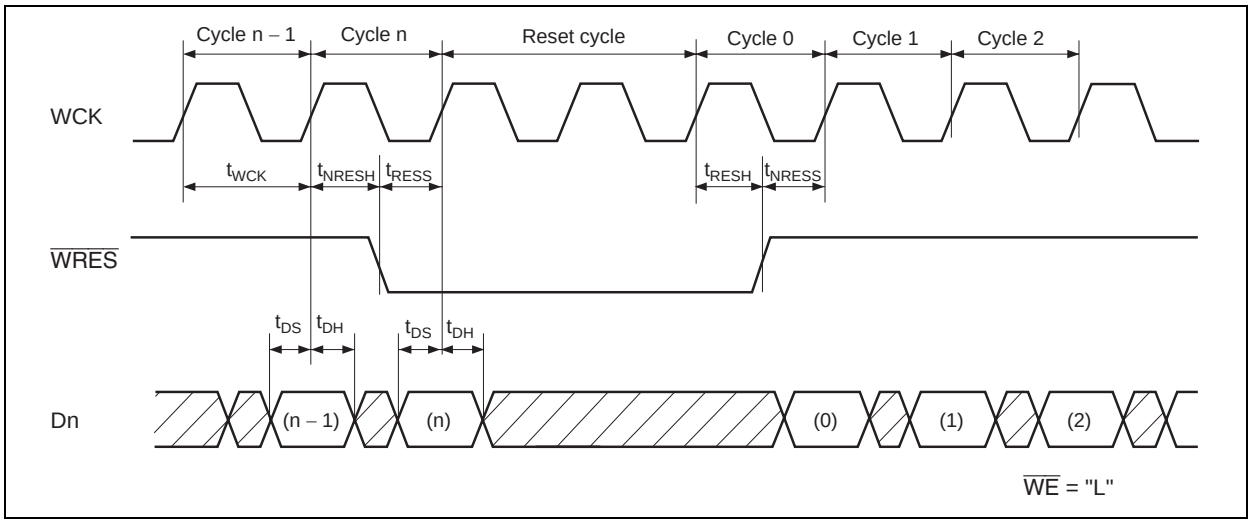
Downloaded from Elcodis.com electronic components distributor

Operating Timing

Write Cycle

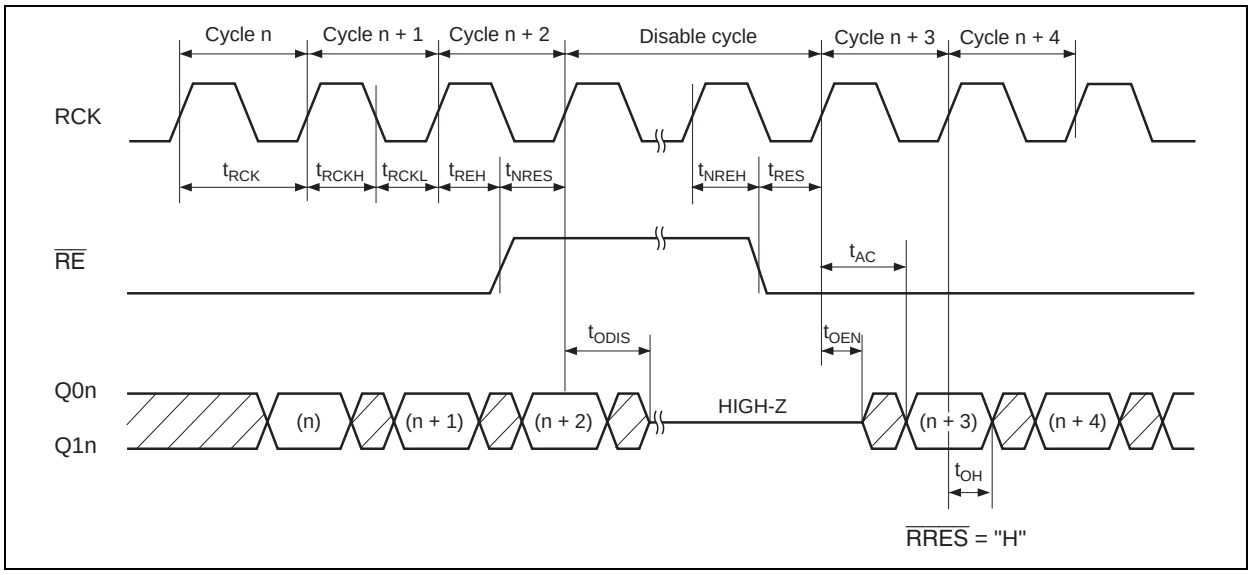


Write Reset Cycle

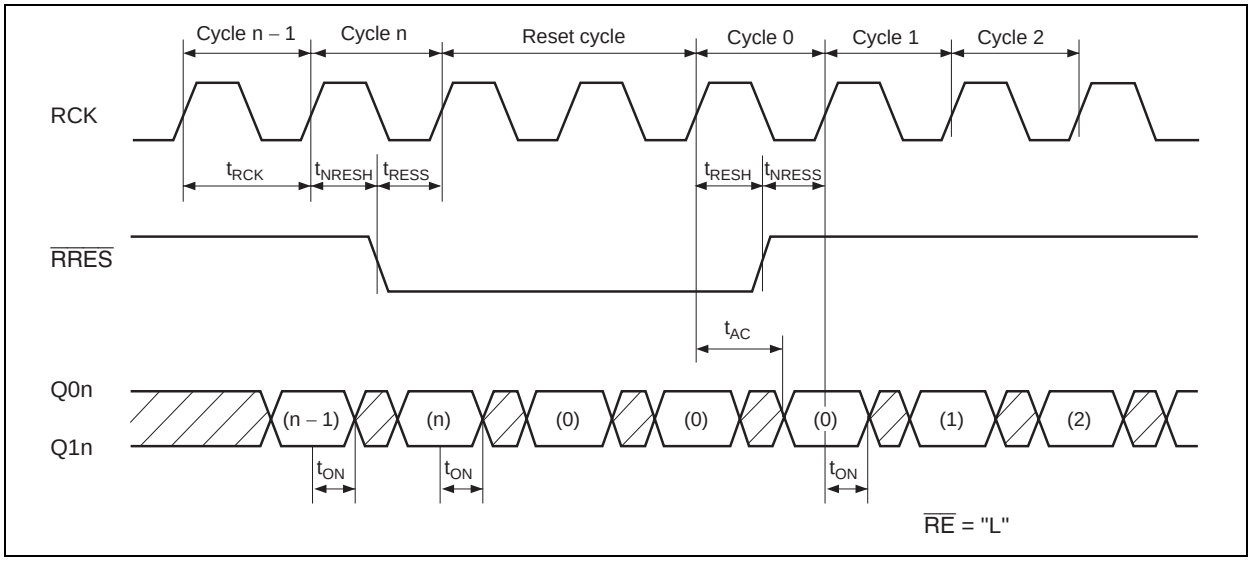


Downloaded from Elcodis.com electronic components distributor

Read Cycle

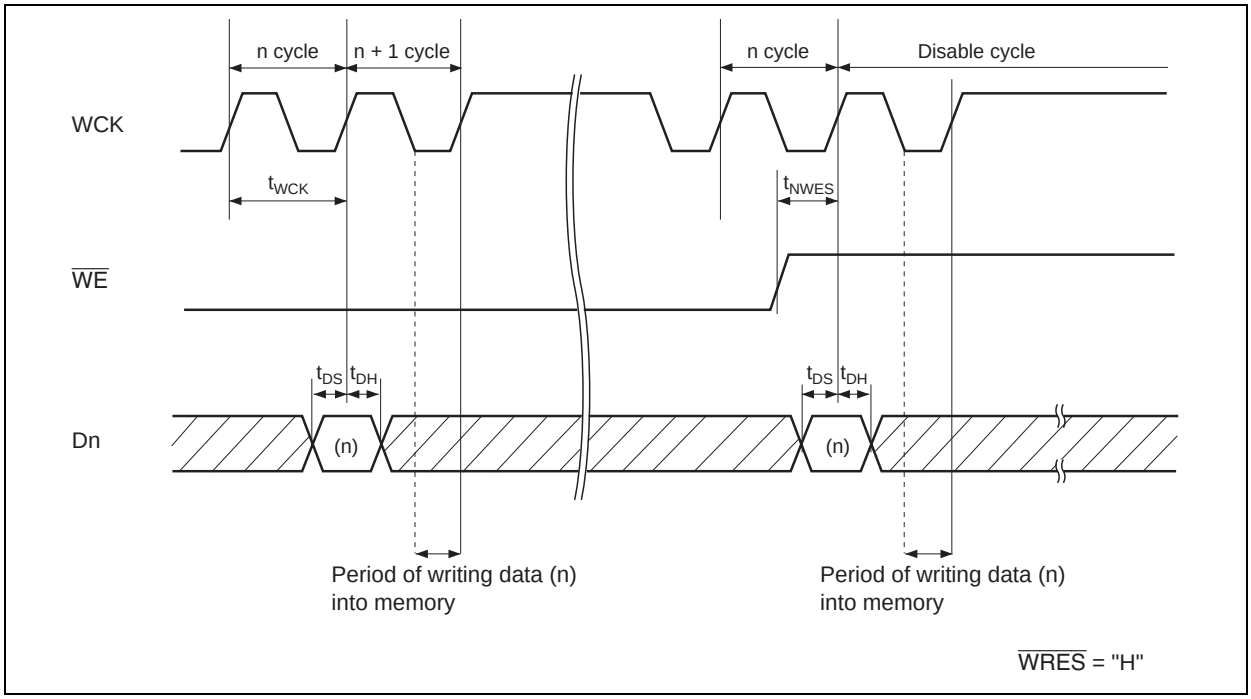


Read Reset Cycle



Downloaded from Elcodis.com electronic components distributor

Note at WCK Stop



Input data Dn of n cycle is read at the rising edge after WCK of n cycle. Writing operation starts in the "L" period of WCK of n + 1 cycle and ends at the rising edge after n + 1 cycle.

To stop reading write data at n cycle, input WCK for up to the rising edge of n + 1 cycle.

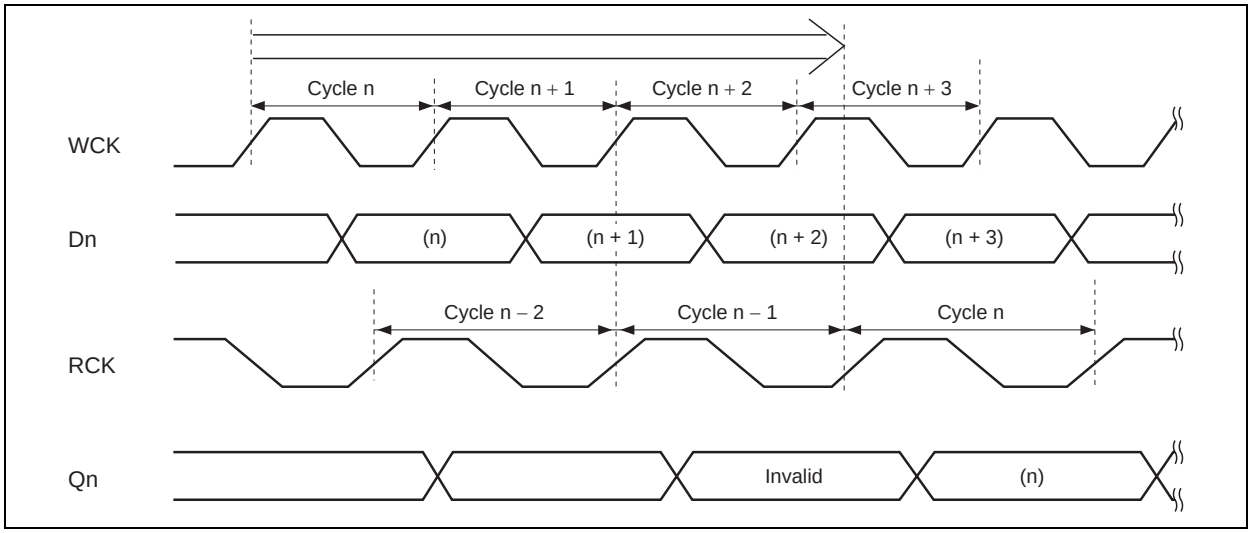
When the cycle next to n cycle is a disable cycle, input of WCK for a cycle is required after a disable cycle as well.

Downloaded from Elcodis.com electronic components distributor

Shortest Read of Data "n" Written in Cycle n

(Cycle n – 1 on read side should be started after end of cycle n + 1 on write side)

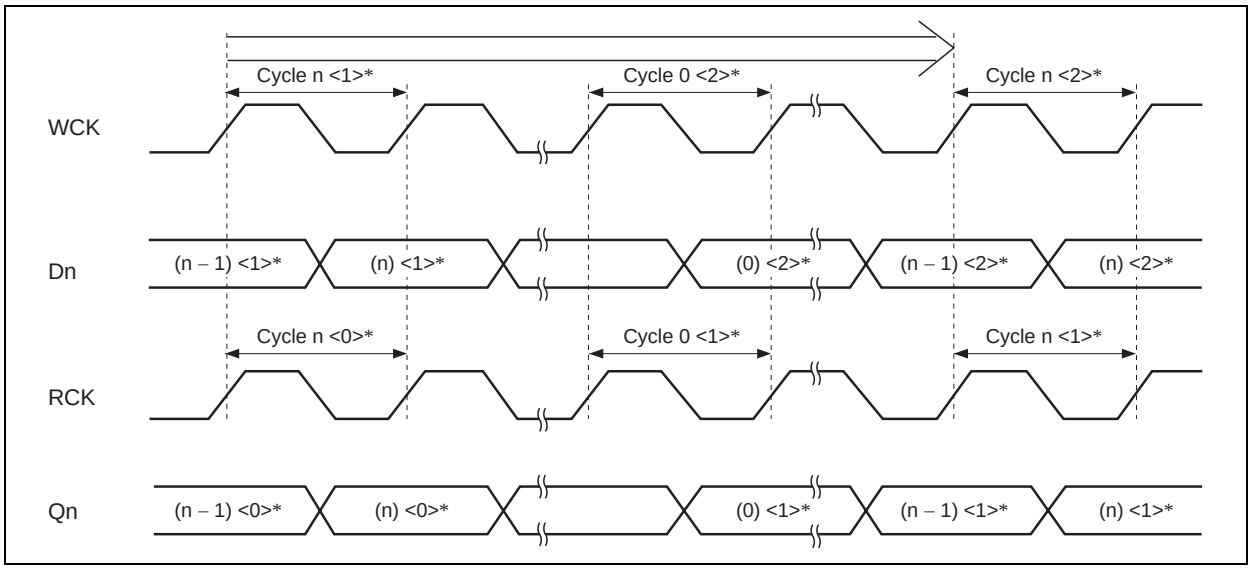
When the start of cycle n – 1 on read side is earlier than the end of cycle n + 1 on write side, output Qn of cycle n becomes invalid. In the figure shown below, the read of cycle n – 1 is invalid.



Longest Read of Data "n" Written in Cycle n: 1-line Delay

(Cycle n <1>* on read side should be started when cycle n <2>* on write is started)

Output Qn of n cycle <1>* can be read until the start of reading side n cycle <1> and the start of writing side n cycle <2>* overlap each other.

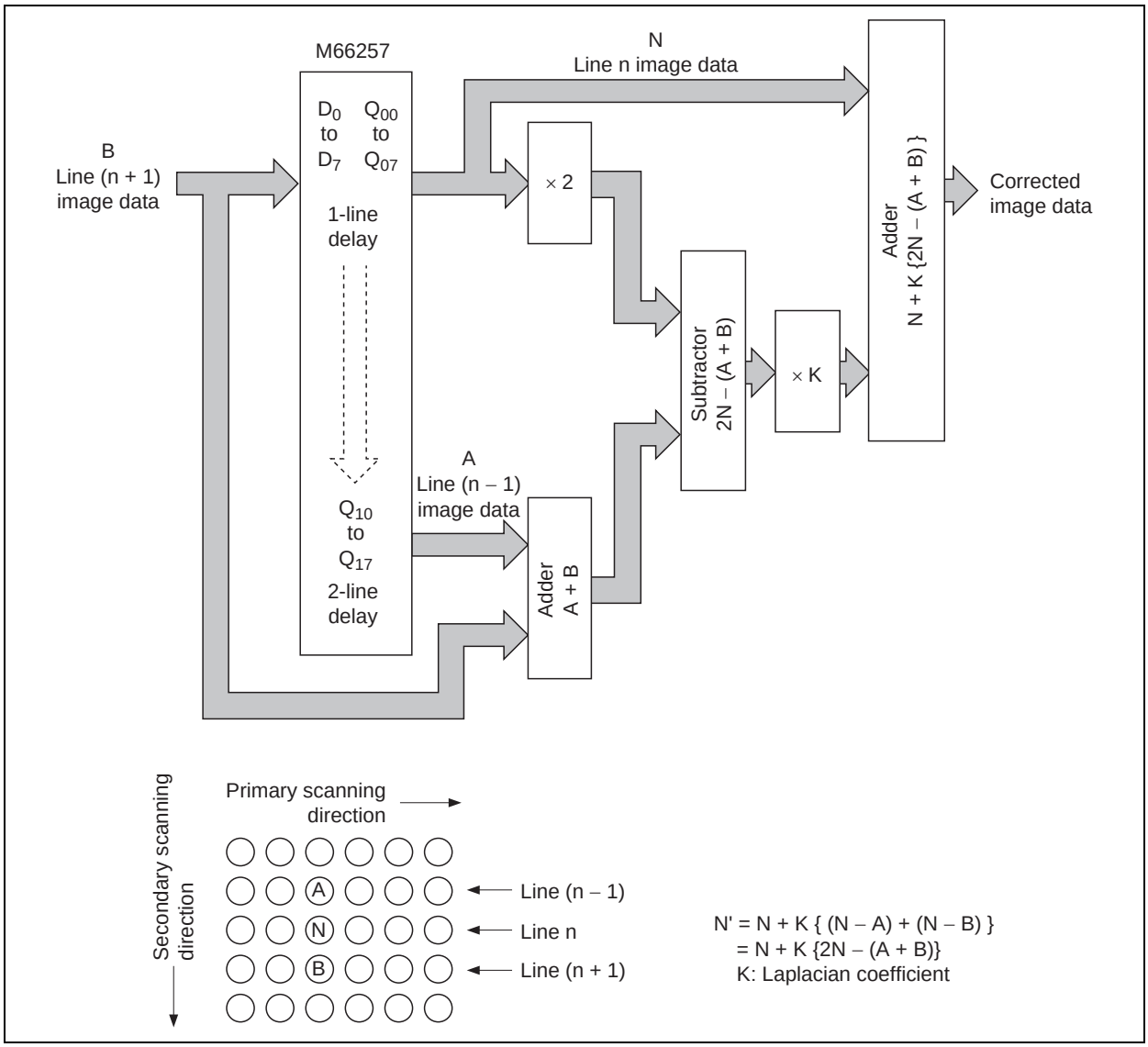


Note: <0>*, <1>* and <2>* indicates a line value.

Downloaded from Elcodis.com electronic components distributor

Application Example

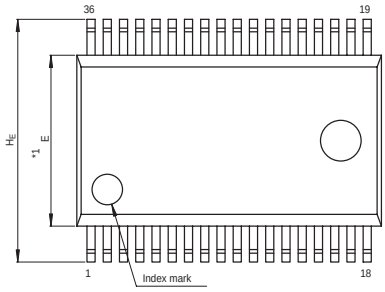
Laplacian Filter Circuit for Correction of Resolution in the Secondary Scanning Direction

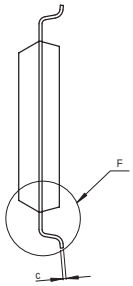


Downloaded from Elcodis.com electronic components distributor

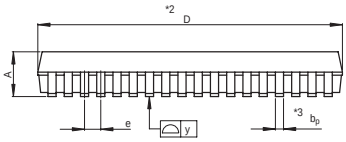
Package Dimensions

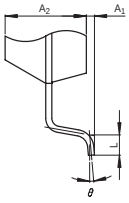
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP36-8.4x15-0.80	PRSP0036GA-A	36P2R-A	0.5g





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.





Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	14.8	15.0	15.2
E	8.2	8.4	8.6
A_2	—	2.0	—
A	—	—	2.4
A_1	0.05	—	—
b_p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	11.63	11.93	12.23
e	0.65	0.8	0.95
y	—	—	0.15
L	0.3	0.5	0.7

Downloaded from Elcodis.com electronic components distributor

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Notes:
1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (http://www.renesas.com)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guaranties regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
   (1) artificial life support devices or systems
   (2) surgical implantations
   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life
   Renesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

© 2007. Renesas Technology Corp., All rights reserved. Printed in Japan.

Colophon .7.0

Downloaded from Elcodis.com electronic components distributor