Winbond
Mobile Keyboard and
Embedded Controller
W83L950D

Revision: 1.0 Date: June 2003

Revision History

	PAGES	DATE	VERSION	VERSION ON WEB	MAIN CONTENTS
1	N.A.	02/Jan.	0.50	N.A.	All of the versions before 0.50 are for internal use.
2	7	02/Feb.	0.51	N.A.	Add LPC definition.
3	109	02/Feb.	0.51	N.A.	Contact information update.
4		03/Feb	0.60	N.A.	Release for C version chip.
5		June 23, 2003	1.0	N.A.	Refine structure and contents.

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LIFE SUPPORT APPLICATIONS

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1. GENERAL DESCRIPTION

The Winbond mobile keyboard and embedded controller W83L950D architecture consists of a Turbo-51 core logic controller and surrounded by various components, 2K+256 bytes of RAM, 40K on-chip MTP-ROM, ISA or LPC host interface, 9 general purpose I/O port with 13 external interrupt source, 4 timers, 2 serial port, 2 SMBus interface for master and slave, 3 PS2 port, two 8-bits and two 16-bits PWM channels, 2 D-A and 8 A-D converters.

2. FEATURES

Pin out

- Pin–to-Pin compatible with Mitsubishi M3886 family (ISA mode)

Core logic

- Turbo 8052 microprocessor based
- 256 bytes internal RAM
- 40K bytes embedded programmable flash memory
- 2K bytes external SRAM
- Host interface -
- Software optional with ISA or LPC interface
- Primary programmable I/O address communication port in LPC mode
- Support either Parallel IRQ in ISA or SERIRQ in LPC interface
- Hardware Fast Gate A20 and KBRST support
- Port 92h support

SMBus

- Support 2 SMBus interface for master and slave.

Timers

- Support 4 Timer signal with 3 pre-scalars.
- Timer 1 and 2 shard the same pre-scalar and are free-running only.
- Timer X and Y have individual pre-scalar and support up to 4 control modes, free running, pulse • output, event counter and pulse width measurement.

PWM

- Support 4 PWM channels
  - PWM 0 and 1 (channel 00/01 or 10/11) are 14bits and worked at fixed frequency 15.6 KHz
  - PWM 2 and 3 are16 bits and programmable frequency from 122 Hz to 16 MHz.

ADC

- Support 2 DA output and 8 AD input

- DA 0, 1 are 8bits resolution
- AD 0-7 are firmware programmable optional with 10 or 8 bits resolution.

PS2

- Support 3 hardware PS2 channels
- Optional PS2 clock inhibit by hardware or firmware.

GPIO

- Support 72 GPIO pins totally, and all are bit–addressable to facility firmware coding.

FLASH

- Support External On-Board Flash via Matrix interface (GP0, 1, 3)

ACPI

- Support ACPI appliance
- Secondary programmable I/O address communication port in LPC mode

Package

- 80-pin LQFP

3. PIN CONFIGURATION

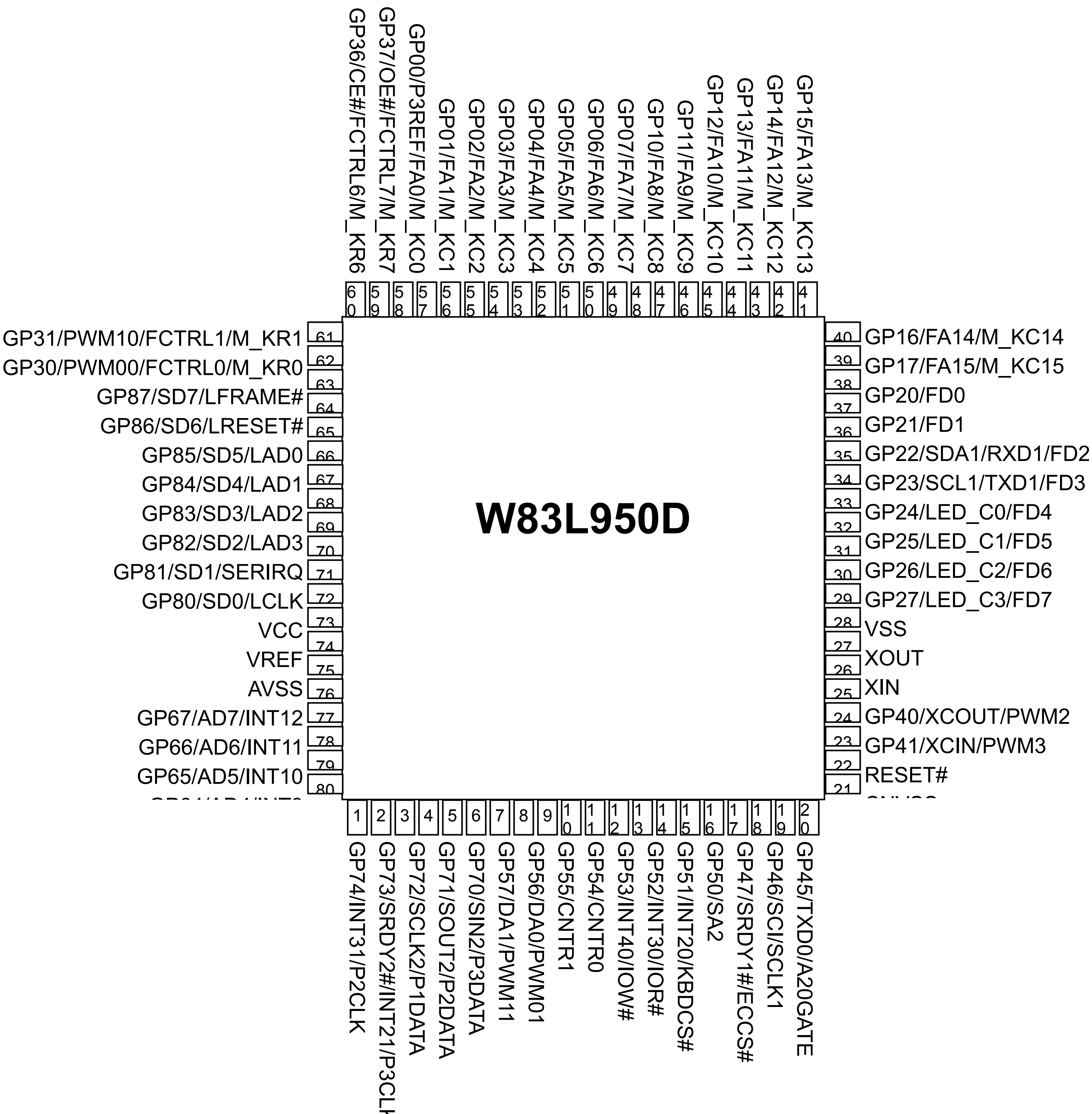


Fig 2.1 Pin configuration

4. PIN DESCRIPTION

TYPE	DESCRIPTION
I/O12t	TTL level bi-directional pin with 12 mA source-sink capability
I/O24c	TTL level output pin with 12 mA source-sink capability and CMOS level input
I/O12c	TTL level output pin with 12 mA source-sink capability and CMOS level input
I/OD12c	TTL level open drain output pin with 12 mA sink capability and CMOS level input.
I/O24c(t)	TTL level output pin with 24mA source-sink capability and CMOS or TTL level input.
I/OD12c(t)	TTL level open drain output pin with 12 mA sink capability and CMOS or TTL level input.
INc	CMOS level input pin
INs	Schmitt-trigger input pin
INt	TTL level input pin
INcu	CMOS level input pin with internal pull up resistor
INa	Analog input
O12	TTL level output pin with 12 m A source-sink capability
OD12	Open-drain output pin with 12 m A sink capability
Oa	Analog output

3.1. Basic KBC Function Signals

SYMBOL	PIN	I/O	FUNCTION
SD [7:0] GPIO 8 [7:0] LPC I/F	63-70	I/O24c(t) I/O24c INc INc I/O24c I/O24c Inc	These signal lines communicate data information over ISA bus to the host. (ISA only) General purpose IO port. Pin63: LFRAME#, Pin64: LRESET#. Pin [68:65]: LAD [3:0], Pin69: SERIRQ Pin70: LCLK These signal lines communicate data information through LPC bus to the host. Bus Type Selection please refer to 10 DBBCON register. (No H/W strapping)
SA2 GPIO 50	17	INt I/O12c	The signal line communicates address information over ISA bus to the host. (ISA only) General purpose IO port.
IOR# GPIO 52 INT30	15	INt I/O12c INs	The signal line communicates control information over ISA bus to the host. (ISA only) General purpose IO port. External interrupt input.
IOW# GPIO 53 INT40	14	INt I/O12c INs	The signal line communicates control information over ISA bus to the host. (ISA only) General purpose IO port. External interrupt input.
IRQ1 GPIO 42 INT0	23	O12 I/O12c(t) INs	ISA IRQ1 Output. (ISA only) General purpose IO port. (Input level selected by PCTRL2_bit0) External interrupt input

SYMBOL	PIN	I/O	FUNCTION
IRQ12 GPIO 43 INT1	22	O12 I/O12c(t) INs	ISA IRQ12 Output. (ISA only) General purpose IO port. (Input level selected by PCTRL2_bit0) External interrupt input.
SCI GPIO 46 SCLK1	19	O12 I/O12c(t) INc	SCI Output. (ISA only) General purpose IO port. (Input level selected by PCTRL2_bit0) Serial I/O 1 function I/O
KBDCS# GPIO 51 INT20	16	Int I/O12c INs	Decode the address 60h and 64h to input chip selected signal. (ISA only) General purpose IO port. External interrupt input.
ECCS# GPIO 47 SRDY1#	18	INt I/O12c(t) INc	Decode the address 62h and 66h to input chip selected signal. (ISA only) General purpose IO port. (Input level selected by PCTRL2_bit0) Serial I/O 1 function I/O
A20GATE GPIO 45 TxD0	20	O12 I/O12c(t) O12	Gate A20 output. This pin is controlled by AKBCCTRL. (External pull-up circuit is needed.) General purpose IO port. (Input level selected by PCTRL2_bit0) Serial I/O1 interface
KBRST# GPIO 44 RxD0	21	O12 I/O12c(t) INc	CPU reset output. It should be connected to Chipset. This pin is high after KBC reset. (External pull-up circuit is needed.) General purpose IO port. (Input level selected by PCTRL2_bit0) Serial I/O1 interface.

SYMBOL	PIN	I/O	FUNCTION
P1CLK	4	INs	PS2 Port 1 Clock.
GPIO 75		I/OD12C(t)	General purpose IO port. (Input level selected by PCTRL2_bit1)
INT41		INs	External interrupt input..
P2CLK	5	INs	PS2 Port 2 Clock.
GPIO 74		I/OD12C(t)	General purpose IO port. (Input level selected by PCTRL2_bit1)
INT31		INs	External interrupt input.
P3CLK	6	INs	PS2 Port 3 Clock.
GPIO 73		I/OD12C(t)	General purpose IO port. (Input level selected by PCTRL2_bit1)
INT21		INs	External interrupt input.
SRDY2#		INs	SERIAL I/O2 INTERFACE
P1DATA	7	INs	PS2 Port 1 Data.
GPIO 72		I/OD12C(t)	General purpose IO port. (Input level selected by PCTRL2_bit1)
SCLK2		INs	SERIAL I/O2 INTERFACE
P2DATA	8	INs	PS2 Port 2 Data.
GPIO 71		I/OD12C(t)	General purpose IO port. (Input level selected by PCTRL2_bit1)
SOUT2		OD12	Serial I/O2 interface.
P3DATA	9	INs	PS2 Port 3 Data.
GPIO 70		I/OD12C(t)	General purpose IO port. (Input level selected by PCTRL2_bit1)
SIN2		INs	Serial I/O2 interface.
LED_C [3:0]	31-34	O12	LED control signal (include Num Lock, Scroll Lock, Caps Lock and Katakana Lock).
GPIO 2[7:4]		I/O12c	General purpose IO port.
GPIO 2[3:0]	35-38	I/O12c	General purpose IO port.
SCL 1	35	INs	SMBus 1 CLOCK interface
SDA1	36	INs	SMBus 1 DATA interface
TxD1	35	O12	SERIAL I/O 1 interface
RxD1	36	INc	SERIAL I/O 1 interface

3.2. Specific Function Signals

SYMBOL	PIN	I/O	FUNCTION
DA [1:0] PWM11 PWM01 GPIO 5[7,6]	10,11	Oa O12 O12 I/O12c	D-A converter output signals. PWM output signals. General purpose IO port.
AD [7:0] GPIO 6[7:0] INT5– INT12	1,74-80	INa I/O12c INs	A-D converter output signal. General purpose IO port. External interrupt input.
SCL 0 GPIO77	2	I/OD12c I/OD12c(t)	SMBus 0 CLOCK signal. General purpose IO port. (Input level selected by PCTRL2_bit1)
SDA 0 GPIO76	3	I/OD12c I/OD12c(t)	SMBus 0 DATA signal. General purpose IO port. (Input level selected by PCTRL2_bit1)
PWM3 Xcin GPIO 41	26	O12 INa I/O12c	PWM interface signal. Sub-clock gen. GENERAL PURPOSE IO PORT.
PWM2 Xcout GPIO 40	27	O12 Oa I/O12c	PWM interface signal. Sub-clock gen. General purpose IO port.

SYMBOL	PIN	I/O	FUNCTION
CNTR 1 GPIO 55	12	INs I/O12c	Timer Y signal. General purpose IO port.
CNTR 0 GPIO 54	13	INs I/O12c	Timer X signal. General purpose IO port.
M_KC [7:0] FA [7:0] GPIO 0[7:0] P3ref	47-54 54	O12 INc I/O12c INa	24 pins Matrix KB Row signals. Address signals of External Memory interface. General purpose IO port. Comparator reference power source input signal.
M_KC [15:8] FA [15:8] GPIO 1[7:0]	39-46	O12 INc I/O12c	24 pins Matrix KB Row signals. Address signals of External Memory interface. General purpose IO port.
M_KR [1:0] PWM10, PWM00 GPIO 3[1:0] FCTRL[1:0]	61,62	INcu O12 O12 I/O12c INc	24 pins Matrix KB Column signals. PWM output signals. PWM output signals. General purpose IO port. External flash program mode control signal (*Internal pull-up controlled by PCTRL1_ BIT4)
M_KR 2 GPIO 32 FCTRL[2]	60	INcu I/O12c INc	24 pins Matrix KB Column signals. General purpose IO port. External flash program mode control signal (*Internal pull-up controlled by PCTRL1_ BIT4)
M_KR 3 GPIO 33 FCTRL[3]	59	INcu I/O12c INc	24 pins Matrix KB Column signals. General purpose IO port. External flash mode control signal (*Internal pull-up controlled by PCTRL1_ BIT4)
M_KR 4 GPIO 34	58	INcu I/O12c	24 pins Matrix KB Column signals. General purpose IO port. (*Internal pull-up controlled by PCTRL1_ BIT5)

SYMBOL	PIN	I/O	FUNCTION
M_KR 5 GPIO 35	57	INcu I/O12c	24 pins Matrix KB Column signals. General purpose IO port. (*Internal pull-up controlled by PCTRL1_ BIT5)
M_KR 6 GPIO 36 CE#	56	INcu I/O12c INc	24 pins Matrix KB Column signals. General purpose IO port. Chip enable signals of external flash program mode (*Internal pull-up controlled by PCTRL1_ BIT5)
M_KR 7 GPIO37 OE#	55	INcu I/O12c INc	24 pins Matrix KB Column signals. General purpose IO port. Read signals of External Flash program mode. (*Internal pull-up controlled by PCTRL1_ BIT5)
GPIO 2[7:0] FD [7:0]	31-38	I/O12c	General purpose IO port. Data signals of External flash program mode interface.

3.3. Power, Rest and Clock Signals

SYMBOL	PIN	I/O	FUNCTION
Vcc	71		+5V/+3.3v
Vref	72		Reference voltage of AD/DA (Less than Vcc)
Vss	30		GND
Avss	73		AGND
CNvss	24	I/O12c	Normal connects to VSS. If this pin is connects to Vcc, the chip is in external flash program mode.
Reset#	25	I/O12c	Chip reset signal input for active low, at least 8 PCICLK wide.
Xin	28	INa	Clock input (8MHz)
Xout	29	Oa	Clock output

5. SYSTEM BLOCK DIAGRAM

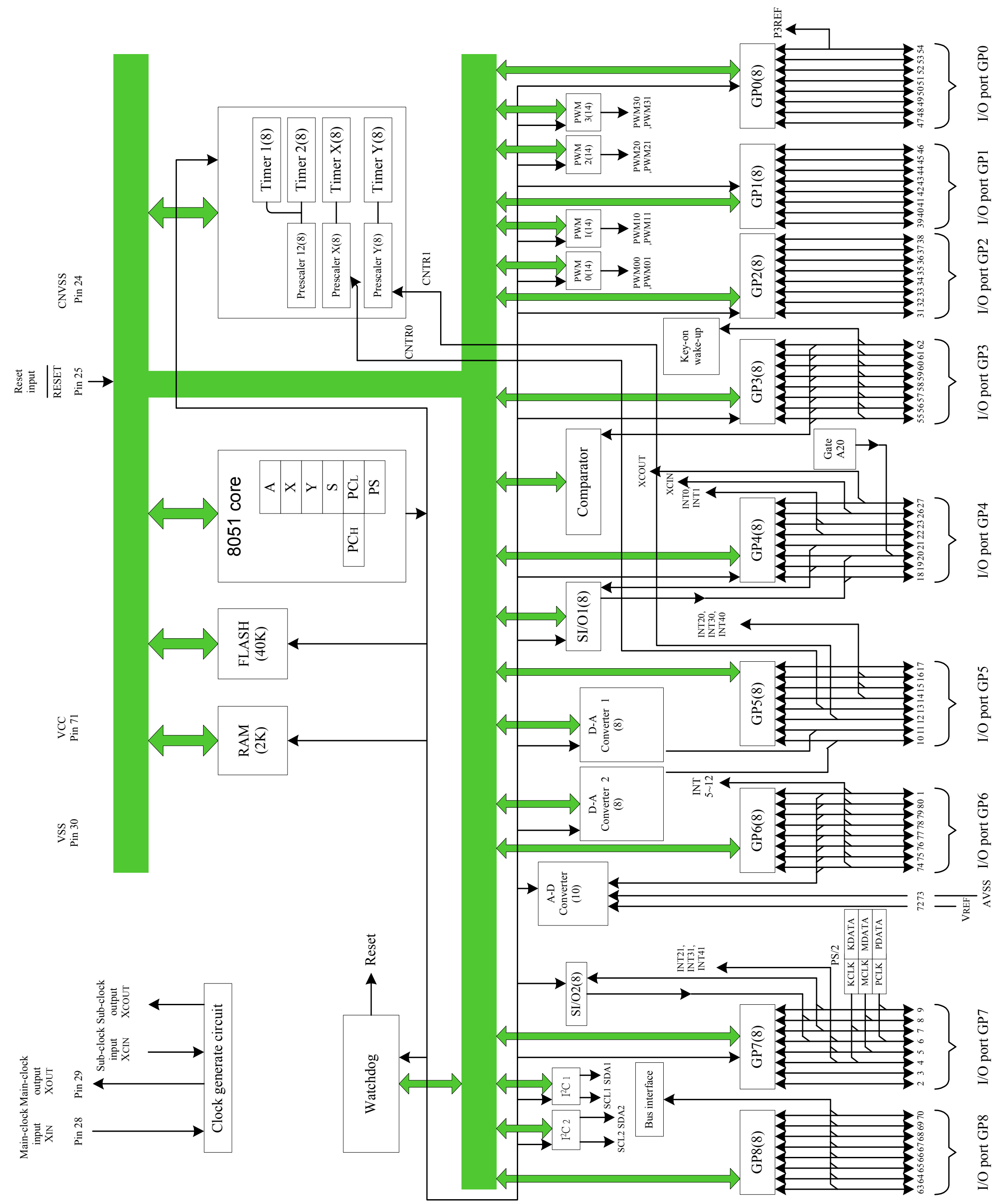


Fig 4.1 System Block Diagram

6. MICRO COMPUTER ARCHITECTURE

The Turbo-51 core logic of Winbond Keyboard controller is based on the industry standard 8032 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8032 instruction set.

The Winbond Keyboard controller separates the memory into two sections, the Program Memory and the Data Memory. The Program Memory, MTP-ROM, is used to store the instruction op-codes, and the Data Memory, RAM, is used to store data and now is consists of a 256 bytes scratch pad RAM and a 2K bytes external SRAM. The external SRAM can be accessed by either MOVX instruction in generally or to be a scratched ultra ROM for special purpose.

The brief descriptions of the internal blocks are shown as follows.

6.1 ALU

The ALU is the heart of the Winbond Keyboard controller. It is responsible for the arithmetic and logical functions. It is also used in decision-making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-codes, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC that is a Special Function Register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals that are stored in the Program Status Word register (PSW).

6.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the Winbond Keyboard controller. Since the Accumulator is directly accessible by the CPU, most of the high-speed instructions make use of the ACC as one argument.

6.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general-purpose register.

6.4 Program Status Word (PSW)

This is an 8-bit SFR, which is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General-purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.5 Data Pointers and Selection

The Data Pointers are used to do 16 bits addressing that can transfer data to and from either external Data Memory or on-chip MTP-ROM. The Winbond Keyboard controller has provided two separate Data Pointers, DPTR (DPH, DPL) and DPTR1 (DPH1, DPL1), and a Data Pointers Selection register, DPS, to select which DPTR should be utilized. The user can switch either of them with minimum software overhead, and thereby greatly increasing the system throughput by setting DPS in sequentially.

6.6 Stack Pointer

The Winbond Keyboard controller has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the Winbond Keyboard controller. Hence the size of the stack is limited by the size of this RAM.

6.7 Program Memory

The Winbond Keyboard controller includes one 40K bytes of main MTP-ROM for application program (APROM). This reality on-chip MTP-ROM begins at address 0000h and continuous through 0AFFFh. After reset, the micro-controller executes the new application program in the main MTP-APROM. The addressing of Program Memory can up to 64K bytes long.

6.8 Scratch Pad RAM

The Winbond Keyboard controller has a 256 bytes on-chip scratch pad RAM which architecture is almost same as industry standard microprocessor 8052. This RAM begins at address 00h to 0FFh, can be used for temporary storage during program execution.

From 00h to 1Fh, is divided into 4 Banks, which is used to provide 4 Register-sets, each bank has individual R0 to R7. Only one Register-set is accessible at a time, which decided by the bit 4,3 of PSW, RS1, RS0.

From 20h to 2Fh, is either a general Byte-addressable memory area or a specific purpose Bit-addressable memory area. No control bit needed here. If it is accessed by a Bit-addressable instruction, the range of bit address is from 00h to 7Fh in linearly to any bit-operational instruction.

From 30h to 7Fh, is a general memory area, which can be accessed by direct or indirect addressing.

From 80h to 0FFh is a special memory area, which can be accessed by only indirect addressing. At the same location which also addressed from 80h to FFh, there is a Special Function Registers (SFRs) Area, can be accessed by only direct addressing. This difference is to provide two physical memory entities coexisted at the same address without contention occurred.

For more detail please refer to below figure.

Address								
FFh – 80h	Indirect RAM							
7Fh – 30h	Direct RAM							
2Fh	7F	7E	7D	7C	7B	7A	79	78
2Eh	77	76	75	74	73	72	71	70
2Dh	6F	6E	6D	6C	6B	6A	69	68
2Ch	67	66	65	64	63	62	61	60
2Bh	5F	5E	5D	5C	5B	5A	59	58
2Ah	57	56	55	54	53	52	51	50
29h	4F	4E	4D	4C	4B	4A	49	48
28h	47	46	45	44	43	42	41	40
27h	3F	3E	3D	3C	3B	3A	39	38
26h	37	36	35	34	33	32	31	30
25h	2F	2E	2D	2C	2B	2A	29	28
24h	27	26	25	24	23	22	21	20
23h	1F	1E	1D	1C	1B	1A	19	18
22h	17	16	15	14	13	12	11	10
21h	0F	0E	0D	0C	0B	0A	09	08
20h	07	06	05	04	03	02	01	00
1Fh – 18h	Bank 3							
17h – 10h	Bank 2							
0Fh – 08h	Bank 1							
07h – 00h	Bank 0							

Fig.5.1 Scratch Pad RAM Map

6.9 SFR Bit Addressable Location

Some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. The following table lists the bit addressable SFR only.

As the below table shown, it is different with traditional industry standard micro-processor 8052, only register ACC, B and PSW are still populated in this bit-addressable table, the others were removed and instead of nine GPIO registers. This may provide a quickly response to firmware's GPIO operation.

The discontinued gaps of the SFR bit addressable location, 0C8h or 0D8h etc, are not available and undefined. Access to them may result in unknown error.

FFH									
F0H	F7	F6	F5	F4	F3	F2	F1	F0	B
E0H	E7	E6	E5	E4	E3	E2	E1	E0	ACC
	CY	AC	F0	RS1	RS0	OV		P	
D0H	D7	D6	D5	D4	D3	D2	D1	D0	PSW
	GP8.7	GP8.6	GP8.5	GP8.4	GP8.3	GP8.2	GP8.1	GP8.0	
C0H	C7	C6	C5	C4	C3	C2	C1	C0	GP8
	GP7.7	GP7.6	GP7.5	GP7.4	GP7.3	GP7.2	GP7.1	GP7.0	
B8H	BF	BE	BD	BC	BB	BA	B9	B8	GP7
	GP6.7	GP6.6	GP6.5	GP6.4	GP6.3	GP6.2	GP6.1	GP6.0	
B0H	B7	B6	B5	B4	B3	B2	B1	B0	GP6
	GP5.7	GP5.6	GP5.5	GP5.4	GP5.3	GP5.2	GP5.1	GP5.0	
A8H	AF		AD	AC	AB	AA	A9	A8	GP5
	GP4.7	GP4.6	GP4.5	GP4.4	GP4.3	GP4.2	GP4.1	GP4.0	
A0H	A7	A6	A5	A4	A3	A2	A1	A0	GP4
	GP3.7	GP3.6	GP3.5	GP3.4	GP3.3	GP3.2	GP3.1	GP3.0	
98H	9F	9E	9D	9C	9B	9A	99	98	GP3
	GP2.7	GP2.6	GP2.5	GP2.4	GP2.3	GP2.2	GP2.1	GP2.0	
90H	97	96	95	94	93	92	91	90	GP2
	GP1.7	GP1.6	GP1.5	GP1.4	GP1.3	GP1.2	GP1.1	GP1.0	
88H	8F	8E	8D	8C	8B	8A	89	88	GP1
	GP0.7	GP0.6	GP0.5	GP0.4	GP0.3	GP0.2	GP0.1	GP0.0	
80H	87	86	85	84	83	82	81	80	GP0

Fig 5.2. Bit Address Location

6.10 External SRAM

The Winbond Keyboard controller has a 2K bytes external SRAM and is read/write accessible. The SRAM begins at address 0000h to 07FFh, is accessed via the MOVX instruction in generally. There is no conflict or overlap among the 256bytes scratch pad RAM and the 2K bytes external SRAM as they use different addressing modes and separate instructions. The addressing of external SRAM can up to 64K bytes long.

6.11 Scratched ULTRA ROM

The external SRAM can be accessed by either general external memory instruction, i.e. MOVX, or to be a scratch ROM for special purpose which achieved by re-mapping this area to a part of logical Program Memory, addressed on 0F800h to 0FFFFh (62K to 64K), unlike the industry standard 8052 derivatives. No control switch is needed here. In other words, using MOVX to transfer data to and jump to it by an absolutely JUMP instruction to accomplish this operation. This feature can increase the system throughput and is convenient to perform On-Chip internal flash task.

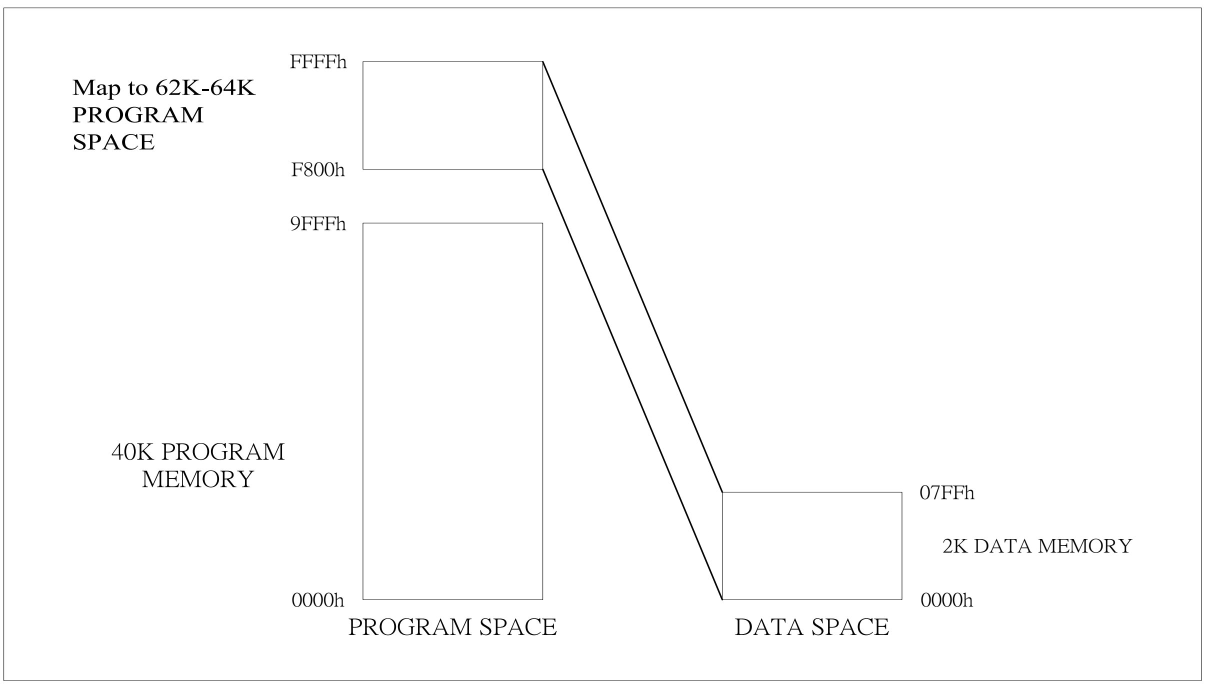


Fig.5.3 Memory Map

7. SPECIAL FUNCTION REGISTER

7.1 Standard SFR Address and Registers

F8h	SFRAL	SFRAH	SFRFD	SFRCN	DEVICE ID	DEVICE REV.		
F0h	+B							
E8h								
E0h	+ACC		ADCON	AD0	AD1	DA0	DA1	CMPD
D8h	DBB0	DBBSTS0	DBBCON	DBB1	DBBSTS1			
D0h	+PSW				PWM0H	PWM0L	PWM1H	PWM1L
C8h	TB/RB	SIO1STS	SIO1CON	UARTCON	BRG	SIO2CON	WDTCON	SIO2
C0h	IREQ	IREQ1	IREQ2		INTSEL1	INTSET2	KBCTR	CHIPSTS
B8h	IP	IE1	IP1	IE2	IP2	IT1	IT2	
B0h	PRE12	T1	T2	TM	PREX	TX	PREY	TY
A8h	IE	I2CISR	I2CFSR	I2CUDR	I2CSCR	I2CTST0	I2CTST1	*(TEST MODE)*
A0h	I2CHSR	I2CHCR	I2CRBC	I2C DFIFO	I2C SADR	I2CHMR	I2CFCR	I2CICR
98h	GP8	GP8D	PCTRL1	PCTRL2	PCTRL3	CLKCTRL	**Advance index**	**Advance data**
90h	GP4	GP4D	GP5	GP5D	GP6	GP6D	GP7	GP7D
88h	GP0	GP0D	GP1	GP1D	GP2	GP2D	GP3	GP3D
80h	CHIPCTRL	SP	DPL	DPH	DPL1	DPH1	DPS	PCON

A register prefixed a "+" sign means it is a bit addressable register. Note that the SFR address which involved x0h or x8h, is no longer to be the bit-addressable register.

The TEST MODE register is an internal purpose register; the user should not access it.

Any gaps of SFR are not defined in Winbond keyboard controller, access them may result in unknown problem.

7.2 Advanced SFR Address and Registers

The Winbond keyboard controller defined another Advanced SFR area to expand the hardware control registers without memory-mapped register. There are two registers, [Advance Index] and [Advance Data], can be used to addressing this Advanced SFR register space. These two registers are located at 09Eh and 09Fh of the Standard SFR register area.

The addressing method is very similar with people well known Super I/O device. For example, if we wish set SIRQ2 to 55h, set [Advance index] to 01h, and then set [Advance data] to 055h.

78h								
70h								
68h								
60h								
58h								
50h								
48h								
40h								
38h								
30h	AI2CISR	AI2CFSR	AI2CUDR	AI2CSCR	AI2CTST0	AI2CTST1		
28h	AI2CHSR	AI2CHCR	AI2CRBC	AI2C DFIFO	AI2C SADR	AI2CHMR	AI2CFCR	AI2CICR
20h	PWM2PL	PWM2PH	PWM2HSL	PWM2HSH	PWM3PL	PWM2PH	PWM2HSL	PWM2HSH
18h	P3PS2DATA	P3PS2CON	P3PS2STS	P3S2STS_2	APWMCON			
10h	P1PS2DATA	P1PS2CON	P1PS2STS		P2PS2DATA	P2PS2CON	P2PS2STS	
08h	AKBCCTRL							
00h	SIRQ1	SIRQ2	ADD1L	ADD1H	ADD2L	ADD2H		ADDCON

8. 8051 AND BASIC CONTROL REGISTER

8.1 Stack Pointer

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

8.2 Data Pointer Low

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard 8032 16-bit data pointer.

8.3 Data Pointer High

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the high byte of the standard 8032 16-bit data pointer.

8.4 Data Pointer Low1

Bit:	7	6	5	4	3	2	1	0
	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0

Mnemonic: DPL1 Address: 84h

This is the low byte of the new additional 16-bit data pointer that has been added to the Winbond Keyboard controller. The user can switch between DPL, DPH and DPL1, DPH1 simply by setting DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH.

8.5 Data Pointer High1

Bit:	7	6	5	4	3	2	1	0
	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0

Mnemonic: DPH1 Address: 85h

This is the high byte of the new additional 16-bit data pointer that has been added to the Winbond Keyboard controller. The user can switch between DPL, DPH and DPL1, DPH1 simply by setting DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH.

8.6 Data Pointer Select

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DPS.0

Mnemonic: DPS Address: 86h

DPS.0 This bit is used to select the DPL, DPH pair or DPL1, DPH1 pair as the active Data Pointer, DPTR. When set to 1, DPL1, DPH1 will be selected, else DPL, DPH will be selected.

DPS.1-7 These bits are reserved but will read 0.

8.7 Power Control

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

GF1-0 These two bits are general-purpose user flags.

PD Setting this bit causes the Winbond Keyboard controller to go into the POWERDOWN mode. In this mode all the clocks are stopped and program execution is frozen.

IDL Setting this bit causes the Winbond Keyboard controller to go into the IDLE mode. In this mode the clocks to the CPU is stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating unhindered. The chip can be wakening to operation mode by active interrupt.

8.8 Program Status Word

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

CY Carry flag: Set for an arithmetic operation, which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.

AC Auxiliary carry: Set when the previous operation resulted in a carry (during addition) or borrow (during subtraction) from the high order nibble.

F0 User flag 0: General-purpose flag that can be set or cleared by the user by software.

RS.1-0 Register bank selects bits:

RS1	RS0	Register bank	Address
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

OV Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation or vice-versa.

F1 User Flag 1: General-purpose flag that can be set or cleared by the user by software

P Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

8.9 Accumulator

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0 The A or ACC register is the standard 8032 accumulator

8.10 B Register

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

B.7-0 The B register is the standard 8032 accumulator

8.11 CLK Controller Register

Bit: 7 6	5 4	3	2	1	0
CLKSEL 1-0	FREQSEL 1-0	-	-RING_EN	PLLEN	CLKSEL#

Mnemonic: CLKCTRL Address: 9Dh

Default: 0x40

B.7-6 PLL CLK OUT SELECT

= 00: 4Mhz

= 01: 8MHz

= 10: Reserved

= 11: Reserved

B.5-4 PLL INPUT CLOCK SOURCE SELECT

PLL CLOCK INPUT is directly connected to Xin and Xout pin.

= 00: 8MHz

= 01: 14.318MHz

= 10: Reserved

= 11: Reserved

B.2 4MHZ RING OSC ENABLE

= 0: 8051 CLK source is from Xin and Xout pin..

= 1: 8051 CLK source is from 4MHZ RING OSC.

B.1 PLL ENABLE

= 0: 8051 CLK source is from Xin and Xout pin. and bit 7-6 is disable.

= 1: 8051 CLK source is from PLL block and bit 7-6 is enable.

B.0 CLK SOURCE SELECT

= 0: CLK source is Xin and Xout.

= 1: CLK source is Xcin and Xcout.

8.12 Chip Controller Register

Bit:	7	6	5	4	3	2	1	0
	-	-	PLLPD	ADCPD	-	-	-FAST PD WAKEUP	RSTEN#

Mnemonic: CHIPCTRL Address: 80h

B.7-6: Reserved

B.5: PLL POWER DOWN BIT (PLLPD)

= 0: PLL NO POWER DOWN

= 1: PLL POWER DOWN.

B.4: ADC POWER DOWN BIT (ADCPD)

= 0: ADC NO POWER DOWN

= 1: ADC POWER DOWN.

B.3-2: Reserved

B.1: FAST 51 PD MODE WAKUP.

=0: NORMAL WAKUP MODE (65535 SYSTEM CLOCK)

=1: FAST WAKUP MODE (1 SYSTEM CLOCK).

B.0: RSTEN#

= 0: PIN RESET# ENABLE (default).

The chip is reset when either Power On Reset or pin Reset#.

= 1: PIN RESET# DISABLE

The chip is reset only when Power On Reset.

8.13 Chip Status Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	WTRF

Mnemonic: CHIPCTRL Address: C7h

B.7-1: Reserve

B.0: WTRF

Hardware will set this bit when the watchdog timer causes the reset. Software can clear it by writing a 0 to this bit.

8.14 Device ID; Device REV Register

Bit:	7	6	5	4	3	2	1	0
Device ID	0-	0	0	1	0	0	0	1
Device Rev.	0	0	0	0	Rev.			

Mnemonic: DEVICE ID, DEVICE REV Address: 0FCh, 0FDh

9. INTERRUPTS

Interrupts occur by 20 sources among 24 sources, 13 external and 11 internal interrupt.

9.1 Interrupt Control

Each interrupt is controlled and corresponding to a bit in Interrupt Enable Register (IE), the Interrupt Type Register (IT), the Interrupt Priority Control Register (IP) and the Interrupt Request Register (IREQ). An interrupt occurs if the corresponding Interrupt Request occur and enable bits is “1”. When several interrupts occur at the same time, the interrupts are received according to priority setting. If interrupts are setting to same priority, then it is decided by hardware internal checking rule.

9.2 Interrupt Source Selection

The below interrupt sources can be selected by the Interrupt Source Selection Register (INTSEL).

1. INT0 or Input buffer full.
2. INT1 or Output buffer empty.
3. Serial I/O1 transmission / SCL, SDA interrupt
4. CNTR0 / SCL, SDA interrupt
5. Serial I/O2 or I2C.
6. INT2 or I2C.
7. CNTR1 or Key-on wake-up.
8. 8 A-D conversion or Key-on wake-up.
9. INT 5 or Auxiliary I2C.
10. INT 6 or Keyboard PS/2 INT.
11. INT 7 or MOUSE PS/2 INT.
12. INT 8 or Internal PS/2 INT.
13. INT 9 or Auxiliary SCL, SDA interrupt.

9.3 External interrupt Pin Selection

The occurrence sources of the external interrupt INT2, INT3, and INT4 can be selected from either input from INT20, INT30, INT40 pin, or input from INT21, INT31, and INT41 pin by the INT2, INT3, INT4 interrupt switch bit (bit 4 of PCTRL2).

9.4 Key Input Interrupt (Key-on Wake Up)

A Key input interrupt request is generated by applying "L" level to any pin of port GP3 that have been set to input mode. In other words, it is generated when AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in blow Figure, where an Interrupt Request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P30-P33.

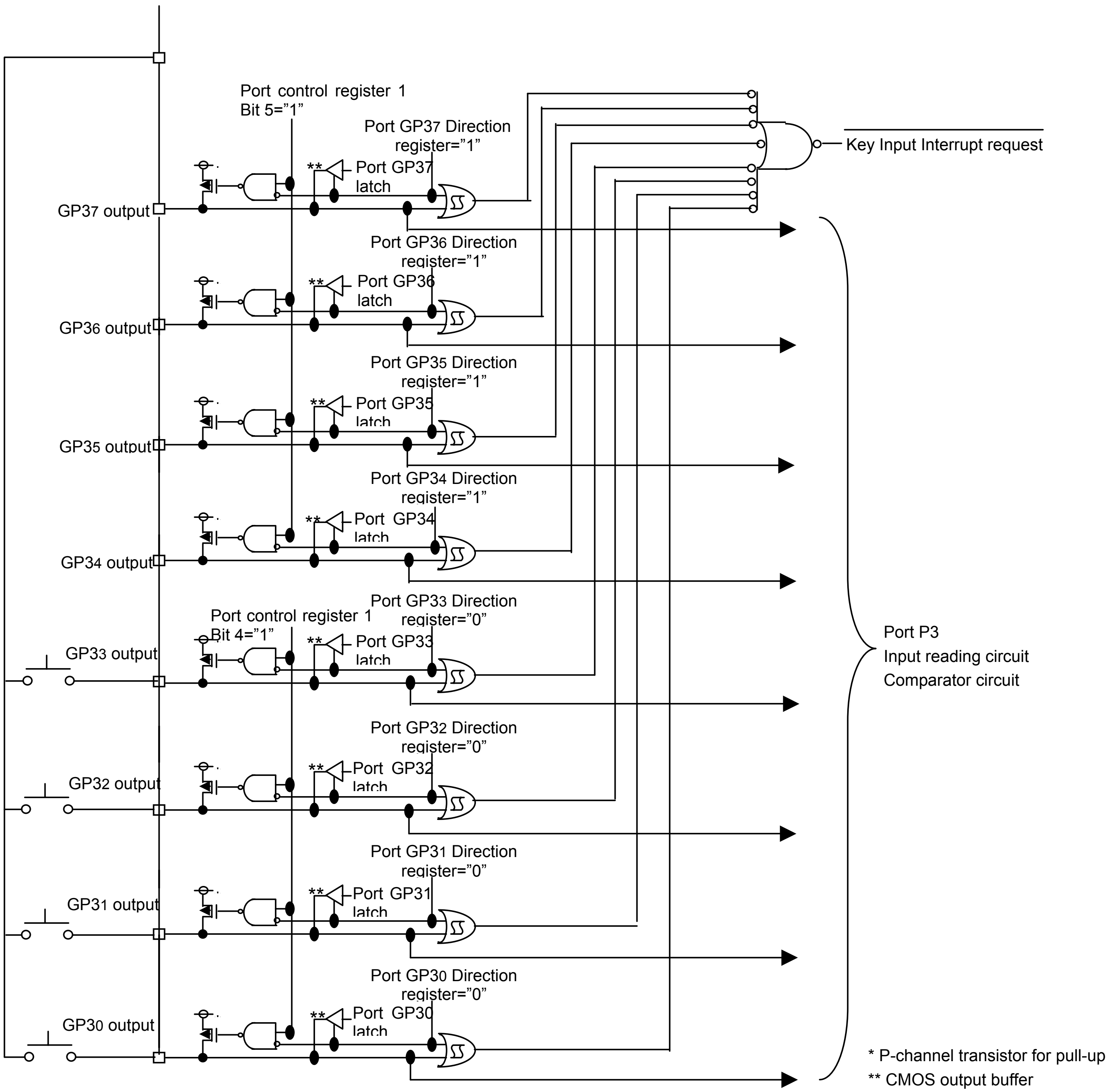


Fig.8.1 Connection Example

9.5 Interrupt Vector Table

SOURCE	VECTOR ADDRESS
RESET	0000H
INT0 / input buffer full interrupt	0003H
INT1 / output buffer empty interrupt	000BH
Serial I/O1 receive interrupt	0013H
Serial I/O1 transmit / SCL, SDA interrupt	001BH
TIMER X interrupt	0023H
TIMER Y interrupt	002BH
TIMER 1 interrupt	0033H
TIMER 2 interrupt	003BH
CNTR0 / SCL, SDA interrupt	0043H
CNTR1 / key-on wake-up interrupt	004BH
Serial I/O 2 / I2C interrupt	0053H
INT2 / I2C interrupt	005BH
INT3	0063H
INT4	006BH
AD convert / key-on wake-up interrupt	0073H
INT5 / Auxiliary I2C	007BH
INT6 / KPS2INT	0083H
INT7 / MPS2INT	008BH
INT8 / PPS2INT	0093H
INT9 / ASCL, ASDA interrupt	009Bh
INT10	00A3h
INT11	00ABh
INT12	00B3h

9.6 Interrupt Enable Register (IE)

SFR address 0xA8
Default value 0x00

Bit 7: The whole chip interrupt enable bit.
0: disable all interrupt.
1: the corresponding enable bit enables the interrupt.
Bit 6: TIMER 1 interrupt enable bit
0: disable.
1: enable.
Bit 5: TIMER Y interrupt enable bit
0: disable.
1: enable.
Bit 4: TIMER X interrupt enable bit
0: disable.
1: enable.
Bit 3: Serial I/O1 transmit / SCL, SDA interrupt enable bit
0: disable.
1: enable.
Bit 2: Serial I/O1 receive interrupt enable bit.
0: disable.
1: enable.
Bit 1: INT1 /output buffer empty interrupt enable bit
0: disable.
1: enable.
Bit 0: INT0 /input buffer full interrupt enable bit
0: disable.
1: enable.

9.7 Interrupt Enable Register 1(IE1)

SFR address 0xB9
Default value 0x00

Bit 7: AD convert / key-on wake-up interrupt enable bit.
0: disable.
1: is enabled by the corresponding enable bit.
Bit 6: INT4 interrupt enable bit
0: disable.
1: enable.
Bit 5: INT3 interrupt enable bit
0: disable.
1: enable.

Bit 4: INT2 / I2C interrupt enable bit
0: disable.
1: enable.
Bit 3: Serial I/O 2 / I2C interrupt enable bit
0: disable.
1: enable.
Bit 2: CNTR1 / key-on wake-up interrupt enable bit
0: disable.
1: enable.
Bit 1: CNTR0 / SCL, SDA interrupt enable bit
0: disable.
1: enable.
Bit 0: TIMER 2 interrupt enable bit
0: disable.
1: enable.

9.8 Interrupt Enable Register 1(IE2)

SFR address 0xBB
Default value 0x00

Bit 7: INT 12
0: disable.
1: enable.
Bit 6: INT 11
0: disable.
1: enable.
Bit 5: INT 10
0: disable.
1: enable.
Bit 4: INT9 / ASCL, ASDA interrupt enable bit
0: disable.
1: enable.
Bit 3: INT8/PPS2INT
0: disable.
1: enable.
Bit 2: INT7/MPS2INT
0: disable.
1: enable.
Bit 1: INT6/KPS2INT
0: disable.
1: enable.

Bit 0: INT5 / AI2CINT

0: disable.

1: enable.

9.9 Interrupt Priority Register (IP)

SFR address 0xB8

Default value 0x00

Bit 7: Reserve.

Bit 6: TIMER 1 interrupts

0: low priority group.

1: high priority group

Bit 5: TIMER Y interrupt

0: low priority group.

1: high priority group

Bit 4: TIMER X interrupts

0: low priority group.

1: high priority group

Bit 3: Serial I/O1 transmit / SCL, SDA interrupt

0: low priority group.

1: high priority group

Bit 2: Serial I/O1 receive interrupt

0: low priority group.

1: high priority group

Bit 1: INT1 /output buffer empty interrupt

0: low priority group.

1: high priority group

Bit 0: INT0 /input buffer full interrupt

0: low priority group.

1: high priority group

9.10 Interrupt Priority Register 1(IP1)

SFR address 0xBA

Default value 0x00

Bit 7: AD convert / key-on wake-up interrupt.

0: low priority group.

1: high priority group

Bit 6: INT4 interrupt

0: low priority group.

1: high priority group

Bit 5: INT3 interrupt

0: low priorty group .

1: high priority group

Bit 4: INT2 / I2C interrupt

0: low priority group.

1: high priority group

Bit 3: Serial I/O 2 / I2C interrupt

0: low priority group.

1: high priority group

Bit 2: CNTR1 / key-on wake-up interrupt

0: low priority group.

1: high priority group

Bit 1: CNTR0 / SCL, SDA interrupt

0: low priority group.

1: high priorty group

Bit 0: TIMER 2 interrupts

0: low priority group.

1: high priority group

9.11 Interrupt Priority Register 1(IP2)

SFR address 0xBC

Default value 0x00

Bit 7: INT 12

0: low priority group.

1: high priorty group

Bit 6: INT 11

0: low priority group.

1: high priority group

Bit 5: INT 10

0: low priority group.

1: high priority group

Bit 4: INT9/ ASCL, ASDA interrupt

0: low priority group.

1: high priorty group

Bit 3: INT8/PPS2INT

0: low priority group.

1: high priority group

Bit 2: INT7/MPS2INT

0: low priority group.

1: high priority group

Bit 1: INT6/KPS2INT

0: low priority group.

1: high priority group

Bit 0: INT5 / AI2CINT

0: low priority group.

1: high priority group

9.12 Interrupt Type Register 1(IT1)

SFR address 0xBD

Default value 0x00

Bit 7: INT7

0: falling edge active.

1: rising edge active

Bit 6: INT6

0: falling edge active.

1: rising edge active

Bit 5: INT5

0: falling edge active.

1: rising edge active

Bit 4: INT4

0: falling edge active.

1: rising edge active

Bit 3: INT3 edge selection bit

0: falling edge active.

1: rising edge active

Bit 2: INT2 edge selection bit

0: falling edge active.

1: rising edge active

Bit 1: INT1 edge selection bit

0: falling edge active.

1: rising edge active

Bit 0: INT0 edge selection bit

0: falling edge active.

1: rising edge active

9.13 Interrupt Type Register 2(IT2)

SFR address 0xBE

Default value 0x00

Bit 7 –5: Reserve

Bit 4: INT12

0: falling edge active.

1: rising edge active

Bit 3: INT11 edge selection bit

0: falling edge active.

1: rising edge active

Bit 2: INT10 edge selection bit

0: falling edge active.

1: rising edge active

Bit 1: INT9 edge selection bit

0: falling edge active.

1: rising edge active

Bit 0: INT8 edge selection bit

0: falling edge active.

1: rising edge active

9.14 Interrupt Request Register (IREQ)

SFR address 0xC0

Default value 0x00

Bit 7: Reserve.

Bit 6: TIMER 1 interrupt

0: no interrupt request.

1: interrupt request.

Bit 5: TIMER Y interrupt

0: no interrupt request.

1: interrupt request.

Bit 4: TIMER X interrupts

0: no interrupt request.

1: interrupt request.

Bit 3: Serial I/O1 transmit / SCL, SDA interrupt

0: no interrupt request.

1: interrupt request.

Bit 2: Serial I/O1 receive interrupt.

0: no interrupt request.

1: interrupt request.

Bit 1: INT1 /output buffer empty interrupt.

0: no interrupt request.

1: interrupt request.

Bit 0: INT0 /input buffer full interrupt.

0: no interrupt request.

1: interrupt request.

9.15 Interrupt Request1 Register 1(IREQ1)

SFR address 0xC1
Default value 0x00

Bit 7: AD convert / key-on wake-up interrupt.
0: no interrupt request.
1: interrupt request.
Bit 6: INT4 interrupt
0: no interrupt request.
1: interrupt request .
Bit 5: INT3 interrupt
0: no interrupt request.
1: interrupt request.
Bit 4: INT2 / I2C interrupt
0: no interrupt request.
1: interrupt request.
Bit 3: Serial I/O 2 / I2C interrupt
0: no interrupt request.
1: interrupt request .
Bit 2: CNTR1 / key-on wake-up interrupt
0: no interrupt request.
1: interrupt request.
Bit 1: CNTR0 / SCL, SDA interrupt
0: no interrupt request.
1: interrupt request.
Bit 0: TIMER 2 interrupts
0: no interrupt request.
1: interrupt request.

9.16 Interrupt Request2 Register 1(IREQ2)

SFR address 0xC2
Default value 0x00

Bit 7: INT 12
0: no interrupt request.
1: interrupt request.
Bit 6: INT 11
0: no interrupt request.
1: interrupt request.
Bit 5: INT 10
0: no interrupt request.
1: interrupt request.

Bit 4: INT9/ ASCL, ASDA interrupt

0: no interrupt request.

1: interrupt request.

Bit 3: INT8/PPS2INT

0: no interrupt request.

1: interrupt request.

Bit 2: INT7/MPS2INT

0: no interrupt request.

1: interrupt request.

Bit 1: INT6/KPS2INT

0: no interrupt request.

1: interrupt request.

Bit 0: INT5 / AI2CINT

0: no interrupt request.

1: interrupt request.

9.17 Interrupt Source Selection Register 1(INTSEL1)

SFR address 0xC4

Default value 0x00

Bit 7: AD convert / key-on wake-up interrupt source selection bit.

0: AD converts interrupt.

1: key-on wake-up interrupts

Bit 6: CNTR1 / key-on wake-up interrupt source selection bit

0: CNTR1. interrupt.

1: key-on wake-up interrupt.

Bit 5: INT2 / I2C interrupt source selection bit

0: INT2. Interrupt

1: I2C interrupt.

Bit 4: Serial I/O 2 / I2C interrupt source selection bit

0: SERIAL I/O 2 interrupt

1: I2C interrupt

Bit 3: CNTR0 /SCL, SDA interrupt source selection bit

0: CNTR0 interrupt.

1: SCL, SDA interrupt

Bit 2: Serial I/O1 transmit /SCL, SDA interrupt source selection bit

0: Serial I/O1 transmit interrupt.

1: SCL, SDA interrupt

Bit 1: INT1 /output buffer empty interrupt source selection bit

0: INT1 interrupt

1: output buffer empty interrupt.

Bit 0: INT0 /input buffer full source selection bit.

0: INT0 interrupt.

1: input buffer full interrupt.

9.18 Interrupt Source Selection Register 2(INTSEL2)

SFR address. 0xC6

Default value 0x00

Bit 7 –5: reserve

Bit 4: INT9 / ASCL, ASDA interrupt source selection bit

0: INT9 transmit interrupt.

1: ASCL, ASDA interrupt.

Bit 3: INT8 / PPS2INT interrupt source selection bit

0: INT8 transmit interrupt.

1: PPS2INT interrupt.

Bit 2: INT7 / MPS2INT interrupt source selection bit

0: INT7 transmit interrupt.

1: MPS2INT interrupt.

Bit 1: INT6 / KPS2INT interrupt source selection bit

0: INT6 transmit interrupt.

1: KPS2INT interrupt.

Bit 0: INT5 / AI2CINT interrupt source selection bit

0: INT5 interrupt

1: AI2CINT interrupt

Bus Interface AND GATEA20 / KBRESET/ Port92h

10. BUS INTERFACE AND GATEA20 / KBRESET/ PORT92H

10.1 Data Bus Buffer Control Register (DBBCON)

SFR address. 0xDA
Default value. 0x00

Bit 7: Bus protocol select
= 0 ISA BUS SELECT
= 1 LPC BUS SELECT

Bit 6: Input level selection bit
= 0 CMOS level input.
= 1 TTL level input.

Bit 5: OBF10 output enable bit
ISA MODE = 0: GP46 function as I/O Port
= 1: GP46 function as OBF10 output pin (SCI)
LPC MODE = 0: disable SERIAL IRQ source for OBF10 (SIRQ2).
= 1: enable SERIAL IRQ source for OBF10 (SIRQ2).

Bit 4: OBF01 output enable bit
ISA MODE = 0: GP43 function as I/O Port.
= 1: GP43 function as OBF01 output pin (IRQ12).
LPC MODE = 0: disable SERIAL IRQ source for OBF01 (SERIRQ12).
= 1: enable SERIAL IRQ source for OBF01 (SERIRQ12).

Bit 3: OBF00 output enable bit
ISA MODE = 0: GP42 function as I/O Port
= 1: GP42 function as OBF00 output pin (IRQ1)
LPC MODE = 0: disable SERIAL IRQ source for OBF00 (SERIRQ1).
= 1: enable SERIAL IRQ source for OBF00 (SERIRQ1).

Bit 2: OBF0 output selection bit
= 0: OBF00 valid (IRQ1)
= 1: OBF01 valid (IRQ12)

Bit 1: Data bus buffer function selection bit
= 0: Single data bus buffer mode (GP47 function as I/O port)
= 1: Double data bus buffer mode (GP47 function as $\overline{S_1}$ input)

Bit 0: Data bus buffer enable bit
= 0: P50 – P53, GP8 I/O port.
= 1: Data bus buffer enabled.

10.2 Data Bus Buffer Register 0(DBB0)

SFR address 0xD8
Default value 0xxx

10.3 Data Bus Buffer Status Register 0(DBBSTS0)

SFR address. 0xD9
Default value. 0x00

Bit 7–4: User definable flag
Bit 3: A00 flag,
This flag indicates the condition of A00 status when the IBF0 flag is set.
Bit 2: User definable flag
Bit 1: Input buffer full flag 0 (IBF0)
= 0: buffer empty
= 1: buffer full
Bit 0: Output buffer full flag 0 (OBF0)
= 0: buffer empty
= 1: buffer full

10.4 Data Bus Buffer Register 1(DBB1)

SFR address 0xDB
Default value xxxxxxxxb

10.5 Data Bus Buffer Status Register 1(DBBSTS1)

SFR address. 0xDC
Default value. 0x00

Bit 7–4: User definable flag
Bit 3: A01 flag
This flag indicates the condition of A00 status when the IBF0 flag is set.
Bit 2: User definable flag
Bit 1: Input buffer full flag 1 (IBF1)
= 0: buffer empty
= 1: buffer full
Bit 0: Output buffer full flag 1 (OBF1)
= 0: buffer empty
= 1: buffer full

10.6 Serial IRQ Select Register 1(SIRQ1)

ASFR address 0x00
Default value 0xc1

The SIRQ1 register is used for LPC mode of DBB interface.
Bit 7-4: These bits select SERIRQ IRQ SOURCE for OBF01. Default is IRQ12.
Bit 3-0: These bits select SERIRQ IRQ SOURCE for OBF00. Default is IRQ1.

10.7 Serial IRQ Select Register 2(SIRQ2)

ASFR address 0x01
Default value 0x0b

The SIRQ2 register is used for LPC mode of DBB interface.

Bit 7: GP46 function as OBF10 in LPC interface.
Bit 6: OBF10 output mode select.
=0: The output of GP46 is OBF10.
=0: The output of GP46 is five system clock open drain low pulse according the OBF10 rising,
Bit 5-4: Reserved. (Should be program to 0.)
Bit 3-0: These bits select SERIRQ IRQ SOURCE for OBF10. Default is IRQ11.

10.8 Data Bus Buffer 0 Address Low Register (DBB0ADDL)

ASFR address 0x02
Default value 0x60

10.9 Data Bus Buffer 0 Address High Register (DBB0ADDH)

ASFR address. 0x03
Default value. 0x00

These two registers are only available in LPC mode, which be used to specify the DBB0 base I/O address. Then the available I/O ports are at base and base+4h.
Default is {00h, 60h}, so available decode address for DBB0 are 60h and 64h.

10.10 Data Bus Buffer 1 Address Low Register (DBB1ADDL)

ASFR address 0x04
Default value 0x62

10.11 Data Bus Buffer 1 Address High Register (DBB1ADDH)

ASFR address 0x05
Default value 0x00

These two registers are only available in LPC mode, which be used to specify the DBB1 base I/O address. Then the available I/O ports are at base and base+4h.

Default is {00h, 62h}, so available decode address for DBB1 are 62h and 66h.

10.12 Hardware GATEA20 and KBRESET and Port 92h Support

The Winbond keyboard controller implements a hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by KBCTRL register as follows:

10.13 Advance Keyboard Controller Register (AKBCTRL)

ASFR address 0x08
Default value 0x00

Bit 7-3: Reserved

Bit 2: = 0: The handshake mode of PS2 is disable. (Auto drive PS2 CLK Low for 100us after start bit received.)

=1: The handshake mode of PS2 is enable. (Auto drive PS2 CLK Low for 100us after start bit received.)

When the handshake mode of PS2 is enabling. The TR bit (BIT 0) of PS2CON is automatically set high at the following conditions.

1:The RDATA_RDY bit (bit 0) of PS2STS of this channel is set

2:The START_DEC bit (bit 6) of PS2STS of the other channel is set

PS: The priority of three PS2 interface is

1: P1PS2
2: P2PS2
3: P3PS2

Bit 1: = 0: The default value is 0 or last D1 command set when the HGA20 enable

= 1: The default value is according to the AKBCTRL bit 0 when the HGA20 enable

Bit 0: The default value for HGA20.

10.13.1 KB Control Register (KBCTRL)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					P92EN	HGA20	HKBRST

The register KBCTRL is effective when the BUS interface is enable.

Bit 2: P92EN (Port 92 Enable)
The Port92 function is effective when the chip is in LPC mode.
A "1" on this bit enables Port 92 to control GATEA20 and KBRESET.
A "0" on this bit disables Port 92 functions.

Bit 1: HGA20 (Hardware GATE A20)
A "1" on this bit selects hardware GATEA20 control logic to control GATE A20 signal.
A "0" on this bit disables hardware GATEA20 control logic function.

Bit 0: HKBRST (Hardware Keyboard Reset)
A "1" on this bit selects hardware KB RESET control logic to control KBRESET signal.
A "0" on this bit disables hardware KB RESET control logic function.

When the KBC receives data that follows a "D1" command, the hardware control logic sets or clears GATE A20 according to the received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on the received data bit 0. When the KBC receives a "FE" command, the KBRESET is pulse low for 6µS(Min.) with 14µS(Min.) delay.

GATEA20 and KBRESET are controlled by either the software control or the hardware control logic and they are mutually exclusive. Then, GATEA20 and KBRESET are merged along with Port92 control logic when P92EN bit is set.

10.13.2 Port 92 Control Register

Host address 0x92
Default Value 0x00

Bit	7	6	5	4	3	2	1	0
Name	Res. (0)	Res. (0)	Res. (1)	Res. (0)	Res. (0)	Res. (1)	SGA20	PLKBRST

SGA20 (Special GATE A20 Control)
A "1" on this bit drives GATE A20 signal to high.
A "0" on this bit drives GATE A20 signal to low.

PLKBRST (Pull-Low KBRESET)
A "1" on this bit causes KBRESET to drive low for 6µS(Min.) with 14µS(Min.) delay. Before issuing another keyboard reset command, the bit must be cleared.

Note:

1. The external pull-up resistor is needed for both GA20 and KBRST pin.
2. The KBRST may cause a pulse low when either the chip power-up or chip reset or LRESET# received a LOW pulse.
3. If Port92 is enabled, the GA20 and KBRST are controlled by Port 92 control logic but command 0D1h or 0FEh command decoder.
4. If no special requirement, to utilize the CHIPSET's A20 and KBRST and Port 92 is recommended now.

11. I/O PORT

11.1 Port GP0 Data Register (GP0)

SFR address 0x88

Default value 0x00

If a pin is programmed to an output, then its respective bit can be read/ritten.

If a pin is programmed to an input, then its respective bit can only be read.

11.2 Port GP0 Direction Register (GP0D)

SFR address 0x89

Default value 0x00

When set to '0', respective pin is programmed as an input.

When set to '1', respective pin is programmed as an output.

11.3 Port GP1 Data Register (GP1)

SFR address 0x8A

Default value 0x00

If a pin is programmed to an output, then its respective bit can be read/ritten.

If a pin is programmed to an input, then its respective bit can only be read.

11.4 Port GP1 Direction Register (GP1D)

SFR address 0x8B

Default value 0x00

When set to '0', respective pin is programmed as an input.

When set to '1', respective pin is programmed as an output.

11.5 Port GP2 Data Register (GP2)

SFR address 0x8C

Default value 0x00

If a pin is programmed to an output, then its respective bit can be read/ritten.

If a pin is programmed to an input, then its respective bit can only be read.

11.6 Port GP2 Direction Register (GP2D)

SFR address 0x8D

Default value 0x00

When set to '0', respective pin is programmed as an input.

When set to '1', respective pin is programmed as an output.

11.7 Port GP3 Data Register (GP3)

SFR address 0x8E

Default value 0x00

If a pin is programmed to an output, then its respective bit can be read/ritten.

If a pin is programmed to an input, then its respective bit can only be read.

11.8 Port GP3 Direction Register (GP3D)

SFR address 0x8F

Default value 0x00

When set to '0', respective pin is programmed as an input.

When set to '1', respective pin is programmed as an output.

11.9 Port GP4 Data Register (GP4)

SFR address 0x90

Default value 0x00

If a pin is programmed to an output, then its respective bit can be read/ritten.

If a pin is programmed to an input, then its respective bit can only be read.

11.10 Port GP4 Direction Register (GP4D)

SFR address 0x91

Default value 0x00

When set to '0', respective pin is programmed as an input.

When set to '1', respective pin is programmed as an output.

11.11 Port GP5 Data Register (GP5)

SFR address 0x92

Default value 0x00

If a pin is programmed to an output, then its respective bit can be read/ritten.

If a pin is programmed to an input, then its respective bit can only be read.

11.12 Port GP5 Direction Register (GP5D)

SFR address 0x93

Default value 0x00

When set to '0', respective pin is programmed as an input.

When set to '1', respective pin is programmed as an output.

11.13 Port GP6 Data Register (GP6)

SFR address 0x94

Default value 0x00

If a pin is programmed to an output, then its respective bit can be read/ritten.

If a pin is programmed to an input, then its respective bit can only be read.

11.14 Port GP6 Direction Register (GP6D)

SFR address 0x95

Default value 0x00

When set to '0', respective pin is programmed as an input.

When set to '1', respective pin is programmed as an output.

11.15 Port GP7 Data Register (GP7)

SFR address 0x96

Default value 0x00

If a pin is programmed to an output, then its respective bit can be read/ritten.

If a pin is programmed to an input, then its respective bit can only be read.

11.16 Port GP7 Direction Register (GP7D)

SFR address 0x97

Default value 0x00

When set to '0', respective pin is programmed as an input.

When set to '1', respective pin is programmed as an output.

11.17 Port GP8 Data Register / Port GP4 Input Register (GP8/GP4)

SFR address 0x98

Default value 0x00

When GP8 function select bit of the Port Control Register 2 is set to 0, the register is defined as Port GP8 data register.

If a pin is programmed to be an output, then its respective bit can be read/written.

If a pin is programmed to be an input, then its respective bit can only be read.

When GP8 function select bit of the Port Control Register 2 is set to 1, the register is defined as Port GP4 input register.

The respective bit can only be read regardless of setting port GP4 direction register.

11.18 Port GP8 Direction Register / Port 7 Input Register (GP8D/GP7)

SFR address 0x99

Default value 0x00

When GP8 function select bit of the Port Control Register 2 is set to 0, the register is defined as Port GP8 direction register.

When set to a '0', respective pin is programmed as an input port.

When set to a '1', respective pin is programmed as an output port.

When GP8 function select bit of the Port Control Register 2 is set to 1, the register is defined as Port GP7 input register.

The respective bit can only be read regardless of setting port GP7 direction register.

11.19 Port Control Register 1(PCTRL1)

SFR address 0x9A

Default value 0x00

Bit 7: PWM1 enable bit

= 0 PWM1 output disable.

= 1 PWM1 output enable.

Bit 6: PWM0 enable bit

= 0 PWM0 output disable.

= 1 PWM0 output enable.

Bit 5: GP34 - GP37 pull-up control bit

= 0 No-pullup

= 1 pull-up

Bit 4: GP30 - GP33 pull-up control bit

= 0 No-pullup

= 1 pull-up

Bit 3: P14 – P17 output structure selection bit

= 0 CMOS

= 1 N-Channel open drain

Bit 2: P10 – P13 output structure selection bit

= 0 CMOS

= 1 N-Channel open drain

Bit 1: P04 – P07 output structure selection bit.

= 0 CMOS

= 1 N-Channel open drain

Bit 0: P00 – P03 output structure selection bit

= 0 CMOS

= 1 N-Channel open drain

11.20 Port Control Register 2 (PCTRL2)

SFR address. 0x9B

Default value. 0x00

Bit 7-6: Reserved.

Bit 5: Timer Y counts source selection bit

= 0 f(Xin)/16

= 1 f(Xcin)

Bit 4: INT2 INT3 INT4 interrupt source from

= 0 INT20/30/40 INTERRUPT

= 1 INT21/31/41 INTERRUPT

Bit 3: GP8 function selection bit

= 0 Port GP8/Port GP8 direction register

= 1 Port 4 input register / Port 7 input register

Bit 2: GP4 output structure selection bit

= 0 CMOS

= 1 N-Channel open drain

Bit 1: GP7 input level selection bit

= 0 CMOS level input

= 1 TTL level input

Bit 0: GP4 input level selection bit

= 0 CMOS level input

= 1 TTL level input

11.21 Port Control Register 3 (PCTRL3)

SFR address 0x9C

Default value 0x00

Bit 7: TIMER1, 2 count stop bit

= 0 Count start

= 1 Count stop

Bit 6: GP77 – GP76 interface select.

= 0 GPIO function.

= 1 SMBus 0 interface.

Bit 5: GP77 – GP76 output structure select

= 0 CMOS TYPE

= 1 N-channel TYPE open drain.

(Note: This feature is disabled now, and they are open drain only.)

Bit 4: GP75 – GP70 output structure select

= 0 CMOS TYPE

= 1 N-channel TYPE open drain.

(Note: This feature is disabled now, and they are open drain only.)

Bit 3-2: Pin 36-35 function select

= 00 GPIO

= 01 Auxiliary SMBus interface, SCL1, SDA1.

= 10 SERIAL I/O 1 TxD, RxD

= 11 Reserved.

(Note: When select item 10b, the TxD/RxD is routed to Pin 35,36, otherwise is routed to Pin 20, 21, if SERIAL IO1 is enabled.

In other words, if enable SERIAL IO1, the output pin is either Pin35, 36 or Pin20, 21.)

Bit 1: PWM3 output enable

= 0 disable PWM3 output

= 1 enable PWM3 output

Bit 0: PWM2 output enable

= 0 disable PWM2 output

= 1 enable PWM2 output

12. TIMER

The Keyboard controller has four timers: timer X, timer Y, timer 1, and timer 2. The division ratio of each timer or pre-scalar is given by 1/n + 1, where n is the value in the corresponding timer or pre-scalar latch. All timers are count down. When the timer reaches "00H", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflow, the corresponding interrupt request bit is set to 1.

12.1 Timer 1 and Timer 2

The count source of pre-scalar 12 is the oscillator frequency divided by 16. The output of pre-scalar 12 is counted for both timer 1 and 2, and a timer underflow sets the interrupt request bit.

12.2 Timer X and Timer Y

Timer X and Timer Y can works in one of four operating modes by setting the timer XY mode register.

12.2.1 Timer Mode

The Timer X only counts f(XIN)/16.

The Timer Y can select the count by f(Xin)/16 or f(Xcin).

12.2.2 Pulse Output Mode

Timer X or timer Y counts f(XIN)/16. Whenever the contents of the timer reach “00H”, the signal output from the CNTR0 (or CNTR1) pin is inverted. If the CNTR0 (or CNTR1) active edge selection bit is 0, the pin is “H” after initial. If it is 1, the pin is “L” after initial.

When using a timer in this mode, set the corresponding direction register of port GP54 (or GP55) to output mode. Also, set timer to this mode may result in the GPIO (GP54, 55) malfunctioned.

12.2.3 Event Counter Mode

Operating on event counter mode is the almost same as in timer mode, except that the timer counts signals input through the CNTR0 or CNTR1 pin. When the CNTR0 (or CNTR1) active edge selection bit is 0, the rising edge on the CNTR0 (or CNTR1) pin is counted. When the CNTR0 (or CNTR1) active edge selection bit is 1, the falling edge on the CNTR0 (or CNTR1) pin is counted.

12.2.4 Pulse Width Measurement Mode

If the CNTR0 (or CNTR1) active edge selection bit is 0, the timer counts f(XIN)/I 6 while the CNTR0 (or CNTR1) pin is H. If the CNTR0 (or CNTR1) active edge selection bit is 1, the timer counts while the CNTR0 (or CNTR1) pin is L.

The count can be stopped by setting a "1" to the timer X (or timer Y) count stop bit in any mode. The corresponding interrupt request bit is set each time a timer overflows.

The count source for timer Y in the timer mode or the pulse output mode can be selected from either f(XIN)/16 or f(XCIN) by the timer Y count source selection bit of the port control register 2 (PCTL2) .

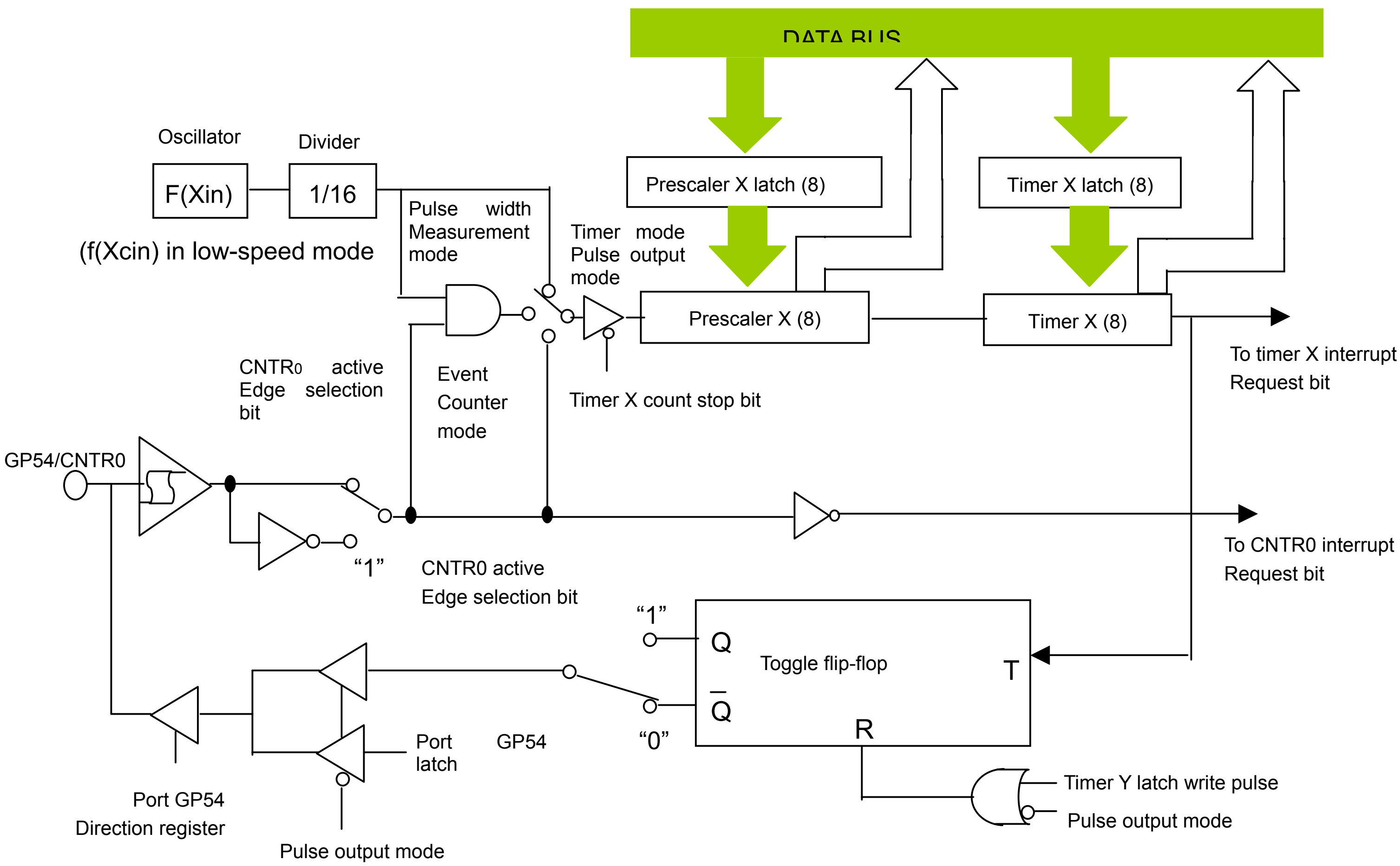


Fig.11.1 Timer X Block Diagram

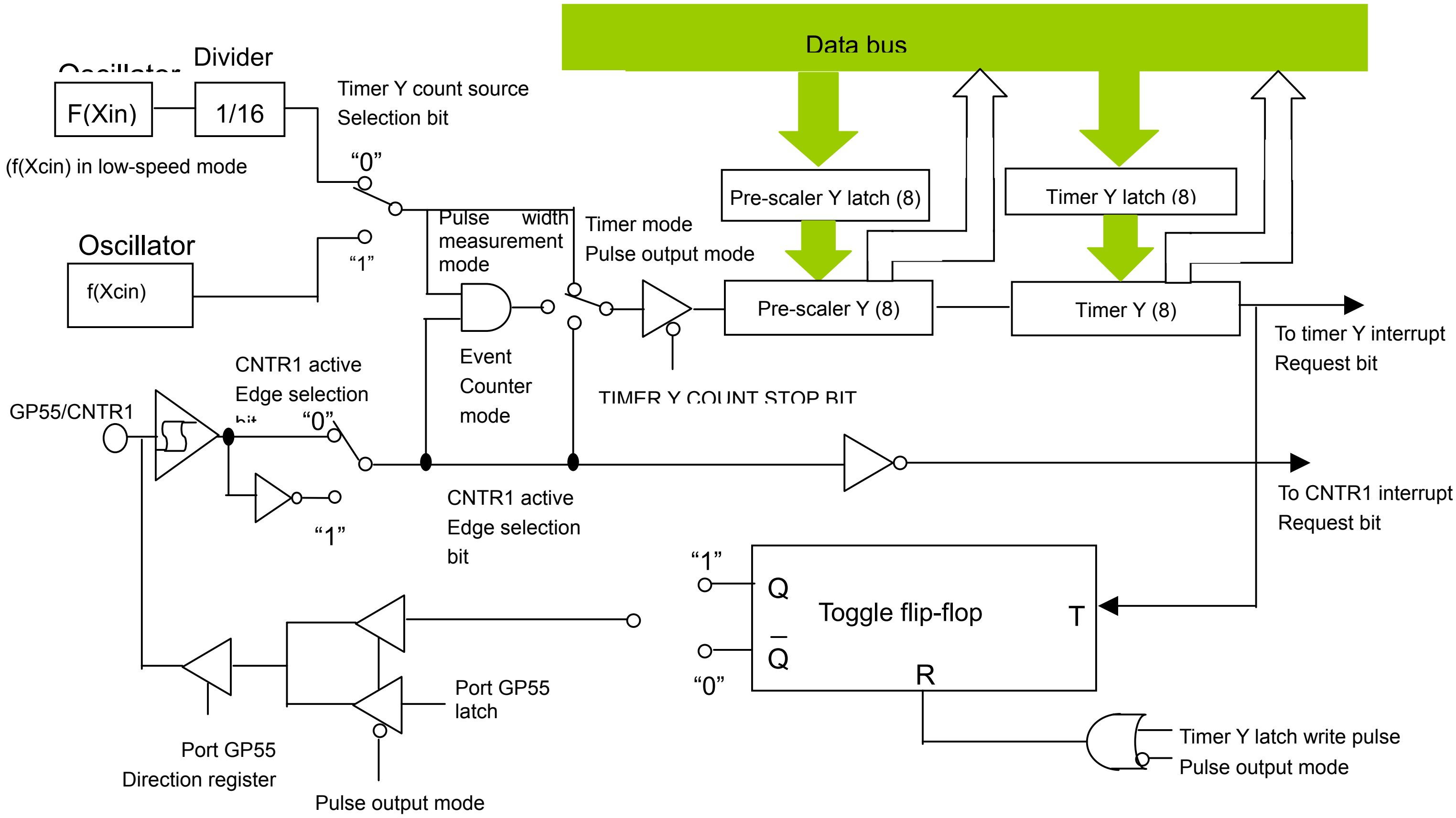


Fig.11.2 Timer Y Block Diagram

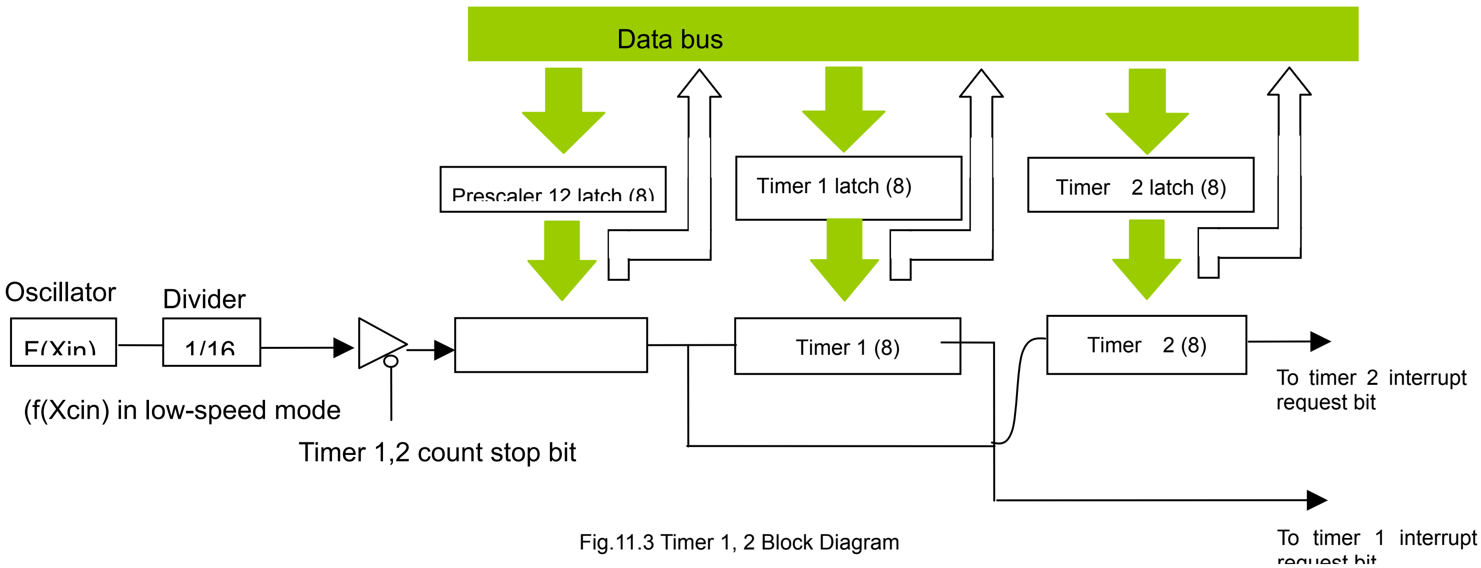


Fig.11.3 Timer 1, 2 Block Diagram

12.3 Prescaler 12 (PRE 12)

SFR address 0xB0
Default value 0xff

12.4 Timer 1 (T1)

SFR address 0xB1
Default value 0x01

12.5 Timer 2 (T2)

SFR address 0xB2
Default value 0xff

12.6 Timer XY mode register (TM)

SFR address 0xB3
Default value 0x88

Bit 7: Timer Y Count stop bit
= 0 Count start.
= 1 Count stop.

Bit 6: CNTR1 active edge selection bit
= 0 Interrupt at falling edge for CNTR1 interrupt.
Count at rising edge in event counter mode.
Output begins at H in pulse output mode.
Count at H duration in PWM mode.

= 1 Interrupt at rising edge for CNTR1 interrupt.
Count at falling edge in event counter mode.
Output begins at L in pulse output mode.
Count at L duration in PWM mode.

Bit 5-4: Timer Y operating bit
= 00: Timer mode
= 01: Pulse output mode
= 10: Event counter mode
= 11: Pulse width measurement mode

Bit 3: Timer X Count stop bit
= 0 Count start.
= 1 Count stop.

Bit 2: CNTR0 active edge selection bit
= 0 Interrupt at falling edge for CNTR0 interrupt.
Count at rising edge in event counter mode.
Output begins at H in pulse output mode.
Count at H duration in PWM mode.
= 1 Interrupt at rising edge for CNTR0 interrupt.
Count at falling edge in event counter mode.
Output begins at L in pulse output mode.
Count at L duration in PWM mode.

Bit 1-0: Timer X operating bit
= 00:Timer mode
= 01:Pulse output mode
= 10:Event counter mode
= 11:Pulse width measurement mode

12.7 Prescaler X (PREX)

SFR address	0xB4
Default value	0xff

12.8 Timer X (TX)

SFR address	0xB5
Default value	0xff

12.9 Prescaler Y (PREY)

SFR address	0xB6
Default value	0xff

12.10 Timer Y (TY)

SFR address	0xB7
Default value	0xff

13. SERIAL I/O

13.1 Serial I/O 1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

13.1.1 Clock Synchronous Serial I/O Mode

Note: There is an extra clock pulse between each data byte, please ensure if target device support this behavior.

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (SIO1CON) to '1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock If an internal clock is used, transfer is started by a write signal to the TB/RB.

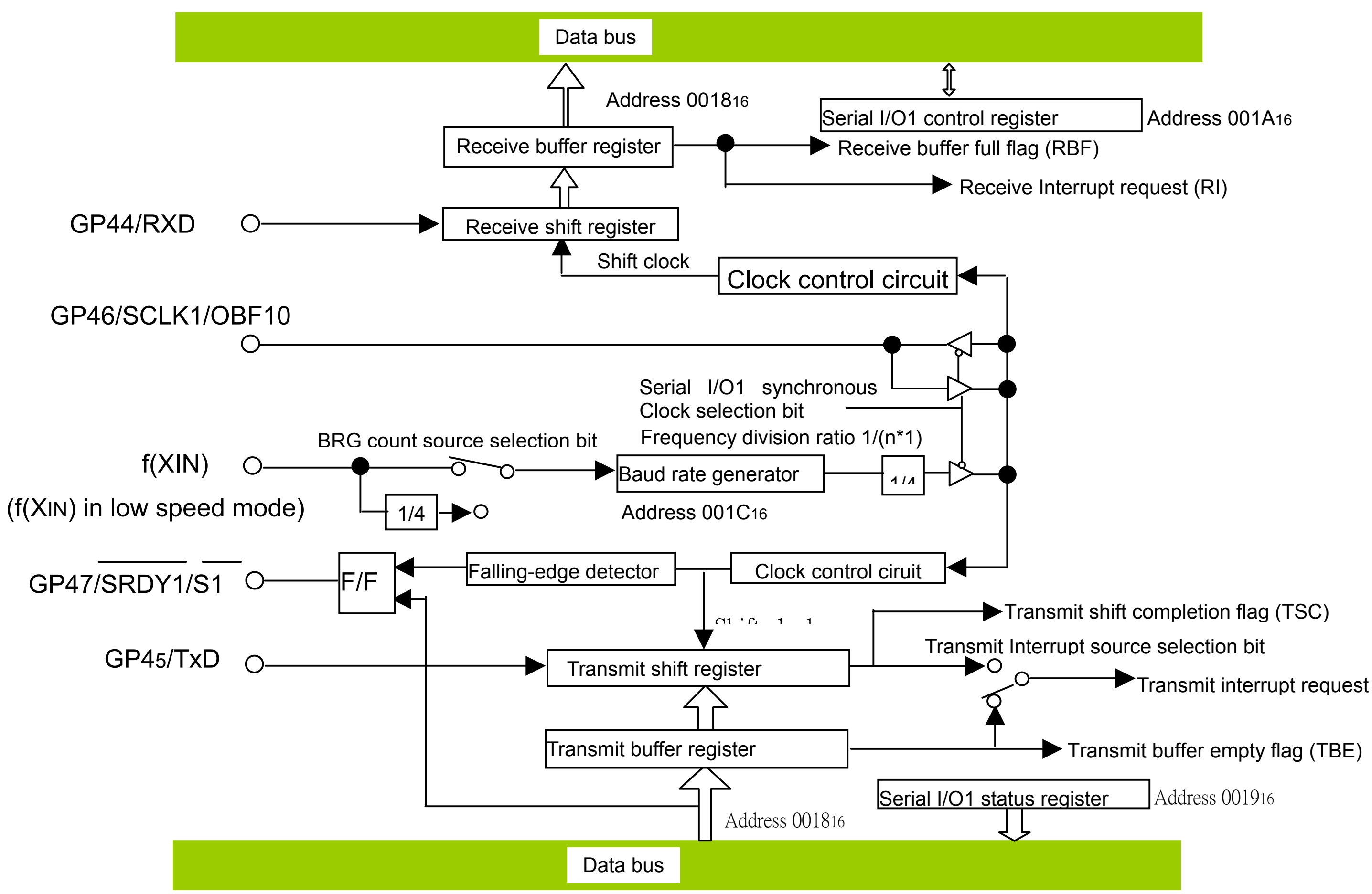


Fig.12.1 Clock Synchronous Serial I/O Mode Block Diagram

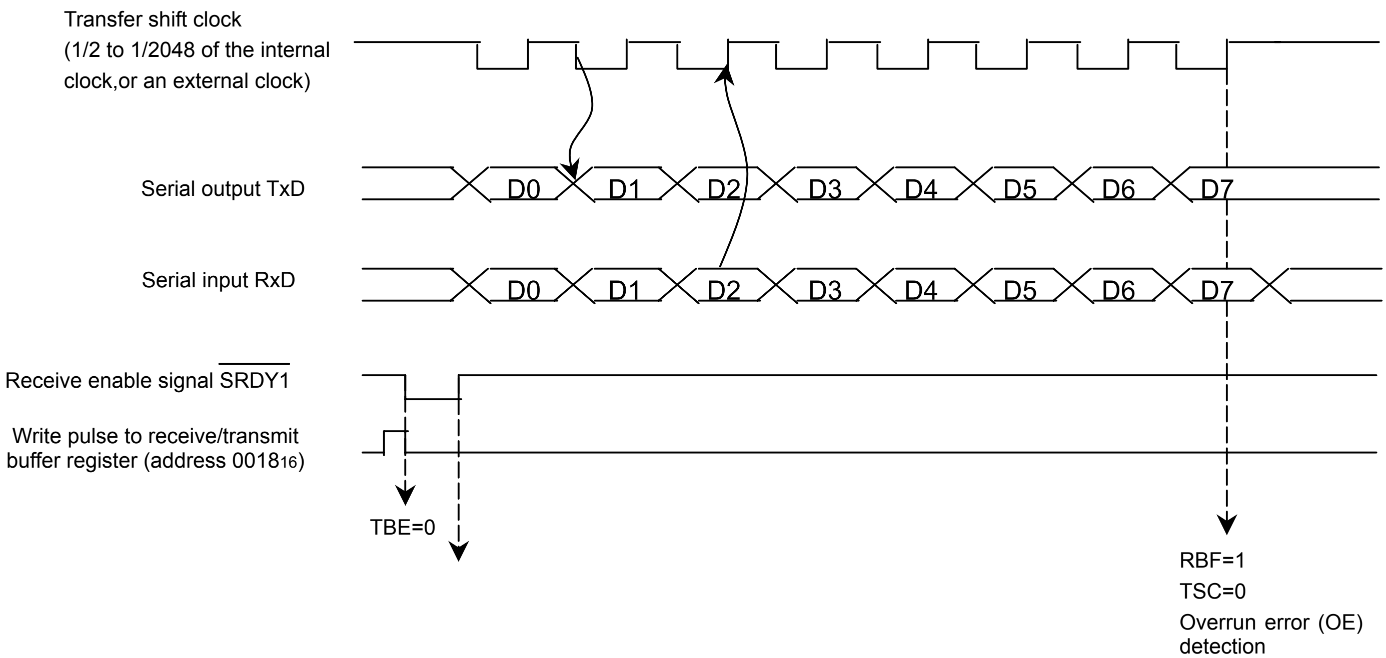


Fig.12.2 Clock Synchronous Serial I/O 1 Mode Operation

13.1.2 Asynchronous Serial I/O (UART) Mode

Universal asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit of the serial I/O1 control register to 0.

Eight serial data transfer formats can be selected, for vary selection of Stop bit, Parity, Parity check, Data length, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register. The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a byte while the next byte is being received.

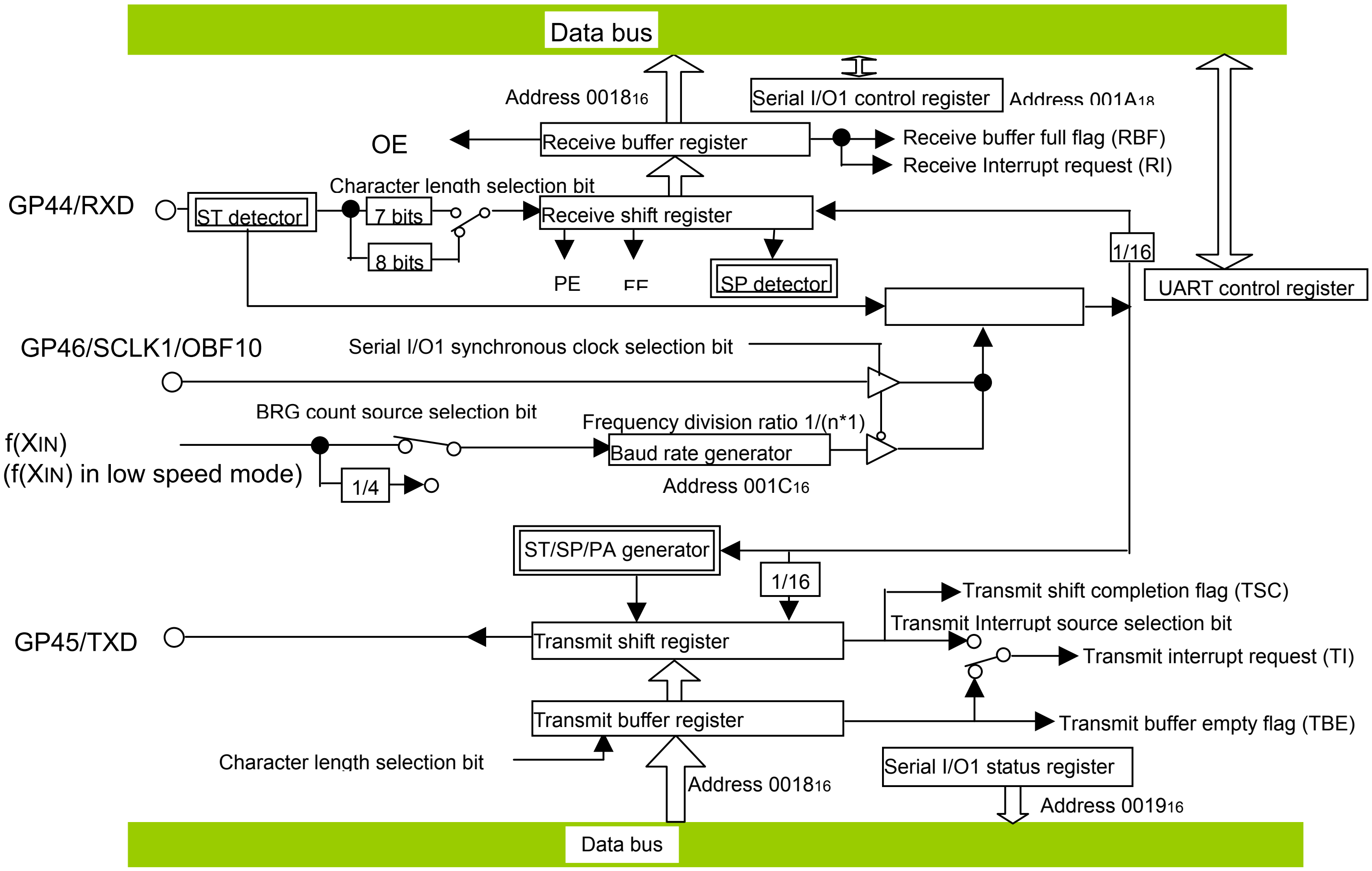


Fig.12.3 UART Serial I/O Diagram

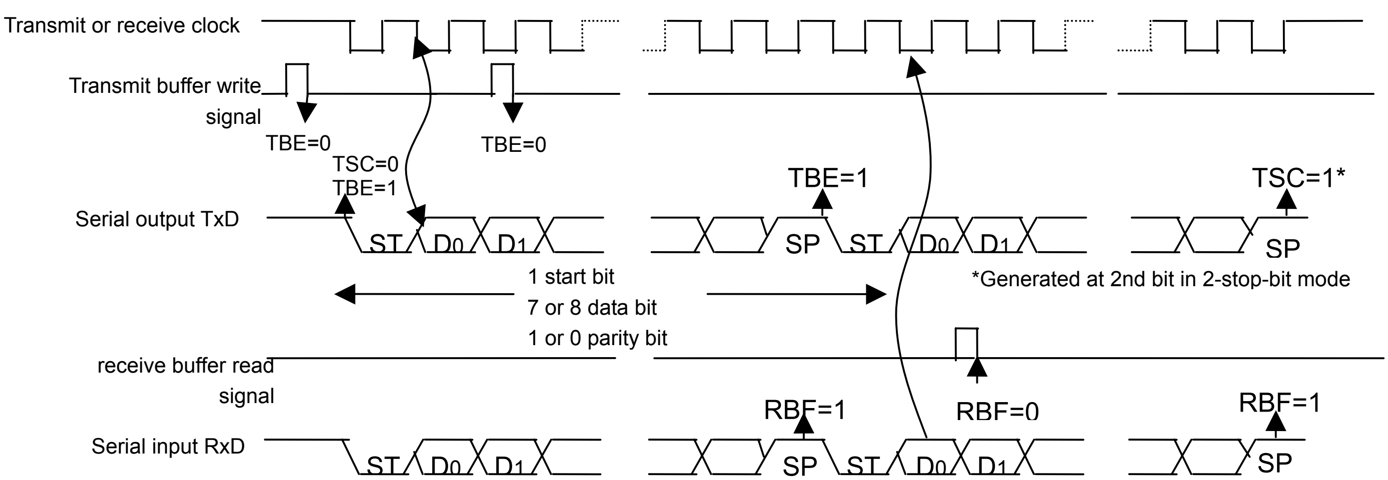


Fig.12.4 UART Serial I/O 1 Function Operation

13.1.3 Transmit / Receive buffer register (TB/RB)

SFR address 0xC8

Default value XX

The transmitting buffer register and the receiving buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits the MSB of data stored in the receive buffer is '0'.

13.1.4 Serial I/O 1 status register (SIO1STS)

SFR address 0xC9

Default value 0x80

Bit 7: No use (return "1" when read)

Bit 6: Summing error flag (SE)

= 0: (OE) U (PE) U (FE) =0

= 1: (OE) U (PE) U (FE) =1

Bit 5: Framing error flag (FE)

= 0: No error

= 1: Framing error

Bit 4: Parity error flag (PE)

= 0: No error

= 1: Parity error

Bit 3: Overrun error flag (OE)

= 0: No error

= 1: Overrun error

Bit 2: Transmit shift completion flag (TSC)

= 0: Transmit shift in process

= 1: Transmit shift complete

Bit 1: Receive buffer full flag (RBF)

= 0: Buffer empty

= 1: Buffer full

Bit 0: Transmit buffer empty flag (TBE)

= 0: Buffer full

= 1: Buffer empty

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) that indicate the operating status of the serial I/O function and various errors. Three of the flags (bits 4 to 6) are valid only in UART mode. The Receive Buffer Full flag (bit 1) is cleared to "0" when the Receive Buffer Register is read. If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O 1 status register clears all the error flags OE, PE, FE, and SE in respectively. Writing "0" to the serial I/O1 enable bit (SIOE), bit 7 of the serial I/O control register, also clears all the status flags, including the error flags. The bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4 of the serial I/O1 control register) has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) are become "1".

13.1.5 Serial I/O 1 control register (SIO1CON)

SFR address 0xCA
Default value 0x00

The serial I/O1 control register consists of eight control bits for the serial I/O function.

Bit 7: Serial I/O1 enable bit (SIOE)
= 0: Serial I/O disable.
= 1: Serial I/O enabled
Bit 6: Serial I/O1 mode selection bit (SIOM)
= 0: Clock asynchronous (UART) serial I/O.
= 1: Clock synchronous serial I/O.
Bit 5: Receive enable bit (RE)
= 0: Receive disabled.
= 1: Receive enable.
Bit 4: Transmit enable bit (TE)
= 0: Transmit disabled.
= 1: Transmit enable.
Bit 3: Transmit interrupt source selection bit (TIC)
= 0: interrupt when transmit buffer has emptied.
= 1: interrupt when transmit shift operation is completed.
Bit 2: $\overline{SRDY1}$ output enable bit (SRDY)
= 0: P47 pin operates as ordinary I/O pin.
= 1: P47 pin operates as $\overline{SRDY1}$ pin.
Bit 1: Serial I/O 1 synchronous clock selection bit (SCS)
= 0 BRG output will divided by 4 when clock synchronous serial I/O is selected. BRG output will divided by 16 when UART is selected.
= 1 External clock input when clock synchronous serial I/O is selected. External clock input divided by 16 when UART is selected.
Bit 0: BRG count source selection bit (CSS).
= 0: f(XIN) (f(Xcin) in low sped mode)
= 1: f(XIN) / 4 (f(Xcin) / 4 in low sped mode)

13.1.6 UART control register (UARTCON)

SFR address 0xCB
Default value 0xE0

Bit 7-5: No used (return 1 when read)
Bit 4: TxD 0/1 output structure bit
= 0: CMOS output.

= 1: N-channel open drain output.

Bit 3: Stop bit length selection bit (STPS)

= 0: 1 stop bit.

= 1: 2 stop bits.

Bit 2: Parity selection bit (PARS).

= 0: Even parity.

= 1: Odd parity.

Bit 1: Parity enable bit (PARE).

= 0: Parity disabled.

= 1: Parity enable.

Bit 0: Character length selection bit(CHAS) .

= 0: 8 bits.

= 1: 7 bits.

The UART control register consists of four control bits (bits 0 to 3) that are valid when asynchronous serial I/O is selected and set the data format of a data transfer and one bit (bit 4), which is always valid and sets the output structure of the TxD 0/1 pin.

13.1.7 Baud rate generator (BRG)

SFR address 0xCC

Default value 0x00

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by 1/(n), where n is the value written to the baud rate generator.

13.2 Serial I/O 2

The serial I/O2 function can be used only for clock synchronous serial I/O. For clock synchronous serial I/O, the transmitter and the receiver must use the same clock If the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

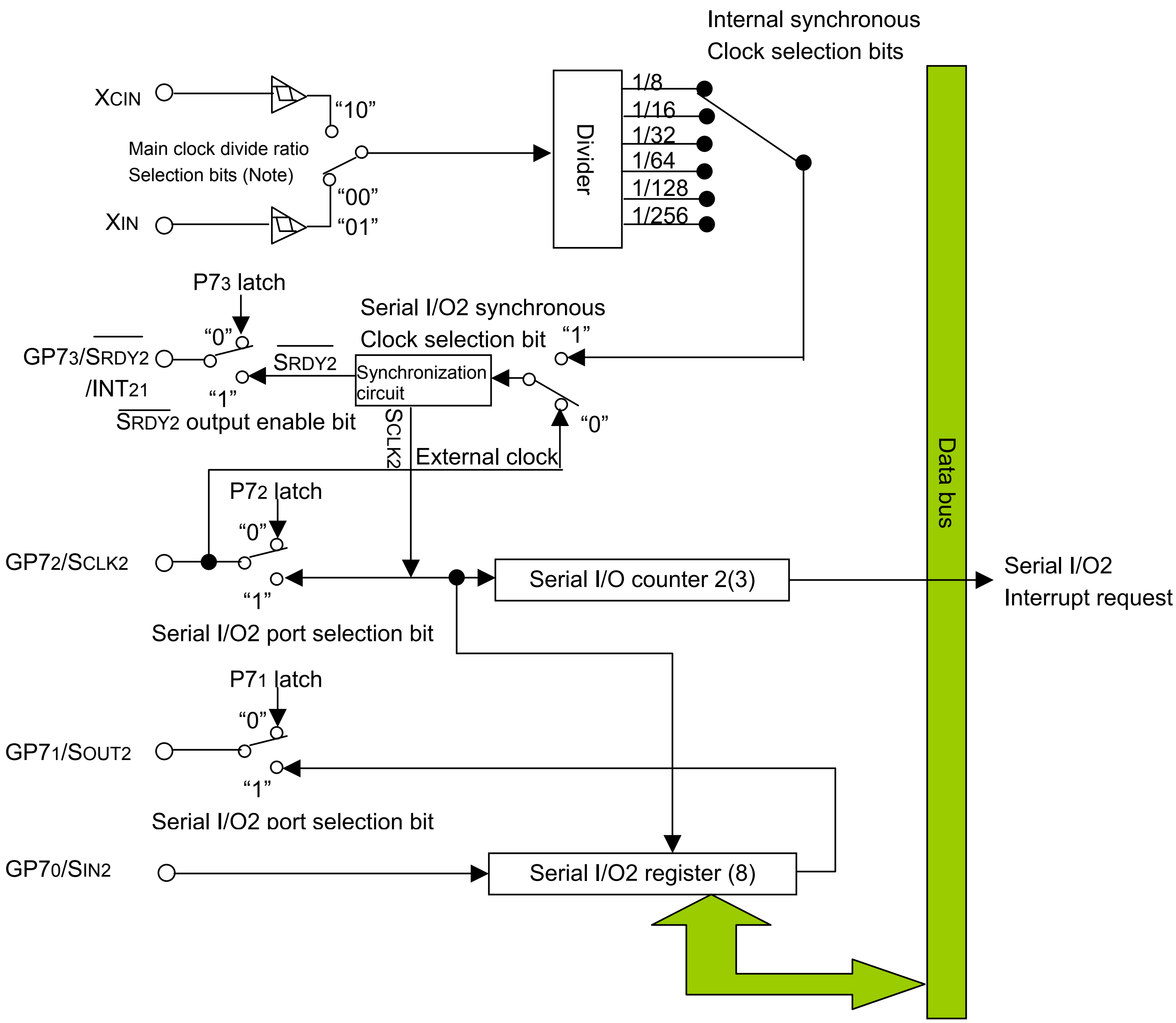


Fig.12.5 Serial I/O 2 Function Block Diagram

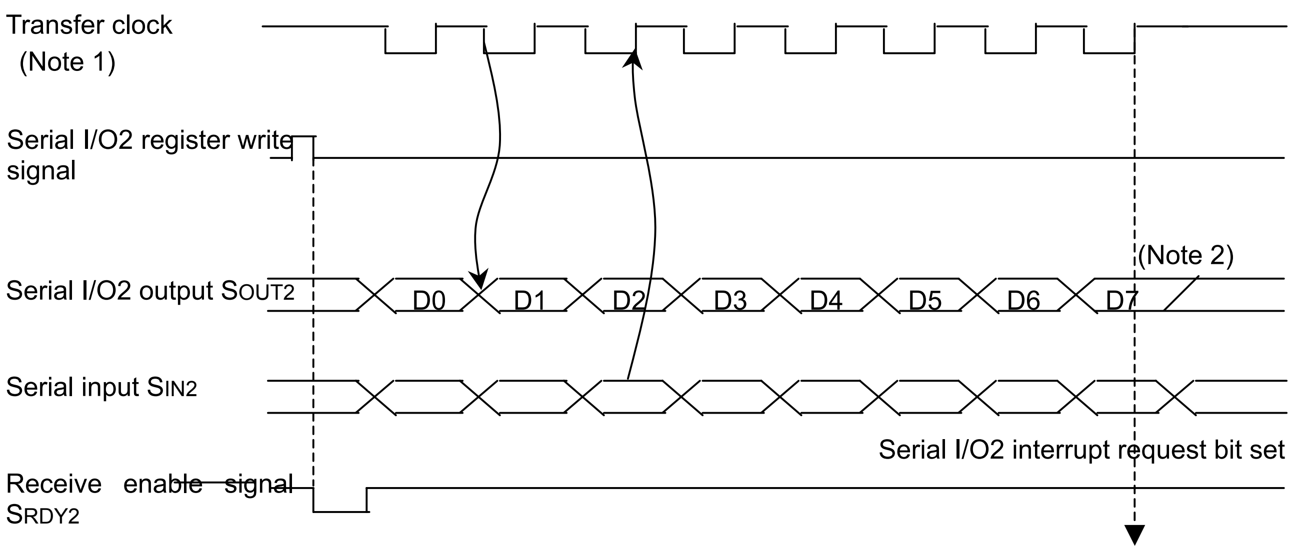


Fig.12.6 Serial I/O 2 Timing

13.3 Serial I/O 2 control register (SIO2CON)

SFR address 0xCD

Default value 0x00

Bit 7: Comparator reference input selection bit.

= 0: P00 /P3ref input.

= 1: Reference input fixed.

Bit 6: Serial I/O2 synchronous clock selection bit.

= 0: external clock.

= 1: internal clock.

Bit 5: Transfer direction selection bit.

= 0: LSB first.

= 1: MSB first.

Bit 4: $\overline{SRDY2}$ output enable bit.

= 0: I/O port.

= 1: $\overline{SRDY2}$ signal output.

Bit 3: Serial I/O2 port selection bit

= 0: I/O port.

= 1: Sout2 Sclk2 signal output.

Bit2 – 0: Internal synchronous clock selection bits.

= 000: f (XIN) / 8 (f (Xcin) / 8 in low sped mode).
= 001: f (XIN) / 16 (f (Xcin) / 16 in low sped mode).
= 010: f (XIN) / 32 (f (Xcin) / 32 in low sped mode).
= 011: f (XIN) / 64 (f (Xcin) / 64 in low sped mode).
= 110: f (XIN) / 128 (f (Xcin) / 128 in low sped mode).
= 111: f (XIN) / 256 (f (Xcin) / 256 in low sped mode).

The serial I/O2 control register contains seven bits, which control various serial I/O functions.

13.4 Serial I/O2 register (SIO2)

SFR address	0xCF
Default value	0x00

14. PWM

There are four PWM output in the Winbond Keyboard controller. The PWM0 and 1 are compatible with the 3886 group of the MITSUBISHI and is 14-bit controller. The PWM2 and 3 is new feature of the Winbond keyboard controller. The relative register of PWM2 and 3 is defined on Advance Register region. And is described in the later chapter.

Note:

The PWM 0,1 enable bit are located in Port Control Register 1(PCTRL1).

The PWM 0,1 output pin selection is located in AD control register (ADCON).

14.1 PWM 0 and 1 Operation

The 14-bit PWM data is divided into the low-order six bits and the high-order eight bits in the PWM latch and are fixed frequency at 15.6KHz. The high-order eight bits PWMH determines how long an "H"-Level signal is output during each period. Each period is divided into 256 grades but 255, hence to set PWMH to maximum 255 may NOT result in Always High output on PWM signal, there is a bit pulse low occurred. The low-order six bits PWML is used to adjust the PWM sub-period, however this sub-period adjustment is no much useful in most application.

For example:

Set PWMH to 192, PWML to 0, may result in a 75% duty cycle.

Set PWMH to 127, PWML to 0, may result in a 50% duty cycle.

and so on.

14.2 Transfer From Register to Latch

Data written to the PWML register is transferred to the PWM latch at each PWM period (every 4096 us), and data written to the PWMH register is transferred to the PWM latch at each sub-period (every 64 us). The signal is output to the PWM output pin is corresponding to the contents of this latch. When the PWML register is read, the latch contents are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is '0" and it is not done when bit 7 is '1".

14.3 PWM0H register (PWM0H)

SFR address 0xD4

Default value xxxxxxxxb

14.4 PWM0L register (PWM0L)

SFR address 0xD5

Default value x0xxxxxxb

14.5 PWM1H register (PWM1H)

SFR address 0xD6

Default value xxxxxxxxb

14.6 PWM1L register (PWM1L)

SFR address 0xD7

Default value x0xxxxxxb

15. AUXILIARY PWM CHANNLE

The PWM2 and 3 is auxiliary PWM channel. These two PWM channels are 16 bits operation .The minimum resolution depend on the input CLK frequency. The frequency may be 8Mhz, 16Mhz, 32Mhz, i.e., 125ns, 62.5ns, 31.25ns.

Note:

The PWM 2,3 enable bit are located in Port Control Register 3(PCTL3).

15.1 AUXILIARY PWM Controller Register (APWMCON)

Advance address 0x1C

Bit 1-0: PWM channel 2 input frequency select

00: 8M.

01: 16M

10: reserve

11: 32M

Bit 2: Reserved.

Bit 3: PWM channel 2 CLOCK SOURCE SELECT

0: PWM channel 2 clock source is PLL and bit 1-0 is effective

1: PWM channel 2 clock source is the same as 8051 CLOCK.

(Note: This selection is disabled. Set to 0 by default.)

Bit 5-4: PWM channel 3 input frequency select

00: 8M.

01: 16M

10: Reserved.

11: 32M

Bit 6: Reserved.

Bit 7: PWM channel 3 CLOCK SOURCE SELECT

0: PWM channel 3 clock source is PLL and bit 5-4 is effective

1: PWM channel 3 clock source is the same as 8051 CLOCK.

(Note: This selection is disabled. Set to 0 by default.)

15.2 PWM CHANNLE 2 PERIOD Low BYTE (PWM2PL)

Advance address 0x20

Default value A0

14.3 PWM CHANNLE 2 PERIOD High BYTE (PWM2PH)

Advance address 0x21

Default value 0x00

The PWM2PH, PWM2PL 16-bit register is defined as PWM 2 period register. For example, if the PWMP2H is 0x00 and the PWMP2L is 0xff, the PWM 2 period is 255 x T (T is 1/current clock source).

14.4 PWM CHANNLE 2 HIGH SIGNAL Low BYTE (PWM2HSL)

Advance address 0x22

Default value 0x50

14.5 PWM CHANNLE 2 HIGH SIGNAL High BYTE (PWM2HSH)

Advance address 0x23

Default value 0x00

The PWM2HSL, PWM2HSH 16-bit register is defined as PWM 2 high signal length register. If the value of {PWM2HSH, PWM2HSL} is larger or equal to the value of the {PWM2PH, PWM2PL}, the PWM channel always output high.

14.6 PWM CHANNLE 3 PERIOD Low BYTE (PWM3PL)

Advance address 0x24

Default value 0xA0

14.7 PWM CHANNLE 3 PERIOD High BYTE (PWM3PH)

Advance address 0x25

Default value 0x00

14.8 PWM CHANNLE 3 HIGH SIGNAL Low BYTE (PWM3HSL)

Advance address 0x26

Default value 0x50

14.9 PWM CHANNLE 3 HIGH SIGNAL High BYTE (PWM3HSH)

Advance address 0x27

Default value 0x00

The four PWM channel 3 registers, PWM3PH, PWM3PL, PWM3HSH, PWM3HSL is the same as PWM2.

The formula for duty cycle is:

PWM2HSH, PWM2HSL

PWM2PH, PWM2PL

For example:

Select clock from 8MHz in bit 1,0 of APWMCON,
Set PWM2PL to 0FFh
Set PWM2PH to 0FFh
Set PWM2HSL to 0FFh
Set PWM2HSH to 07Fh
May generate a 122Hz and 50% duty cycle output signal .

16. A-D CONVERTER

The A-D conversion register is a read-only register that stores the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

Bit 7 of the A-D conversion register 2 is the conversion mode selection bit. When this bit to "0", the A-D converter becomes the 10-bit A-D mode. When this bit is set to "1", that becomes the 8-bit A-D mode. The conversion result of the 8-bit A-D mode is stored in the A-D conversion register 1. As for 10-bit A-D mode, 10-bit reading or 8-bit reading can be performed by selecting the reading procedure of the A-D conversion register 1, 2 after A-D Conversion is completed. (in blowing figure).

10-bit reading (Read AD2 before AD1)

AD2

						b9	b8

AD1

b7	b6	b5	b4	b3	b2	b1	b0

8-bit reading (Read only AD1)

AD1

b9	b8	b7	b6	b5	b4	b3	b2

The A-D conversion register 1 performs the 8-bit reading inclined to MSB. After reset, the A-D conversion is started, or reading of the A-D converter register 1 is generated; and the register becomes the 8-bit reading inclined to LSB after the A-D converter register 2 is generated.

Note: The AD pins should be programmed to INPUT mode for AD input purpose.

Channel Selector

The channel selector selects one of ports GP60/AD0 to GP67/AD7, and inputs the voltage to the comparator.

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage, and then stores the result in the A-D conversion registers 1,2. When an A-D conversion is completed, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to '1".

16.1 AD/DA control register 0(ADCON)

SFR address 0xE2

Default value 0000,1000b

Bit 7: DA1 output enable bit
- 0: A1 output disabled.
- 1: A1 output enable.

Bit 6: DA0 output enable bit
- 0: DA0 output disabled.
- 1: DA0 output enable.

Bit 5: PWM1 output pin selection bit
- 0: P57 / PWM11
- 1: P31 / PWM10

Bit 4: PWM0 output pin selection bit
- 0: P56 / PWM01
- 1: P30 / PWM00

Bit 3: A-D conversion complete bit
- 0: conversion in progress.
- 1: conversion completed.

Bit 2-0: Analog input pin selection bits
- 000: P60/AD0
- 001: P61/AD1
- 010: P62/AD2
- 011: P63/AD3
- 100: P64/AD4
- 101: P65/AD5
- 110: P66/AD6
- 110: P67/AD7

The AD/DA control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at “0" during an A-D conversion, and changes to "1" when an A-D conversion end. Writing '0" to this bit starts the A-D conversion.

16.2 A/D conversion register 0(AD0)

SFR address 0xE3

Default value 0x00

16.3 A/D conversion register 1(AD1)

SFR address 0xE4

Default value. 0x00

16.4 D-A Converter

The keyboard controller has two internal D-A converters (DA1 and DA0) with 8-bit resolution. The result of D-A conversion is output from the DA1 or DA0 pin by setting the DA output enable bit to "1".

When using the D-A converter, the corresponding port direction register bit (P56/DA0/PWM01 or P57/DA1/PWM11) must be set to '0" (input state). The output analog voltage V is determined by the value n (decimal notation) in the D-A conversion register as follows,

V - VREF X n/256 (n - 0 to 255), where VREF is the reference voltage.

At reset, the D-A conversion registers are cleared to "00h", the DA output enable bits are cleared to "0", and the P56/DA0/PWM01 and P57/DA1/PWM11 pins become high impedance. The DA output does not have buffers accordingly, connect an external buffer when driving a low-impedance load.

16.5 D-A Conversion Register 0(DA0)

SFR address 0xE5

Default value 0x00

16.6 D-A Conversion Register 1(DA1)

SFR address 0xE6

Default value 0x00

17. COMPARATOR CIRCUIT

The comparator circuit consists of resistors, comparators, a comparator control circuit, the comparator reference input selection bit (bit 7 of SIO2CON), a comparator data register (CMPD), the comparator reference power source input pin (P00/ P3REF) and analog signal input pins (P3o-P37) The analog input pin (P30-P37) also functions as an ordinary digital port

17.1 Comparator Operation

To activate the comparator, first set port P3 to input mode by set- ting the corresponding direction register (P3D to "0" to use port P3 as an analog voltage input pin. The internal fixed analog voltage (Voc x 29/32) can be generated by setting "1" to the comparator reference input selection bit (bit 7) of the serial 1/O2 control register (SIO2CON) (The internal fixed analog volt- age becomes about 4 5 V at VCC - 50 V). When setting "0" to the comparator reference input selection bit, the P00/P3REF pin be- comes the comparator reference power source input pin and it is possible to input the comparator reference power source optionally from the external.

The voltage comparison is immediately performed by the writing operation to the comparator data register (CMPD). If the analog input voltage is greater than the internal reference voltage, each bit of this register is '1 "; if it is less than the internal reference voltage, each bit of this register is "0" .To perform another comparison, the voltage comparison must be performed again by writing to the comparator data register (CMPD).

17.2 Comparator Data Register (CMPD)

SFR address	0xE7
Default value	xxxxxxxxb

18. WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset state when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit timer L and an 8-bit timer H.

17.1. Standard Operation of Watchdog Timer

When any data is not written into the watchdog timer control register (WDTCON) after resetting, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (WDTCON) and an internal reset occurs at an underflow of the watchdog timer H. Accordingly, programming is usually performed so that writing to the watchdog timer control register (WDTCON) should be started before an underflow. When the watchdog timer control register (WDTCON) is read, the values of the high-order 6 bits of the watchdog timer H, IDLE mode disable bit, and watchdog timer H count source selection bit are read.

17.2. Initial Value of Watchdog Timer

At reset or writing to the watchdog timer control register (WDTCON), each watchdog timer H and L is set to 0FFh.

17.3. Watchdog Timer H Count Source Selection Bit Operation

Bit 7 of the watchdog timer control register (WDTCON) permits selecting a watchdog timer H count source. When this bit is set to '0", the count source becomes the underflow signal of watchdog timer L. The detection time is set to f(XIN) = 131.072 ms at 8 MHz frequency and f(XCIN) = 32.768 s at 32 KHz frequency. When this bit is set to '1", the count source becomes the signal divided by 16 for f (XIN) or f (XCIN). The detection time in this case is set to f(XIN) = 512 us at 8 MHz frequency and f(XCIN) = 128 ms at 32 kHz frequency. This bit is cleared to '0" after reset.

17.4. IDLE Mode Disable Bit

Bit 6 of the watchdog timer control register (WDTCON) permits disabling the IDLE mode when the watchdog timer is in operation. When this bit is "0", the IDLE bit of PCON can be written to "1". When this bit is "1', the IDLE mode is disabled. When this bit is set to "1", it cannot be rewritten to "0" by program, this bit is cleared to '0" after reset.

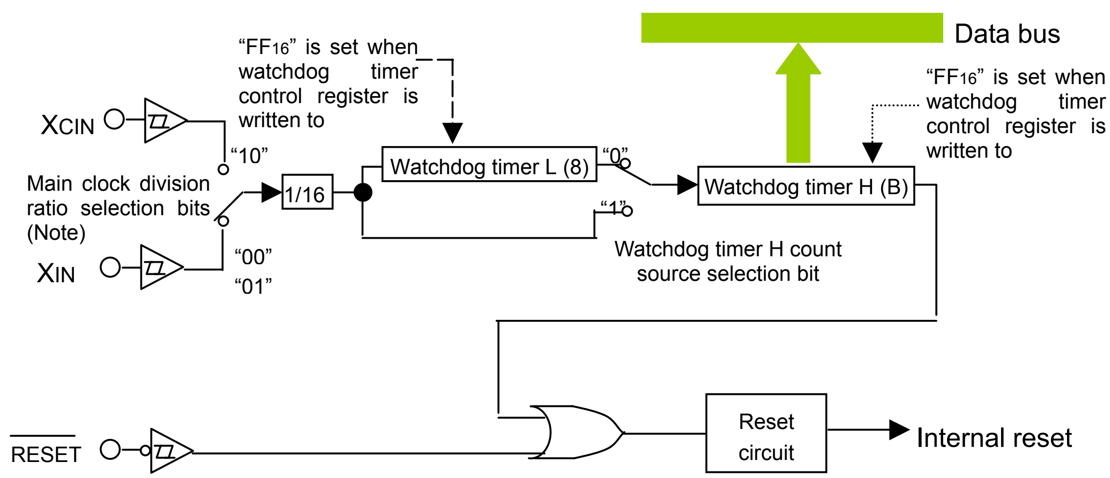


Fig.17.1 Watchdog Timer Block Diagram

17.5. Watchdog timer control register (WDTCON)

SFR address 0xCE

Default value 0011,1111b

Bit 7: Watchdog timer H count source selection bit

0: Watchdog timer L underflow.

1: f (XIN)/16 or f(Xcin)/16.

Bit 6: Watchdog timer IDLE mode disable bit

0: Enable IDLE mode when watchdog timer running.

1: Disable IDLE mode when watchdog timer running.

Bit 5 – 0: Watchdog timer H

(For read-out of high-order 6 bit)

19. FLASH MEMORY

19.1 On chip program flash memory

19.1.1 SFRAH, SFRAL(0F9h, 0F8h)

The programming address of on-chip flash memory is separated into two registers. The SFRAH contains the high order byte of address; the SFRAL contains the low-order byte of address.

18.1.1 SFRFD (0FAh)

This is a programming data byte for on-chip flash memory.

18.1.2 SFRCN (0FBh)

This is a flash control byte for on-chip flash memory.

BIT	NAME	FUNCTION
7	NOE	MTP-ROM output enable
6	NCE	MTP-ROM chip enable
5-4	Reserved	
3-0	CTRL[3:0]	The flash control signals

MODE	NOE	NCE	CTRL<3:0>	SFRAH, SFRAL	SFRFD
Erase all bank	1	0	0110	X	X
Program APROM	1	0	0001	Address in	Data in
Read APROM	0	0	0000	Address in	Data out

19.2 External Programming Mode

The context of flash in Winbond Keyboard controller is empty by default. At the first use, you must program the flash by external writer device. For programming the flash by external device, the Winbond Keyboard controller must enter the flash-programming mode by CNvss is connected to VCC. RESET# is connected to VCC, GP35 is connected to VSS. FA<7:0> and FD<7:0> port is combined to GP07 to GP00. FA<7:0> is latched by the GP34.

The setting conditions and the timing are shown as following.

MODE	GP37 (FOEN)	GP36 (FCEN)	GP33-GP30 (FCTRL<3:0>)	GP1<7:0>, GP0<7:0> (FA<15:0>)	GP0<7:0>
Standby	1	1	X	X	X
Read APROM	0	0	0000	Address in	Data out
Program APROM	1	0	0001	Address in	Data in
Erase All	1	0	0110	X	X
Erase one page (512 bytes)	1	0	1111	Address in	X
40K program verify	0	0	1010	Address in	Data out
40K erase verify	0	0	1001	Address in	Data out
40K Read-Disturb	0	0	1110	Address in	Data out

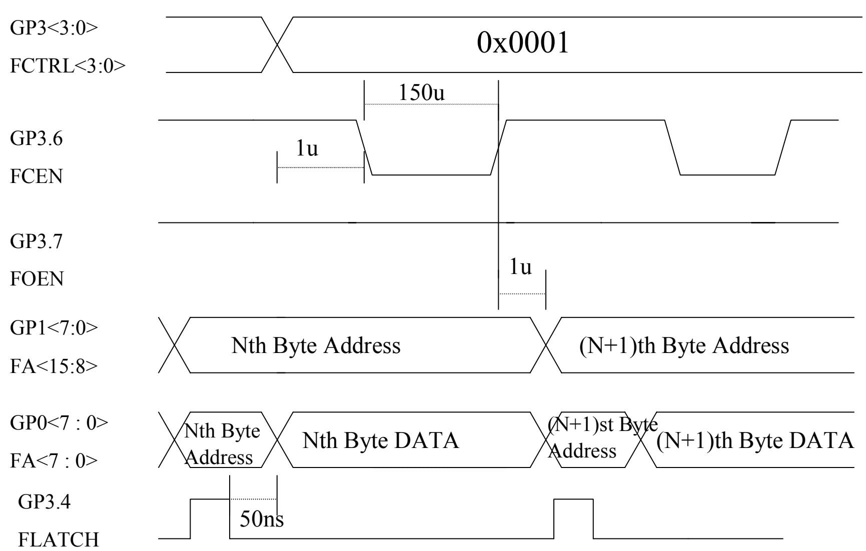


Fig.18.1 The Programming Timing

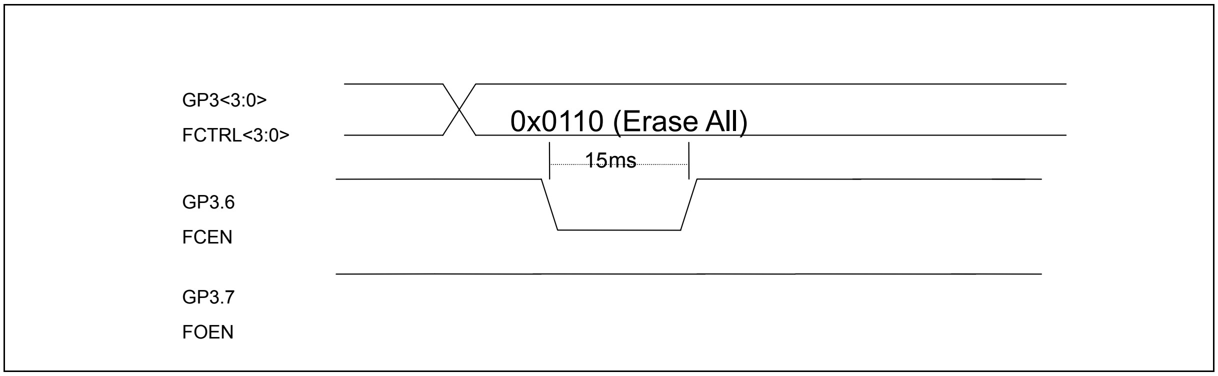


Fig.18.2 The Erase Timing

Note: The delay timing for ERASE should be extended to 30ms.

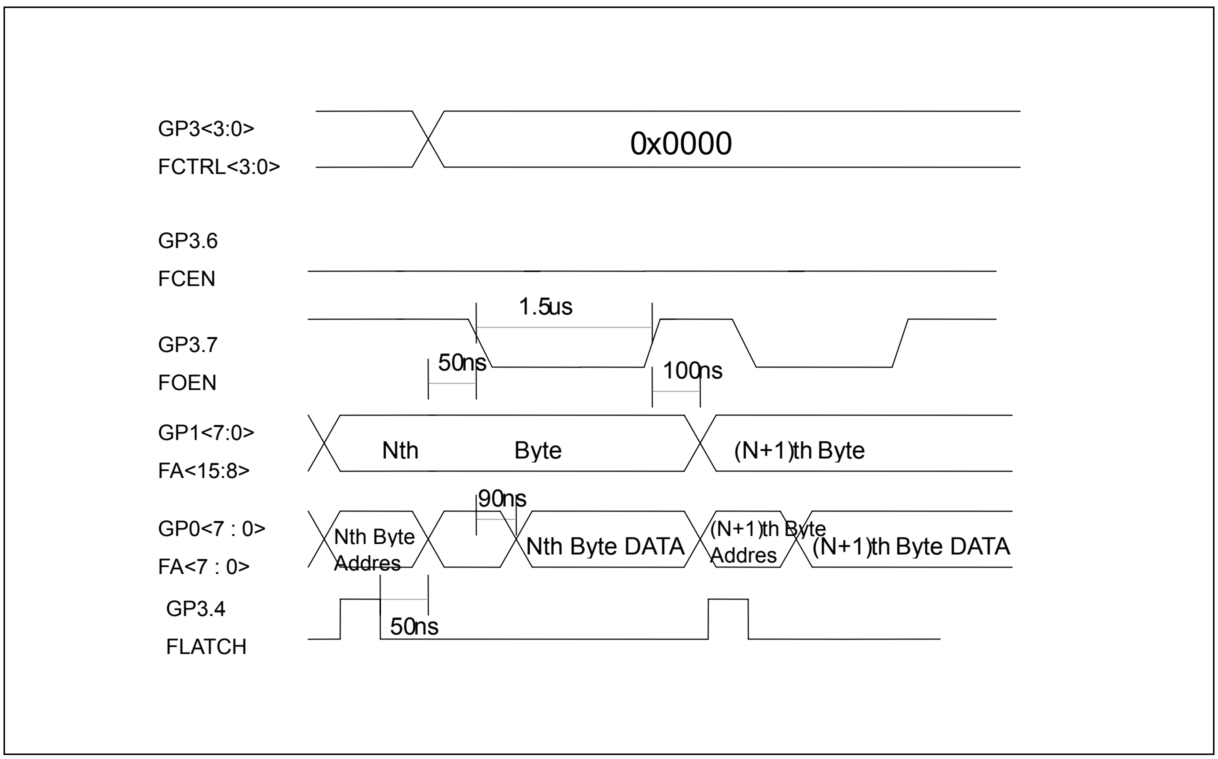


Fig.18.3 The Read Timing

20. PS/2 DEVICE INTERFACE

The Winbond Keyboard controller has three hardware PS/2 channels. Each of them uses the synchronous serial protocol to communicate with the auxiliary device. Each PS/2 channel has two exclusive signal lines, Clock and Data, which are bi-directional and employed as open drain structure. The relative register is defined on Advance register space .The PS2DATA, PS2CON and PS2STS is defined individually for each PS/2 channel. PS2STS_2 is only one register for all PS/2 register to indicate each PS2 channel's busy state.

20.1 PS/2 Transmit and Receive DATA Registers (PS2DATA)

Advance address 0x10, 0x14, 0x18

The PS2 control logic employs two internal registers, Transmit Register and Receive Register, to serve the data transmission and reception. In order to these two registers shared the same SFR address, accessing to either of them should obey the rule described below.

20.1.1 Transmit Register

When PS2_T/R, PS2_EN, and XMIT_IDLE are set, and RDATA_RDY is cleared, a data writing to this register invokes a transmission on PS2 channel. If any of three bits (PS2_T/R, PS2_EN, and XMIT_IDLE) are not set, then writes to this register is ignored. Even If PS2_T/R, PS2_EN, and XMIT_IDLE are all set but RDATA_RDY is set, a data writing to this register will not kick off a transmission but stayed in Transmit Register until the RDATA_RDY is cleared (by a read of Receive Register). A data where stored in Receive Register should be read before next transmission.

After a success of transmission or upon a Transmit Time-out condition, the PS2_T/R bit is automatically cleared and the XMIT_IDLE bit is automatically set. Before transfer data to an auxiliary device, be sure the PS2_T/R bit is set to a '1' is required. An interrupt is generated on the low to high transition of XMIT_IDLE. All bits of this register are write-only.

20.1.2 Receive Register

When PS2_EN = 1 and PS2_T/R = 0, the PS2 Channel is set to automatically receive mode, which both CLK and DATA signals are float to indicate the channel now is in "Auxiliary device transmit permission mode" by pull-up them to 1.

After a success of reception, a data is placed in this register and the RDATA_RDY bit is set and the CLK line is driven to LOW until a read of this register. Also the RDATA_RDY is cleared after this read. This feature intends to provide a fluent reception flow control. Besides, there are some of auxiliary device has a restriction of data package rate, the firmware should read the data from this register as quickly as possible to maintain the best performance. All bits of this register are read-only.

The Receive Register is initialized to 0FFh after a read or after a Timeout has occurred. An interrupt is generated on the low to high transition of RDATA_RDY.

If a receive timeout (REC_TIMEOUT=1) or a transmit timeout (XMIT_TIMEOUT =1) occurred, the PS2 control logic will drive CLK LOW for 300us to signal the auxiliary device there is an error occurred. During this 300us CLK LOW period, writing to the Transmit Register is also permitted. But a data transmission will be invoked when all condition asserted.

20.2 PS/2 Control Registers (PS2CON)

Advance address 0 x 11, 0 x 15, 0 x 19)

Bit 7: NOISE FILTER ENABLE

0: Disable noise filter for clock line

1: Enable noise filter for clock line

Note: Turn ON this switch may NOT need to add the capacitor on PS2 line.

Bit 6: Inhibit bit

The LOW to HIGH transition of Inhibit bit generates a 100us LOW pulse on PS2 CLK line. This operation is logical OR'ed with PS2 internal CLK LOW control logic. This is an optional operation which be used for the firmware expects to prevent the PS2 line contention.

Bit 5-4: STOP

Bits [5:4] of the Control Register are used to set the level of the stop bit expected by the PS/2 channel state machine.

These bits are only valid when PS2_EN=1.

Bits [5:4]

= 00: Receiver expects an active high stop bit.

= 01: Receiver expects an active low stop bit.

= 10: Receiver ignores the level of the Stop bit (11th bit is not interpreted as a stop bit).

= 11: Reserved.

Bit 3-2: PARITY

Bits [3:2] of the Control Register are used to set the parity expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN=1.

Bits [3:2]

= 00: Receiver expects Odd Parity (default).

= 01: Receiver expects Even Parity.

= 10: Receiver ignores level of the parity bit (10th bit is not interpreted as a parity bit).

= 11: Reserved.

Bit 1: PS2_EN - PS2 Channel Enable (Default = 0).

Set this bit to enable the PS/2 hardware control logic.

If the PS2_EN bit is cleared while the PS2 is under receiving data before the falling edge of the 10th (parity bit) clock, the received data is discarded and RDATA_RDY won' t be set. And if not, the data is stored in the Receive Register and RDATA_RDY is set, also the parity error flag will not be set.

Bit 0: PS2_T/R - PS/2 Channel Transmit/Receive (default = 0).
This bit is only valid when PS2_EN=1.

1 = Transmit data.
This bit should be set before a data write to Transmit Register. Otherwise, the written data will be ignored.

After setting the PS2_T/R bit, the PS2 control logic will drive CLK line to LOW and then float the DATA line until a data written to the Transmit Register or until the PS2_T/R bit is cleared.
After writing on the Transmit Register to invoke a transmission, the PS2 control logic drives the data line low and, within 80ns, floats the clock line to signal auxiliary device that a data expects to transmit is now available.

If RDATA_RDY=1, set PS2_T/R bit will result in PS2 control logic floats DATA line and drives CLK line LOW until a read of Receive Register.

If the PS2_T/R bit is set while the channel is under receiving data before the falling edge of the 10th (parity bit) clock, the received data is discarded and RDATA_RDY won't be set. And if not, the received data is stored in the Receive Register and RDATA_RDY is set.

The PS2_T/R bit is cleared on the 11th clock edge of the transmission or if a Transmit Timeout error condition occurs.

0 = Receive data
If RDATA_RDY=0, clear PS2_T/R bit will floats both CLK and DATA line and waiting for the auxiliary device sending data in.

20.3 PS/2 Status Registers (PS2STS)

Advance address 0x12, 0 x 16, 0 x 1A

Bit 7: Reserved.

Bit 6: START_DEC START BIT DETECT
This bit is set on detecting start bit of receive condition.
The START_DEC bit is cleared when the Status Register is read.

Bit 5: XMIT_TIMEOUT
This bit will be set on either of 3 transmit conditions occurred, and then PS2 control logic will generate a 300us LOW pulse on CLK line following assertion of the XMIT_TIMEOUT bit. The PS2_T/R bit is also cleared.

1: When the transmitter bit time (time between falling edges) exceeds 300us.
2: When the transmitter start bit is not received within 25ms from signaling a transmit start event.
3: If the time from the 1st (start) bit to the 10th (parity) bit exceeds 2ms.

Bit 4: XMIT_IDLE - Transmitter Idle:

The XMIT_IDLE bit is a status bit indicating whether the PS2 channel is actively transmitting data to the auxiliary device. After a success of writing to the Transmit Register the XMIT_IDLE bit will be cleared to 0 until one of the following conditions occurred.

1) The falling edge of the 11th CLK; upon a Transmit Timeout condition (XMIT_TIMEOUT goes high)
2) Upon the PS2_T/R bit being written to 0.
3) Upon the PS2_EN bit being written to 0.

An interrupt is generated on the low to high transition of XMIT_IDLE.

Bit3: FE - Framing Error

If the received stop bit (11th bit) is different with the expected setting of PS2CON register, the FE and REC_TIMEOUT are set and an interrupt also generated.

Bit2: PE Parity Error:

If the received parity bit (10th bit) is different with the expected setting of PS2CON register, the PE and REC_TIMEOUT are set and an interrupt also generated.

Bit 1: REC_TIMEOUT

When operating in PS2 receiving mode, PS2_T/R is 0, this bit is set on either of 4 conditions asserted. And PS2 control logic will generate a 300us LOW pulse on CLK line following the bit set. An Interrupt is generated on the low to high transition of the REC_TIMEOUT bit. The REC_TIMEOUT bit is cleared when the Status Register is read.

1) When the receiver bit time (time between falling edges) exceeds 300us.
2) If the time from the 1st (start) bit to the 10th (parity) bit exceeds 2ms.
3) On a receive parity error along with the parity error (PE) bit.
4) On a receive framing error due to an incorrect STOP bit along with the framing error (FE) bit.

Bit 0: RDATA_RDY Receive Data Ready:

When operating in PS2 receiving mode, after a data byte was received successfully, and no FE, PE and REC_TIMEOUT, this bit is set until a read of Receive Register. An Interrupt is generated on the low to high transition of the RDATA_RDY bit. Switching PS2_EN or PS2_T/R bits under certain conditions will also clear or set this bit in exception.

20.4 PS/2 Status_2 Registers (PS2STS_2)

Advance address 0x1B

When a BUSY bit is set, the corresponding PS2 channel is busy in receiving data. Otherwise, the channel is idle.

Bit 0: Port 1 PS2 busy
= 0, IDLE
= 1, BUSY

Bit 1: Reserved.

Bit 2: Port 2 PS2 busy

= 0, IDLE

= 1, BUSY

Bit 3: Reserved.

Bit 4: Port 3 PS2 busy

= 0, IDLE

= 1, BUSY

Bit 7-5: Reserved.

21. SMBUS ADDRESS AND REGISTERS

21.1 SMBus Host Status Register (HSR)

SFR Address 0xA0

Default Value 0x00

Attribute: Read/Write Clear

BIT	DESCRIPTION
7	NOT ACK Command Received (NOT_ACK). 1= SMBus controller cannot receive the acknowledge command from the host writing address or data. Write 1 to clear this bit.
6	Receive FIFO Full (RX_FULL). 1= The receive data FIFO has filled 16-bytes data from the SMBus receiver. Write 1 to clear this bit
5	Receiver FIFO Time-out (RXTIMEOUT). 1 = If the received data in the FIFO does not over the FIFO threshold level and the time is over 1 ms, the interrupt also be generated to inform the micro-controller. Perhaps this bit is always inactive in the polling mode or using package-end status in the interrupt mode. Write 1 clear this bit. This bit is a source of interrupt.
4	SMBus FAILED (FAIL). 1 = The source of the interrupt was a failed bus transaction. This bit is set in response to the KILL bit being set to terminate the host transaction. Write 1 clear this bit.
3	SMBus Collision (BUS_COL). 1 = The source of the interrupt was a transaction collision or arbitration fail. Write 1 clear this bit.
2	Device Error (DEV_ERR). 1 = Host Device Time-out Error. Writing 1 to this bit. The micro-controller will then de-assert the interrupt.
1	REMOTE TX_TIMEOUT (RE_TXTIMEOUT) 1 = When local device is in receiver mode, set this bit to indicate remote device transmission timeout.
0	HOST_BUSY (H_BUSY)- Read Only. 1 = SMBus Controller is processing a command from the host interface or receiving SMBus data. 0 = SMBus controller host interface is not processing a command.

21.2 SMBus Host Control Register (HCR)

SFR Address 0xA1
Default Value 0x80
Attribute: Read/Write

<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>Reserved.</td></tr>
<tr><td>6:4</td><td>Baud Rate Select (BAUDRATE). Select SMBus clock baud rate
This clock is based on Xin or PLL input frequency.
<table>
<tr><th>BAUDRATE</th><th>Clock (if 8MHz)</th><th>Clock (if 16MHz)</th></tr>
<tr><td>000</td><td><10K Reserved.</td><td>12.5K Hz</td></tr>
<tr><td>001</td><td>12.5KHz</td><td>25K Hz</td></tr>
<tr><td>010</td><td>25KHz</td><td>50K Hz</td></tr>
<tr><td>011</td><td>50KHz</td><td>100K Hz (Default)</td></tr>
<tr><td>100</td><td>200KHz</td><td>400K Hz</td></tr>
<tr><td>101</td><td>400KHz</td><td>800K Hz</td></tr>
<tr><td>110</td><td>Reserved.</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved.</td><td>Reserved</td></tr>
</table>
Note: The baud rate of both Master and Slave mode are settled in same bits. When operated on Slave mode and deal with a different speed device, the user may resetting this baud rate for Slave transaction.</td></tr>
<tr><td>3</td><td>Enable SMBus Device (EN_SMBUS). Set 1, enable SMBus device.</td></tr>
<tr><td>2</td><td>LAST_BYTE. This bit is used for Host Continue Read Mode.
1 = Software sets this bit to indicate that the next byte will be the last byte to be received for the data stream. The SMBus controller will send a NOT ACK (instead of an ACK) after receiving the last byte. Write 0 to disable this function until the last byte is received or wait the bit of package end status be set to 1.</td></tr>
<tr><td>1</td><td>Host Continue Read Mode (H_CONTRD). This bit is used to determine the control method for NOT ACK generation when operated on Master-receive mode.
0 = The SMBus controller determines the expected number of data byte for host read by setting the H_RBC (SFR address 0A2h) before a transaction start-off.
1 = The firmware determines when to generate NOT ACK by setting the bit 2 (LAST_BYTE) to 1, in front of the coming last byte.</td></tr>
<tr><td>0</td><td>KILL SMBus (KILL). Set this bit to 1, the data FIFO and SMBus controller device will be reset and also invoke the bit 4 (FAIL) of HSR set.
Once this bit set, must be cleared to allow the SMBus Host Controller to function normally.
Note: It is suggested to user don't reset SMBus via setting this bit.
Set bit 0 of SCR (SFR address 0ACh) is recommended.</td></tr>
</table>

21.3 SMBus Host Read Byte Count Register (H_RBC)

SFR Address 0xA2
Default Value 0x00
Attribute: Read/Write

Bit	Description
7:0	Host Read Byte Count (H_RBC). This bit is used for Host Continue Read Mode which is determine the number of data byte host should read and then generate a NOT ACK. This register is only available when H_CONTRD set to 1.

21.4 SMBus Host/Slave Data FIFO Register (DFIFO)

SFR Address 0xA3
Default Value 0x00
Attribute: Read/Write

Bit	Description
7:0	Host/Slave Data FIFO Register (HS_DATAFIFO). This is a 16-bytes data FIFO for Host/Master/Slave transmit and receive. During the host/master mode, when a sequential 8-bit data fills into this data FIFO register, the data are also sequent printing out on SMBus. In the Slave-transmit mode, the SMBus will hold CLK low until each returned data byte written to FIFO. This feature will be disabled in Slave-receive mode during the NOT ACK receive operation.

21.5 SMBus Host-Slave Address Register (SADR)

SFR Address 0xA4
Default Value 0x00
Attribute: Read/Write

Bit	Description
7:1	Host-Slave Address Register (HS_ADDR). When the host serves as slave mode, this register should be compared. If the external master transmits the address matched this register, the host will be ready to receive or transmit data.
0	Reserved for general call.

21.6 SMBus Host/Slave Mode and FIFO Level Length Register (HMR)

SFR Address 0xA5
Default Value 0x00
Attribute: Read Only

Bit	Description
7:5	Host/Slave Mode (HS_MODE). These two bits indicate the SMBus controller state. Bit7: 5 Mode 000 Standby 100 Master transmit 101 Master receive 110 Slave transmit 111 Slave receive Others Reserved.
4:0	Host/Slave FIFO Level Length. Indicate the number of byte is stay in Data FIFO.

21.7 SMBus Host/Slave FIFO Control Register (FCR)

SFR Address 0xA6
Default Value 0x00
Attribute: Read/Write

Bit	Description
7:4	Reserved.
3	Write Tag Command (TAG). Master-transmit will be terminated a package transmission in the Data FIFO when writes a TAG command before the last byte that for written. Note that this bit should write first before the last byte is written to the Data FIFO. This bit will be automatically clear to 0. Note: Set this bit is used to generate a STOP or REPEAT START.
2	Reset Data FIFO (RST_DATAFIFO). Set this bit to 1, the data FIFO will be clear and the FIFO read/write pointer will be set to zero. This bit will be normal operation when set to 0.

1:0	Transmit or Receive FIFO Threshold Level (TXRX_LEVEL). These two bits are used to active the threshold interrupt when Transmitter or Receiver Data FIFO is below or over threshold level, respectively. Bit1:0 / RX/TX FIFO Threshold: 00 — 1 01 — 4 10 — 8 11 — 13

Bit1:0	RX/TX FIFO Threshold
00	1
01	4
10	8
11	13

21.8 SMBus Host/Slave interrupt Control Register (ICR)

SFR Address 0xA7

Default Value 0x00

Attribute: Read/Write

Bit	Description
7	Global Interrupt Enable (GLOBAL_EN). Enable global interrupt, if set to 1.
6	Receive Data Ready Interrupt Enable (RXDATA_EN). Enable Data ready interrupt.
5	Host Slave Address Match Interrupt Enable (ADDR_MATCH_EN). Enable the matched host slave address interrupt if set to 1
4	Master/Slave Receive Package End Interrupt Enable (RXEND_EN). Enable receiver package end interrupt, if set to 1.
3	Host Status Interrupt Enable (HSTATUS_EN). Enable host status interrupt, if set to 1
2	Transmit Empty Interrupt Enable (TXEMP_EN). Enable transmitter FIFO empty interrupt, if set to 1.
1	Transmit Threshold Interrupt Enable (TXTH_EN). Enable transmitter FIFO threshold register interrupt, if set to 1.
0	Receive Threshold Interrupt Enable (RXTH_EN). Enable receiver FIFO threshold register interrupt, if set to 1.

Note: If disable a bit in ICR, then the corresponding bit in ISR will NOT be set, when corresponding event occurred. In other words, if disable the bit 5 of ICR, then the bit 5 of ISR is never be set.

21.9 SMBus Host/Slave interrupt Status Register (ISR)

SFR Address 0xA9
Default Value 0x00
Attribute: Read/Write

Bit	Description
7	Reserved.
6	Receive Data Ready Interrupt (RXDATARDY_I). 1 = Indicates the receive FIFO data is ready. Write 1 to clear this bit.
5	Host Slave Address Match Interrupt (ADDRMATCH_I). 1 = Host slave SMBus device has detected the matched address. Write 1 to clear this bit. Note: The bit will be set when received Slave Address + Write or Slave Address + Read.
4	Master Receiver Package End Interrupt (RXEND_I). 1 = The SMBus package has a grace Read Stop which is NOT ACK to respond the slave and hardware STOP is finished. Write 1 to clear this bit.
3	Host Status Interrupt (HSTATUS_I). 1 = When SMBus fail, collision, or device error is detected by the SMBus controller. Write 1 to clear this bit. Note: The HSR details error status bits.
2	Transmitter Empty Interrupt Status (TXEMP_I). 1 = When transmitter Data FIFO is empty. Write 1 to clear this bit.
1	Transmitter Threshold Level Interrupt (TXTHL_I). 1 = The transmitter FIFO is below the threshold level. Write 1 to clear this bit.
0	Receiver Threshold Level Interrupt (RXTHL_I). 1 = The receiver FIFO is over the threshold level. Write 1 to clear this bit.

Note: After Slave Address Match (bit 5 of ISR) set, the data ready (bit 6 of ISR) will be set after 1 clock.

21.10 SMBus Host/Slave FIFO Status Register (FSR)

SFR Address 0xAA
Default Value 0x06
Attribute: Read/Write

Bit	Description
7:3	Reserved.
2	Transmit Shift Register Empty (TXSREMP). This bit indicates transmit shift register is empty.
1	Transmit FIFO Empty (TXFIFOEMP). This bit indicates transmit FIFO is empty.
0	Receive Data Ready (RXRDY). This bit indicates the data is ready to read when the I^2C is operating at Master receive or Slave receive.

21.11 SMBus User Defined Register (UDR)

SFR Address 0xAB
Default Value 0x00
Attribute: Read/Write

Bit	Description
7:0	User Defined Register (UDREG)

21.12 SMBus System Control Register (SCR)

SFR Address 0xAC
Default Value 0x80
Attribute: Read/Write

Bit	Description
7	SCL / SDA interrupt pin poiarty 0: falling edge 1: rising edger
6	SCL / SDA interrupt pin selection bit. 0: SDA vaild 1: SCL valid
5:1	Reserved.
0	Software Reset (SOFT_RST). 1 = Generate one clock pulse as reset signal. It will cause a reset on SMBus controller.

21.13 SMBus Test 0 Register (TST0)

SFR Address 0xAD
Default Value 0x00
Attribute: Read/Write

Bit	Description
7	IDLE. Current Idle status.
6	STA. Current start status.
5	STO. Current stop status.
4:0	state. Show the current FIFO Control state.

21.14 SMBus Test 1 Register (TST1)

SFR Address 0xAE
Default Value 0x00
Attribute: Read/Write

Bit	Description
7:4	S1STA. Show the current system state.
3:1	Reserved.
0	test0. Shorten timeout generation duration from 1 ms to 24 SCL clocks.

22. AUXILIARY SMBUS ADDRESS AND REGISTERS

22.1 Auxiliary SMBus Host Status Register (AHSR)

Advanced SFR Address 0x28
Default Value 0x00
Attribute: Read/Write Clear

Bit	Description
7	NOT ACK Command Received (NOT_ACK). 1= SMBus controller cannot receive the acknowledge command from the host writing address or data. Write 1 to clear this bit.
6	Receive FIFO Full (RX_FULL). 1= The receive data FIFO has filled 16-bytes data from the SMBus receiver. Write 1 to clear this bit
5	Receiver FIFO Time-out (RXTIMEOUT). 1 = If the received data in the FIFO does not over the FIFO threshold level and the time is over 1 ms, the interrupt also be generated to inform the micro-controller. Perhaps this bit is always inactive in the polling mode or using package-end status in the interrupt mode. Write 1 clear this bit. This bit is a source of interrupt.
4	SMBus FAILED (FAIL). 1 = The source of the interrupt was a failed bus transaction. This bit is set in response to the KILL bit being set to terminate the host transaction. Write 1 clear this bit.
3	SMBus Collision (BUS_COL). 1 = The source of the interrupt was a transaction collision or arbitration fail. Write 1 clear this bit.
2	Device Error (DEV_ERR). 1 = Host Device Time-out Error. Writing 1 to this bit. The micro-controller will then de-assert the interrupt.
1	REMOTE TX_TIMEOUT (RE_TXTIMEOUT) 1 = When local device is in receiver mode, set this bit to indicate remote device transmission timeout.
0	HOST_BUSY (H_BUSY)- Read Only. 1 = SMBus Controller is processing a command from the host interface or receiving SMBus data. 0 = SMBus controller host interface is not processing a command.

22.2 Auxiliary SMBus Host Control Register (AHCR)

Advanced SFR Address 0x29

Default Value 0x80

Attribute: Read/Write

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>7</td><td>Reserved.</td></tr>
<tr><td>6:4</td><td>Baud Rate Select (BAUDRATE). Select SMBus clock baud rate.
This clock is based on Xin or PLL input frequency.
<table>
<tr><td>BAUDRATE</td><td>Clock (if 8MHz)</td><td>Clock (if 16MHz)</td></tr>
<tr><td>000</td><td><10K Reserved.</td><td>12.5K Hz</td></tr>
<tr><td>001</td><td>12.5KHz</td><td>25K Hz</td></tr>
<tr><td>010</td><td>25KHz</td><td>50K Hz</td></tr>
<tr><td>011</td><td>50KHz</td><td>100K Hz (Default)</td></tr>
<tr><td>100</td><td>200KHz</td><td>400K Hz</td></tr>
<tr><td>101</td><td>400KHz</td><td>800K Hz</td></tr>
<tr><td>110</td><td>Reserved.</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved.</td><td>Reserved</td></tr>
</table>
Note: The baud rate of both Master and Slave mode are settled in same bits. When operated on Slave mode and deal with a different speed device, the user may resetting this baud rate for Slave transaction.</td></tr>
<tr><td>3</td><td>Enable SMBus Device (EN_SMBUS). Set 1, enable SMBus device.</td></tr>
<tr><td>2</td><td>LAST_BYTE. This bit is used for Host Continue Read Mode.
1 = Software sets this bit to indicate that the next byte will be the last byte to be received for the data stream. The SMBus controller will send a NOT ACK (instead of an ACK) after receiving the last byte. Write 0 to disable this function until the last byte is received or wait the bit of package end status be set to 1.</td></tr>
<tr><td>1</td><td>Host Continue Read Mode (H_CONTRD). This bit is used to determine the control method for NOT ACK generation when operated on Master-receive mode.
0 = The SMBus controller determines the expected number of data byte for host read by setting the AH_RBC (Advanced SFR address 2Ah) before a transaction start-off.
1 = The firmware determines when to generate NOT ACK by setting the bit 2 (LAST_BYTE) to 1, in front of the coming last byte.</td></tr>
<tr><td>0</td><td>KILL SMBus (KILL).Set this bit to 1, the data FIFO and SMBus controller device will be reset and also invoke the bit 4 (FAIL) of HSR set.
Once this bit set, must be cleared to allow the SMBus Host Controller to function normally.
Note: It is suggested to user don’t reset SMBus via setting this bit.
Set bit 0 of ASCR (Advanced SFR address 033h) is recommended.</td></tr>
</table>

22.3 Auxiliary SMBus Host Read Byte Count Register (AH_RBC)

Advanced SFR Address 0x2A
Default Value 0x00
Attribute: Read/Write

Bit	Description
7:0	Host Read Byte Count (H_RBC). This bit is used for Host Continue Read Mode which is determine the number of data byte host should read and then generate a NOT ACK. This register is only available when H_CONTRD set to 1.

22.4 Auxiliary SMBus Host/Slave Data FIFO Register (ADFIFO)

Advanced SFR Address 0x2B
Default Value 0x00
Attribute: Read/Write

Bit	Description
7:0	Host/Slave Data FIFO Register (HS_DATAFIFO). This is a 16-bytes data FIFO for Host/Master/Slave transmit and receive. During the host/master mode, when a sequential 8-bit data fills into this data FIFO register, the data are also sequent printing out on SMBus. In the Slave-transmit mode, the SMBus will hold CLK low until each returned data byte written to FIFO. This feature will be disabled in Slave-receive mode during the NOT ACK receive operation.

22.5 Auxiliary SMBus Host-Slave Address Register (ASADR)

Advanced SFR Address 0x2C
Default Value 0x00
Attribute: Read/Write

Bit	Description
7:1	Host-Slave Address Register (HS_ADDR). When the host serves as slave mode, this register should be compared. If the external master transmits the address matched this register, the host will be ready to receive or transmit data.
0	Reserved for general call.

22.6 Auxiliary SMBus Host/Slave Mode and FIFO Level Length Register(AHMR)

Advanced SFR Address 0x2D
Default Value 0x00
Attribute: Read Only

Bit	Description
7:5	Host/Slave Mode (HS_MODE). These two bits indicate the SMBus controller state. Bit7:5 Mode 000 Standby 100 Master transmit 101 Master receive 110 Slave transmit 111 Slave receive Others Reserved.
4:0	Host/Slave FIFO Level Length. Indicate the number of byte is stay in Data FIFO.

22.7 Auxiliary SMBus Host/Slave FIFO Control Register (AFCR)

Advanced SFR Address 0x2E
Default Value 0x00
Attribute: Read/Write

Bit	Description
7:4	Reserved.
3	Write Tag Command (TAG). Master-transmit will be terminated a package transmission in the Data FIFO when writes a TAG command before the last byte that for written. Note that this bit should write first before the last byte is written to the Data FIFO. This bit will be automatically clear to 0. Note: Set this bit is used to generate a STOP or REPEAT START.
2	Reset Data FIFO (RST_DATAFIFO). Set this bit to 1, the data FIFO will be clear and the FIFO read/write pointer will be set to zero. This bit will be normal operation when set to 0.
1:0	Transmit or Receive FIFO Threshold Level (TXRX_LEVEL). These two bits are used to active the threshold interrupt when Transmitter or Receiver Data FIFO is below or over threshold level, respectively.

Bit1:0	RX/TX FIFO Threshold
00	1
01	4
10	8
11	13

22.8 Auxiliary SMBus Host/Slave interrupt Control Register (AICR)

Advanced SFR Address 0x2F
Default Value 0x00
Attribute: Read/Write

Bit	Description
7	Global Interrupt Enable (GLOBAL_EN). Enable global interrupt, if set to 1.
6	Receive Data Ready Interrupt Enable (RXDATA_EN). Enable Data ready interrupt.
5	Host Slave Address Match Interrupt Enable (ADDR_MATCH_EN). Enable the matched host slave address interrupt if set to 1
4	Master/Slave Receive Package End Interrupt Enable (RXEND_EN). Enable receiver package end interrupt, if set to 1.
3	Host Status Interrupt Enable (HSTATUS_EN). Enable host status interrupt, if set to 1
2	Transmit Empty Interrupt Enable (TXEMP_EN). Enable transmitter FIFO empty interrupt, if set to 1.
1	Transmit Threshold Interrupt Enable (TXTH_EN). Enable transmitter FIFO threshold register interrupt, if set to 1.
0	Receive Threshold Interrupt Enable (RXTH_EN). Enable receiver FIFO threshold register interrupt, if set to 1.

Note: If disable a bit in AICR, then the corresponding bit in AISR will NOT be set, when corresponding event occurred. In other words, if disable the bit 5 of AICR, then the bit 5 of AISR is never be set.

22.9 Auxiliary SMBus Host/Slave interrupt Status Register (AISR)

Advanced SFR Address 0x30
Default Value 0x00
Attribute: Read/Write

Bit	Description
7	Reserved.
6	Receive Data Ready Interrupt (RXDATARDY_I). 1 = Indicates the receive FIFO data is ready. Write 1 to clear this bit.
5	Host Slave Address Match Interrupt (ADDRMATCH_I). 1 = Host slave SMBus device has detected the matched address. Write 1 to clear this bit. Note: The bit will be set when received Slave Address + Write or Slave Address + Read.
4	Master/Slave Receiver Package End Interrupt (RXEND_I). 1 = The SMBus package has a grace Read Stop which is NOT ACK to respond the slave and hardware STOP is finished. Write 1 to clear this bit.
3	Host Status Interrupt (HSTATUS_I). 1 = When SMBus fail, collision, or device error is detected by the SMBus controller. Write 1 to clear this bit. Note: The HSR details error status bits.
2	Transmitter Empty Interrupt Status (TXEMP_I). 1 = When transmitter Data FIFO is empty. Write 1 to clear this bit.
1	Transmitter Threshold Level Interrupt (TXTHL_I). 1 = The transmitter FIFO is below the threshold level. Write 1 to clear this bit.
0	Receiver Threshold Level Interrupt (RXTHL_I). 1 = The receiver FIFO is over the threshold level. Write 1 to clear this bit.

Note: After Slave Address Match (bit 5 of AISR) set, the data ready (bit 6 of AISR) will be set after 1 clock.

22.10 Auxiliary SMBus Host/Slave FIFO Status Register (AFSR)

Advanced SFR Address 0x31
Default Value 0x06
Attribute: Read/Write

Bit	Description
7:3	Reserved.
2	Transmit Shift Register Empty (TXSREMP). This bit indicates transmit shift register is empty.
1	Transmit FIFO Empty (TXFIFOEMP). This bit indicates transmit FIFO is empty.
0	Receive Data Ready (RXRDY). This bit indicates the data is ready to read when the I^2C is operating at Master receive or Slave receive.

22.11 Auxiliary SMBus User Defined Register (AUDR)

Advanced SFR Address 0x32
Default Value 0x00
Attribute: Read/Write

Bit	Description
7:0	User Defined Register (UDREG)

22.12 Auxiliary SMBus System Control Register (ASCR)

Advanced SFR Address 0x33
Default Value 0x80
Attribute: Read/Write

Bit	Description
7	SCL / SDA interrupt pin poiarty 0: falling edge 1: rising edger
6	SCL / SDA interrupt pin selection bit. 0: SDA vaild 1: SCL valid
5:1	Reserved.
0	Software Reset (SOFT_RST). 1 = Generate one clock pulse as reset signal. It will cause a reset on SMBus controller.

22.13 Auxiliary SMBus Test 0 Register (ATST0)

Advanced SFR Address 0x34
Default Value 0x00
Attribute: Read/Write

Bit	Description
7	IDLE. Current Idle status.
6	STA. Current start status.
5	STO. Current stop status.
4:0	state. Show the current FIFO Control state.

22.14 Auxiliary SMBus Test 1 Register (ATST1)

Advanced SFR Address 0x35
Default Value 0x00
Attribute: Read/Write

Bit	Description
7:4	S1STA. Show the current system state.
3:1	Reserved.
0	test0. Shorten timeout generation duration from 1 ms to 24 SCL clocks.

23. ELECTRICAL CHARACTERISTICS

23.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

23.2 DC Characteristics (V_{DD} = 5V)

(Ta = 0° C to 70° C, V_{DD} = **5V** ± 10%, V_{SS} = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O24$_t$ - TTL level bi-directional pin with 24 mA source-sink capability						
Input Low Voltage	VIL	-0.5		0.8	V	
Input High Voltage	VIH	2.0		V_{DD}+0.5	V	
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
Output High Voltage	VOH	2.4			V	IOH = -24 mA
I/O$_{12t}$ - TTL level bi-directional pin with 12 mA source-sink capability						
Input Low Voltage	VIL	-0.5		0.8	V	
Input High Voltage	VIH	2.0		V_{DD}+0.5	V	
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
I/O$_{12s}$- TTL level output pin with 12 mA source-sink capability and Schmitt-trigger input pin						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	Vt+	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	VTH	1.5	2		V	V_{DD} = 5 V
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
I/OD$_{12c}$ - TTL level open-drain output pin with 12 mA source-sink capability and CMOS level input pin						
Input Low Voltage	VIL	-0.5		0.3XV_{DD}	V	
Input High Voltage	VIH	0.7XV_{DD}		V_{DD}+0.5	V	
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12c} - TTL level output pin with 12 mA source-sink capability and CMOS level input pin						
Input Low Threshold Voltage	VIL	-0.5		$0.3XV_{DD}$	V	V_{DD} = 5 V
Input High Threshold Voltage	VIH	$0.7XV_{DD}$		$V_{DD}+0.5$	V	V_{DD} = 5 V
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
IN_t - TTL level input pin						
Input Low Voltage	VIL	-0.5		0.8	V	
Input High Voltage	VIH	2.0		$V_{DD}+0.5$	V	
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN_s - Schmitt-triggered input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 5 V
Hystersis	VTH	0.5	1.2		V	VDD = 5 V
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN_c - CMOS level input pin						
Input Low Threshold Voltage	VIL	-0.5		$0.3XV_{DD}$	V	
Input High Threshold Voltage	VIH	$0.7XV_{DD}$		$V_{DD}+0.5$	V	
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN_{cu} - CMOS level input pin with internal pull-up resistor						
Input Low Threshold Voltage	VIL	-0.5		$0.3XV_{DD}$	V	
Input High Threshold Voltage	VIH	$0.7XV_{DD}$		$V_{DD}+0.5$	V	
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V

23.3 DC Characteristics (V_{DD} = 3.3V)

(Ta = 0° C to 70° C, VDD = 3.3V ±10%, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O24$_t$ - TTL level bi-directional pin with 24 mA source-sink capability						
Input Low Voltage	VIL	-0.33		0.8	V	
Input High Voltage	VIH	2.0		V_{DD}+0.33	V	
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
Output High Voltage	VOH	2.4			V	IOH = -24 mA
I/O$_{12t}$ - TTL level bi-directional pin with 12 mA source-sink capability						
Input Low Voltage	VIL	-0.33		0.8	V	
Input High Voltage	VIH	2.0		V_{DD}+0.33	V	
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
I/O$_{12S}$- TTL level output pin with 12 mA source-sink capability and Schmitt-trigger input pin						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	V_{DD} = 3.3 V
Input High Threshold Voltage	Vt+	3.2	3.5	3.8	V	V_{DD} = 3.3 V
Hystersis	VTH	1.5	2		V	V_{DD} = 3.3 V
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
I/OD$_{12c}$ - TTL level open-drain output pin with 12 mA source-sink capability and CMOS level input pin						
Input Low Voltage	VIL	-0.33		0.2XV_{DD}	V	
Input High Voltage	VIH	0.7XV_{DD}		V_{DD}+0.33	V	
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA

DC Characteristics, continued

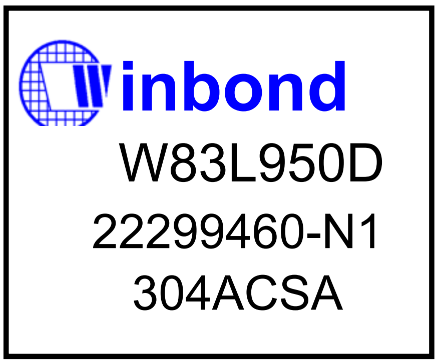
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12c} - TTL level output pin with 12 mA source-sink capability and CMOS level input pin						
Input Low Voltage	VIL-	-0.33	1.5	$0.2XV_{DD}$	V	V_{DD} = 3.3 V
Input High Voltage	VIH	$0.7XV_{DD}$	3.5	V_{DD}+0.33	V	V_{DD} = 3.3 V
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
IN_t - TTL level input pin						
Input Low Voltage	VIL	-0.33		0.8	V	
Input High Voltage	VIH	2.0		V_{DD}+0.33	V	
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN_s - Schmitt-triggered input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	V_{DD} = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	V_{DD} = 3.3 V
Hystersis	VTH	0.5	1.2		V	V_{DD} = 3.3 V
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN_c - CMOS level input pin						
Input Low Voltage	VIL	-0.33		$0.2XV_{DD}$	V	
Input High Voltage	VIH	$0.7XV_{DD}$		V_{DD}+0.33	V	
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN_{cu} - CMOS level input pin with internal pull-up resistor						
Input Low Voltage	VIL	-0.33		$0.2XV_{DD}$	V	
Input High Voltage	VIH	$0.7XV_{DD}$		V_{DD}+0.33	V	
Input High Leakage	ILIH			+10	μA	VIN = V_{DD}
Input Low Leakage	ILIL			-10	μA	VIN = 0 V

* After Power On Reset, until KBC into a stable state, it takes less than 1ms.

24. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83L950D	80-PIN LQFP	Commercial, 0°C to +70°C

25. HOW TO READ THE TOP MARKING



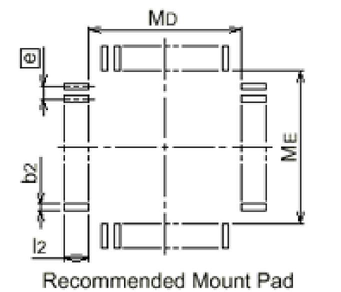
1st line: Winbond logo
2nd line: W83L950D, chip part number
3rd line: Tracking code 2 2299460-N1
2: Manufacturing in FAB II
2299460-N1: The lot no.
4th line: Tracking code 304 A C SA
304: packages made in '03, week 04
A: assembly house ID; A means ASE, O means OSE, G means GR…
C: IC revision
SA: Internal version

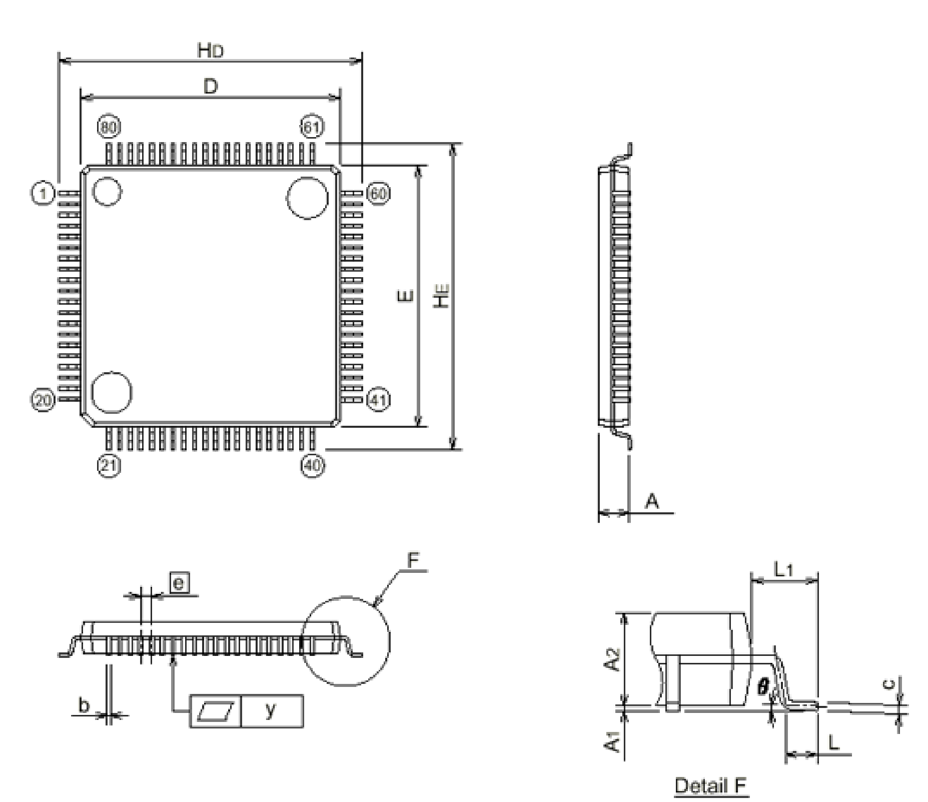
26. PACKAGE DIMENSIONS

Package- 80-pin LQFP

80P6Q-A **Plastic 80pin 12×12mm body LQFP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.5	–		Cu Alloy





Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	–	0.5	–
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	1.0	–	–
M_D	–	12.4	–
M_E	–	12.4	–

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

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